Programmable Array Logic Family PAL® Series 24 AP With Programmable Output Polarity

ADVANCE INFORMATION

Features/Benefits

- 25 ns maximum propagation delay
- Programmable output polarity
- Programmable replacement for TTL logic
- Expedites prototyping and board layout
- Programmed on standard PAL programmers
- Last fuse prevents duplication

Functional Description

The PAL series 24 AP represents an enhancement of existing PAL architectures which provides greater design flexibility and higher speed. The PAL series 24 AP comes with programmable output polarity and is pin-for-pin compatible with the standard PAL 24 series.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

General Description

The PAL series utilizes Monolithic Memories' advanced self-aligned washed-emitter high-speed bipolar process and the bipolar fusible-link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the system engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform the desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from the PC board and are placed on silicon where they can be easily modified during prototype check-out or production.

Product Description

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL12P10A	JS, NS, (L), (NL)	Deca 12-input And-Or
PAL14P8A	JS, NS, (L), (NL)	Octal 14-input And-Or
PAL16P6A	JS, NS, (L), (NL)	Hex 16-input And-Or
PAL18P4A	JS, NS, (L), (NL)	Quad 18-input And-Or
PAL20P2A	JS, NS, (L), (NL)	Dual 20-input And-Or
PAL20C1A	JS, NS, (L), (NL)	20-input And-Or

NOTE: L and NL options are 28-pin chip carriers.

The PAL transfer function is the familiar sum of products. The PAL has a single array of fusible links which is a programmable AND array driving a fixed OR array.

Unused inputs are tied directly to VCC or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state.

The entire PAL family is programmed on inexpensive conventional PAL programmers with appropriate personality and socket adapter modules. Once the PAL is programmed and verified two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Preliminary Data

- T_{PD} (max) = 25 ns propagation delay
- I_{CC} (max) = 100 mA

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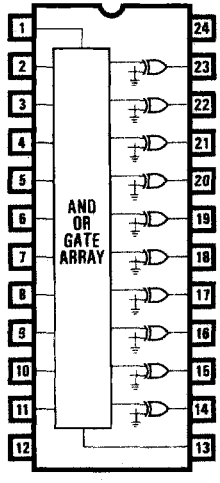
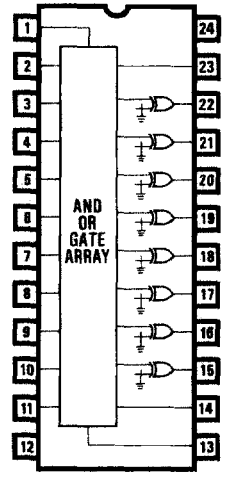
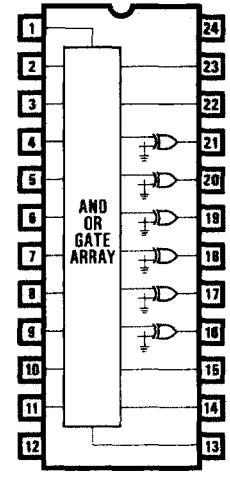
PAL12P10A



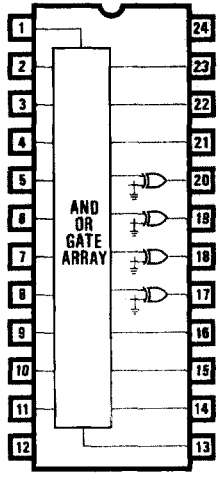
PAL14P8A



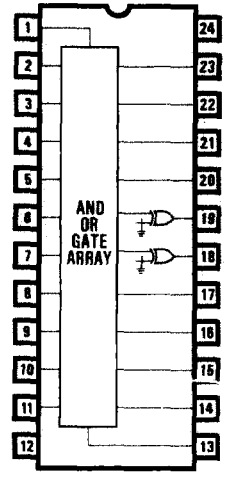
PAL16P6A



PAL18P4A



PAL20P2A



PAL20C1A