Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

DESCRIPTION

The NE701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.5V for compatibility with the new CMOS UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The maximum supply current is 2.8mA allowing application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the HS4+ process (the bipolar portion of the QUBiC process). The circuit will be available in an 8 pin SO package with 150 mil package width.

FEATURES

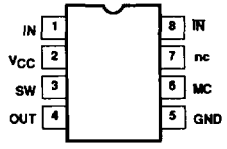
- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE701D
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA701D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to V_{CC}	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance	90	°C/W

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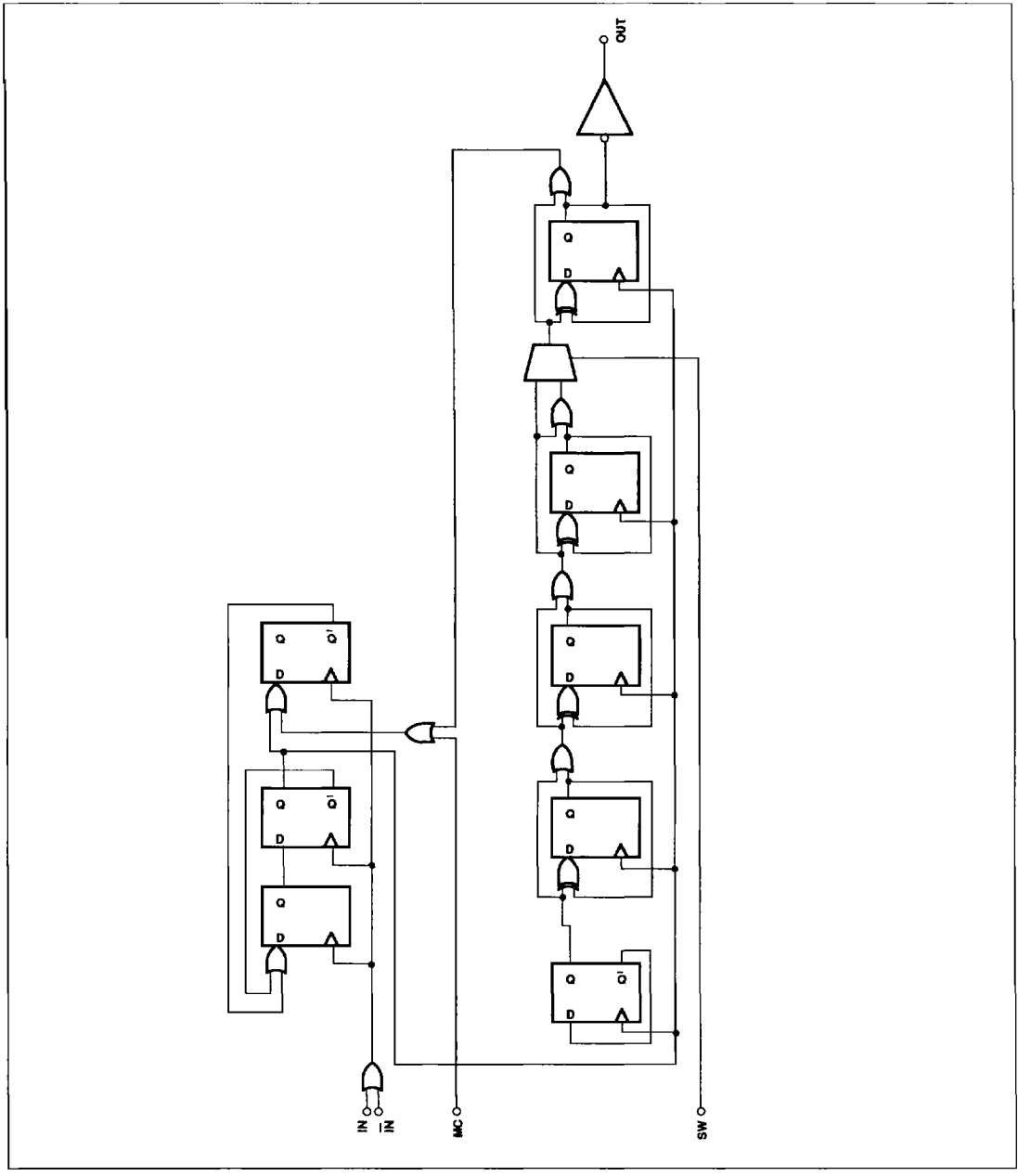
BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.5		6.0	V
I_{CC}	Supply current				2.8	mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level	V_{CC} ≥ 3.2V			V_{CC}-3.0	V
		V_{CC} < 3.2V			0.2	V
V_{IH}	MC input high threshold	I_{MC} = 60μA	2.0			V
V_{IL}	MC input low threshold	I_{MC} = 20μA			0.8	V
I_I	MC input current	V_{MC} = V_{CC} = 5.0V			150	μA
V_{IH}	SW input high threshold		2.0			V
V_{IL}	SW input low threshold				0.8	V
I_I	SW input current	V_{SW} = V_{CC} = 5.0V			100	μA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for V_{CC} = 3.0V, -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude	1000pF input coupling	0.1		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement	5			kΩ
C_I	Input capacitance				TBD	pF
V_O	Output voltage	V_{CC} = 5.0V	1.6			V_{P-P}
		V_{CC} = 3.0V	1.2			V_{P-P}
t_S	Modulus set-up time	f_{IN} = 1.2GHz		TBD		ns
t_H	Modulus hold time	f_{IN} = 1.2GHz		TBD		ns
t_{PD}	Propagation time			TBD		ns

DESCRIPTION OF OPERATION

The NE701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a fixed 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the NE701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed.

A truth table for the modulus values is given below:

Table.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

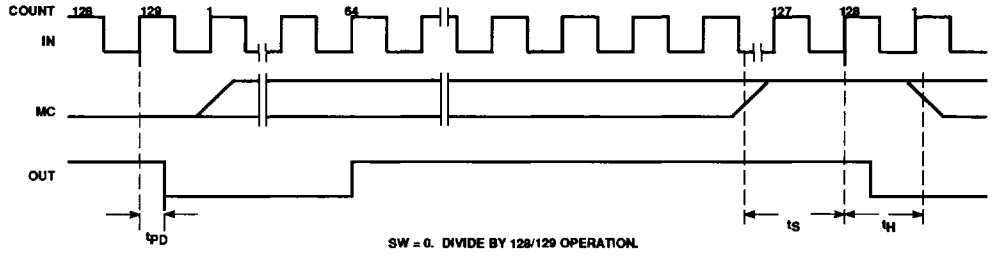
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

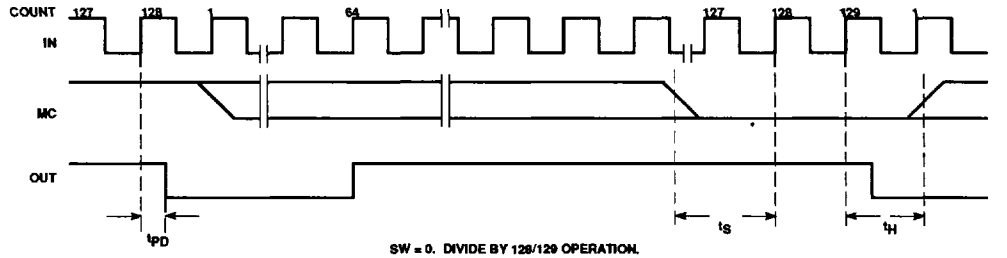
The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

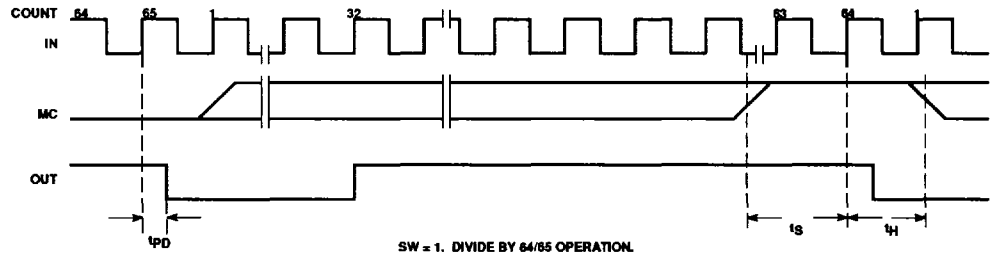
AC TIMING CHARACTERISTICS



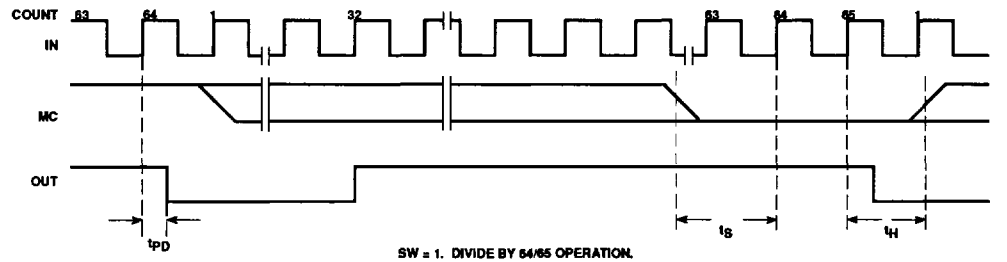
SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.