NCV8518

Low Dropout Linear Regulator with Watchdog, Wake Up, $\overline{\text{RESET}}$, and ENABLE

The NCV8518 device is a precision micropower voltage regulator. It has a fixed output voltage of 5.0 V and regulates within ±2%. It is suitable for use in all automotive environments and contains all the required functions to control a microprocessor. This device has low dropout voltage and low quiescent current. It includes a watchdog timer, adjustable reset, wake up and enable function. Also encompassed in this device are safety features such as thermal shutdown and short circuit protection. It is capable of handling up to 45 V transients.

Features

- Output Voltage of 5.0 V
- ±2% Output Voltage Tolerance
- Output Current up to 250 mA
- Micropower Compatible Control Functions:
  - ENABLE
  - Watchdog
  - $\overline{\text{RESET}}$
  - Wake Up
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Low Dropout Voltage
- Low Quiescent Current of 100 μA
- Protection Features:
  - Thermal Shutdown
  - Short Circuit
- Low Sleep Mode Current less than 1.0 μA
- AEC Qualified
- PPAP Capable
- These are Pb−Free Devices

Applications

- Tire Pressure Monitor
- Battery Powered Consumer Electronics

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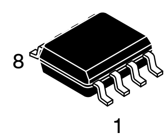
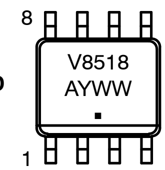
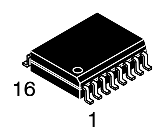
MARKING DIAGRAMS

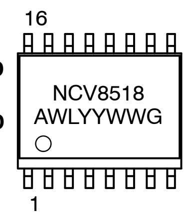


SOIC−8 EXPOSED PAD CASE 751AC





SOIC−16 LEAD WIDE BODY EXPOSED PAD CASE 751AG



A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
▪, or G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV8518PDG	SOIC−8*	98 Units / Rail
NCV8518PDR2G	SOIC−8*	2500 / Tape & Reel
NCV8518PWG	SOIC−16*	47 Units / Rail
NCV8518PWR2G	SOIC−16*	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*These packages are inherently Pb−Free.

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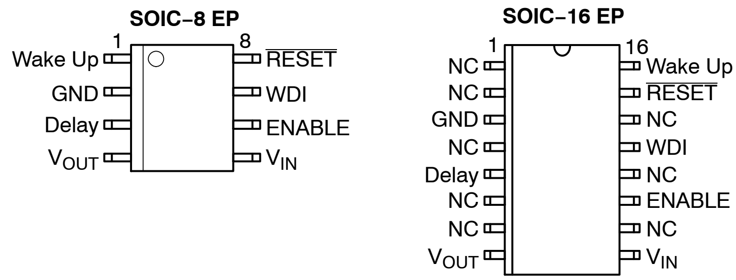
October, 2008 − Rev. 7

Publication Order Number:
NCV8518/D

PIN CONNECTIONS



PIN FUNCTION DESCRIPTION

Pin			
SOIC−8 EP	**SOIC−16 E PAD**	**Symbol**	**Description**
4	8	V_{OUT}	Regulated output voltage.
5	9	V_{IN}	Input supply voltage.
7	13	WDI	CMOS compatible Watchdog input. The watchdog function monitors the falling edge of the incoming signal.
2	3	GND	Ground connection.
6	11	ENABLE	ENABLE control for the IC. Positive logic.
8	15	$\overline{\text{RESET}}$	CMOS compatible output $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct watchdog signal.
3	5	Delay	Buffered reference voltage used to create timing current for $\overline{\text{RESET}}$ and Watchdog threshold frequency from R_{Delay}.
−	1, 2, 4, 6, 7, 10, 12, 14	NC	No Connection.
1	16	Wake Up	Continuously generated signal that interrupts the microprocessor from sleep mode.
EPAD	EPAD	EPAD	Connect to Ground potential or leave unconnected.

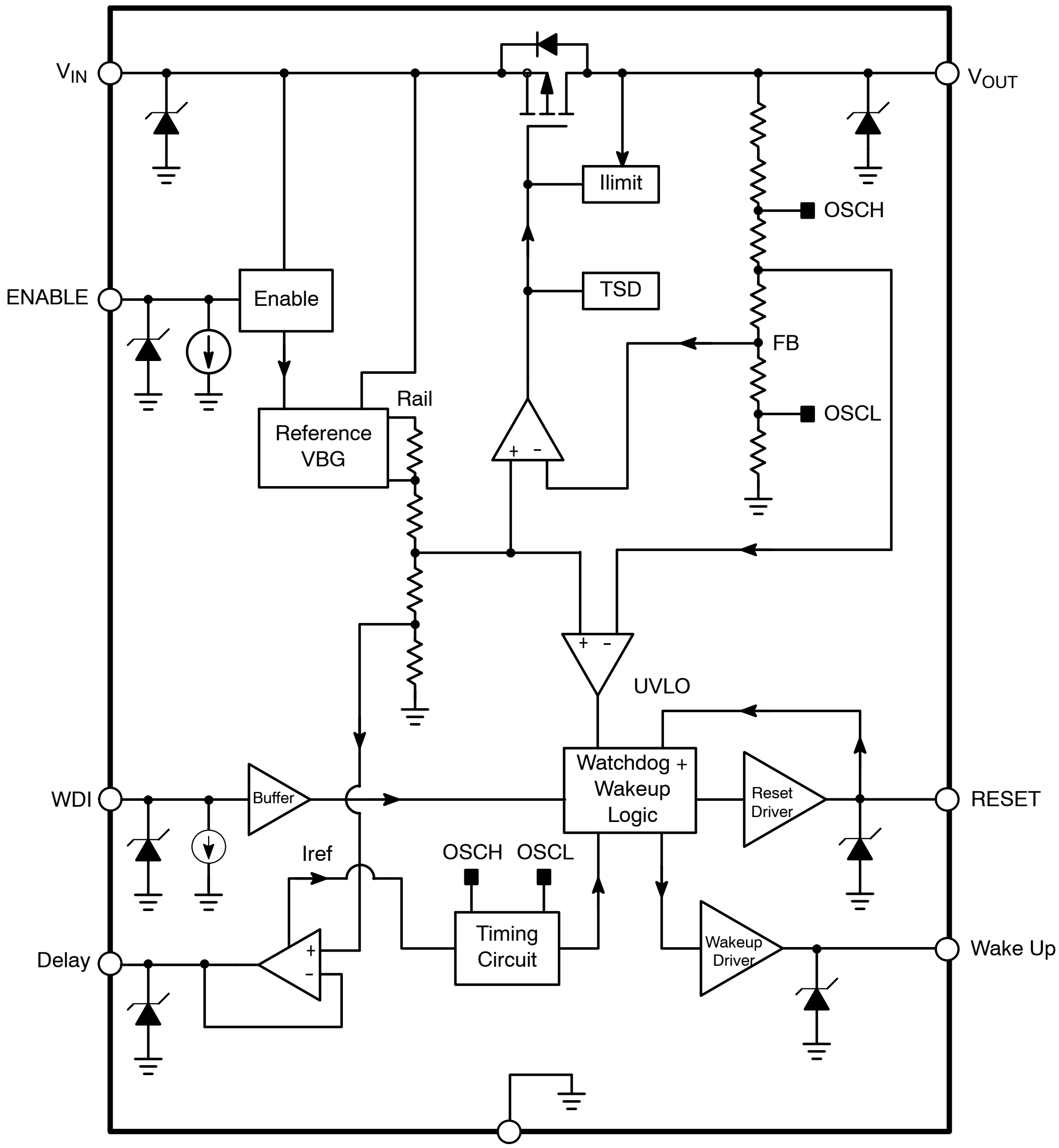


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}, ENABLE	−0.3 to 45	V
Output Voltage	V_{OUT}	−0.3 to +7.0	V
$\overline{\text{RESET}}$ Voltage	V_{RESET}	0 V to V_{OUT}	V
$\overline{\text{RESET}}$ Current ($\overline{\text{RESET}}$ may be incidentally shorted either to V_{OUT} or to GND without damage)	I_{RESET}	Internally Limited	mA
ESD Susceptibility (Human Body Model)	–	2.0	kV
Logic Inputs/Outputs (Reset, WDI, Wake Up, Delay)	–	−0.3 to +7.0	V
Operating Junction Temperature	T_J	−40 to150	°C
Storage Temperature Range	T_S	−55 to +150	°C
Moisture Sensitivity Level SOIC−16 EP (Case 751R) SOIC−8 EP (Case 751AC)	MSL	 1 3	
Lead Temperature Soldering: Reflow Leaded Part 60−150 sec above 183°C, 30 sec max at peak Lead−Free Part 60−150 sec above 217°C, 40 sec max at peak	 – –	 240 peak 265 peak	 °C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

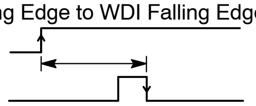
Parameter	Board/Mounting Conditions Typical Value		Unit
SO−8 Exposed Pad Package			
	minimum−pad board (Note 1)	1 sq. inch spreader board (Note 2)	
Junction to case top (Ψ−JT, θ_{JT})	19	8	°C/W
Junction to pin1 (Ψ−JL1, θ_{JL1})	68	63	°C/W
Junction to board (Ψ−JB, θ_{JB})[3]	9	10	°C/W
Junction to ambient ($R_{\theta JA}$, θ_{JA})	235	57	°C/W
SO−16 Exposed Pad Package			
	minimum−pad board (Note 3)	1 sq. inch spreader board (Note 2)	
Junction to case top (Ψ−JT, θ_{JT})	30	16	°C/W
Junction to pin1 (Ψ−JL1, θ_{JL1})	70	65	°C/W
Junction to board (Ψ−JB, θ_{JB}) (Note 4)	15	17	°C/W
Junction to ambient ($R_{\theta JA}$, θ_{JA})	150	55	°C/W

Specific notes on thermal characterization conditions:

All boards are 0.062” thick FR4, 3” square, with varying amounts of copper heat spreader, in still air (free convection) conditions. Numerical values are derived from an axisymmetric finite−element model where active die area, total die area, flag area, pad area, and board area are equated to the actual corresponding areas.

1. 1 oz copper, 6 x 9 mm, 0.062” thick FR−4.
2. 1 oz copper, 645 mm^2 ($1in^2$) spreader area (includes exposed pad).
3. 1 oz copper, 17.2 mm^2 spreader area (minimum exposed pad, not including traces which are assumed).
4. “board” is defined as center of exposed pad soldered to board; this is the recommended number to be used for thermal calculations, as it best represents the primary heat flow path and is least sensitive to board and ambient properties.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 150°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output					
Output Voltage	V_{OUT}	4.9 −2%	5.00	5.10 +2%	V
Dropout Voltage ($V_{IN} - V_{OUT}$, I_{OUT} = 150 mA) (Note 5)	V_{DO}	–	425	750	mV
Load Regulation (V_{IN} = 13.5 V, 100 μA ≤ I_{OUT} ≤ 150 mA)	Reg_{load}	–	5.0	30	mV
Line Regulation (6.0 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 5.0 mA)	Reg_{line}	–	5.0	20	mV
Current Limit	I_{lim}	255	400	–	mA
Thermal Shutdown (Guaranteed by Design)	T_{Jmax}	150	180	210	°C
Quiescent Current (V_{IN} = 13.5 V, I_{OUT} = 100 μA, 150 mA, ENABLE = 2.0 V) (ENABLE = 0 V)	I_Q	 – –	 100 –	 150 1.0	μA
$\overline{\text{RESET}}$					
Threshold Voltage	–	4.50	4.65	4.75	V
Output Low (R_{LOAD} = 10 k to V_{OUT}, V_{OUT} = 1.0 V)	–	–	0.2	0.4	V
Output High (R_{LOAD} = 10 k to GND)	–	$V_{OUT} -$ 0.4	$V_{OUT} -$ 0.2	–	V
Power On Reset Delay Time (V_{IN} = 13.5 V, R_{Delay} = 60 k, I_{OUT} = 5.0 mA) (V_{IN} = 13.5 V, R_{Delay} = 120 k, I_{OUT} = 5.0 mA) V_{IN} = 13.5 V, R_{Delay} = 500 k, I_{OUT} = 5.0 mA)	t_D	 2.0 – –	 3.0 6.0 25	 4.0 – –	ms
Watchdog Input					
Threshold	WDI_{high}	30	50	70	$\%V_{OUT}$
Hysteresis	WDI_{hys}	25	100	–	mV
Input Current (WDI = 6.0 V)	–	–	0.1	2.0	μA
Wake Up Rising Edge to WDI Falling Edge Delay Wake Up WDI 	–	5.0	–	–	μs
ENABLE (Note 6)					
Input Threshold Logic Low Logic High	$V_{th(EN)}$	 – 2.0	 – –	 0.8 –	V
Input Current (ENABLE = 2.0 V)	–	–	3.0	10	μA

5. Measured when the output voltage has dropped 2% from the nominal value.
6. If ENABLE is connected to V_{IN}, a 20 kΩ resistor must be placed in series.

ELECTRICAL CHARACTERISTICS (continued) ($-40°C \le T_J \le 150°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Wake Up Output ($V_{IN} = 14\ V$, $I_{OUT} = 5.0\ mA$)					
Wake Up Period ($R_{DELAY} = 60\ k$) ($R_{DELAY} = 120\ k$) ($R_{DELAY} = 500\ k$)	–	 18 – –	 25 50 208	 32 – –	ms
Wake Up Duty Cycle Nominal	–	45	50	55	%
$\overline{RESET}$ HIGH to Wake Up Rising Delay Time ($R_{DELAY} = 60\ k$) 50% $\overline{RESET}$ Rising Edge to 50% Wake Up Edge ($R_{DELAY} = 120\ k$) ($R_{DELAY} = 500\ k$)	–	 9.0 – –	 12.5 25 104	 16 – –	ms
Wake Up Response to Watchdog Input 50% WDI Falling Edge to 50% Wake Up Falling Edge	–	–	0.1	5.0	μs
Wake Up Response to $\overline{RESET}$ 50% $\overline{RESET}$ Falling Edge to 50% Wake Up Falling Edge ($V_{OUT} = 5.0\ V \rightarrow 4.5\ V$)	–	–	0.1	5.0	μs
Output Low ($R_{LOAD} = 10\ k$)	–	–	0.2	0.4	V
Output High ($R_{LOAD} = 10\ k$)	–	$V_{OUT} - 0.5$	$V_{OUT} - 0.25$	–	V
Delay					
Output Voltage ($R_{DELAY} = 60\ k, 120\ k, 500\ k$)	–	–	0.48	–	V

DEFINITION OF TERMS

Dropout Voltage: The input−to−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current with no load.

Current Limit: Peak current that can be delivered to the output.

TIMING DIAGRAMS

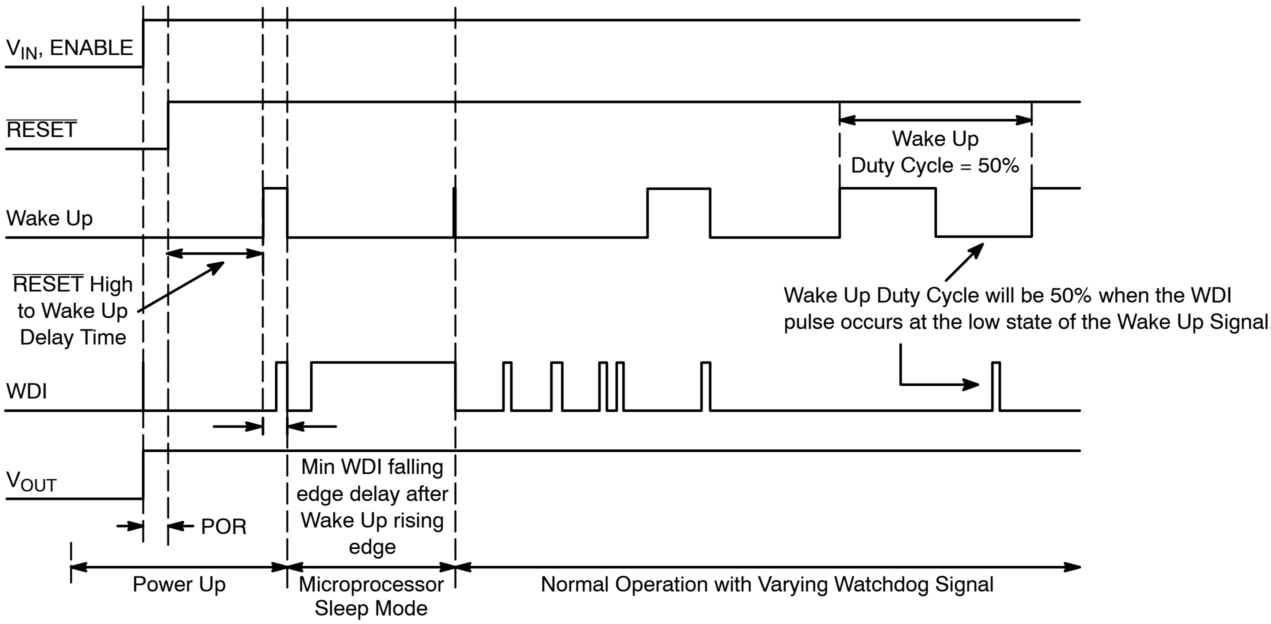


Figure 2. Power Up, Sleep Mode and Normal Operation

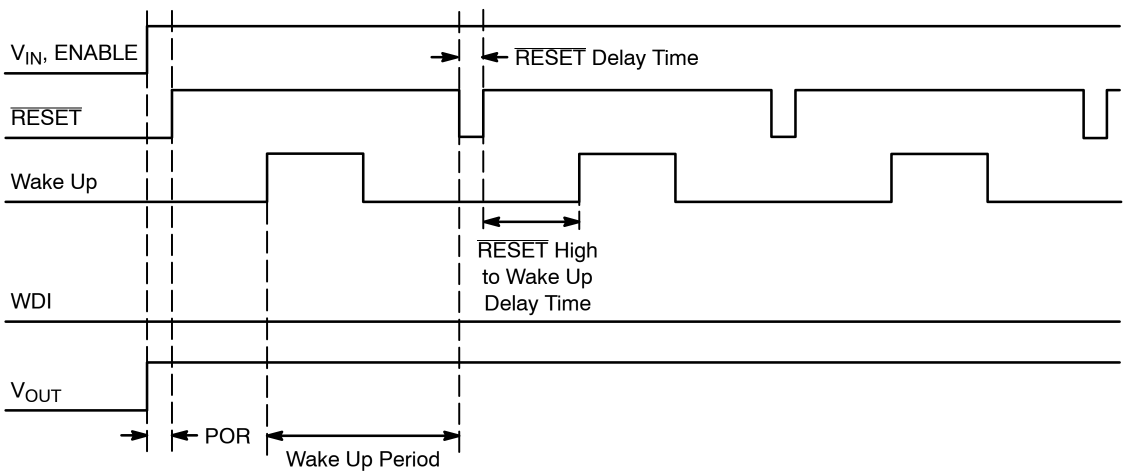


Figure 3. Error Condition: Watchdog Remains Low and a RESET is Issued

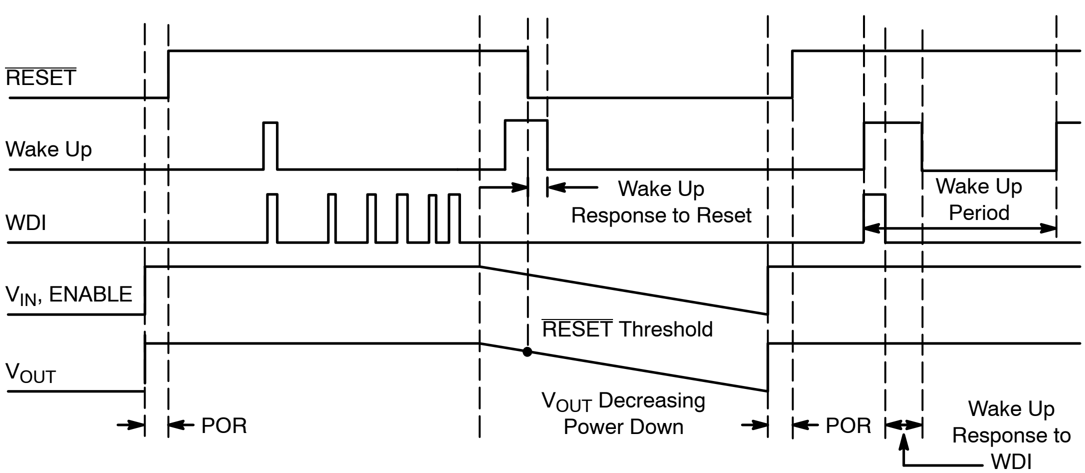


Figure 4. Power Down, Restart Sequence, and Wake Up Response to WDI

TYPICAL PERFORMANCE CHARACTERISTICS

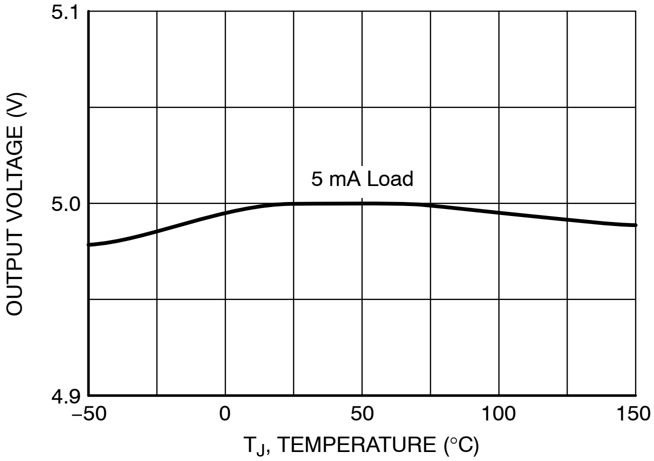


Figure 5. Output Voltage vs. Temperature

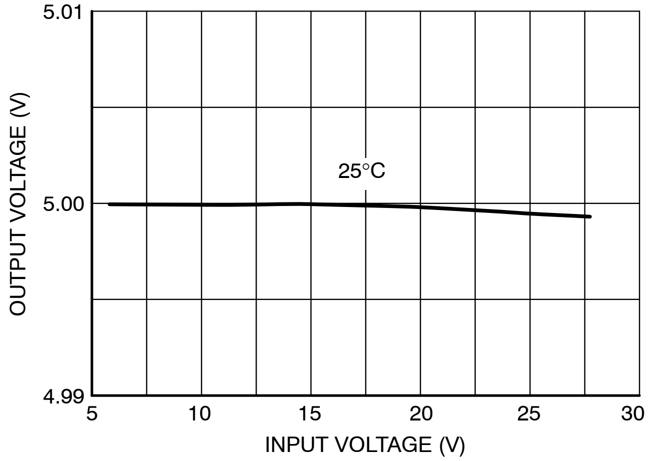


Figure 6. Output Voltage vs. Input Voltage

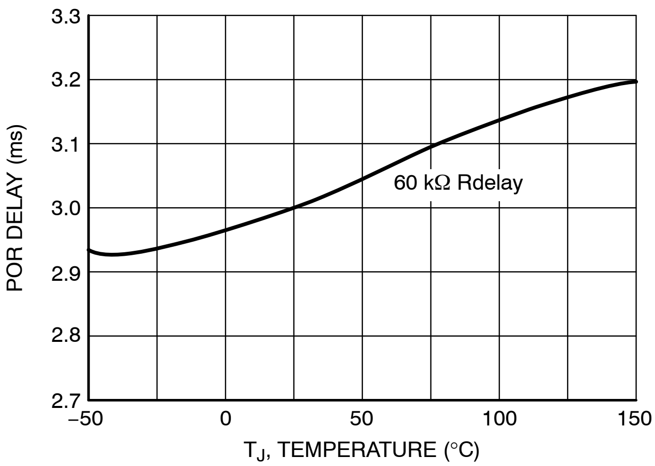


Figure 7. POR Delay vs. Temperature, 60 kΩ Rdelay

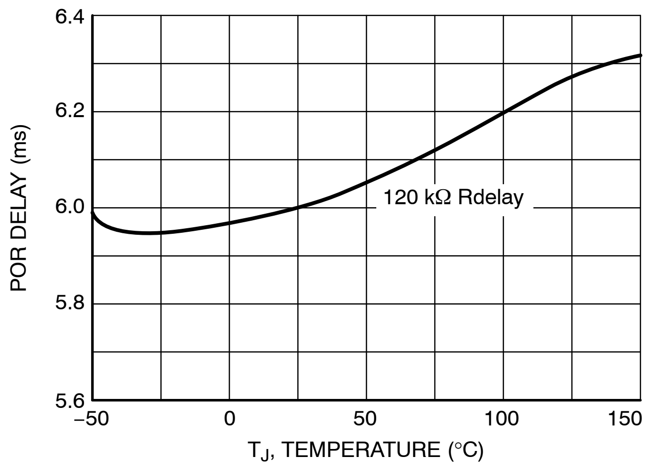


Figure 8. POR Delay vs. Temperature, 120 kΩ Rdelay

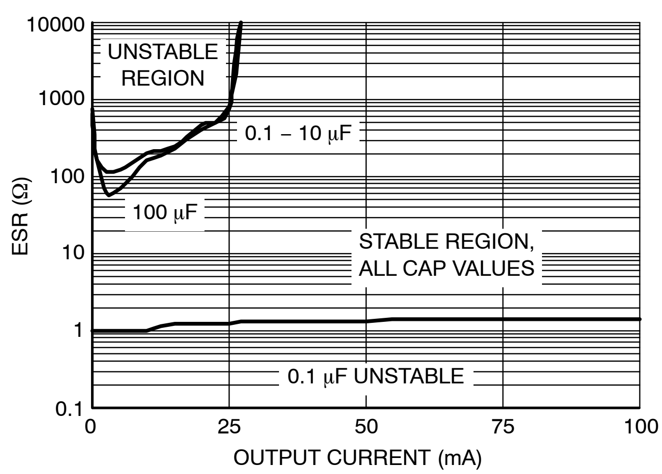


Figure 9. Stability Region of Capacitive ESR vs. Output Current

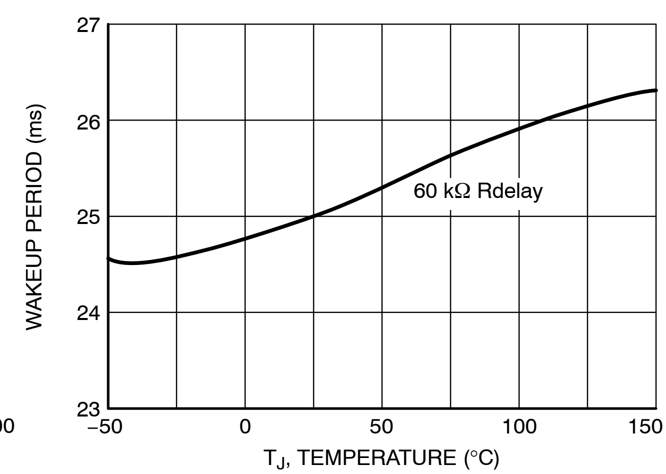


Figure 10. Wakeup Period vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

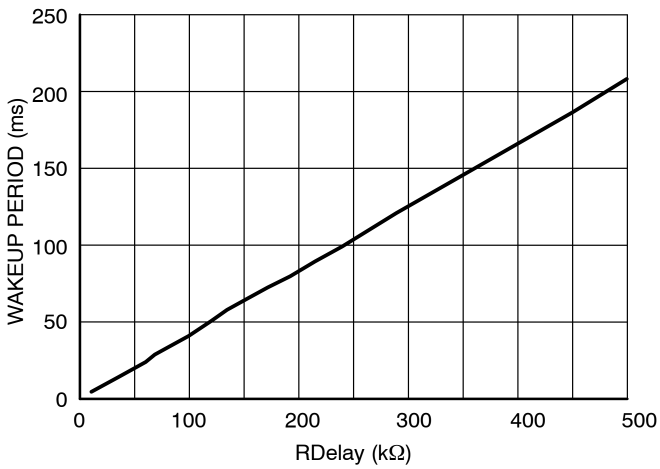


Figure 11. Wakeup Period vs. RDelay

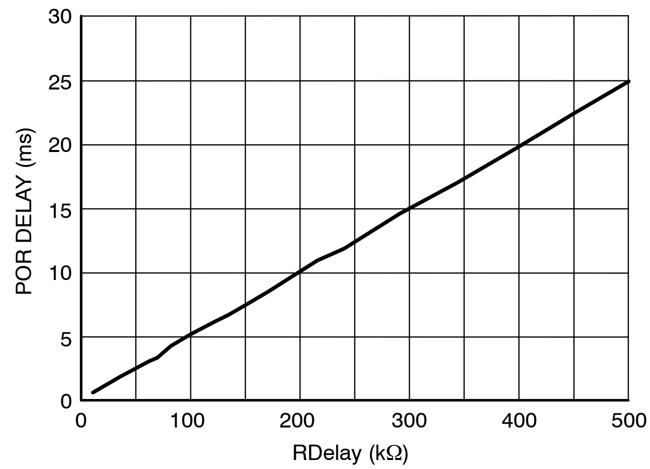


Figure 12. POR Delay vs. RDelay

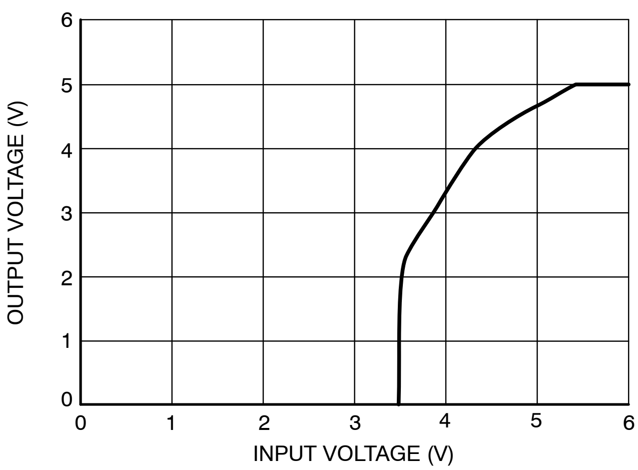


Figure 13. Output Voltage vs. Input Voltage, 5 mA Load

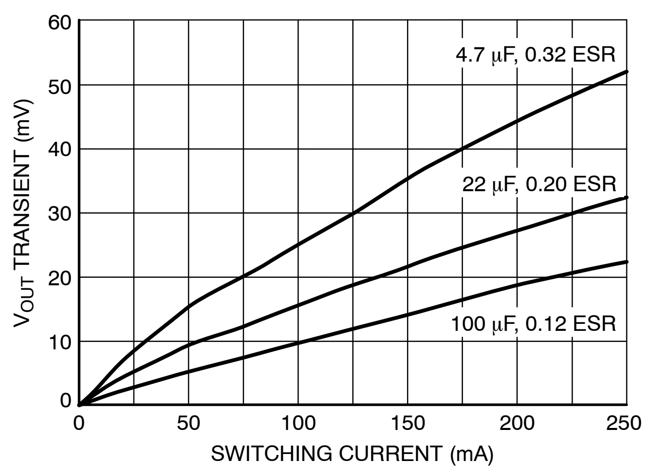


Figure 14. Load Transient Response

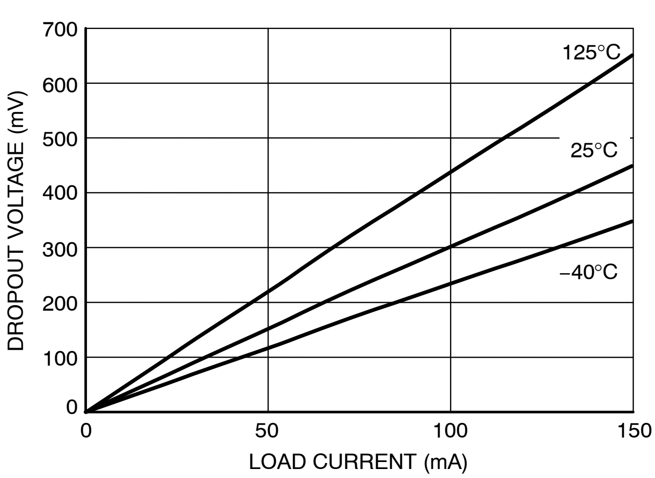


Figure 15. Dropout Voltage vs. Output Current

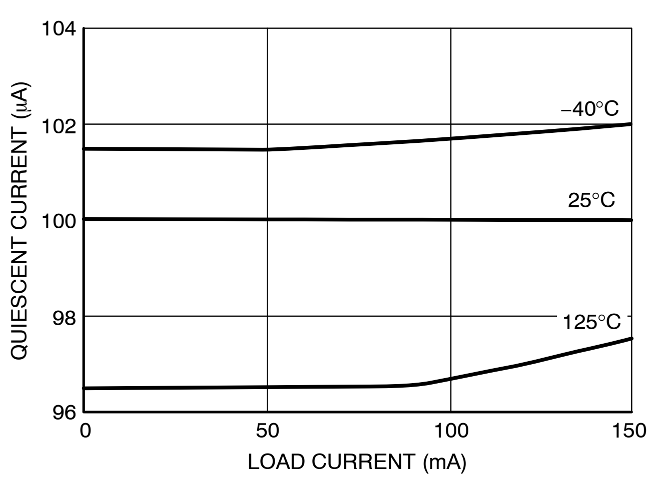


Figure 16. Quiescent Current vs. Output Current

OPERATING DESCRIPTION

General

The NCV8518 is a precision micropower voltage regulator featuring low quiescent current (100 μA typical at 250 mA load) and low dropout voltage (450 mV typical at 150 mA). Integrated microprocessor control functions include Watchdog, Wakeup and $\overline{\text{RESET}}$. An Enable input is provided for logic level control of the regulator state. The combination of low quiescent current and comprehensive microprocessor interface functions make the NCV8518 ideal for use in both battery operated and automotive applications.

The NCV8518 is internally protected against short circuit and thermal runaway conditions. No external components are required to engage these protective mechanisms. The device continues to operate through 45 volt input transients, an important consideration in automotive environments.

Wakeup and Watchdog

To reduce battery drain, a microprocessor or microcontroller can transition to a low current consumption (“sleep”) mode when code execution is suspended or complete. The NCV8518 Wakeup signal is generated and output periodically to interrupt sleep mode. The nominal Wakeup output is a 5 volt square wave (generated from VOUT) with a duty cycle of 50%, at a frequency determined by external timing resistor R_{DELAY}. In response to the rising edge of the Wakeup signal, the microprocessor will subsequently output a Watchdog pulse and check its inputs to decide if it should resume normal operation or remain in sleep mode.

The NCV8518 responds to the falling edge of the Watchdog signal, which it expects at least once during each Wakeup period. When the correct Watchdog signal is received, the Wakeup output is forced low. Other Watchdog pulses received within the same cycle are ignored. The Watchdog circuitry continuously monitors the input Watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wakeup cycle will cause a Reset pulse to be output at the end of the Wakeup cycle (see Figure 4).

$\overline{\text{RESET}}$

As output voltage falls, the $\overline{\text{RESET}}$ output will maintain its current state down to V_{OUT} = 1 V. A Reset signal (active low) is asserted for any of four conditions:

1. During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation.
2. During operation, if the output voltage falls below the Reset threshold, $\overline{\text{RESET}}$ switches low, and will remain low until both the output voltage has recovered and the Reset delay timer cycle has completed following that recovery.
3. $\overline{\text{RESET}}$ will switch low if the regulator does not receive a Watchdog input signal within a Wakeup period.
4. Regardless of output voltage, $\overline{\text{RESET}}$ will switch low if the regulator input voltage V_{IN}, falls below a level required to sustain the internal control circuits. The specific voltage is temperature dependent, and is approximately 4.75 V at 20°C.

The Wakeup output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wakeup cycle begins again (see Figure 4).

The $\overline{\text{RESET}}$ Delay Time, Wakeup signal frequency and $\overline{\text{RESET}}$ high to Wakeup delay time are all set by one external resistor, RDelay, according to the following equations:

$$\text{Wakeup Period (seconds)} = (4.17 \times 10^{-7}) * R_{DELAY}\ (\Omega)$$

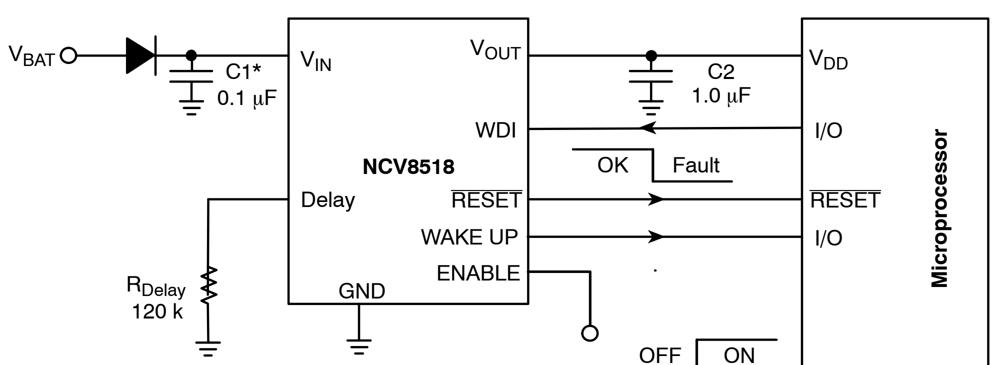
$$\overline{\text{RESET}}\ \text{Delay Time (seconds)} = (5.21 \times 10^{-8}) * R_{DELAY}\ (\Omega)$$

$$\overline{\text{RESET}}\ \text{High to Wakeup Delay Time (seconds)} = (2.08 \times 10^{-7}) * R_{DELAY}\ (\Omega)$$

The voltage present at the Delay pin is a buffered bandgap voltage (~1.25 V) and can be used as a reference for an external tracking regulator.

Enable

This is a standard TTL and CMOS logic compatible input that can be used to turn the regulator on or off. Logic high enables the regulator; logic low disables it (also called *shutdown*). In the disabled/shutdown state, the pass transistor is off and total quiescent current is less than 1 μA.

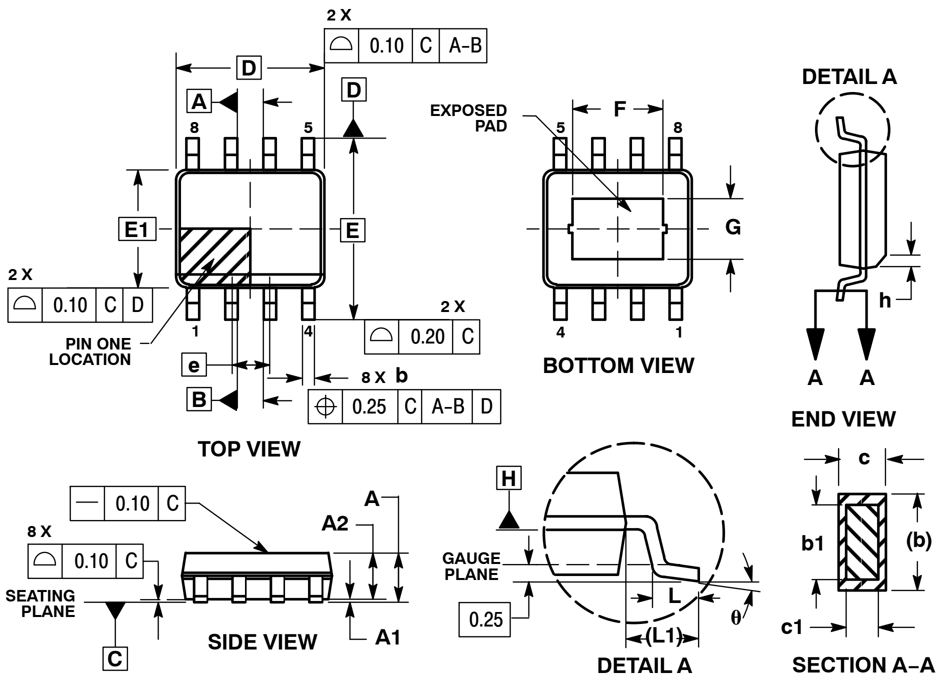


*C1 required if regulator is located far from power supply filter.

Figure 17. Application Circuit

PACKAGE DIMENSIONS

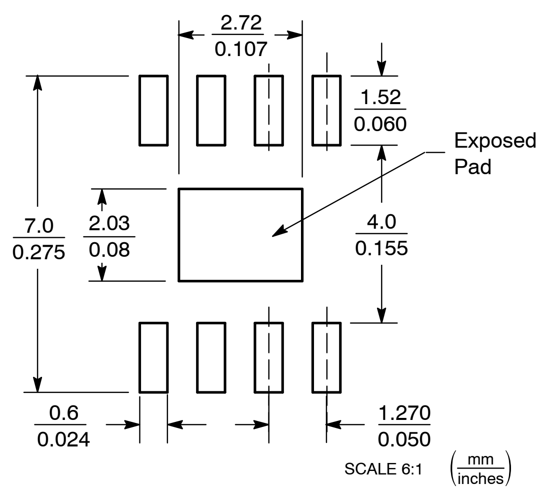
SOIC−8 EP
D SUFFIX
CASE 751AC−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

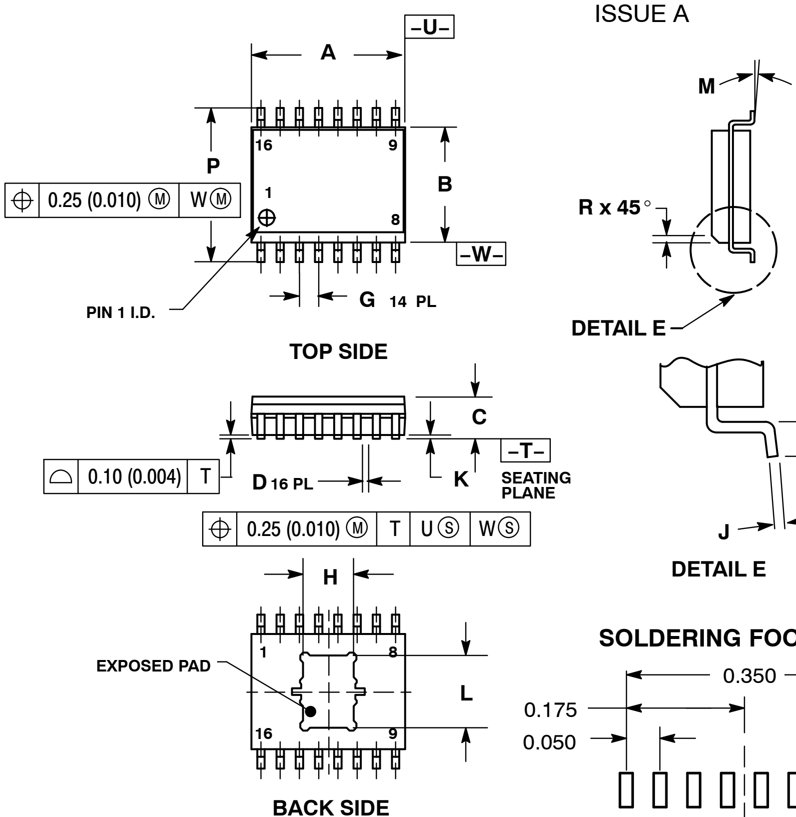
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

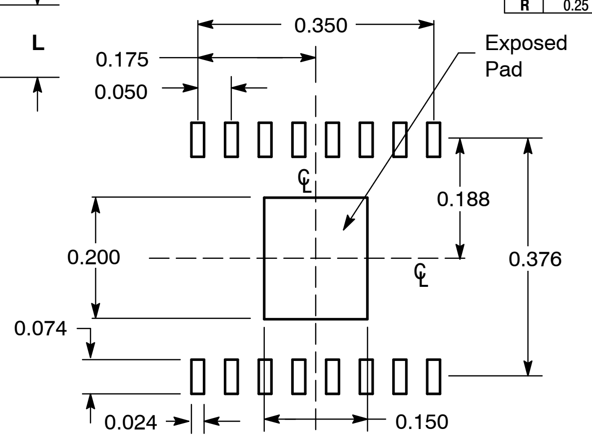
SOIC−16 LEAD WIDE BODY, EXPOSED PAD
PDW SUFFIX
CASE 751AG−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R−01 OBSOLETE, NEW STANDARD 751R−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SOLDERING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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