Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in **Table 1**. Keep V_{IN} and V_{OUT} within the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Current Drain per Pin (Excluding V_{DD} and V_{SS})	I	25	mA
Input Voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
EPROM Programming Voltage	V_{PP}	16.75	V
Storage Temperature Range	T_{STG}	–65 to +150	°C

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***5.0 V DC Electrical Characteristics*** on page 135 *and* ***3.3 V DC Electrical Characteristics*** on page 136 *for guaranteed operating conditions.*

Operating Temperature Range

Table 2. Operating Temperature Range

Package Type	Symbol	Value	Unit
MC68HC705P9P[1], DW[2], S[3] (Standard) MC68HC705P9C[4]P, CDW, CS (Extended) MC68HC705P9V[5]P, VDW, VS (Automotive) MC68HC705P9M[6]P, MDW, MS (Automotive)	T_A	T_L to T_H 0 to 70 –40 to +85 –40 to +105 –40 to +125	°C

1. P = Plastic dual in-line package (PDIP)
2. DW = Small outline integrated circuit (SOIC)
3. S = Ceramic dual in-line package (Cerdip)
4. C = Extended temperature range (–40 to +85 °C)
5. V = Automotive temperature range (–40 to +105 °C)
6. M = Automotive temperature range (–40 to +125 °C)

Thermal Characteristics

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Dual In-Line Package (PDIP) Small Outline Integrated Circuit (SOIC) Ceramic Dual In-Line Package (Cerdip)	θ_{JA}	 60 60 60	°C/W

Power Considerations

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:

T_A = ambient temperature in °C
θ_{JA} = package thermal resistance, junction to ambient in °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$ = chip internal power dissipation
$P_{I/O}$ = power dissipation on input and output pins (user-determined)

For most applications, $P_{I/O} \ll P_{INT}$ and can be neglected.

Ignoring $P_{I/O}$, the relationship between P_D and T_J is approximately:

$$P_D = \frac{K}{T_J + 273\ °C} \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273\,°C) + \theta_{JA} \times (P_D)^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

5.0 V DC Electrical Characteristics

Table 4. DC Electrical Characteristics (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Typ[2]	Max	Unit
Output Voltage I_{LOAD} = 10.0 µA I_{LOAD} = −10.0 µA	V_{OL} V_{OH}	— V_{DD} − 0.1	— —	0.1 —	V
Output High Voltage (I_{LOAD} = −0.8 mA) PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, TCMP	V_{OH}	V_{DD} − 0.8	—	—	V
Output Low Voltage (I_{LOAD} = 1.6 mA) PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, TCMP	V_{OL}	—	—	0.4	V
Input High Voltage PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, PD7/TCAP, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, PD7/TCAP, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current[3] [4] [5] [6] Run Mode Wait Mode (ADC On) Wait Mode (ADC Off) Stop Mode 25 °C 0 to 70 °C (Standard) −40 to 125 °C	I_{DD}	 — — — — — —	 4.7 2.1 1.3 2 — —	 6.5 2.9 1.9 30 50 100	 mA mA mA µA µA µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5	I_{IL}	—	—	±10	µA
ADC Ports Hi-Z Leakage Current	I_{OZ}	—	—	±1	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, PD7/TCAP	I_{IN}	—	—	±1	µA
Capacitance Ports (As Inputs or Outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}	C_{OUT} C_{IN}	— —	— —	12 8	pF
Programming Voltage	V_{PP}	16.25	16.5	16.75	V
Programming Current	I_{PP}	—	5	10	mA
Programming Time per Byte	t_{EPGM}	4	—	—	ms

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted
2. Typical values at midpoint of voltage range, 25 °C only
3. Run mode and wait mode I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode and stop mode I_{DD} measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} − 0.2 V
5. Stop mode I_{DD} measured with OSC1 = V_{SS}
6. Wait mode I_{DD} affected linearly by OSC2 capacitance

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3.3 V DC Electrical Characteristics

Table 5. DC Electrical Characteristics (V_{DD} = 3.3 Vdc)[1]

Characteristic	Symbol	Min	Typ[2]	Max	Unit
Output Voltage ($I_{LOAD} \leq 10.0\ \mu A$)	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output High Voltage ($I_{LOAD} = -0.2$ mA) PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, TCMP	V_{OH}	$V_{DD} - 0.3$	—	—	V
Output Low Voltage ($I_{LOAD} = 0.4$ mA) PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, TCMP	V_{OL}	—	—	0.3	V
Input High Voltage PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, PD7/TCAP, $\overline{IRQ}/V_{PP}$, $\overline{RESET}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input Low Voltage PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5, PD7/TCAP, $\overline{IRQ}/V_{PP}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Data-Retention Mode Supply Voltage	V_{RM}	2.0	—	—	V
Supply Current[3] [4] [5] [6]					
Run Mode	I_{DD}	—	1.6	2.3	mA
Wait Mode (ADC On)		—	0.9	1.3	mA
Wait Mode (ADC Off)		—	0.4	0.6	mA
Stop Mode					
25 °C		—	1.0	20	µA
0 to 70 °C (Standard)		—	—	40	µA
–40 to 125 °C		—	—	50	µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7/SCK–PB5/SDO, PC7/V_{RH}–PC0, PD5	I_{IL}	—	—	±10	µA
Input Current $\overline{RESET}$, $\overline{IRQ}/V_{PP}$, OSC1, PD7/TCAP	I_{IN}	—	—	±1	µA
Capacitance					
Ports (As Inputs or Outputs)	C_{OUT}	—	—	12	pF
$\overline{RESET}$, $\overline{IRQ}/V_{PP}$	C_{IN}	—	—	8	

1. V_{DD} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H unless otherwise noted
2. Typical values at midpoint of voltage range, 25 °C only
3. Run mode and wait mode I_{DD} measured using external square wave clock source (f_{OSC} = 2.1 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode and stop mode I_{DD} measured with all ports configured as inputs; V_{IL} = 0.2 V; $V_{IH} = V_{DD} - 0.2$ V
5. Stop mode I_{DD} measured with OSC1 = V_{SS}
6. Wait mode I_{DD} affected linearly by OSC2 capacitance

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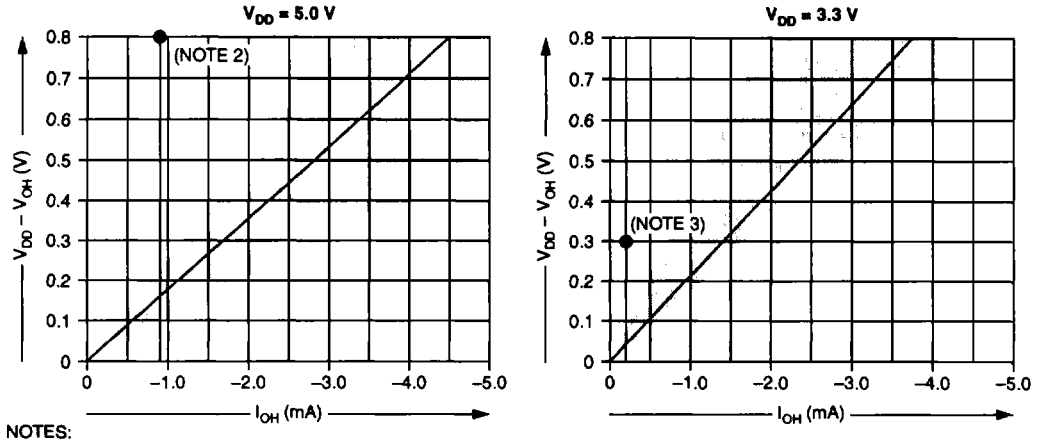
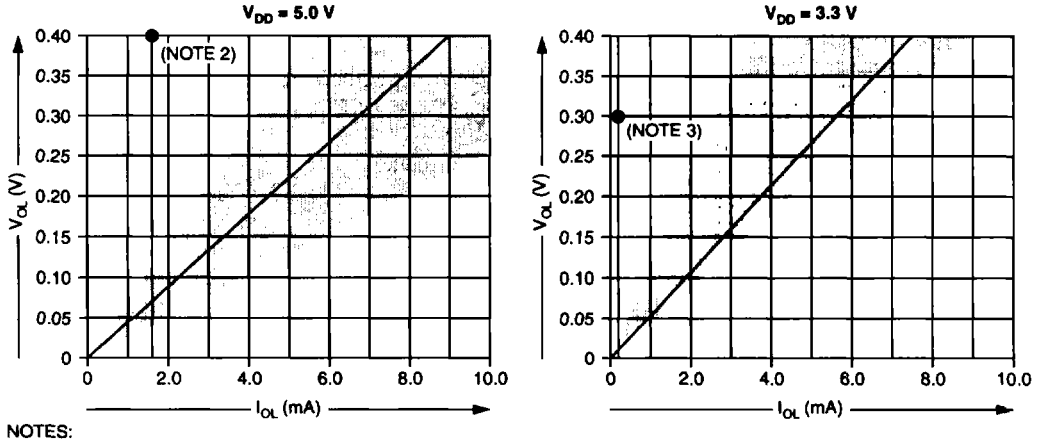
Driver Characteristics



NOTES:
1. Shaded area indicates variation in driver characteristics due to changes in temperature and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 800$ mV @ $I_{OL} = -0.8$ mA.
3. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 300$ mV @ $I_{OL} = -0.2$ mA.

Figure 1. Typical High-Side Driver Characteristics



NOTES:
1. Shaded area indicates variation in driver characteristics due to changes in temperature and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 400$ mV @ $I_{OL} = 1.6$ mA.
3. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 300$ mV @ $I_{OL} = 0.4$ mA.

Figure 2. Typical Low-Side Driver Characteristics

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Typical Supply Current vs. Internal Clock Frequency

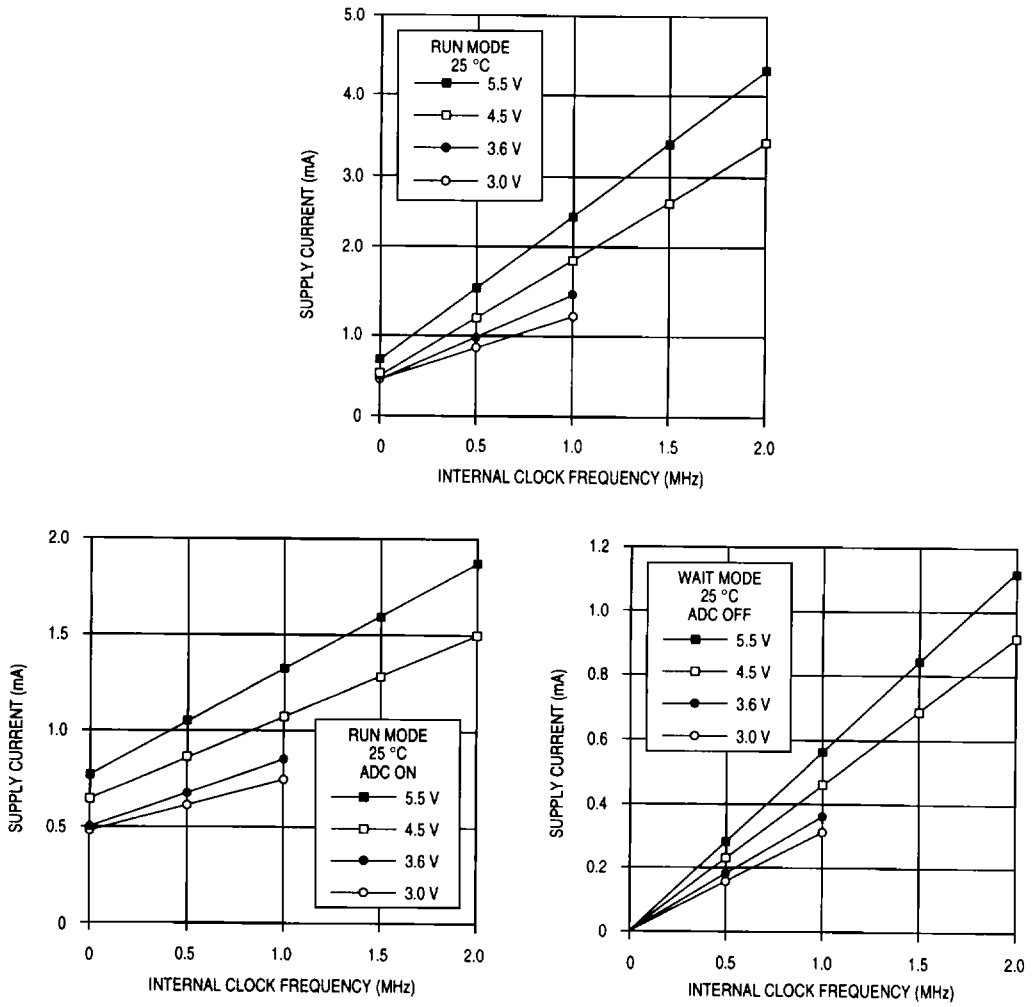

Figure 3. Typical Supply Current vs. Internal Clock Frequency

Maximum Supply Current vs. Internal Clock Frequency

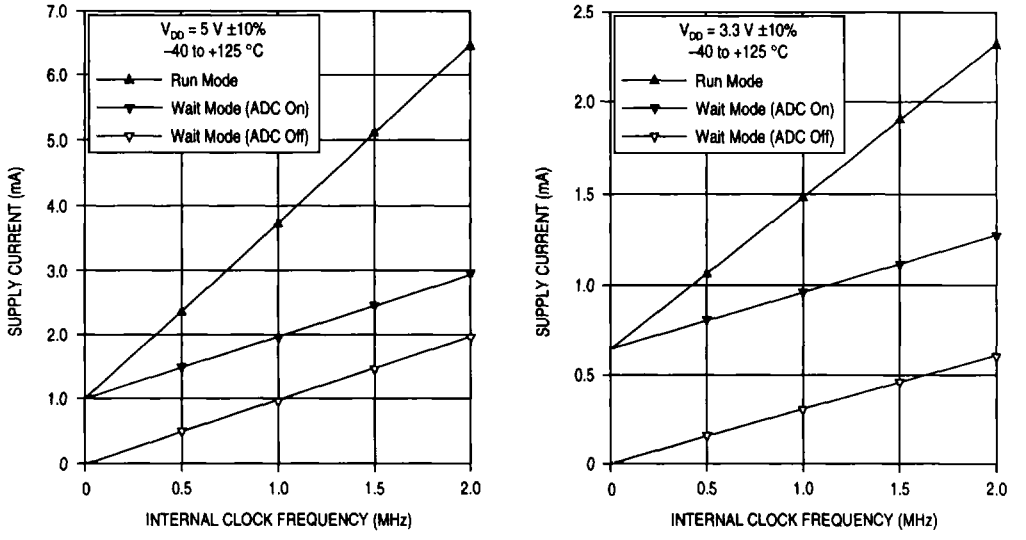

Figure 4. Maximum Supply Current vs. Internal Clock Frequency

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5.0 V Control Timing

Table 6. Control Timing (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{OSC}	— dc	4.2 4.2	MHz
Internal Operating Frequency (f_{OSC} ÷ 2) Crystal External Clock	f_{OP}	— dc	2.1 2.1	MHz
Cycle Time (1 ÷ f_{OP})	t_{CYC}	480	—	ns
Crystal Oscillator Startup Time	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution[2] Input Capture Pulse Width Input Capture Pulse Period	 t_{RESL} t_H, t_L t_{TLTL}	 4.0 125 Note[3]	 — — —	 t_{CYC} ns t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
Interrupt Pulse Period	t_{ILIL}	Note[4]	—	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	—	ns
RC Oscillator Stabilization Time	t_{RCON}	—	5	µs
ADC On Current Stabilization Time	t_{ADON}	—	100	µs

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted
2. A 2-bit prescaler in the timer is the limiting factor as it counts 4 t_{CYC}
3. The minimum t_{TLTL} should not be less than the number of interrupt service routine cycles plus 19 t_{CYC}
4. The minimum t_{ILIL} should not be less than the number of interrupt service routine cycles plus 19 t_{CYC}

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3.3 V Control Timing

Table 7. Control Timing (V_{DD} = 3.3 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{OSC}	— dc	2.0 2.0	MHz
Internal Operating Frequency (f_{OSC} ÷ 2) Crystal External Clock	f_{OP}	— dc	1.0 1.0	MHz
Cycle Time (1 ÷ f_{OP})	t_{CYC}	1	—	ms
Crystal Oscillator Startup Time	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution[2] Input Capture Pulse Width Input Capture Pulse Period	 t_{RESL} t_H, t_L t_{TLTL}	 4.0 250 Note[3]	 — — —	 t_{CYC} ns t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	250	—	ns
Interrupt Pulse Period	t_{ILIL}	Note[4]	—	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	—	ns

1. V_{DD} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted
2. A 2-bit prescaler in the timer is the limiting factor as it counts 4 t_{CYC}
3. The minimum t_{TLTL} should not be less than the number of interrupt service routine cycles plus 19 t_{CYC}
4. The minimum t_{ILIL} should not be less than the number of interrupt service routine cycles plus 19 t_{CYC}

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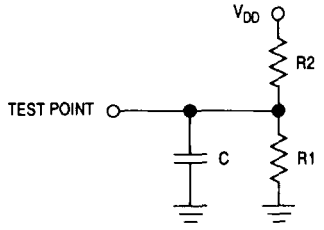
Test Load



PINS	R1	R2	C
PA7–PA0	3.26 kΩ	2.38 kΩ	50 pF
PB7/SCK–PB5/SDO			
PC7/V_{RH}–PC0			

Figure 5. Test Load

Mechanical Specifications

The MC68HC705P9 is available in the following packages:

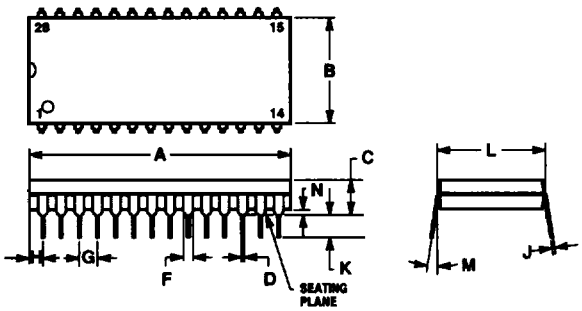
- 710 — Plastic dual in-line package (PDIP)
- 733 — Ceramic dual in-line package (Cerdip)
- 751F — Small outline integrated circuit (SOIC)

The following figures show the latest packages at the time of this publication. To make sure that you have the latest package specifications, contact one of the following:

- Local Motorola Sales Office
- Motorola Mfax
  - Phone 602-244-6609
  - EMAIL rmfax0@email.sps.mot.com
- Worldwide Web (wwweb) at http://design-net.com

Follow Mfax or wwweb on-line instructions to retrieve the current mechanical specifications.

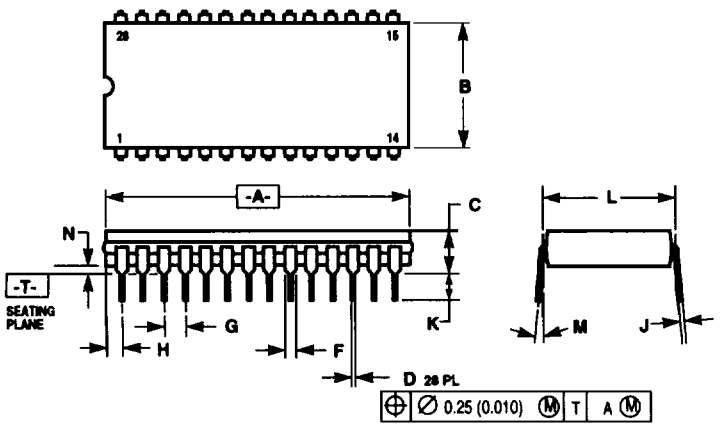
28-Pin PDIP —
Case #710



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

28-Pin Cerdip —
Case #733



NOTES:
1. DIMENSIONS A AND B INCLUDES MENISCUS.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.490	36.45	37.84
B	0.500	0.605	12.70	15.36
C	0.160	0.230	4.06	5.84
D	0.015	0.022	0.38	0.55
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.160	3.18	4.06
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.050	0.51	1.27

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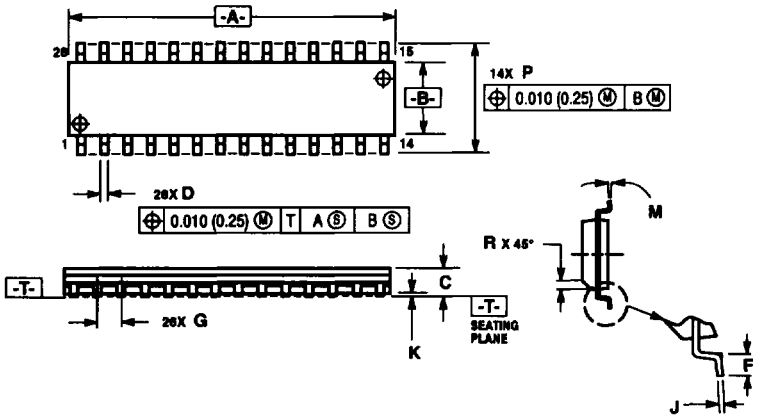
28-Pin SOIC — Case #751F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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