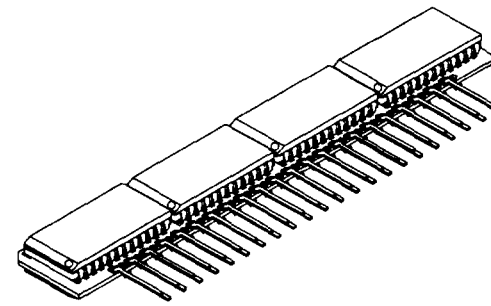
DPS8256P8

256K X 8 CMOS SRAM MODULE



DESCRIPTION:

The DPS8256P8-25, -35, -45, -55 is a high speed 256K x 8 Static Random Access Memory (SRAM) module constructed on an epoxy laminate substrate using eight 256K x 1 CMOS RAM's in plastic surface mount packages. The DPS8256P8 features separate data inputs and outputs and is intended for use in applications where high speed is required and board space is of prime concern.

PIN NAMES	
A0-A17	Address Inputs
DI0-DI7	Data In
DO0-DO7	Data Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FEATURES:

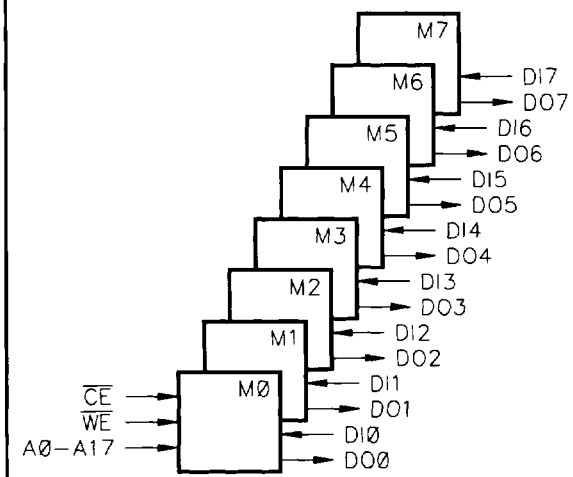
- Fast Access Times:
  - DPS8256P8-25 - 25ns (max.)
  - DPS8256P8-35 - 35ns (max.)
  - DPS8256P8-45 - 45ns (max.)
  - DPS8256P8-55 - 55ns (max.)
- Fully Static Operation; No Clock or Refresh Required
- Low Operating Power 6.2 watts (Typical)
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Separate Data Input and Output
- On Board Decoupling Capacitors
- Space Efficient 44-Pin ZIP Design

PIN-OUT DIAGRAM

BOTTOM VIEW

INDEX →			1	VSS
VDD	2		3	DI1
DIØ	4		5	DO1
DOØ	6		7	A1
AØ	8		9	A3
A2	1Ø		11	A5
A4	12		13	A6
A17	14		15	DI3
VSS	16		17	DO3
DI2	18		19	VDD
DO2	2Ø		21	A7
$\overline{WE}$	22		23	DI5
A8	24		25	DO5
$\overline{CE}$	26		27	VSS
VDD	28		29	A9
DI4	3Ø		31	A16
DO4	32		33	A11
A1Ø	34		35	A13
A12	36		37	DI7
A14	38		39	DO7
A15	4Ø		41	DO6
DI6	42		43	VDD
VSS	44			

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Temperature Range	0		70	°C

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-10 to + 85	°C
V_{DD}	Supply Voltage[1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage[1]	-0.5 to V_{DD} + 0.5	V

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{WE}$	Output	Supply Current
Not Selected	H	X	HIGH-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

L = LOW H = HIGH X = Don't Care

CAPACITANCE[4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	90	pF	V_{IN} = 0V
C_{ADR}	Address Input	90		
C_{WE}	Write Enable	90		
C_{DI}	Data Input	35		
C_{DO}	Data Output	35		

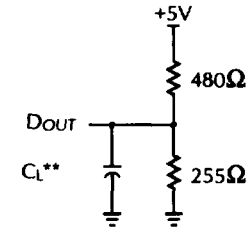
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

Output Load		
Load	C_L	Parameters Measured
1	30 pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{WLZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges					
Symbol	Characteristics	Test Conditions	Commercial		Unit
			Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-40	-40	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		800	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		1120	mA
I_{SB1}	Full Standby Supply Current	$V_{IN} \le$ 0.2V or $V_{IN} \ge V_{DD}$ -0.2V $\overline{CE} \ge V_{DD}$ -0.2V		80	mA
I_{SB2}	Standby Supply	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}		240	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	2.4		V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		ns
2	t_{AA}	Address Access Time (See Figure 1)		25		35		45		55	ns
3	t_{CO}	Chip Enable to Output Valid (See Figure 1)		25		35		45		55	ns
4	t_{OH}	Output Hold from Address Change	5		10		10		10		ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	10		10		10		10		ns
6	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]	0	15	0	20	0	25	0	30	ns
7	t_{AS}	Address Set-up Time***	0		0		0		0		ns

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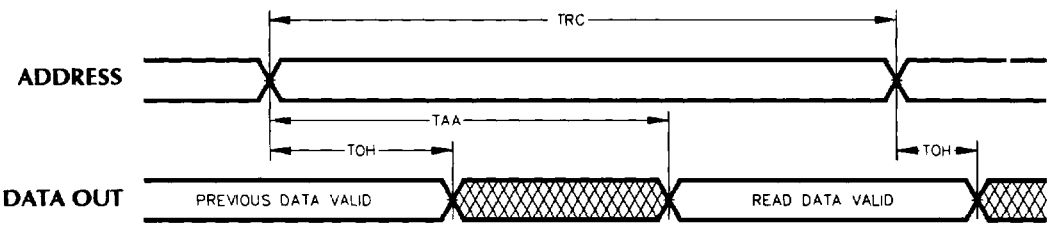
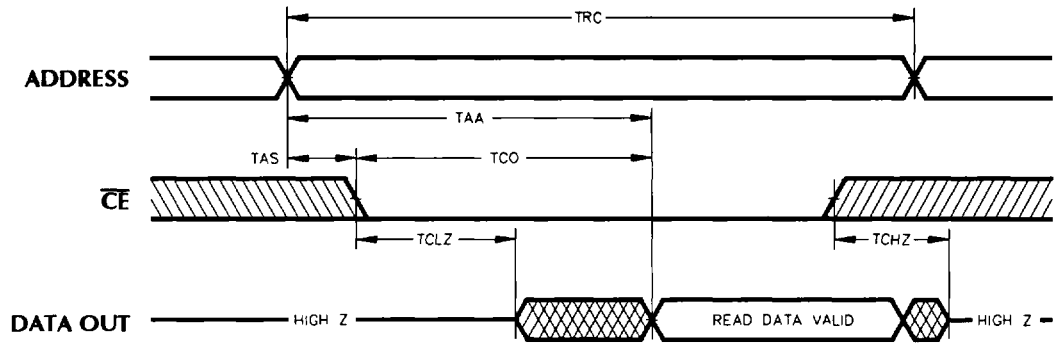
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges											
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t_{WC}	Write Cycle Time	25		35		45		55		ns
9	t_{AW}	Address Valid to End of Write	20		30		40		50		ns
10	t_{CW}	Chip Enable to End of Write	20		30		40		50		ns
11	t_{DW}	Data Valid to End of Write	20		20		30		30		ns
12	t_{DH}	Data Hold Time	0		0		0		0		ns
13	t_{WP}	Write Pulse Width	20		30		40		40		ns
14	t_{AH}	Address Hold Time	0		0		0		0		ns
15	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]	0	15	0	20	0	25	0	25	ns
16	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	5		5		5		5		ns

*** Valid for both Read and Write Cycles.

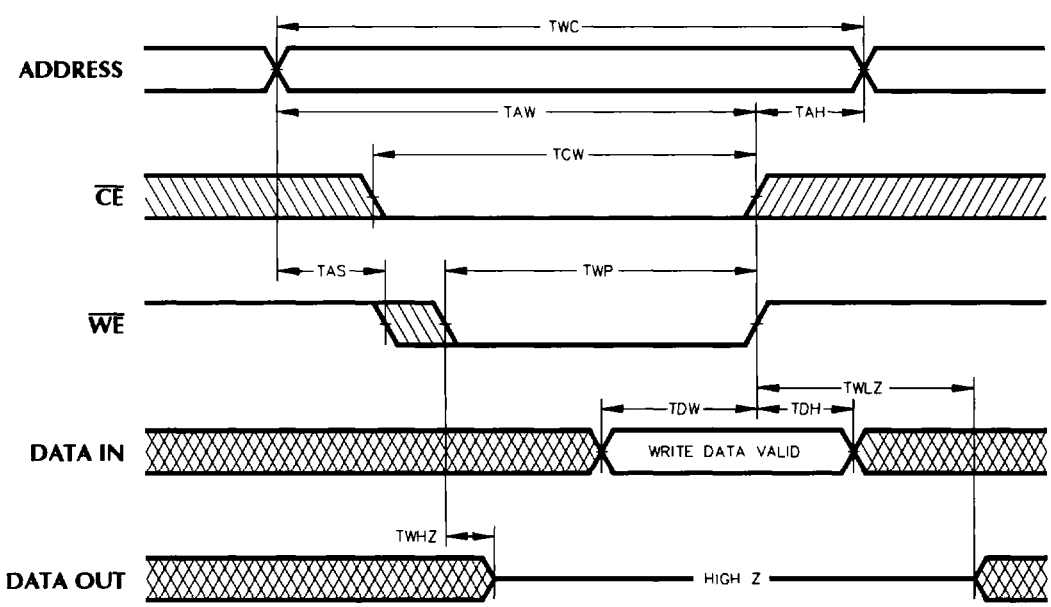
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ is LOW.



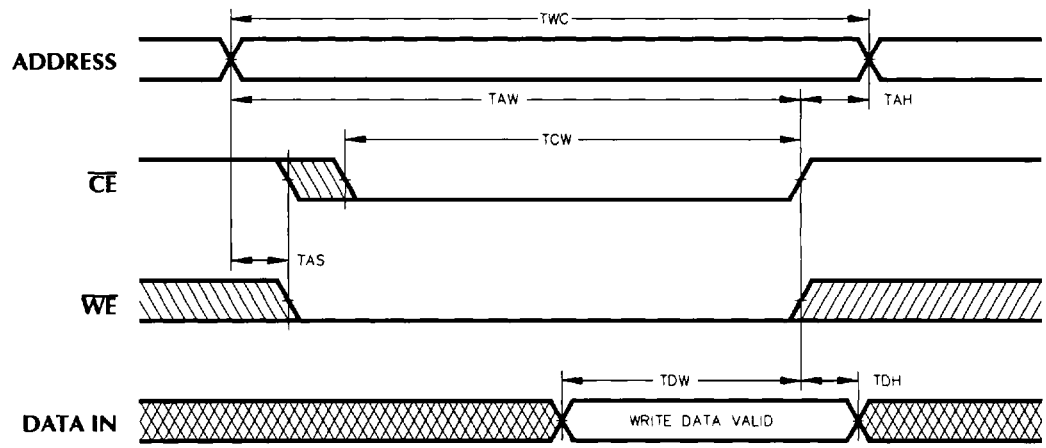
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled.



WRITE CYCLE 2: $\overline{CE}$ Controlled.



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NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage, with specified load shown in Figure 1.

WAVEFORM KEY

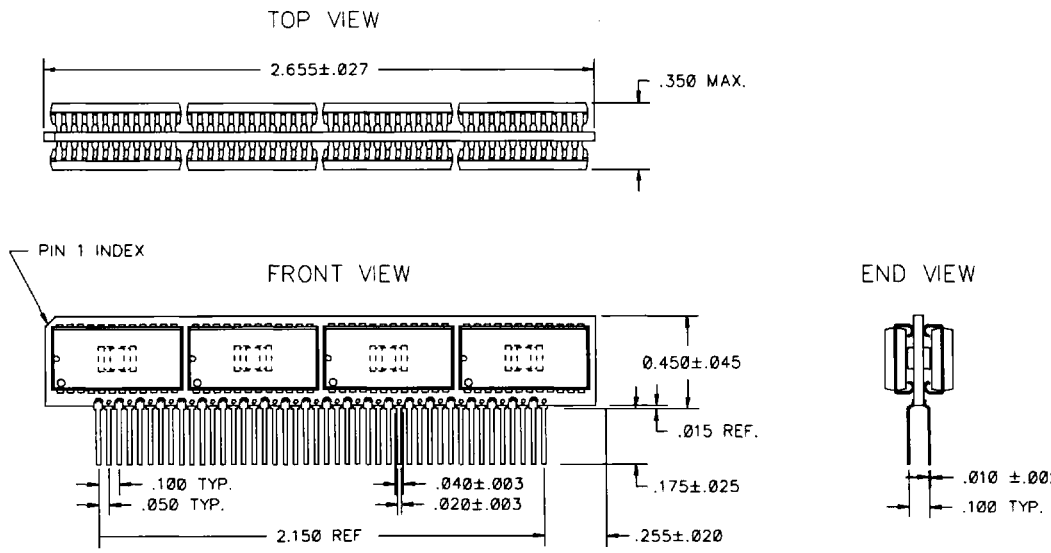
Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION

DP S8256P8 – XX X

PREFIX		
DEVICE TYPE		
SPEED		
GRADE	C	COMMERCIAL 0°C to +70°C
	25	25ns
	35	35ns
	45	45ns
	55	55ns
		256K X 8 CMOS SRAM 44 PIN ZIP MODULE

MECHANICAL DIAGRAM



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