

# 128 Megabit CMOS DDR SDRAM

## DPDD16MX8RSBY5

**DESCRIPTION:**

The Memory Stack™ series is a family of interchangeable memory modules. The 128 Megabit Double Data Rate Synchronous DRAM module is a member of this family which utilizes the space saving LP-Stack™ TSOP stacking technology. The devices are constructed with two 8 Meg x 8 DDR DRAMs.

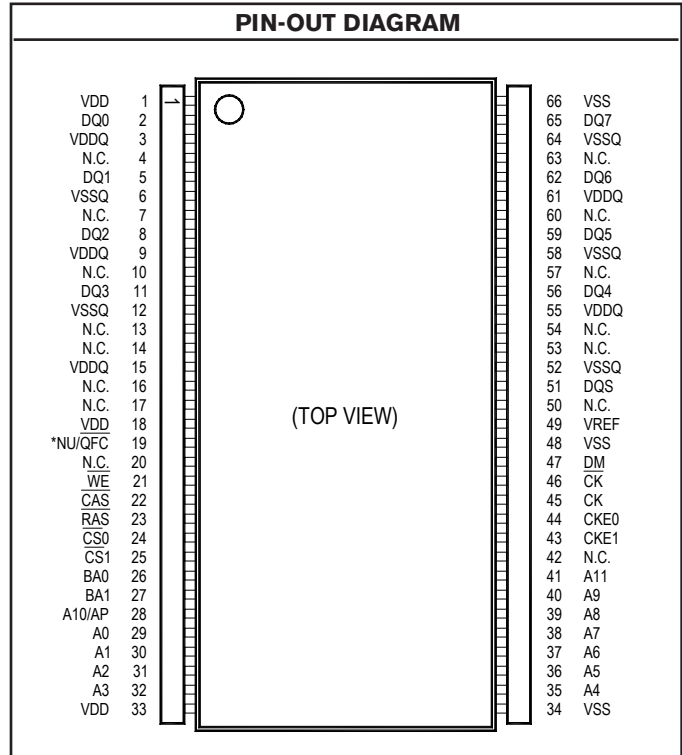
The 64 Megabit based LP-Stack™ module, DPDD16MX8RSBY5, has been designed to fit the same footprint as the 8 Meg x 8 DDR SDRAM TSOP monolithic. This allows for system upgrade without electrical or mechanical redesign, providing an immediate and low cost memory solution.

**FEATURES:**

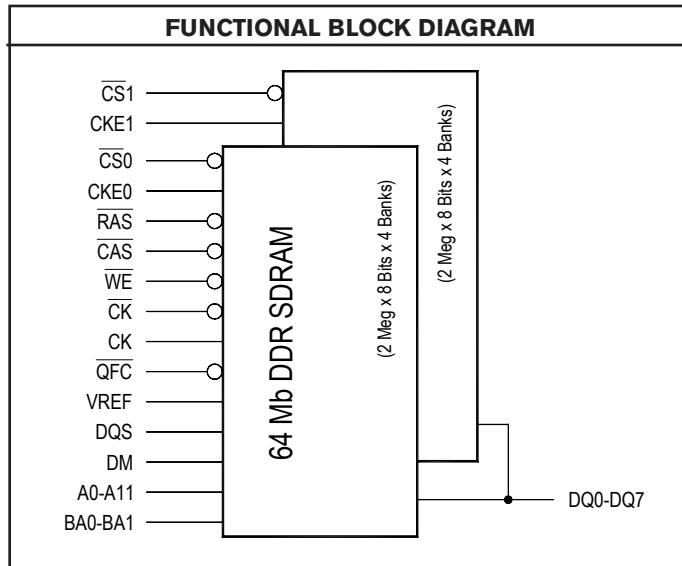
- Configuration Available:  
16 Meg x 8 (2 Banks of 2 Meg x 8 bits x 4 banks)
- Clock Frequency:  
100, 125, 133, 143, 167 MHz
- 2.5 Volt DQ Supply
- JEDEC Standard SSTL\_2 Interface for all Inputs/Outputs
- Four Bank Operation
- Programmable Burst Type:  
Burst Length and Read Latency
- Refresh: 4096 Cycles/64ms
- Refresh Types: Auto and Self
- JEDEC Approved Footprint and Pinout
- IPC-A-610 Manufacturing Standards
- Package: 66-Pin Leaded TSOP Stack

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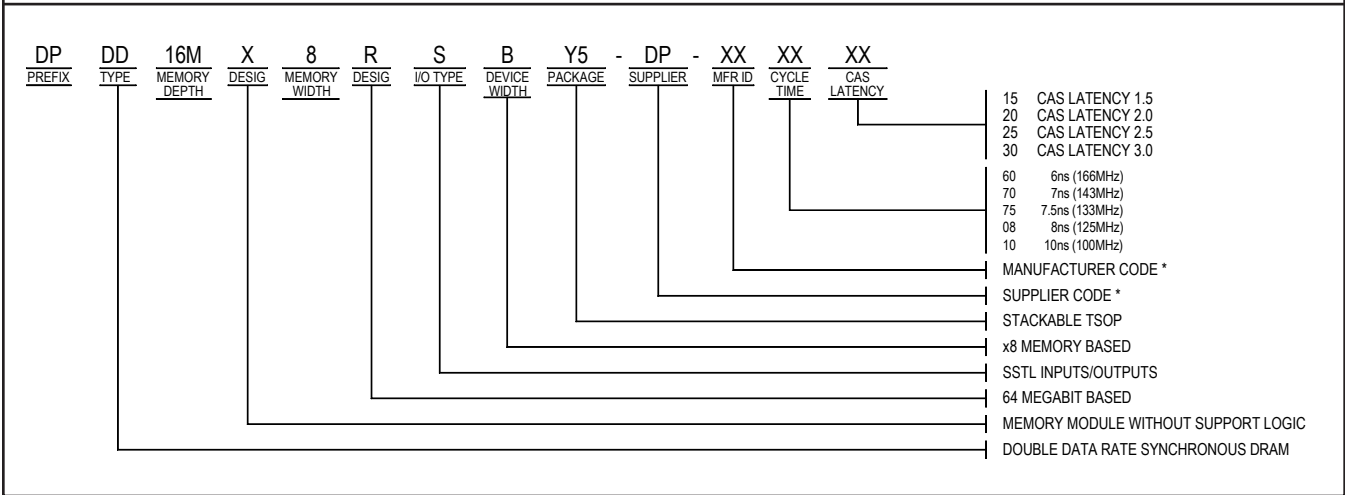
PIN NAMES	
A0-A11	Row Address: A0-A11 Column Address: A0-A8
BA0,BA1	Bank Select Address
A10/AP	Auto Precharge
DQ0-DQ7	Data In/Data Out
CAS	Column Address Strobe
CS0, CS1	Chip Selects
RAS	Row Address Strobe
WE	Data Write Enable
CK, CK	Differential Clock Inputs
CKE0, CKE1	Clock Enables
DQS	Data Strobe
DM	Data Mask
QFC	DQ FET Switch Control
VDD	Power Supply (+2.5V)
VSS	Ground
VDDQ	DQ Power Supply (+2.5V)
VSSQ	DQ Ground
VREF	Reference Voltage for inputs
N.C.	No Connect
NU	Not Used, Electrical Connect is Present



\* This pin is a No Connect for Some Manufacturers.

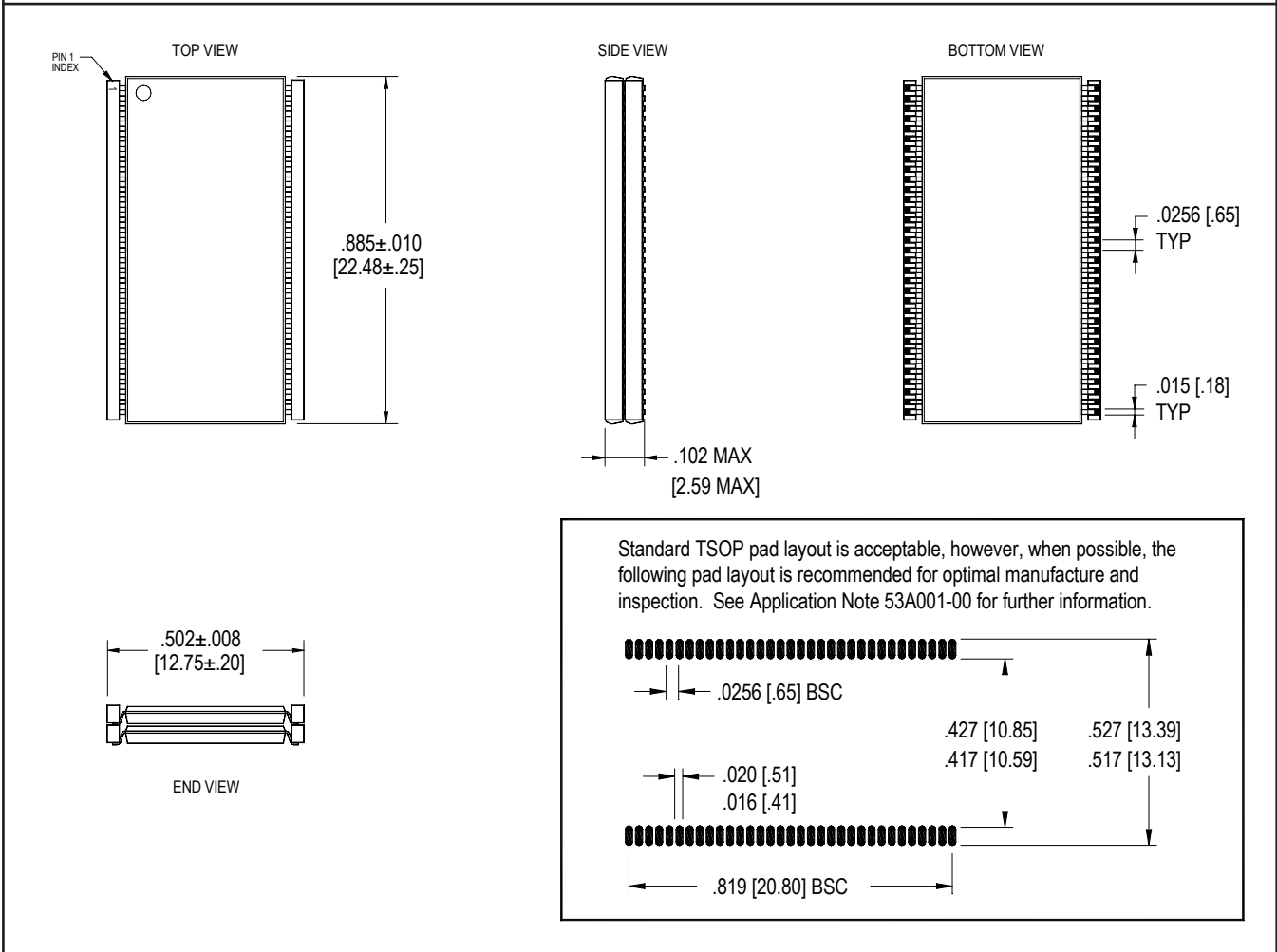


**ORDERING INFORMATION**



\* Contact your sales representative for supplier and manufacturer codes.

**MECHANICAL DRAWING**



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