April 2004

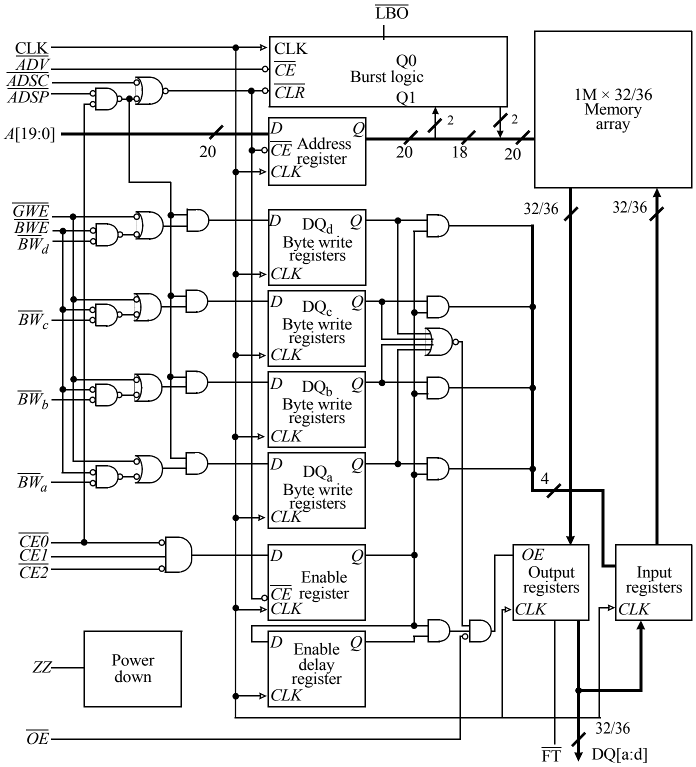
# AS7C251MPFS32A
# AS7C251MPFS36A

## 2.5V 1M × 32/36 pipelined burst synchronous SRAM

## Features

- Organization: 1,048,576 words × 32 or 36 bits
- Fast clock speeds to 200 MHz in LVTTL/LVCMOS
- Fast clock to data access: 3.1/3.4/3.8 ns
- Fast $\overline{OE}$ access time: 3.1/3.4/3.8 ns
- Fully synchronous register-to-register operation
- Single register flow-through mode
- Single-cycle deselect
  - Dual-cycle deselect also available (AS7C252MPFD18A, AS7C251MPFD32A/ AS7C251MPFD36A)
- Asynchronous output enable control
- Available in 100-pin TQFP and 165-ball BGA packages
- Individual byte write and global write
- Multiple chip enables for easy expansion
- 2.5V core power supply
- Linear or interleaved burst control
- Snooze mode for reduced power-standby
- Common data inputs and data outputs
- Boundary scan using IEEE 1149.1 JTAG function
- NTD™[1] pipelined architecture available (AS7C252MNTD18A, AS7C251MNTD32A/ AS7C251MNTD36A)

## Logic block diagram



## Selection guide

| | -200 | -167 | -133 | Units |
|---|---|---|---|---|
| Minimum cycle time | 5 | 6 | 7.5 | ns |
| Maximum clock frequency | 200 | 167 | 133 | MHz |
| Maximum pipelined clock access time | 3.1 | 3.4 | 3.8 | ns |
| Maximum operating current | 400 | 350 | 325 | mA |
| Maximum standby current | 120 | 110 | 100 | mA |
| Maximum CMOS standby current (DC) | 70 | 70 | 70 | mA |

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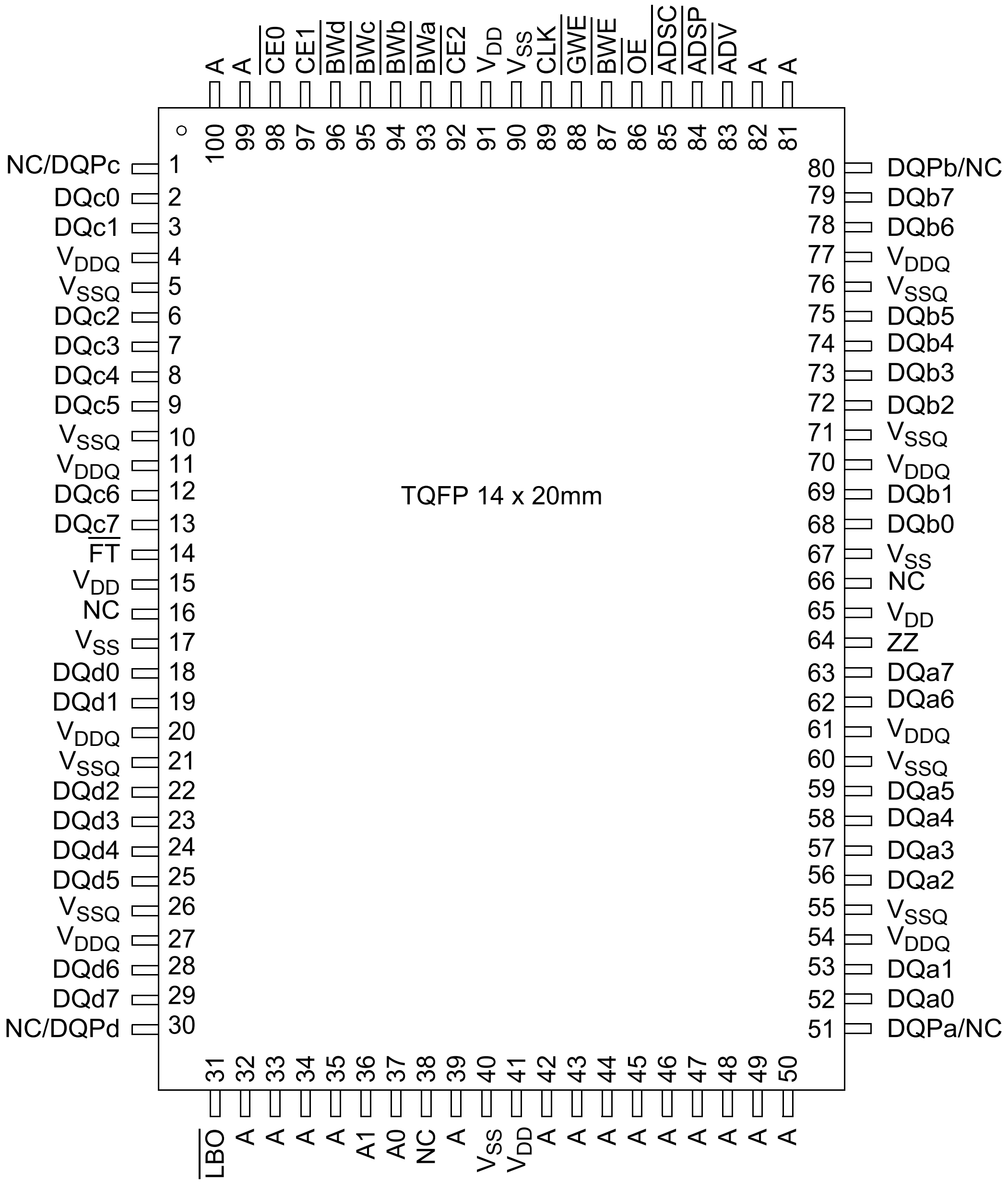
[1] NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners.

## Pin and ball assignment

### 100-pin TQFP - top view



Note: For pins 1, 30, 51, and 80, NC applies to the x32 configuration. DQPn applies to the x36 configuration.

## Ball assignment for 165-ball BGA for 1M x 36

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC | A | $\overline{\text{CE0}}$ | $\overline{\text{BWc}}$ | $\overline{\text{BWb}}$ | $\overline{\text{CE2}}$ | $\overline{\text{BWE}}$ | $\overline{\text{ADSC}}$ | $\overline{\text{ADV}}$ | A | NC |
| **B** | NC | A | CE1 | $\overline{\text{BWd}}$ | $\overline{\text{BWa}}$ | CLK | $\overline{\text{GWE}}$ | $\overline{\text{OE}}$ | $\overline{\text{ADSP}}$ | A | NC |
| **C** | DQPc | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | DQPb |
| **D** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **E** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **F** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **G** | DQc | DQc | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQb | DQb |
| **H** | $\overline{\text{FT}}$ | $V_{SS}$ | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **K** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **L** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **M** | DQd | DQd | $V_{DDQ}$ | $V_{DD}$ | Vss | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | DQa | DQa |
| **N** | DQPd | NC | $V_{DDQ}$ | $V_{SS}$ | NC | A | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | DQPa |
| **P** | NC | NC | A | A | TDI | A1[1] | TDO | A | A | A | A |
| **R** | $\overline{\text{LBO}}$ | A | A | A | TMS | A0[1] | TCK | A | A | A | A |

[1] A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

## Functional description

The AS7C251MPFS32A/36A is a high-performance CMOS 32-Mbit synchronous Static Random Access Memory (SRAM) device organized as 1,048,576 words x 32/36. It incorporates a two-stage register-register pipeline for highest frequency on any given technology.

Fast cycle times of 5/6/7.5 ns with clock access times ($t_{CD}$) of 3.1/3.4/3.8 ns enable 200,167and 133MHz bus frequencies. Three chip enable ($\overline{\text{CE}}$) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{\text{ADSC}}$), or the processor address strobe ($\overline{\text{ADSP}}$). The burst advance pin ($\overline{\text{ADV}}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WE}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register when $\overline{\text{ADSP}}$ is sampled low, the chip enables are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In a read operation, the data accessed by the current address registered in the address registers by the positive edge of CLK are carried to the data-out registers and driven on the output pins on the next positive edge of CLK. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{\text{ADV}}$ is sampled low and both address strobes are high. Burst mode is selectable with the $\overline{\text{LBO}}$ input. With $\overline{\text{LBO}}$ unconnected or driven high, burst operations use an interleaved count sequence. With $\overline{\text{LBO}}$ driven low, the device uses a linear count sequence.

Write cycles are performed by disabling the output buffers with $\overline{\text{OE}}$ and asserting a write command. A global write enable $\overline{\text{GWE}}$ writes all 32/36 bits regardless of the state of individual $\overline{\text{BW[a:d]}}$ inputs. Alternately, when $\overline{\text{GWE}}$ is high, one or more bytes may be written by asserting $\overline{\text{BWE}}$ and the appropriate individual byte $\overline{\text{BWn}}$ signals.

$\overline{\text{BWn}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ low, but it is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{\text{BWn}}$ is sampled LOW regardless of $\overline{\text{OE}}$. Data is clocked into the data input register when $\overline{\text{BWn}}$ is sampled low. Address is incremented internally to the next burst address if $\overline{\text{BWn}}$ and $\overline{\text{ADV}}$ are sampled low. This device operates in single-cycle deselect feature during read cycles.

Read or write cycles may also be initiated with $\overline{\text{ADSC}}$ instead of $\overline{\text{ADSP}}$. The differences between cycles initiated with $\overline{\text{ADSC}}$ and $\overline{\text{ADSP}}$ follow.

$\overline{\text{ADSP}}$ must be sampled high when $\overline{\text{ADSC}}$ is sampled low to initiate a cycle with $\overline{\text{ADSC}}$.

$\overline{\text{WE}}$ signals are sampled on the clock edge that samples $\overline{\text{ADSC}}$ low (and $\overline{\text{ADSP}}$ high).

Master chip enable $\overline{\text{CE0}}$ blocks $\overline{\text{ADSP}}$, but not $\overline{\text{ADSC}}$.

The AS7C251MPFS32A/36A family operates from a core 2.5V power supply. These devices are available in a 100-pin TQFP and 165-ball BGA packages.

## TQFP and BGA capacitance

| Parameter | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN} = 0V$ | - | 5 | pF |
| I/O capacitance | $C_{I/O}$ | $V_{OUT} = 0V$ | - | 7 | pF |

## TQFP and BGA thermal resistance

| Description | Conditions | | Symbol | Typical | Units |
|---|---|---|---|---|---|
| Thermal resistance (junction to ambient)[1] | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 1–layer | $\theta_{JA}$ | 40 | °C/W |
| | | 4–layer | $\theta_{JA}$ | 22 | °C/W |
| Thermal resistance (junction to top of case)[1] | | | $\theta_{JC}$ | 8 | °C/W |

[1] This parameter is sampled

## Signal descriptions

| Pin | I/O | Properties | Description |
|---|---|---|---|
| CLK | I | CLOCK | Clock. All inputs except $\overline{\mathrm{OE}}$, $\overline{\mathrm{FT}}$, ZZ, and $\overline{\mathrm{LBO}}$ are synchronous to this clock. |
| A,A0,A1 | I | SYNC | Address. Sampled when all chip enables are active and when $\overline{\mathrm{ADSC}}$ or $\overline{\mathrm{ADSP}}$ are asserted. |
| DQ[a,b,c,d] | I/O | SYNC | Data. Driven as output when the chip is enabled and when $\overline{\mathrm{OE}}$ is active. |
| $\overline{\mathrm{CE0}}$ | I | SYNC | Master chip enable. Sampled on clock edges when $\overline{\mathrm{ADSP}}$ or $\overline{\mathrm{ADSC}}$ is active. When $\overline{\mathrm{CE0}}$ is inactive, $\overline{\mathrm{ADSP}}$ is blocked. Refer to the “Synchronous truth table” for more information. |
| CE1, $\overline{\mathrm{CE2}}$ | I | SYNC | Synchronous chip enables, active high, and active low, respectively. Sampled on clock edges when $\overline{\mathrm{ADSC}}$ is active or when $\overline{\mathrm{CE0}}$ and $\overline{\mathrm{ADSP}}$ are active. |
| $\overline{\mathrm{ADSP}}$ | I | SYNC | Address strobe processor. Asserted low to load a new address or to enter standby mode. |
| $\overline{\mathrm{ADSC}}$ | I | SYNC | Address strobe controller. Asserted low to load a new address or to enter standby mode. |
| $\overline{\mathrm{ADV}}$ | I | SYNC | Advance. Asserted low to continue burst read/write. |
| $\overline{\mathrm{GWE}}$ | I | SYNC | Global write enable. Asserted low to write all 32/36 and 18 bits. When high, $\overline{\mathrm{BWE}}$ and $\overline{\mathrm{BW[a:d]}}$ control write enable. |
| $\overline{\mathrm{BWE}}$ | I | SYNC | Byte write enable. Asserted low with $\overline{\mathrm{GWE}}$ high to enable effect of $\overline{\mathrm{BW[a:d]}}$ inputs. |
| $\overline{\mathrm{BW[a,b,c,d]}}$ | I | SYNC | Write enables. Used to control write of individual bytes when $\overline{\mathrm{GWE}}$ is high and $\overline{\mathrm{BWE}}$ is low. If any of $\overline{\mathrm{BW[a:d]}}$ is active with $\overline{\mathrm{GWE}}$ high and $\overline{\mathrm{BWE}}$ low, the cycle is a write cycle. If all $\overline{\mathrm{BW[a:d]}}$ are inactive, the cycle is a read cycle. |
| $\overline{\mathrm{OE}}$ | I | ASYNC | Asynchronous output enable. I/O pins are driven when $\overline{\mathrm{OE}}$ is active and chip is in read mode. |
| $\overline{\mathrm{LBO}}$ | I | STATIC | Selects Burst mode. When tied to $V_{DD}$ or left floating, device follows interleaved Burst order. When driven Low, device follows linear Burst order. *This signal is internally pulled High.* |
| TDO | O | SYNC | Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK (BGA only). |
| TDI | I | SYNC | Serial data-in to the JTAG circuit. Sampled on the rising edge of TCK (BGA only). |
| TMS | I | SYNC | This pin controls the Test Access Port state machine. Sampled on the rising edge of TCK (BGA only). |
| TCK | I | Test Clock | Test Clock. All inputs are sampled on the rising edge of TCK. All outputs are driven from the falling edge of TCK. |
| $\overline{\mathrm{FT}}$ | I | STATIC | Selects Pipeline or Flow-through mode. When tied to $V_{DD}$ or left floating, enables Pipeline mode. When driven Low, enables single register Flow-through mode. *This signal is internally pulled High.* |
| ZZ | I | ASYNC | Snooze. Places device in low power mode; data is retained. Connect to GND if unused. |
| NC | - | - | No connects |

## Write enable truth table (per byte)

| Function | $\overline{\mathrm{GWE}}$ | $\overline{\mathrm{BWE}}$ | $\overline{\mathrm{BWa}}$ | $\overline{\mathrm{BWb}}$ | $\overline{\mathrm{BWc}}$ | $\overline{\mathrm{BWd}}$ |
|---|---|---|---|---|---|---|
| Write All Bytes | L | X | X | X | X | X |
| | H | L | L | L | L | L |
| Write Byte a | H | L | L | H | H | H |
| Write Byte c and d | H | L | H | H | L | L |
| Read | H | H | X | X | X | X |
| | H | L | H | H | H | H |

**Key:** X = don’t care, L = low, H = high, n = a, b, c, d; $\overline{\mathrm{BWE}}$, $\overline{\mathrm{BWn}}$ = internal write signal.

## Burst sequence table

| Interleaved burst address | | | | | Linear burst address | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | A1 A0 | A1 A0 | A1 A0 | A1 A0 | | A1 A0 | A1 A0 | A1 A0 | A1 A0 |
| Starting Address | 0 0 | 0 1 | 1 0 | 1 1 | Starting Address | 0 0 | 0 1 | 1 0 | 1 1 |
| First Increment | 0 1 | 0 0 | 1 1 | 1 0 | First Increment | 0 1 | 1 0 | 1 1 | 0 0 |
| Second Increment | 1 0 | 1 1 | 0 0 | 0 1 | Second Increment | 1 0 | 1 1 | 0 0 | 0 1 |
| Third Increment | 1 1 | 1 0 | 0 1 | 0 0 | Third Increment | 1 1 | 1 0 | 0 1 | 1 0 |

## Synchronous truth table

| $\overline{\text{CE0}}$[1] | CE1 | $\overline{\text{CE2}}$ | $\overline{\text{ADSP}}$ | $\overline{\text{ADSC}}$ | $\overline{\text{ADV}}$ | $\overline{\text{WRITE}}$[2] | $\overline{\text{OE}}$ | Address accessed | CLK | Operation | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | L | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | L | X | L | X | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | L | X | H | L | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | X | H | L | X | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | X | H | H | L | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | H | L | L | X | X | X | L | External | L to H | Begin read | Q |
| L | H | L | L | X | X | X | H | External | L to H | Begin read | Hi–Z |
| L | H | L | H | L | X | H | L | External | L to H | Begin read | Q |
| L | H | L | H | L | X | H | H | External | L to H | Begin read | Hi–Z |
| X | X | X | H | H | L | H | L | Next | L to H | Continue read | Q |
| X | X | X | H | H | L | H | H | Next | L to H | Continue read | Hi–Z |
| X | X | X | H | H | H | H | L | Current | L to H | Suspend read | Q |
| X | X | X | H | H | H | H | H | Current | L to H | Suspend read | Hi–Z |
| H | X | X | X | H | L | H | L | Next | L to H | Continue read | Q |
| H | X | X | X | H | L | H | H | Next | L to H | Continue read | Hi–Z |
| H | X | X | X | H | H | H | L | Current | L to H | Suspend read | Q |
| H | X | X | X | H | H | H | H | Current | L to H | Suspend read | Hi–Z |
| L | H | L | H | L | X | L | X | External | L to H | Begin write | D[3] |
| X | X | X | H | H | L | L | X | Next | L to H | Continue write | D |
| H | X | X | X | H | L | L | X | Next | L to H | Continue write | D |
| X | X | X | H | H | H | L | X | Current | L to H | Suspend write | D |
| H | X | X | X | H | H | L | X | Current | L to H | Suspend write | D |

[1] X = don’t care, L = low, H = high

[2] For $\overline{\text{WRITE}}$, L means any one or more byte write enable signals ($\overline{\text{BWa}}$, $\overline{\text{BWb}}$, $\overline{\text{BWc}}$ or $\overline{\text{BWd}}$) and $\overline{\text{BWE}}$ are LOW or $\overline{\text{GWE}}$ is LOW. $\overline{\text{WRITE}}$ = HIGH for all $\overline{\text{BWx}}$, $\overline{\text{BWE}}$, $\overline{\text{GWE}}$ HIGH. See "Write enable truth table (per byte)," on page 5 for more information.

[3] For write operation following a READ, $\overline{\text{OE}}$ must be high before the input data set up time and held high throughout the input hold time

## Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power supply voltage relative to GND | $V_{DD}$, $V_{DDQ}$ | –0.3 | +3.6 | V |
| Input voltage relative to GND (input pins) | $V_{IN}$ | –0.3 | $V_{DD}$ + 0.3 | V |
| Input voltage relative to GND (I/O pins) | $V_{IN}$ | –0.3 | $V_{DDQ}$ + 0.3 | V |
| Power dissipation | $P_d$ | – | 1.8 | W |
| Short circuit output current | $I_{OUT}$ | – | 20 | mA |
| Storage temperature (TQFP) | $T_{stg}$ (TQFP) | –65 | +150 | $^oC$ |
| Storage temperature (BGA) | $T_{stg}$ (BGA) | –65 | +125 | $^oC$ |
| Temperature under bias | $T_{bias}$ | –65 | +135 | $^oC$ |

Stresses greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

## Recommended operating conditions

| Parameter | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage for inputs | $V_{DD}$ | 2.375 | 2.5 | 2.625 | V |
| Supply voltage for I/O | $V_{DDQ}$ | 2.375 | 2.5 | 2.625 | V |
| Ground supply | Vss | 0 | 0 | 0 | V |

## DC electrical characteristics

| Parameter | Sym | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input leakage current | $\|I_{LI}\|$ | $V_{DD}$ = Max, OV ≤ $V_{IN}$ ≤ $V_{DD}$ | -2 | 2 | µA |
| Output leakage current | $\|I_{LO}\|$ | OE ≥ $V_{IH}$, $V_{DD}$ = Max, OV ≤ $V_{OUT}$ ≤ $V_{DDQ}$ | -2 | 2 | µA |
| Input high (logic 1) voltage | $V_{IH}$ | Address and control pins | 1.7 | $V_{DD}$+0.3 | V |
| | | I/O pins | 1.7 | $V_{DDQ}$+0.3 | V |
| Input low (logic 0) voltage | $V_{IL}$ | Address and control pins | -0.3* | 0.7 | V |
| | | I/O pins | -0.3* | 0.7 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{DDQ}$ = 2.375V | 1.7 | – | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, $V_{DDQ}$ = 2.625V | – | 0.7 | V |

*$V_{IL}$ min = -1.5 for pulse width less than 0.2 X $t_{CYC}$

## $I_{DD}$ operating conditions and maximum limits

| Parameter | Sym | Conditions | -200 | -167 | -133 | Unit |
|---|---|---|---|---|---|---|
| Operating power supply current[1](pipelined mode) | $I_{CC}$ | $\overline{CE0}$ = $V_{IL}$, CE1 = $V_{IH}$, $\overline{CE2}$ = $V_{IL}$, f = $f_{Max}$, $I_{OUT}$ = 0 mA | 400 | 350 | 325 | mA |
| Operating power supply current[1](flow-through mode) | $I_{CC}$<br>(FT) | | 325 | 280 | 260 | mA |
| Standby power supply current | $I_{SB}$ | Deselected, f = $f_{Max}$, ZZ ≤ $V_{IL}$ | 120 | 110 | 100 | mA |
| | $I_{SB1}$ | Deselected, f = 0, ZZ ≤ 0.2V, all $V_{IN}$ ≤ 0.2V or ≥ $V_{DD}$ – 0.2V | 70 | 70 | 70 | |
| | $I_{SB2}$ | Deselected, f = $f_{Max}$, ZZ ≥ $V_{DD}$ – 0.2V, all $V_{IN}$ ≤ $V_{IL}$ or ≥ $V_{IH}$ | 60 | 60 | 60 | |

1 $I_{CC}$ given with no output loading. $I_{CC}$ increases with faster cycle times and greater output loading.

## Timing characteristics over operating range

| Parameter | Sym | –200 | | –167 | | -133 | | Unit | Notes[1] |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock frequency | $f_{Max}$ | – | 200 | – | 167 | – | 133 | MHz | |
| Cycle time (pipelined mode) | $t_{CYC}$ | 5 | – | 6 | – | 7.5 | – | ns | |
| Cycle time (flow-through mode) | $t_{CYCF}$ | 7.5 | – | 8.5 | – | 12 | – | ns | |
| Clock access time (pipelined mode) | $t_{CD}$ | – | 3.1 | – | 3.4 | – | 3.8 | ns | |
| Clock access time (flow-through mode) | $t_{CDF}$ | – | 6.5 | – | 7.5 | – | 10 | ns | |
| Output enable low to data valid | $t_{OE}$ | – | 3.1 | – | 3.4 | – | 3.8 | ns | |
| Clock high to output low Z | $t_{LZC}$ | 0 | – | 0 | – | 0 | – | ns | 2,3,4 |
| Data output invalid from clock high (pipelined mode) | $t_{OH}$ | 1.5 | – | 1.5 | – | 1.5 | – | ns | 2 |
| Data Output invalid from clock high (flow-through mode) | $t_{OHF}$ | 3.0 | – | 3.0 | – | 3.0 | – | ns | 2 |
| Output enable low to output low Z | $t_{LZOE}$ | 0 | – | 0 | – | 0 | – | ns | 2,3,4 |
| Output enable high to output high Z | $t_{HZOE}$ | – | 3.0 | – | 3.4 | – | 3.8 | ns | 2,3,4 |
| Clock high to output high Z | $t_{HZC}$ | – | 3.0 | – | 3.4 | – | 3.8 | ns | 2,3,4 |
| Output enable high to invalid output | $t_{OHOE}$ | 0 | – | 0 | – | 0 | – | ns | |
| Clock high pulse width | $t_{CH}$ | 2.0 | – | 2.4 | – | 2.4 | – | ns | 5 |
| Clock low pulse width | $t_{CL}$ | 2.0 | – | 2.3 | – | 2.4 | – | ns | 5 |
| Address setup to clock high | $t_{AS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Data setup to clock high | $t_{DS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Write setup to clock high | $t_{WS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6,7 |
| Chip select setup to clock high | $t_{CSS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6,8 |
| Address hold from clock high | $t_{AH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| Data hold from clock high | $t_{DH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| Write hold from clock high | $t_{WH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6,7 |
| Chip select hold from clock high | $t_{CSH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6,8 |
| $\overline{\text{ADV}}$ setup to clock high | $t_{ADVS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| $\overline{\text{ADSP}}$ setup to clock high | $t_{ADSPS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| $\overline{\text{ADSC}}$ setup to clock high | $t_{ADSCS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| $\overline{\text{ADV}}$ hold from clock high | $t_{ADVH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| $\overline{\text{ADSP}}$ hold from clock high | $t_{ADSPH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| $\overline{\text{ADSC}}$ hold from clock high | $t_{ADSCH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |

[1] See “Notes” on page 20.

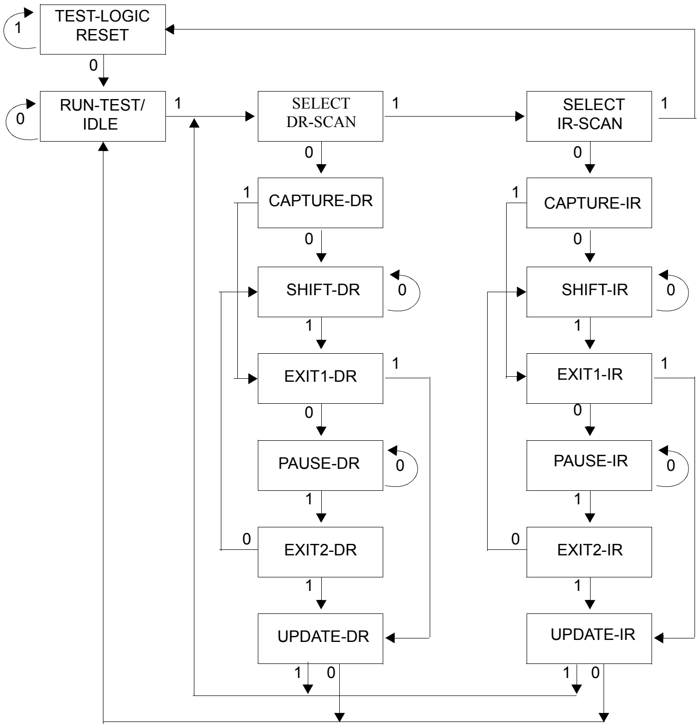
## IEEE 1149.1 serial boundary scan (JTAG)

The SRAM incorporates a serial boundary scan test access port (TAP). The port operates in accordance with IEEE Standard 1149.1-1990. The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

## Disabling the JTAG feature

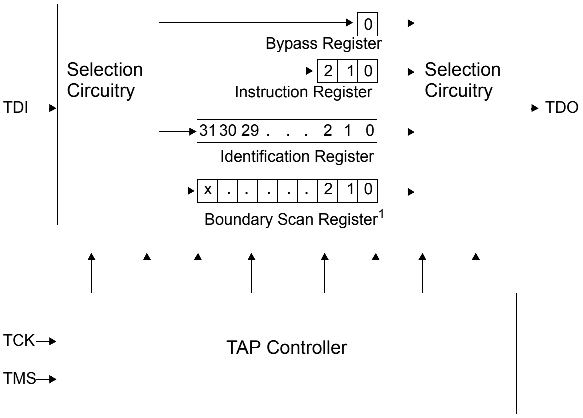
If the JTAG function is not being implemented, TCK should be grounded to avoid mid-level input. At power-up, the device will come up in a reset state which will not interfere with the operation of the device.

## TAP controller state diagram



**Note:** The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

## TAP controller block diagram



$^1$ x = 75

# Test access port (TAP)

## Test clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

## Test mode select (TMS)

The TAP controller receives commands from TMS input. It is sampled on the rising edge of TCK. You can leave this pin/ball unconnected if the TAP is not used. The pin/ball is pulled up internally, resulting in a logic high level.

### Test data-in (TDI)

The TDI pin/ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

### Test data-out (TDO)

The TDO output pin/ball serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See the TAP Controller State Diagram.)

### Performing a TAP RESET

You can perform a RESET by forcing TMS high ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and can be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

## TAP registers

Registers are connected between the TDI and TDO pins/balls. They allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin/ball on the rising edge of TCK. Data is output on the TDO pin/ball on the falling edge of TCK.

### Instruction register

You can serially load three-bit instructions into the instruction register. The register is loaded when it is placed between the TDI and TDO pins/balls as shown in the TAP Controller Block Diagram. The instruction register is loaded with the IDCODE instruction at power up and also if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level series test data path.

### Bypass register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins/balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set low (Vss) when the BYPASS instruction is executed.

### Boundary scan register

The boundary scan register is connected to all the input and bidirectional pins/balls on the SRAM. The chip has a 76-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins/balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The boundary scan order table shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The most significant bit (MSB) of the register is connected to TDI, and the least significant bit (LSB) is connected to TDO.

### Identification (ID) register

The ID register has a vendor code and other information described in the Identification Register Definitions table. The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state.

## TAP instruction set

Eight different instructions are possible with the 3-bit instruction register. All combinations are listed in the Instruction Codes table. One of these instructions is reserved and should not be used.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins/balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

## EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

## IDCODE

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state. The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the identification register. It also places the identification register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

## SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins/balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high-Z state.

## SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAM's input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet.Because the RAM clock is independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be accepted. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tCS plus tCH). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

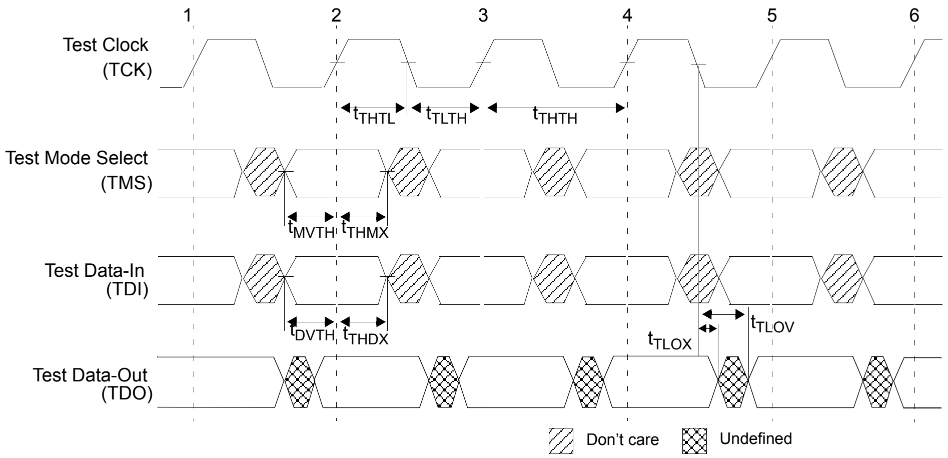
## BYPASS

The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board. When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO.

## RESERVED

Do not use a reserved instruction. These instructions are not implemented but are reserved for future use.

## TAP timing diagram



## TAP AC electrical characteristics

For notes 1 and 2, $+10^{o}C \le T_J \le +110^{o}C$ and $+2.4V \le V_{DD} \le +2.6V$.

| Description | Symbol | Min | Max | Units |
|---|---|---|---|---|
| **Clock** | | | | |
| Clock cycle time | $^{t}$THTH | 50 | | ns |
| Clock frequency | $^{f}$TF | | 20 | MHz |
| Clock high time | $^{t}$THTL | 20 | | ns |
| Clock low time | $^{t}$TLTH | 20 | | ns |
| **Output Times** | | | | |
| TCK low to TDO unknown | $^{t}$TLOX | 0 | | ns |
| TCK low to TDO valid | $^{t}$TLOV | | 10 | ns |
| TDI valid to TCK high | $^{t}$DVTH | 5 | | ns |
| TCK high to TDI invalid | $^{t}$THDX | 5 | | ns |
| **Setup Times** | | | | |
| TMS setup | $^{t}$MVTH | 5 | | ns |
| Capture setup | $^{t}$CS[1] | 5 | | ns |
| **Hold Times** | | | | |
| TMS hold | $^{t}$THMX | 5 | | ns |
| Capture hold | $^{t}$CH[1] | 5 | | ns |

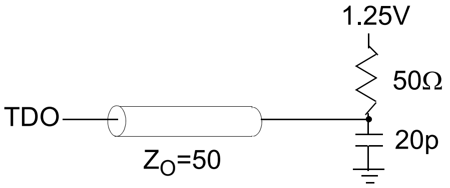
[1] $^{t}$CS and $^{t}$CH refer to the setup and hold time requirements of latching data from the boundary scan register.

[2] Test conditions are specified using the load in the figure TAP AC output load equivalent.

## TAP AC test conditions

| | |
|---|---|
| Input pulse levels. . . . . . . . . . . . . . . . | Vss to 2.5V |
| Input rise and fall times. . . . . . . . . . . . . . | 1 ns |
| Input timing reference levels. . . . . . . . . . | 1.25V |
| Output reference levels . . . . . . . . . . . . . . | 1.25V |
| Test load termination supply voltage. . . . | 1.25V |

## TAP AC output load equivalent



## TAP DC electrical characteristics and operating conditions

($+10^{o}C \le T_J \le +110^{o}C$ and $+2.4V \le V_{DD} \le +2.6V$ unless otherwise noted)

| Description | Conditions | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Input high (logic 1) voltage | | $V_{IH}$ | 1.7 | $V_{DD} + 0.3$ | V | 1, 2 |
| Input low (logic 0) voltage | | $V_{IL}$ | -0.3 | 0.7 | V | 1, 2 |
| Input leakage current | $0V \le V_{IN} \le V_{DD}$ | $IL_I$ | -5.0 | 5.0 | µA | |
| Output leakage current | Outputs disabled,<br>$0V \le V_{IN} \le V_{DDQ}$(DQx) | $IL_O$ | -5.0 | 5.0 | µA | |
| Output low voltage | $I_{OLC} = 100\mu A$ | $V_{OL1}$ | | 0.2 | V | 1 |
| Output low voltage | $I_{OLT} = 2mA$ | $V_{OL2}$ | | 0.7 | V | 1 |
| Output high voltage | $I_{OHS} = -100\mu A$ | $V_{OH1}$ | 2.1 | | V | 1 |
| Output high voltage | $I_{OHT} = -2mA$ | $V_{OH2}$ | 1.7 | | V | 1 |

1. All voltage referenced to $V_{SS}$(GND).

2. Overshoot: $V_{IH}(AC) \le V_{DD} + 1.5V$ for $t \le {}^{t}$KHKH/2

Undershoot:$V_{IL}(AC) \ge -0.5$ for $t \le {}^{t}$KHKH/2

Power-up: $V_{IH} \le +2.6V$ and $V_{DD} \le 2.4V$ and $V_{DDQ} \le 1.4V$ for $t \le 200ms$

During normal operation, $V_{DDQ}$ must not exceed $V_{DD}$. Control input signals (such as $\overline{LD}$, R/$\overline{W}$, etc.) may not have pulsed widths less than $t_{KHKL}$(Min) or operate at frequencies exceeding $f_{KF}$(Max).

## Identification register definitions

| Instruction field | 1M x 36 | Description |
|---|---|---|
| Revision number (31:28) | xxxx | Reserved for version number. |
| Device depth (27:23) | xxxxx/xxxxx | Defines the depth of 1M words. |
| Device width (22:18) | xxxxx/xxxxx | Defines the width of x32 or x36 bits. |
| Device ID (17:12) | xxxxxx | Reserved for future use. |
| JEDEC ID code (11:1) | 00000110100 | Allows unique identification of SRAM vendor. |
| ID register presence indicator (0) | 1 | Indicates the presence of an ID register. |

## Scan register sizes

| Register name | Bit size |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary scan | x36:76 |

## Instruction codes

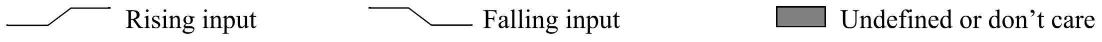
| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high-Z state. |
| RESERVED | 101 | Do not use. This instruction is reserved for future use. |
| SAMPLE/ PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. |
| BYPASS | 111, 011, 110 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |

## 165-ball BGA boundary scan exit order (x36)

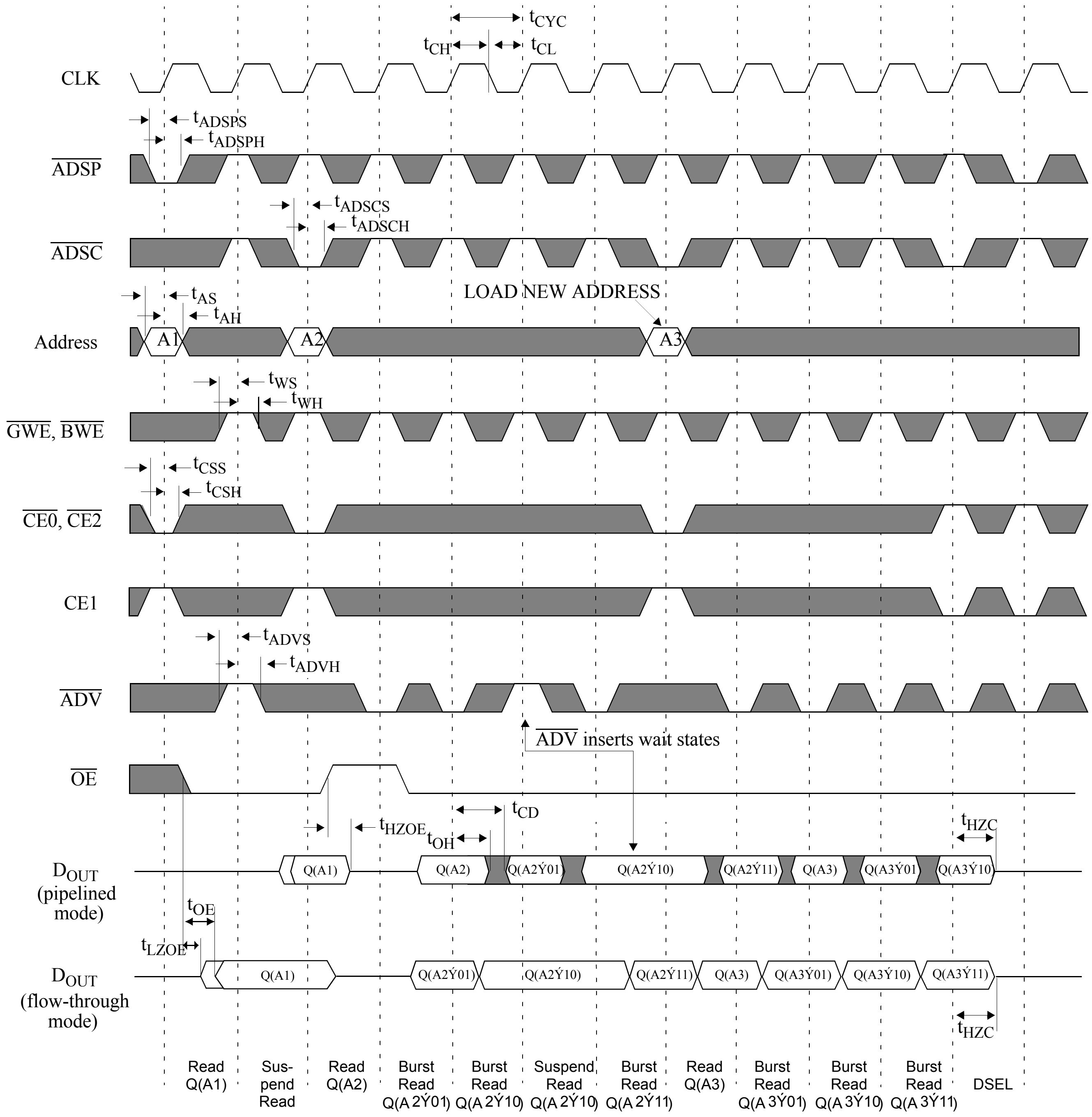
| Bit #s | Signal Name | Ball ID |
|---|---|---|
| 1 | A | 6N |
| 2 | A | 8P |
| 3 | A | 8R |
| 4 | A | 9R |
| 5 | A | 9P |
| 6 | A | 10P |
| 7 | A | 10R |
| 8 | A | 11R |
| 9 | A | 11P |
| 10 | ZZ | 11H |
| 11 | DQPa | 11N |
| 12 | DQa | 11M |
| 13 | DQa | 11L |
| 14 | DQa | 11K |
| 15 | DQa | 11J |
| 16 | DQa | 10M |
| 17 | DQa | 10L |
| 18 | DQa | 10K |
| 19 | DQa | 10J |
| 20 | DQb | 11G |
| 21 | DQb | 11F |
| 22 | DQb | 11E |
| 23 | DQb | 11D |
| 24 | DQb | 10G |
| 25 | DQb | 10F |
| 26 | DQb | 10E |
| 27 | DQb | 10D |
| 28 | DQPb | 11C |
| 29 | NC | 11A |
| 30 | NC | 11B |
| 31 | A | 10A |
| 32 | A | 10B |
| 33 | $\overline{\text{ADV}}$ | 9A |
| 34 | $\overline{\text{ADSP}}$ | 9B |
| 35 | $\overline{\text{ADSC}}$ | 8A |
| 36 | $\overline{\text{OE}}$ | 8B |
| 37 | $\overline{\text{BWE}}$ | 7A |
| 38 | $\overline{\text{GWE}}$ | 7B |
| 39 | CLK | 6B |
| 40 | $\overline{\text{CE2}}$ | 6A |
| 41 | $\overline{\text{BWa}}$ | 5B |
| 42 | $\overline{\text{BWb}}$ | 5A |
| 43 | $\overline{\text{BWc}}$ | 4A |
| 44 | $\overline{\text{BWd}}$ | 4B |
| 45 | CE1 | 3B |
| 46 | $\overline{\text{CE0}}$ | 3A |
| 47 | A | 2A |
| 48 | A | 2B |
| 49 | NC | 1B |
| 50 | NC | 1A |
| 51 | DQPc | 1C |
| 52 | DQc | 1D |
| 53 | DQc | 1E |
| 54 | DQc | 1F |
| 55 | DQc | 1G |
| 56 | DQc | 2D |
| 57 | DQc | 2E |
| 58 | DQc | 2F |
| 59 | DQc | 2G |
| 60 | DQd | 1J |
| 61 | DQd | 1K |
| 62 | DQd | 1L |
| 63 | DQd | 1M |
| 64 | DQd | 2J |
| 65 | DQd | 2K |
| 66 | DQd | 2L |
| 67 | DQd | 2M |
| 68 | DQPd | 1N |
| 69 | A | 2R |
| 70 | $\overline{\text{LBO}}$ | 1R |
| 71 | A | 3P |
| 72 | A | 3R |
| 73 | A | 4R |
| 74 | A | 4P |
| 75 | A1 | 6P |
| 76 | A0 | 6R |

Note: NC and $V_{SS}$ pins included in the scan exit order are read as “X” (i.e. Don’t care)

## Key to switching waveforms

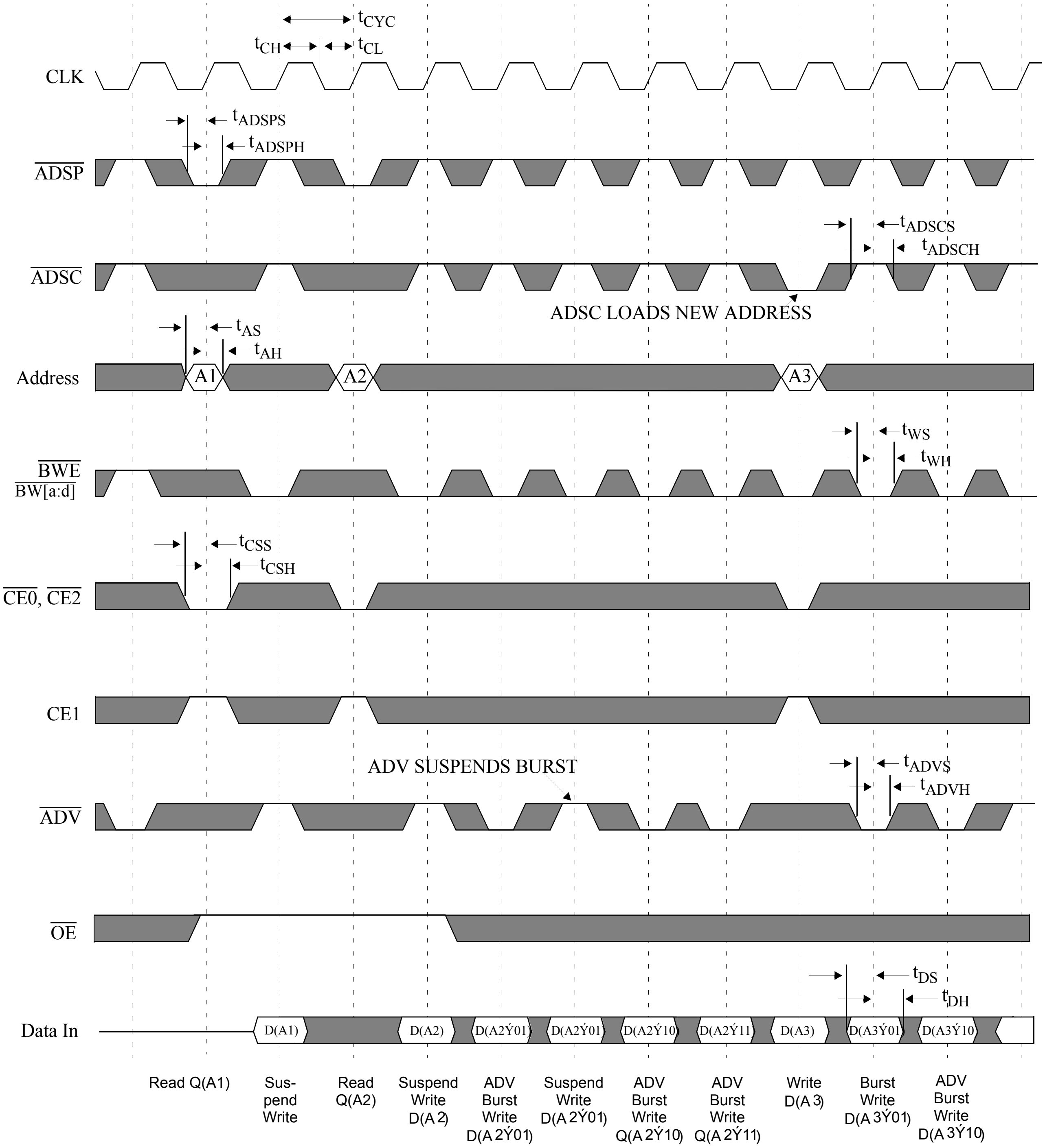


## Timing waveform of read cycle



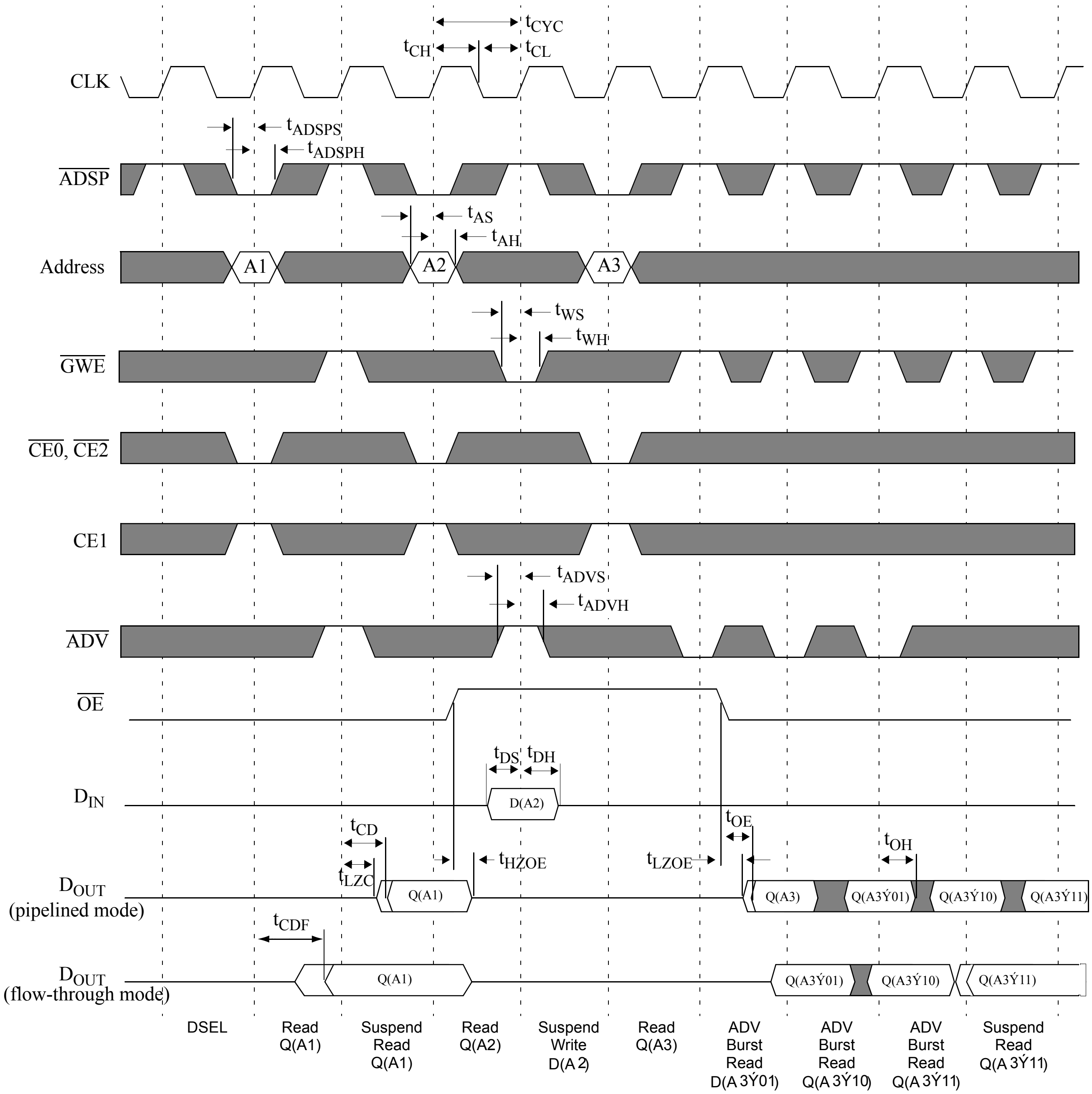
Note: Ý = XOR when $\overline{\text{LBO}}$ = high/no connect; Ý = ADD when $\overline{\text{LBO}}$ = low. $\overline{\text{BW[a:d]}}$ is don’t care.

## Timing waveform of write cycle



Note: Ý = XOR when LBO = high/no connect; Ý = ADD when LBO = low.

## Timing waveform of read/write cycle



Note: Ý = XOR when $\overline{\text{LBO}}$ = high/no connect; Ý = ADD when $\overline{\text{LBO}}$ = low.

## AC test conditions

- Output load: For $t_{LZC}$, $t_{LZOE}$, $t_{HZOE}$, $t_{HZC}$, see Figure C. For all others, see Figure B.
- Input pulse level: GND to 2.5V. See Figure A.
- Input rise and fall time (measured at 0.25V and 2.25V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.25V.

***Thevenin equivalent:***

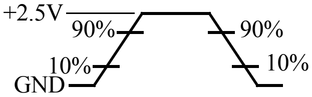


Figure A: Input waveform

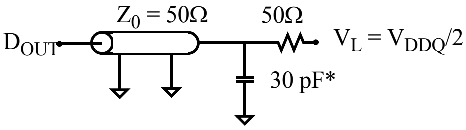


Figure B: Output load (A)

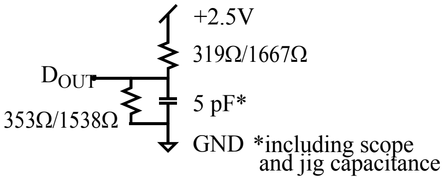


Figure C: Output load(B)

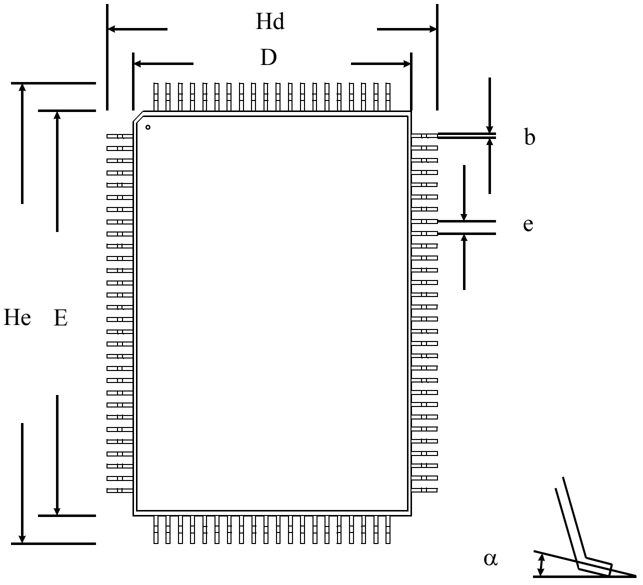
## Notes

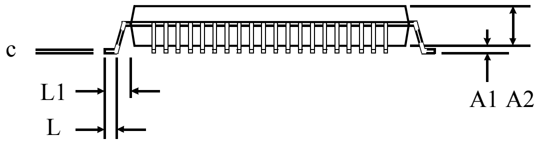
1 For test conditions, see “AC test conditions”, Figures A, B, and C.
2 This parameter is measured with output load condition in Figure C.
3 This parameter is sampled but not 100% tested.
4 $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZC}$ is less than $t_{LZC}$ at any given temperature and voltage.
5 $t_{CH}$ is measured as high if above VIH, and $t_{CL}$ is measured as low if below VIL.
6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
7 Write refers to $\overline{GWE}$, $\overline{BWE}$, and $\overline{BW[a:d]}$.
8 Chip select refers to $\overline{CE0}$, CE1, and $\overline{CE2}$.

## Package dimensions

### 100-pin quad flat pack (TQFP)

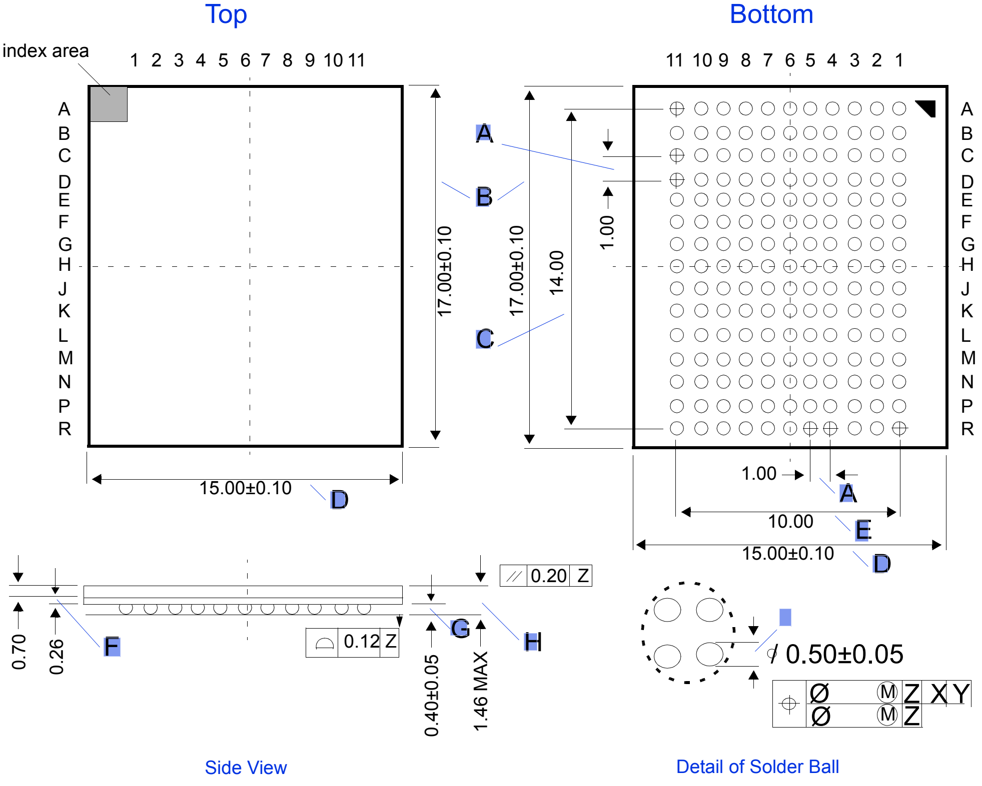
| | TQFP | |
|---|---|---|
| | Min | Max |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.22 | 0.38 |
| c | 0.09 | 0.20 |
| D | 13.90 | 14.10 |
| E | 19.90 | 20.10 |
| e | 0.65 nominal | |
| Hd | 15.85 | 16.15 |
| He | 21.80 | 22.20 |
| L | 0.45 | 0.75 |
| L1 | 1.00 nominal | |
| α | 0° | 7° |
| Dimensions in millimeters | | |





### 165-ball BGA (ball grid array)

| All measurements are in mm. | | | |
|---|---|---|---|
| | Min | Typ | Max |
| **A** | | 1.00 | |
| **B** | 16.90 | 17.00 | 17.10 |
| **C** | | 14.00 | |
| **D** | 14.90 | 15.00 | 15.10 |
| **E** | | 10.00 | |
| **F** | | 0.26 | |
| **G** | 0.35 | 0.40 | 0.45 |
| **H** | 1.26 | 1.36 | 1.46 |
| **I** | 0.45 | 0.50 | 0.55 |



## Ordering information

| Package & Width | 200 MHz | 167 MHz | 133 MHz |
|---|---|---|---|
| TQFP x32 | AS7C251MPFS32A-200TQC | AS7C251MPFS32A-167TQC | AS7C251MPFS32A-133TQC |
| | AS7C251MPFS32A-200TQI | AS7C251MPFS32A-167TQI | AS7C251MPFS32A-133TQI |
| TQFP x36 | AS7C251MPFS36A-200TQC | AS7C251MPFS36A-167TQC | AS7C251MPFS36A-133TQC |
| | AS7C251MPFS36A-200TQI | AS7C251MPFS36A-167TQI | AS7C251MPFS36A-133TQI |
| BGA x32 | AS7C251MPFS32A-200BC | AS7C251MPFS32A-167BC | AS7C251MPFS32A-133BC |
| | AS7C251MPFS32A-200BI | AS7C251MPFS32A-167BI | AS7C251MPFS32A-133BI |
| BGA x36 | AS7C251MPFS36A-200BC | AS7C251MPFS36A-167BC | AS7C251MPFS36A-133BC |
| | AS7C251MPFS36A-200BI | AS7C251MPFS36A-167BI | AS7C251MPFS36A-133BI |

Note:
Add suffix ‘N’ to the above part numbers for lead free parts (Ex AS7C251MPFS32A-200TQCN)

## Part numbering guide

| AS7C | 25 | 1M | PF | S | 32/36 | A | –XXX | TQ or B | C/I | X |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

1. Alliance Semiconductor SRAM prefix

2. Operating voltage: 25 = 2.5V

3. Organization: 1M = 1Meg

4. Pipelined/flow-through mode (each device works in both modes)

5. Deselect: S = single cycle deselect

6. Organization: 32 = x 32; 36 = x 36

7. Production version: A = first production version

8. Clock speed (MHz)

9. Package type: TQ = TQFP, B = BGA

10. Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)
11. N = Lead Free Part

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Document Version: v.1.0

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