Aptos SEMICONDUCTOR

AP9A128
AP9A129

32K x 8 High Speed CMOS Static RAM

Features

- Fast access times: 12, 15, 20 ns
- Fast output enable (t_{DOE}) for cache applications
- Low active power: 400 mW (Typical)
- Low standby power
- Fully static operation, no clock or refresh required
- TTL-compatible inputs and outputs
- TSOP (only) offered in "reverse" TSOP package for easy 2-sided board assembly
- Single 5V 10% power supply
- Commercial, industrial and military temperature range

Functional Description

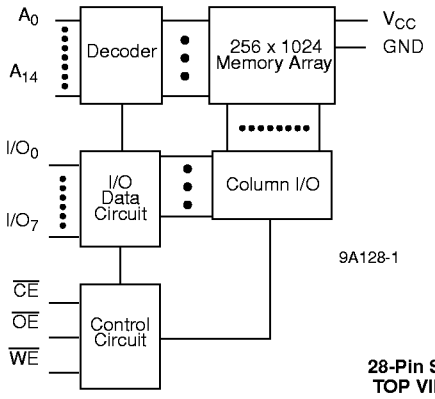
The Aptos AP9A128/9 is a high speed, low power, 32,768-word by 8-bit CMOS static RAM. It is fabricated using Aptos' high-performance CMOS, double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12ns (Max).

When Chip Enable ($\overline{CE}$) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 10 µW (typical) at CMOS input levels.

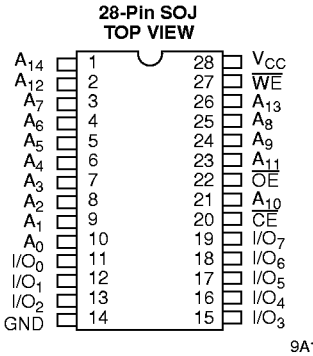
Easy memory expansion is provided by using asserted LOW $\overline{CE}$ and asserted LOW output enable inputs ($\overline{OE}$). The asserted LOW write enable ($\overline{WE}$) controls both writing and reading of the memory.

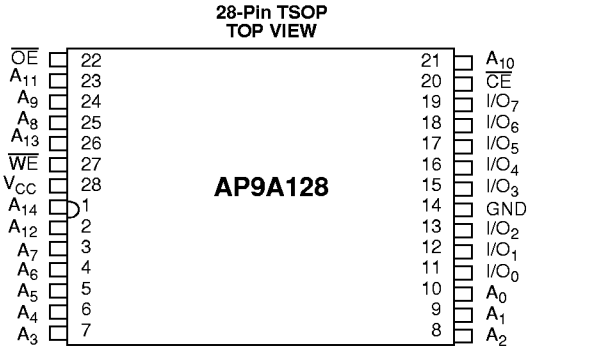
The AP9A128 is pin-compatible with other 32K x 8 SRAMs in the SOJ, and TSOP package. *The AP9A129, available in TSOP only, is a reverse (or mirror-image) pin-out option.*

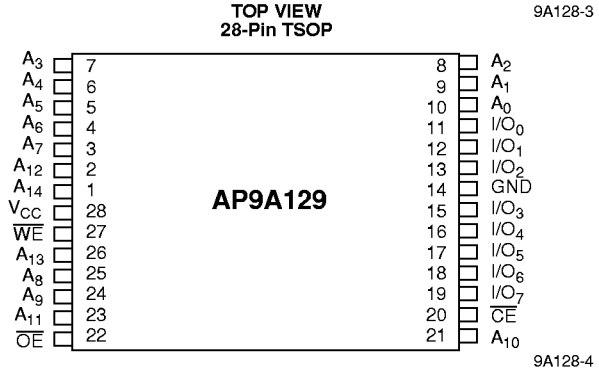
Block Diagram



Pin Configurations







Selection Guide

	AP9A128-12 AP9A129-12	AP9A128-15 AP9A129-15	AP9A128-20 AP9A129-20
Maximum Access Time (ns)	12	15	20
Maximum Operating Current (mA)	100	95	90
Maximum Standby Current (mA)	10	10	10

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AP9A128
AP9A129

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C
Ambient Temperature
with Power Applied ..... -55°C to +125°C

V_{CC} Supply Relative to GND ..... -1.0 V to +7.0 V
Voltage on Any Pin Relative to GND ..... -0.5 V to V_{CC} +0.5 V
Short Circuit Output Current[1] ..... ±50 mA
Power Dissipation ..... 1.0 W

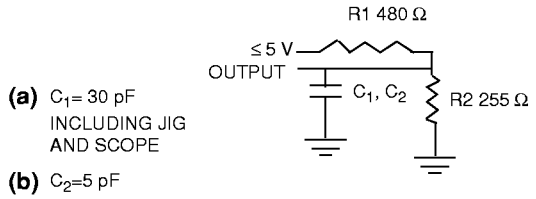
Electrical Characteristics Over the Operating Range (0 °C ≤ T_A ≤ 70 °C, V_{CC} = 5V ±10%) -*Commercial*

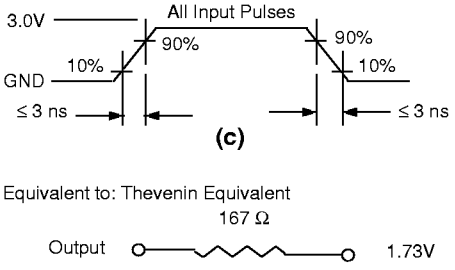
Symbol	Parameter	Test Conditions	9A128-12 9A129-12		9A128-15 9A129-15		9A128-20 9A129-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = fmax.		100		95		90	mA
I_{CC2}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = 0		80		80		80	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f=fmax.		35		35		35	mA
I_{SB2}	CMOS Standby Current-CMOS Inputs	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2 V, f = 0		10		10		10	mA
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	-1	1	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = - 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Capacitance

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	I/O Capacitance	5	pF

AC Test Loads and Waveforms





Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may effect these parameters.
3. V_{IL} = -3.0 V for pulse width less than 3 ns.

Electrical Characteristics Over the Operating Range (-40 °C ≤ T_A ≤ 85 °C, V_{CC} = 5V ±10%) *-Industrial*

Symbol	Parameter	Test Conditions	9A128-12		9A128-15		9A128-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = fmax.		120		115		110	mA
I_{CC2}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = 0		100		100		100	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f=Max.		55		55		55	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2 V, f = 0		25		25		25	mA
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	-1	1	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = - 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Electrical Characteristics Over the Operating Range (-55 °C ≤ T_A ≤ 125 °C, V_{CC} = 5V ±10%) *-Military*

Symbol	Parameter	Test Conditions	9A128-12		9A128-15		9A128-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = fmax.		150		135		130	mA
I_{CC2}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = 0		100		100		100	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f=Max.		60		55		55	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2 V, f = 0		25		25		25	mA
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	-1	1	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = - 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Switching Characteristics Over the Operating Range [1]

Parameter	Description	9A128-12 9A129-12		9A128-15 9A129-15		9A128-20 9A129-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address Access Time		12		15		20	ns
t_{OHA}	Output Hold Time	3		3		3		ns
t_{ACE}	$\overline{CE}$ Access Time		12		15		20	ns
t_{DOE}	$\overline{OE}$ Access Time		5		7		8	ns
t_{LZOE}	$\overline{OE}$ to Low-Z Output	0		0		0		ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output		5		6		7	ns
t_{LZCE}	$\overline{CE}$ to Low-Z Output	3		3		3		ns
t_{HZCE}	$\overline{CE}$ to High-Z Output		6		8		9	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		12		15		20	ns
Write Cycle[3]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ to Write End	8		10		12		ns
t_{AW}	Address to Set-up Time to Write End	8		10		12		ns
t_{HA}	Address Hold to Write End	0		0		0		ns
t_{SA}	Address Set-up Time	0		0		0		ns
t_{PWE1}[4]	$\overline{WE}$ Pulse Width ($\overline{OE}$ =HIGH)	8		10		12		ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =LOW)	12		12		15		ns
t_{SD}	Data Set-up to Write End	6		7		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output		6		7		9	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	2		2		2		ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 - 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*.
2. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ±500mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but either can be deasserted to terminate the Write. The Data Input Set-up and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ High.
5. $\overline{WE}$ is HIGH for a Read Cycle.
6. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
7. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.
8. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

Pin Descriptions

A_0 - A_{14}: Address Inputs

These 15 address inputs select one of the 32,768 8-bit words in the RAM.

$\overline{CE}$: Chip Enable Input

$\overline{CE}$ is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while $\overline{CE}$ is asserted (LOW) and $\overline{WE}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is deasserted.

$\overline{WE}$: Write Enable Input

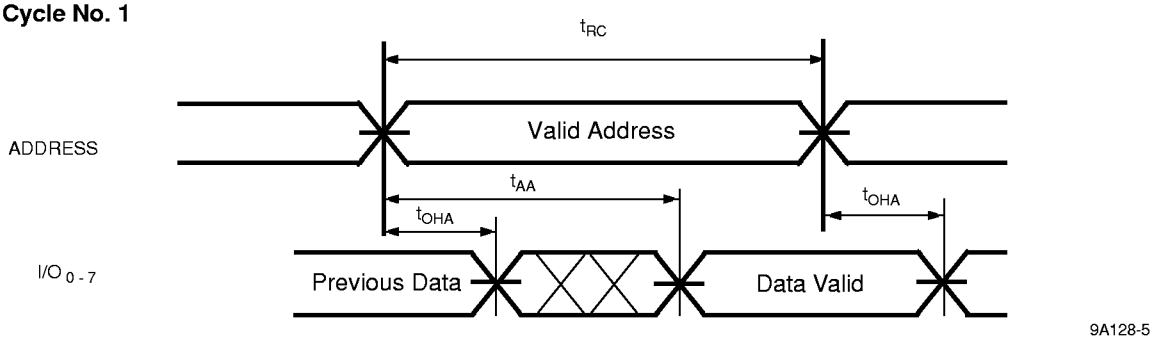
The Write Enable input is asserted LOW and controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

I/O_0 - I/O_7: Common Input/Output Pins

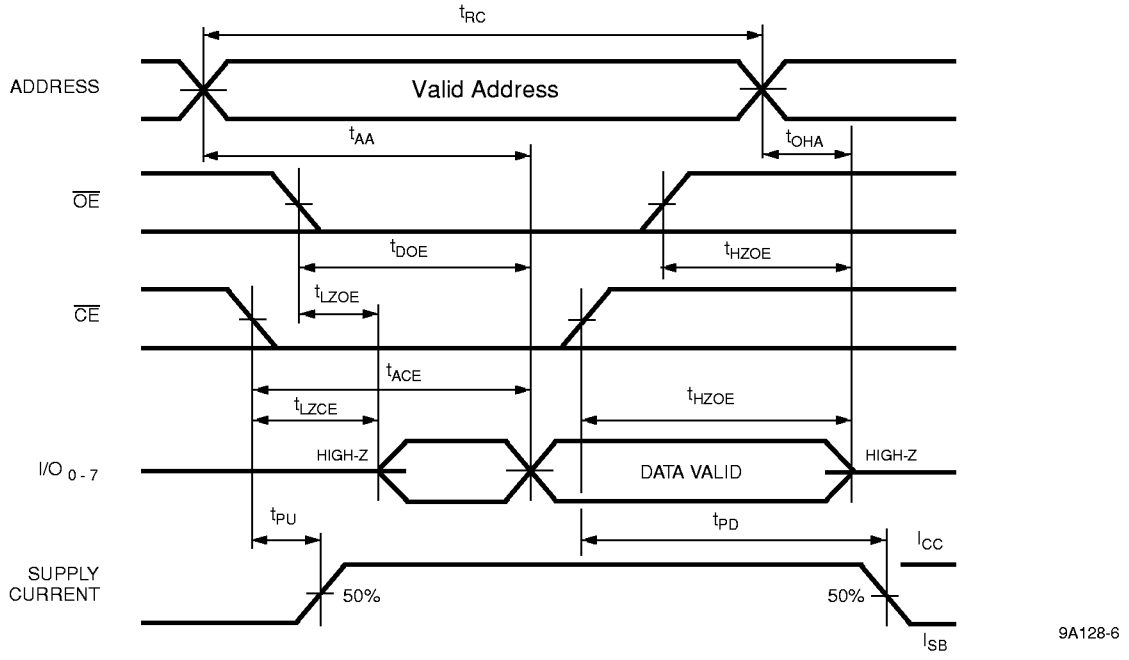
GND: Ground

Switching Waveforms

Read Cycle No. 1

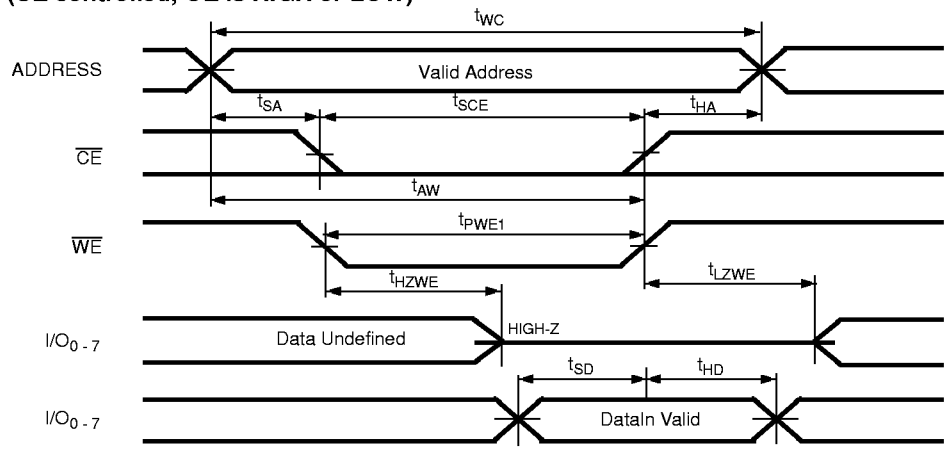


Read Cycle No. 2



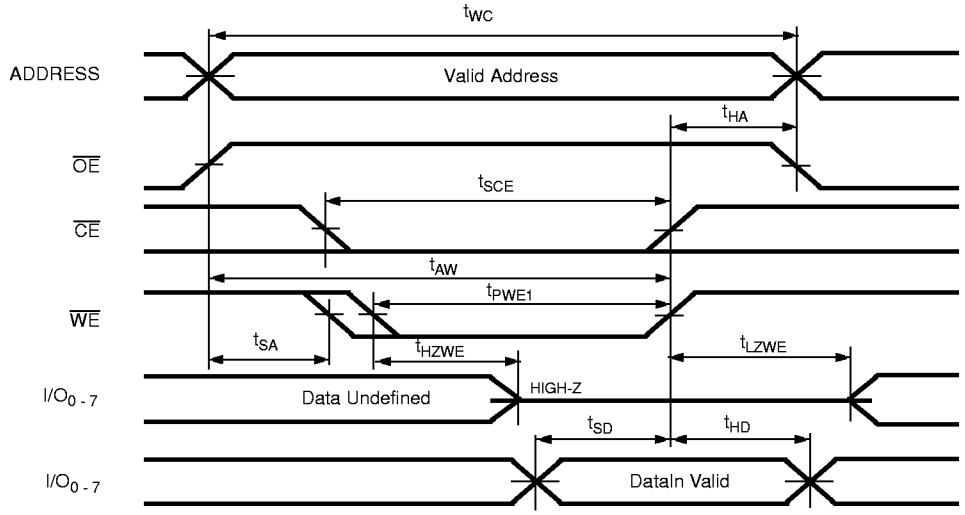
Switching Waveforms (continued)

Write Cycle No.1 ($\overline{CE}$ controlled, $\overline{OE}$ is HIGH or LOW)



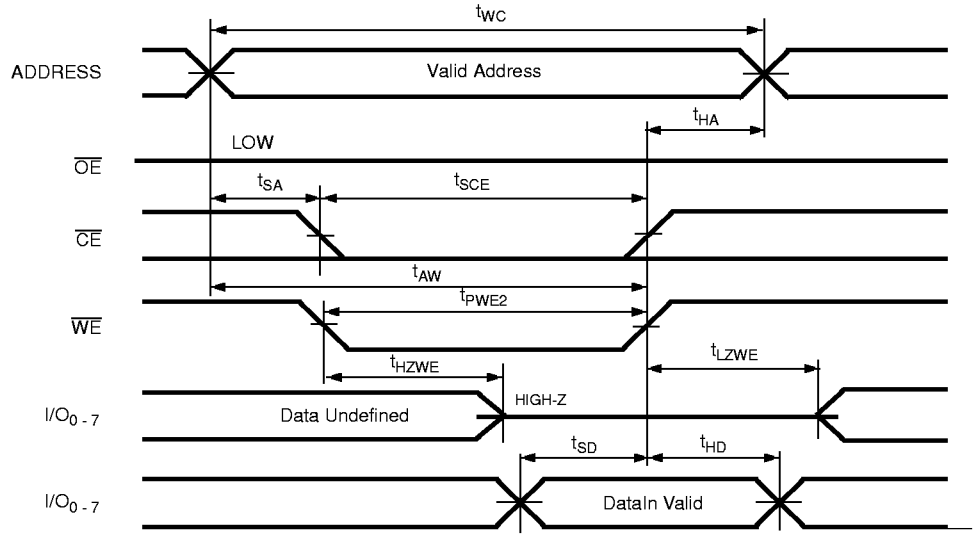
9A128-7

Write Cycle No.2 ($\overline{OE}$ is HIGH During Write Cycle)



9A128-8

Write Cycle No.3 ($\overline{OE}$ is LOW During Write Cycle)



9A128-9

Truth Table

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O	I_{CC}
Not Selected (Power Down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

Ordering Information

Speed	Part Number	Package Name	Package Type	Temperature Range
12	AP9A128-12VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A128-12VI	V28.1	28-Pin Small Outline J-Bend	Industrial
	AP9A128-12VM	V28.1	28-Pin Small Outline J-Bend	Military
	AP9A128-12TC	T28.1	28-Pin Thin Small Outline Package	Commercial
15	AP9A128-15VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A128-15VI	V28.1	28-Pin Small Outline J-Bend	Industrial
	AP9A128-15VM	V28.1	28-Pin Small Outline J-Bend	Military
	AP9A128-15TC	T28.1	28-Pin Thin Small Outline Package	Commercial
20	AP9A128-20VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A128-20VI	V28.1	28-Pin Small Outline J-Bend	Industrial
	AP9A128-20VM	V28.1	28-Pin Small Outline J-Bend	Military
	AP9A128-20TC	T28.1	28-Pin Thin Small Outline Package	Commercial

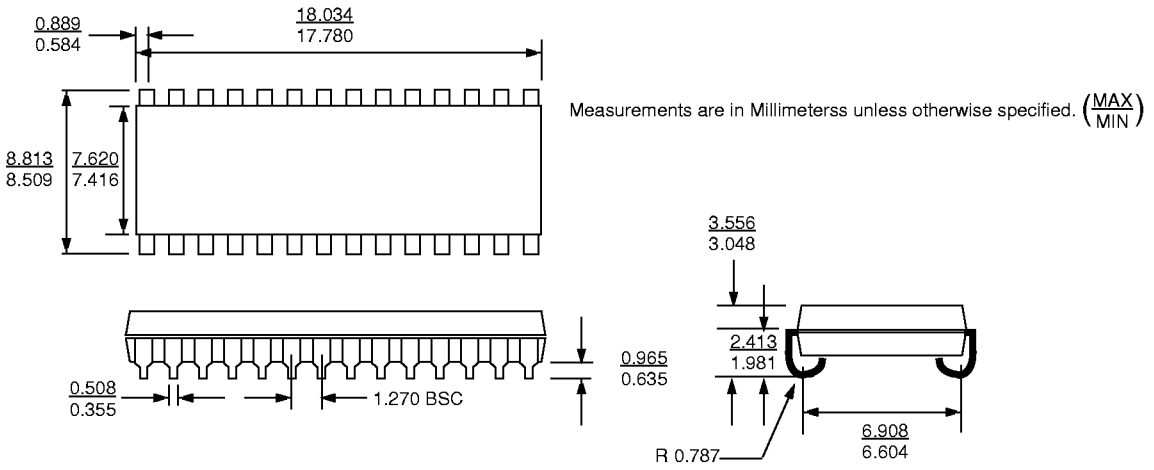
Reverse Pin-Out TSOP, only

Speed	Part Number	Package Name	Package Type	Temperature Range
12	AP9A129-12TC	T28.1	28-Pin Thin Small Outline Package	Commercial
15	AP9A129-15TC	T28.1	28-Pin Thin Small Outline Package	Commercial
20	AP9A129-20TC	T28.1	28-Pin Thin Small Outline Package	Commercial

Document # DS-00007-Rev E

Package Diagrams

V28.1 - 28-Pin Small Outline J-Bend (SOJ)



T28.1 - 28-Pin Thin Small Outline Package (TSOP)