



## P-Channel 100-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>c</sup>	$Q_g$ (Typ.)
- 100	0.043 at $V_{GS} = - 10$ V	- 36	54 nC
	0.048 at $V_{GS} = - 4.5$ V	- 34.4	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 %  $R_g$  Tested
- Compliant to RoHS Directive 2002/95/EC

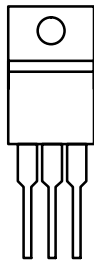


RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- LCD Inverter
- Backlighting

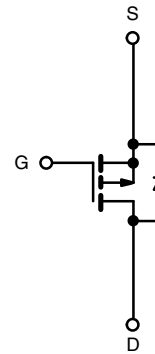
TO-220AB



G D S

Top View

Drain connected to Tab



P-Channel MOSFET

Ordering Information: SUP40P10-43-GE3 (Lead (Pb)-free and Halogen-free)

### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	- 100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>c</sup>	$I_D$	$T_C = 25$ °C	- 36	A
		$T_C = 125$ °C	- 16	
Pulsed Drain Current	$I_{DM}$	- 40		
Avalanche Current	$I_{AS}$	- 35		
Single Pulse Avalanche Energy <sup>a</sup>	$E_{AS}$	61	mJ	
Power Dissipation	$P_D$	$T_C = 25$ °C	125 <sup>b</sup>	W
		$T_A = 25$ °C	2.0	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air	$R_{thJA}$	62	°C/W
Junction-to-Case	$R_{thJC}$	1.0	

Notes:

a. Duty cycle  $\leq 1$  %.

b. See SOA curve for voltage derating.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-109		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = -250\text{ }\mu\text{A}$		5.9		
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			-200	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-40			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		0.036	0.043	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -10\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.078	
		$V_{GS} = -10\text{ V}, I_D = -10\text{ A}, T_J = 150\text{ }^\circ\text{C}$			0.088	
		$V_{GS} = -4.5\text{ V}, I_D = -8\text{ A}$		0.040	0.048	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -10\text{ A}$		38		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -50\text{ V}, f = 1\text{ MHz}$		4600		$\mu\text{F}$
Output Capacitance	$C_{oss}$			230		
Reverse Transfer Capacitance	$C_{rss}$			175		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		106	160	nC
		$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		54	81	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		14		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			26		
Gate Resistance	$R_g$	$f = 1.0\text{ MHz}$	0.8	4	8	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.3\text{ }\Omega$ $I_D \cong -8\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1.0\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			20	30	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			110	165	
Fall Time <sup>c</sup>	$t_f$			100	150	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.3\text{ }\Omega$ $I_D \cong 8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1.0\text{ }\Omega$		42	65	
Rise Time <sup>c</sup>	$t_r$			160	240	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			100	150	
Fall Time <sup>c</sup>	$t_f$			100	150	
<b>Source-Drain Diode Ratings and Characteristics <math>T_C = 25\text{ }^\circ\text{C}</math><sup>b</sup></b>						
Continuous Current	$I_S$				-40	A
Pulsed Current	$I_{SM}$				-40	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = -10\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = -8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		60	90	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			-5	-7.5	A
Reverse Recovery Charge	$Q_{rr}$				150	225

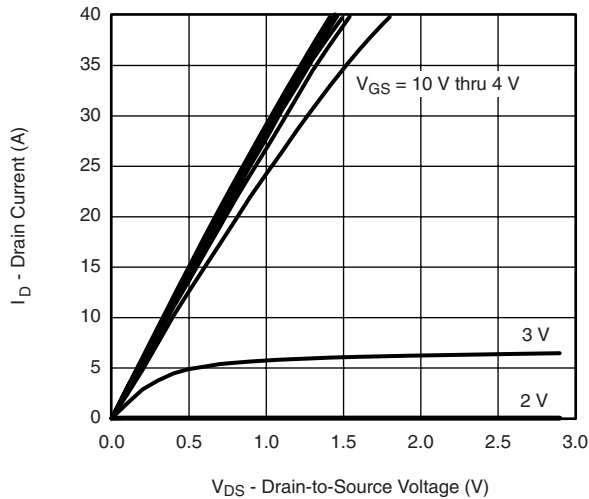
## Notes:

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

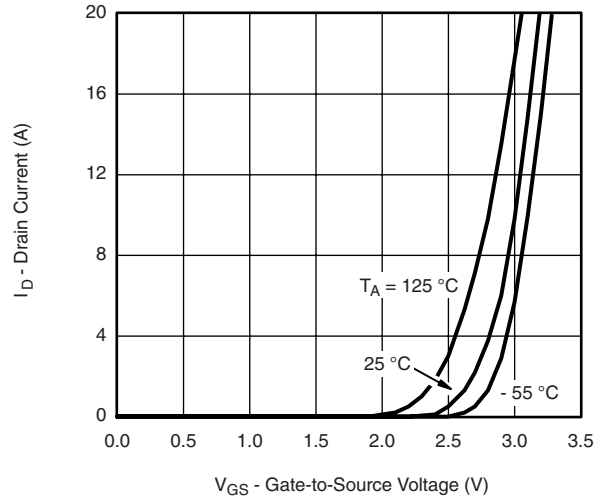


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



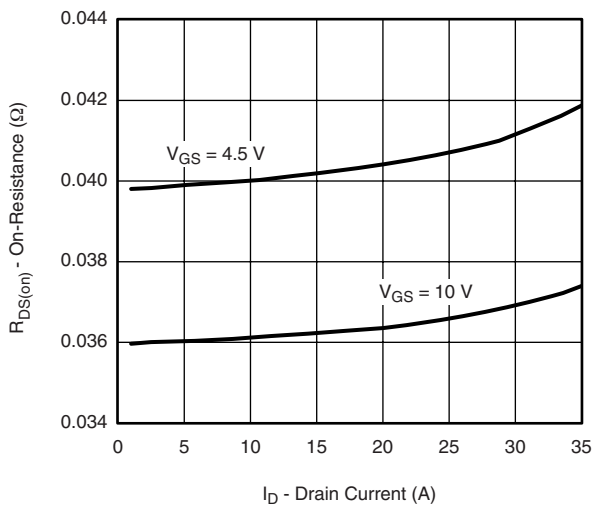
$V_{DS}$  - Drain-to-Source Voltage (V)

**Output Characteristics**

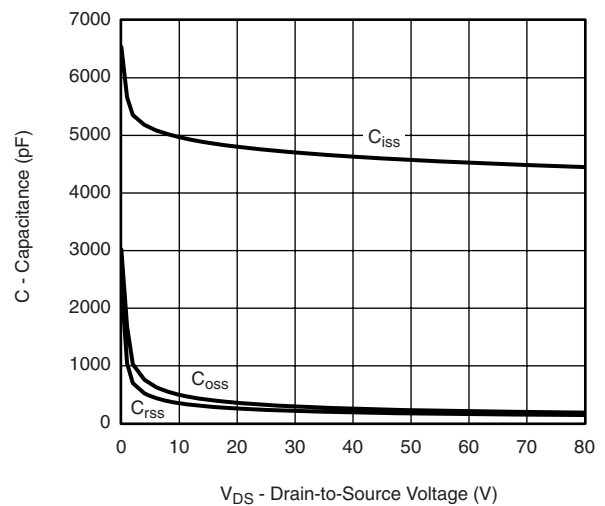


$V_{GS}$  - Gate-to-Source Voltage (V)

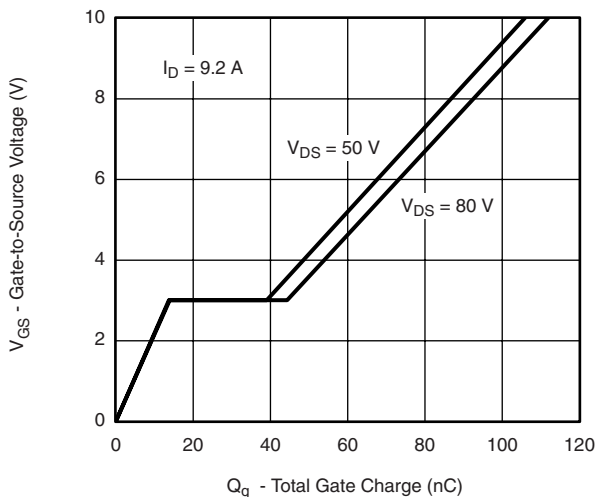
**Transfer Characteristics**



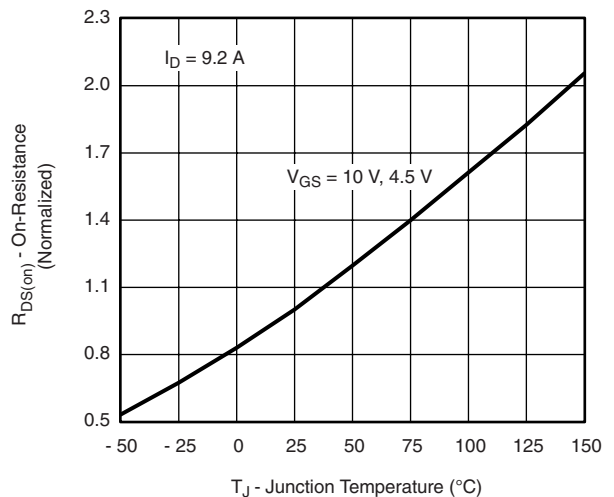
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



**Gate Charge**



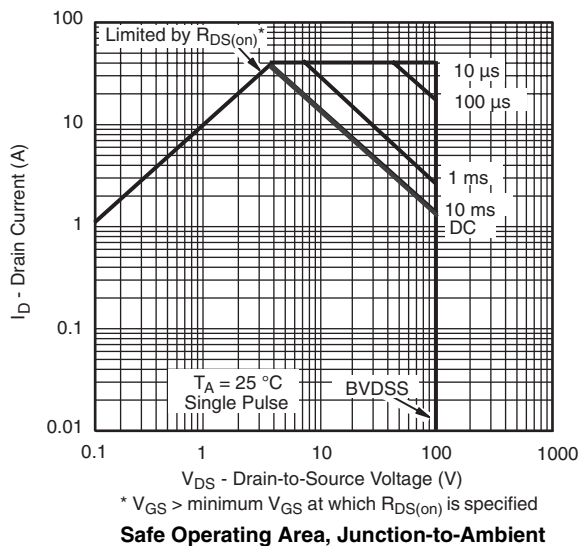
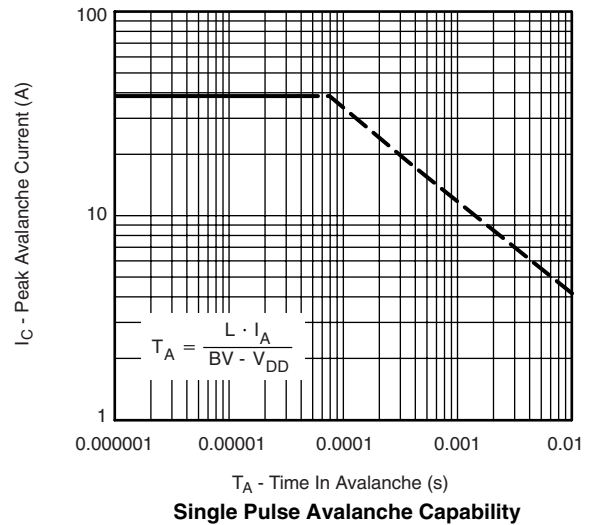
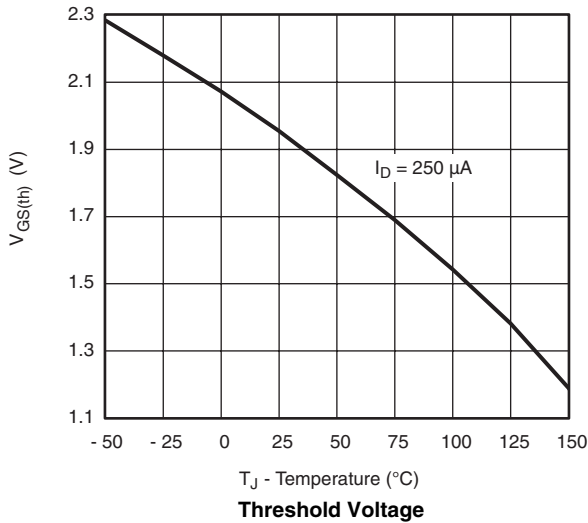
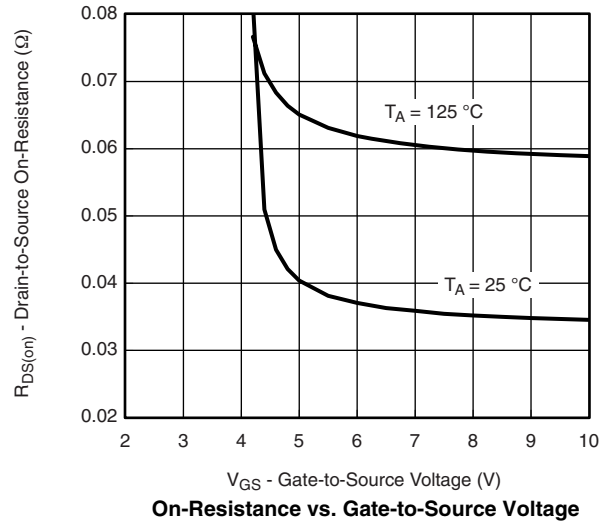
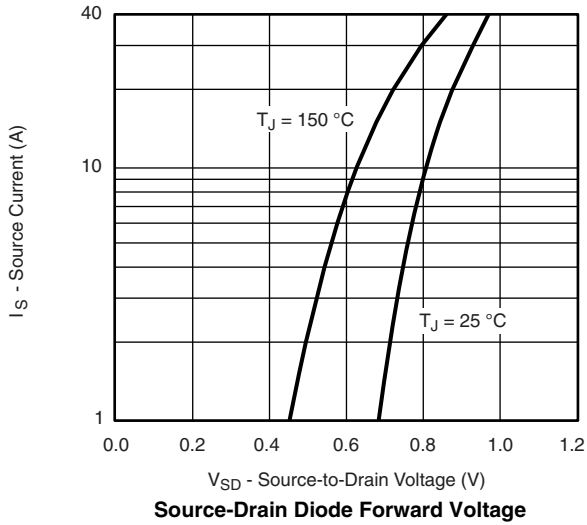
**On-Resistance vs. Junction Temperature**

# SUP40P10-43



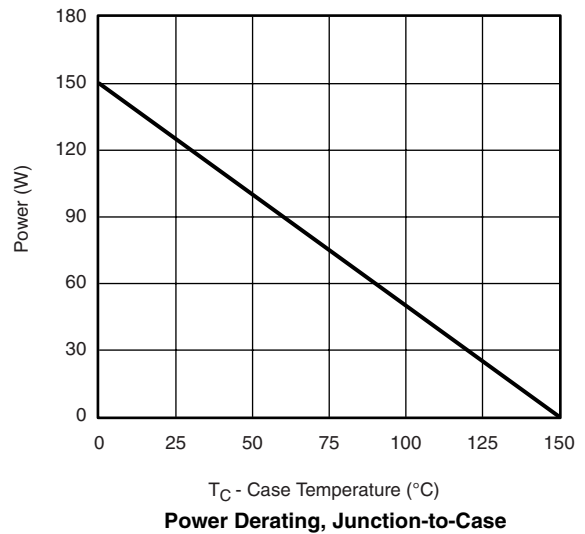
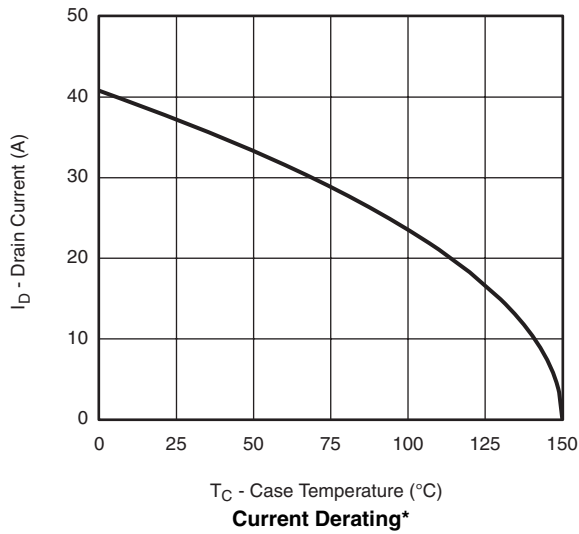
Vishay Siliconix

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

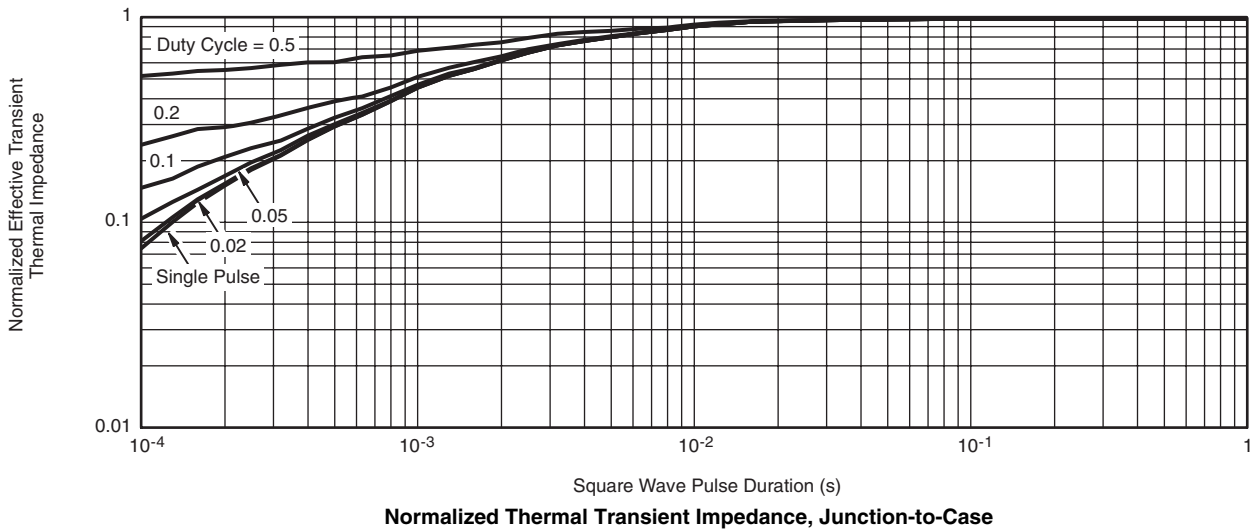




**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

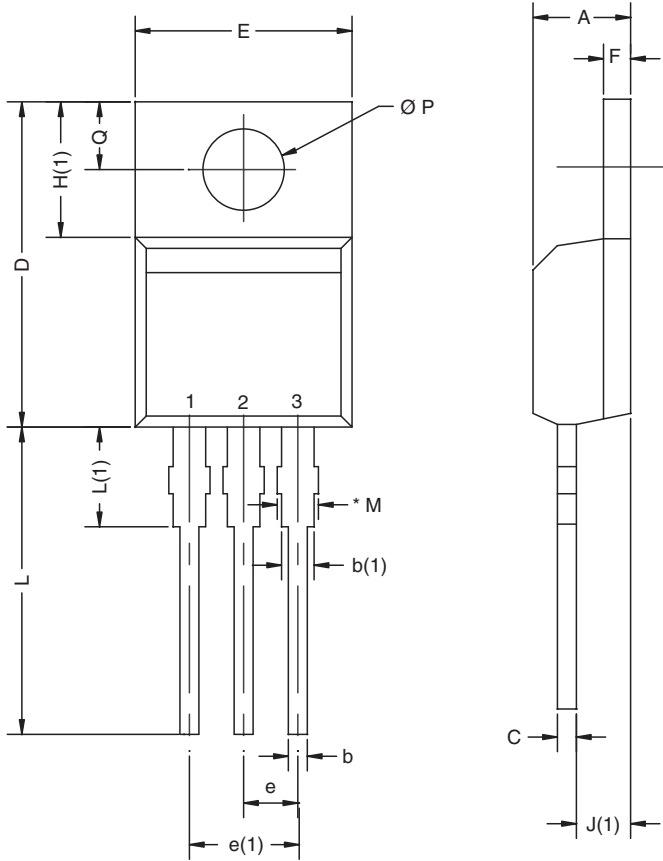


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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## TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X10-0416-Rev. M, 01-Nov-10  
DWG: 5471

**Note**

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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