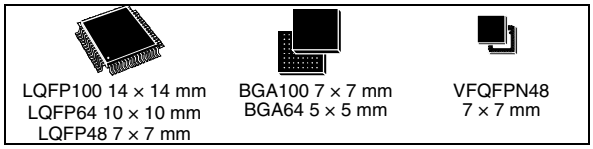
STM32L151xx
STM32L152xx

Ultralow power ARM-based 32-bit MCU with up to 128 KB Flash, RTC, LCD, USB, USART, I2C, SPI, timers, ADC, DAC, comparators

Preliminary data

Features

- Operating conditions
  - Operating power supply range: 1.65 V to 3.6 V (without BOR) or 1.8 V to 3.6 V (with BOR option)
  - Temperature range: –40 to 85 °C
- Low power features
  - 4 modes: Sleep, Low-power run (15 µA at 32 kHz), Low-power sleep (4 µA), Stop with RTC (1.2 µA), Stop (0.5 µA), Standby (0.27 µA)
  - Dynamic core voltage scaling down to 233 µA/MHz
  - Ultralow leakage per I/O: 50 nA
  - Fast wakeup from Stop: 8 µs
  - Three wakeup pins
- Core: ARM 32-bit Cortex™-M3 CPU
  - 32 MHz maximum frequency, 33.3 DMIPS peak (Dhrystone 2.1)
  - Memory protection unit
- Reset and supply management
  - Low power, ultrasafe BOR (brownout reset) with 5 selectable thresholds
  - Ultralow power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 1 to 24 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 16 MHz factory-trimmed RC
  - Internal 37 kHz low consumption RC
  - Internal multispeed low power RC, 64 kHz to 4 MHz with a consumption down to 1.5 µA
  - PLL for CPU clock and USB (48 MHz)
- Low power calendar RTC
  - Alarm, periodic wakeup from Stop/Standby
- Memories
  - Up to 128 Kbyte of Flash memory with ECC



  - 4 Kbyte of data EEPROM with ECC
  - Up to 16 Kbyte of RAM
- Up to 83 fast I/Os (73 of which are 5 V-tolerant) all mappable on 16 external interrupt vectors
- Development support
  - Serial wire debug, JTAG and trace
- DMA: 7-channel DMA controller, supporting timers, ADC, SPIs, I^2Cs and USARTs
- LCD 8 × 40 or 4 × 44 with step-up converter
- 12-bit ADC up to 1 Msps/24 channels
  - Temperature sensor and internal voltage reference
  - Operates down to 1.8 V
- 2 × 12-bit DACs with output buffers
- 2 ultralow power comparators
  - Window mode and wakeup capability
- 10 timers:
  - 6 × 16-bit general-purpose timers, each with up to 4 IC/OC/PWM channels
  - 2 × 16-bit basic timers
  - 2 × watchdog timers (independent and window)
- Up to 8 communication interfaces
  - Up to 2 × I^2C interfaces (SMBus/PMBus)
  - Up to 3 × USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 × SPIs (16 Mbit/s)
  - USB 2.0 full-speed interface
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32L151xx	STM32L151CB, STM32L151RB, STM32L151VB, STM32L151C8, STM32L151R8, STM32L151V8
STM32L152xx	STM32L152CB, STM32L152RB, STM32L152VB, STM32L152C8, STM32L152R8, STM32L152V8

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xx and STM32L152xx ultralow power ARM Cortex™-based microcontrollers product line.

The ultralow power STM32L15xxx family includes devices in 3 different package types: from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultralow power STM32L15xxx microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the *www.arm.com* website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337g.

Figure 1 shows the general block diagram of the device family.

2 Description

The ultralow power STM32L15xxx incorporates the connectivity power of the universal serial bus (USB) with the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer a 12-bit ADC, 2 DACs and 2 ultralow power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases. Moreover, the STM32L15xxx devices contain standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs and a USB. They also include a real-time clock and a set of backup registers that remain powered in Standby mode. Finally, the integrated LCD controller has a built-in LCD voltage generator that allows you to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultralow power STM32L15xxx operates from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications

2.1 Device overview

Table 2. Ultralow power STM32L15xxx device features and peripheral counts

Peripheral		STM32L15xCx		STM32L15xRx		STM32L15xVx	
Flash - Kbytes		64	128	64	128	64	128
RAM - Kbytes		10	16	10	16	10	16
Timers	General-purpose	6		6		6	
	Basic	2		2		2	
Communication interfaces	SPI	2		2		2	
	I^2C	2		2		2	
	USART	3		3		3	
	USB	1		1		1	
GPIOs		37		51		83	
12-bit synchronized ADC Number of channels		1 16 channels		1 20 channels		1 24 channels	
12-bit DAC Number of channels		2 2		2 2		2 2	
LCD (STM32L152xx Only) COM x SEG		4x16		4x32 8x28		4x44 8x40	
Comparator		2		2		2	
CPU frequency		32 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V (down to 1.65 V at power-down) without BOR option					
Operating temperatures		Ambient temperatures: –40 to +85 °C Junction temperature: –40 to + 105 °C					
Packages		LQFP48, VFQFN48		LQFP64, BGA64		LQFP100, BGA100	

2.2 Ultralow power device continuum

The ultralow power STM32L151xx and STM32L152xx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultralow power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics 0.13 µm ultralow leakage process.

Note: The ultralow power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultralow power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L15xxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC, and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L15xx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultralow consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

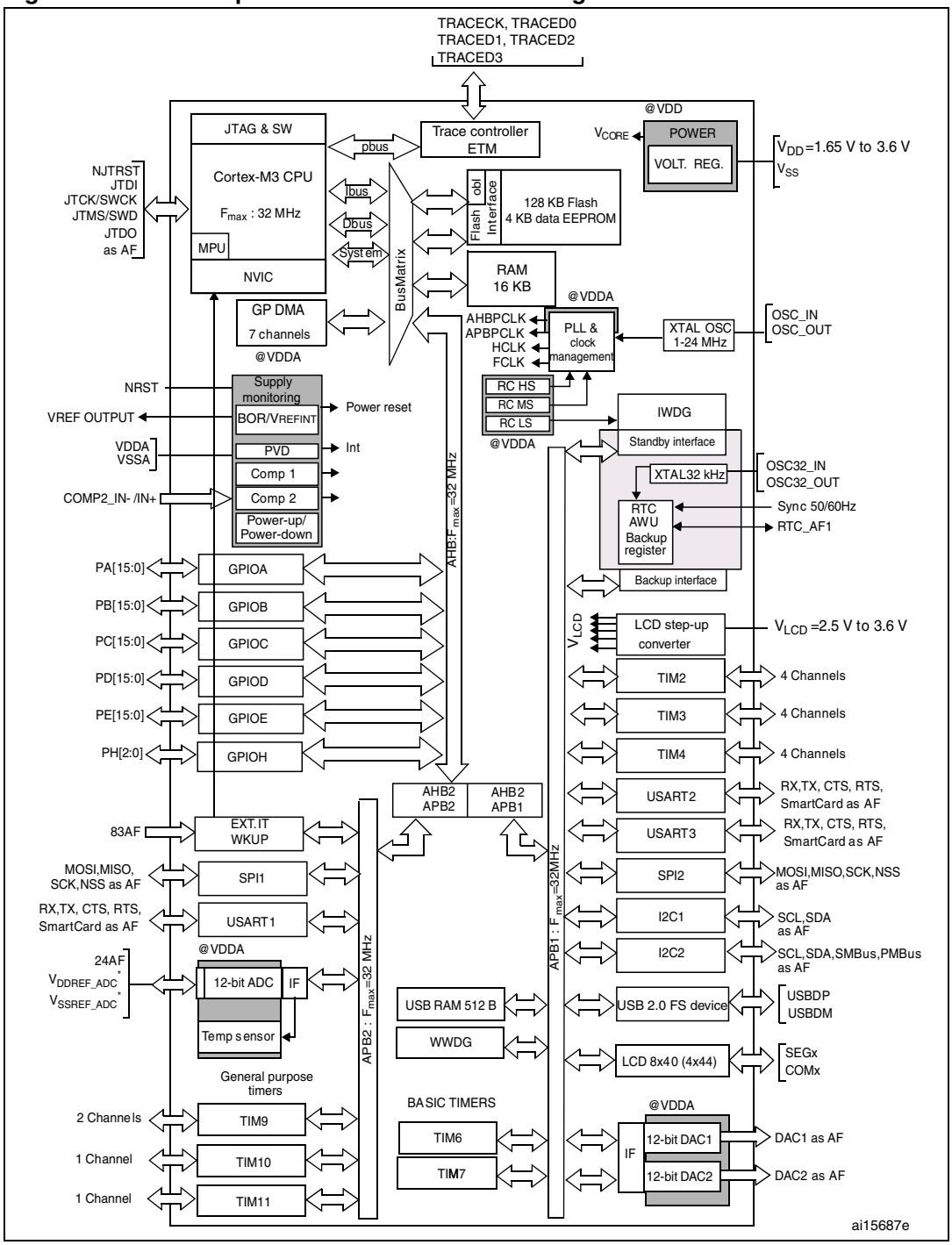
ST ultralow power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

3 Functional overview

Figure 1 shows the block diagrams.

Figure 1. Ultralow power STM32L15xxx block diagram



1. T_A = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

3.1 Low power modes

The ultralow power STM32L15xxx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply. When executing from Flash memory, the consumptions are:

- In range 1 (V_{DD} range limited to 2.0-3.6 V), with the CPU running at up to 32 MHz, the consumption is: 290 µA/MHz
- In range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz, the consumption is: 235 µA/MHz
- In range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source), the consumption is: 200 µA/MHz.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. The Sleep mode power consumption at 16 MHz is of about 1 mA with all peripherals off.

- **Low power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (64 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

  The Low power run mode consumption can be as low as 10.5 µA when executing code from RAM at 32 kHz.

- **Low power sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on. The Low power sleep mode consumption is as low as 4 µA when no peripheral is enabled. It is of 5 µA with one timer operating at 32 kHz.

- **Stop** mode (with or without RTC)

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The voltage regulator is in the low power mode.
  The device can be woken up from the Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm(s), the USB wakeup, the RTC tamper event, the RTC timestamp event, the RTC Wakeup, the Comparator 1 event or Comparator 2 event. The Stop mode consumption with the RTC on the LSE is of 1.3 µA (at 1.8 V) and 1.6 µA (at 3.0 V). The Stop mode consumption without the RTC is of 0.5 µA.

- **Standby** mode (with or without RTC)

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The

PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC CSR).

The device exits the Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event. The Standby mode consumption is of 1µA (at 1.8 V) and 1.3 µA (at 3.0 V) with the RTC on, and of 270 nA with the RTC off.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

3.2 ARM® Cortex™-M3 core with MPU

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L15xxx is compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultralow power STM32L15xxx embeds a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

For devices operating between 1.8 and 3.6 V, the BOR is always active at power-on and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V). Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms.
For devices operating between 1.65 V and 3.6 V, the BOR is permanently disabled.
Consequently, the start-up time at power-on can be decreased down to 1ms typically.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode: the regulator output is high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC CSR)

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. For further details please refer to AN2606.

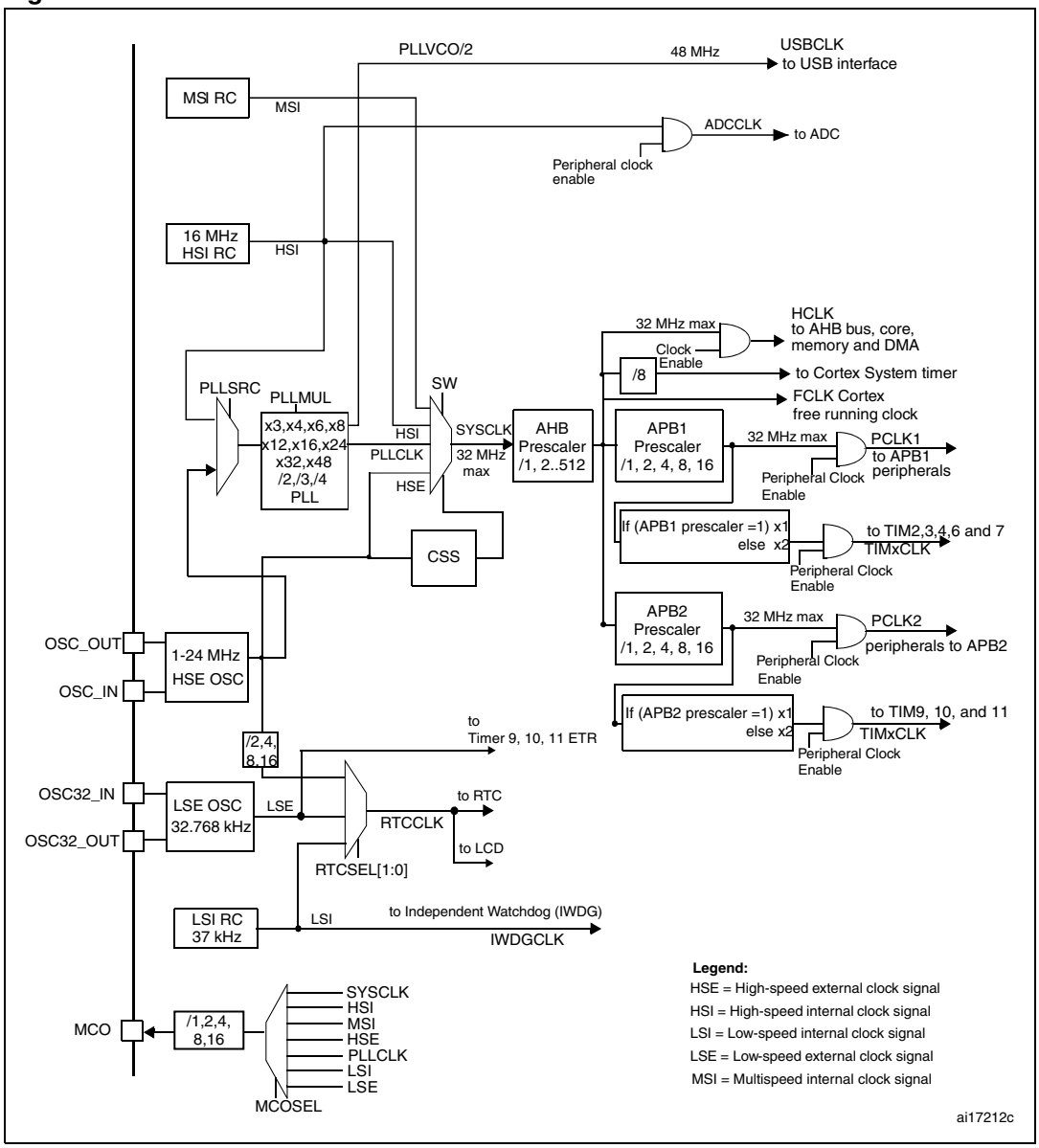
3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best tradeoff between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock source**: three different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (64 kHz, 128 kHz, 256 kHz, 512 kHz, 1.02 MHz, 2.05 MHz, 4.1 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultralow power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



3. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.

3.5 Low power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made

automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.

- The programmable wakeup time ranges from 120 µs to 36 hours
- Stop mode consumption with LSI and Auto-wakeup: 1.2 µA (at 1.8 V) and 1.4 µA (at 3.0 V)
- Stop mode consumption with LSE, calendar and Auto-wakeup: 1.3 µA (at 1.8V), 1.6 µA (at 3.0 V)

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high-current-capable except for analog pins. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines.

3.7 Memories

The STM32L15xxx devices have the following features:

- Up to 16 Kbyte of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 64 or 128 Kbyte of embedded Flash program memory
  - 4 Kbyte of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L15xxx devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers.

The ADC includes a specific low power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L15xxx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultralow power comparators and reference voltage

The STM32L15xxx embeds two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

3.14 Timers and watchdogs

The ultralow power STM32L15xxx devices include six general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.14.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L15xxx devices (see *Table 3* for differences).

TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.14.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals. They support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.15.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.15.4 Universal serial bus (USB)

The STM32L15xxx embeds a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.16 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.17 Development support

Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L15xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pin descriptions

Figure 3. STM32L15xxx UFBGA100 ballout

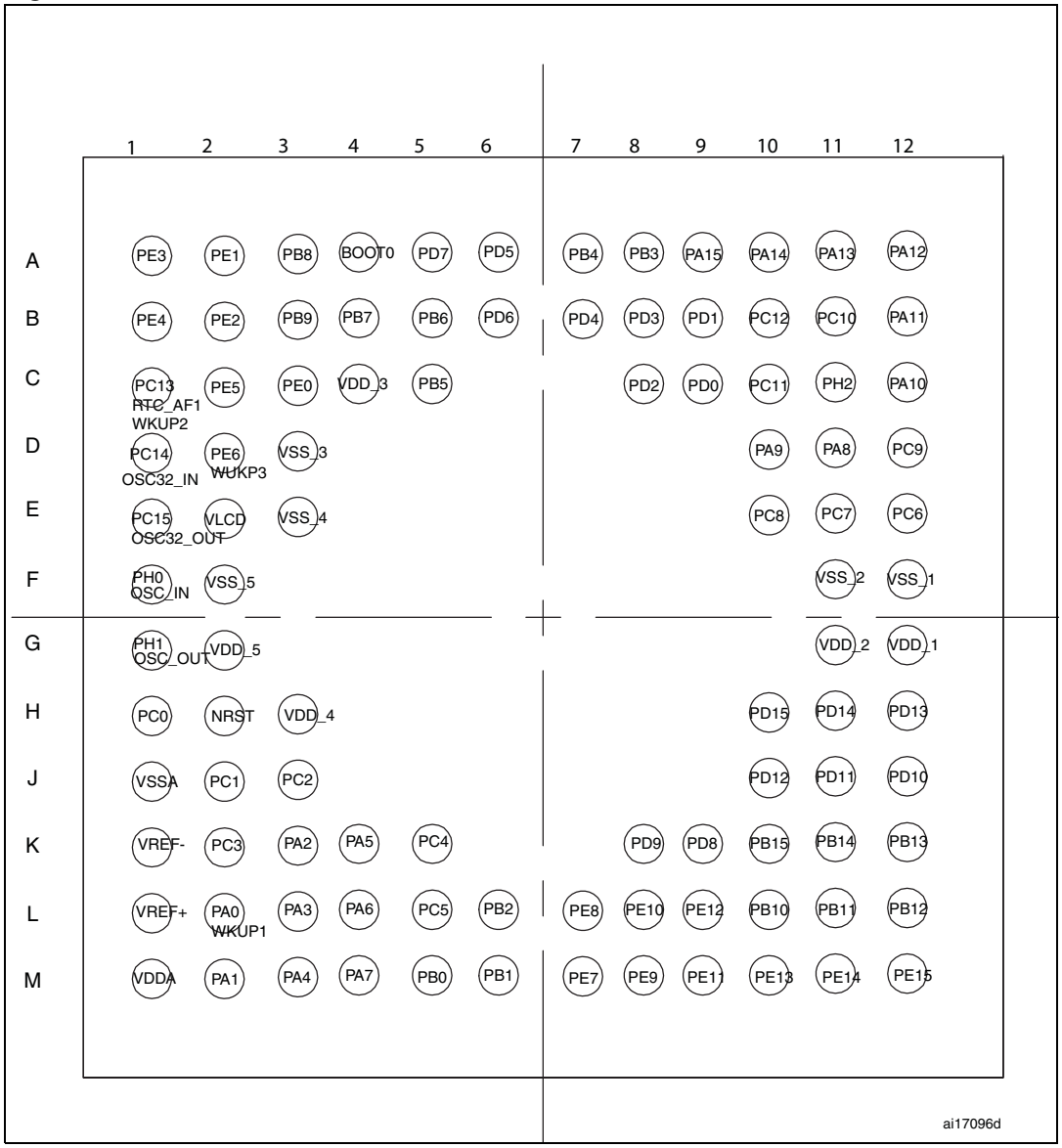


Figure 4. STM32L15xxx TFBGA64 ballout

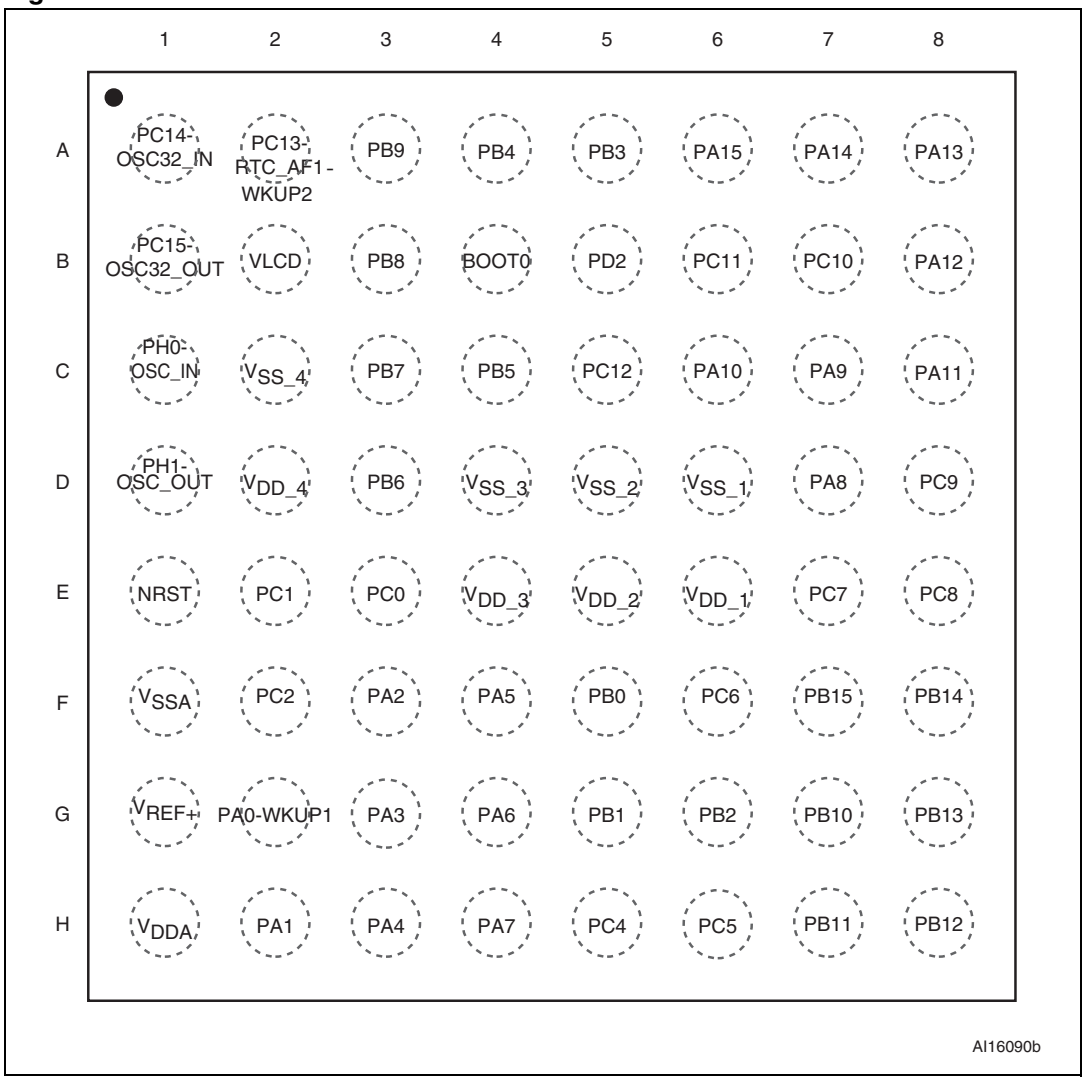


Figure 5. STM32L15xxx LQFP100 pinout

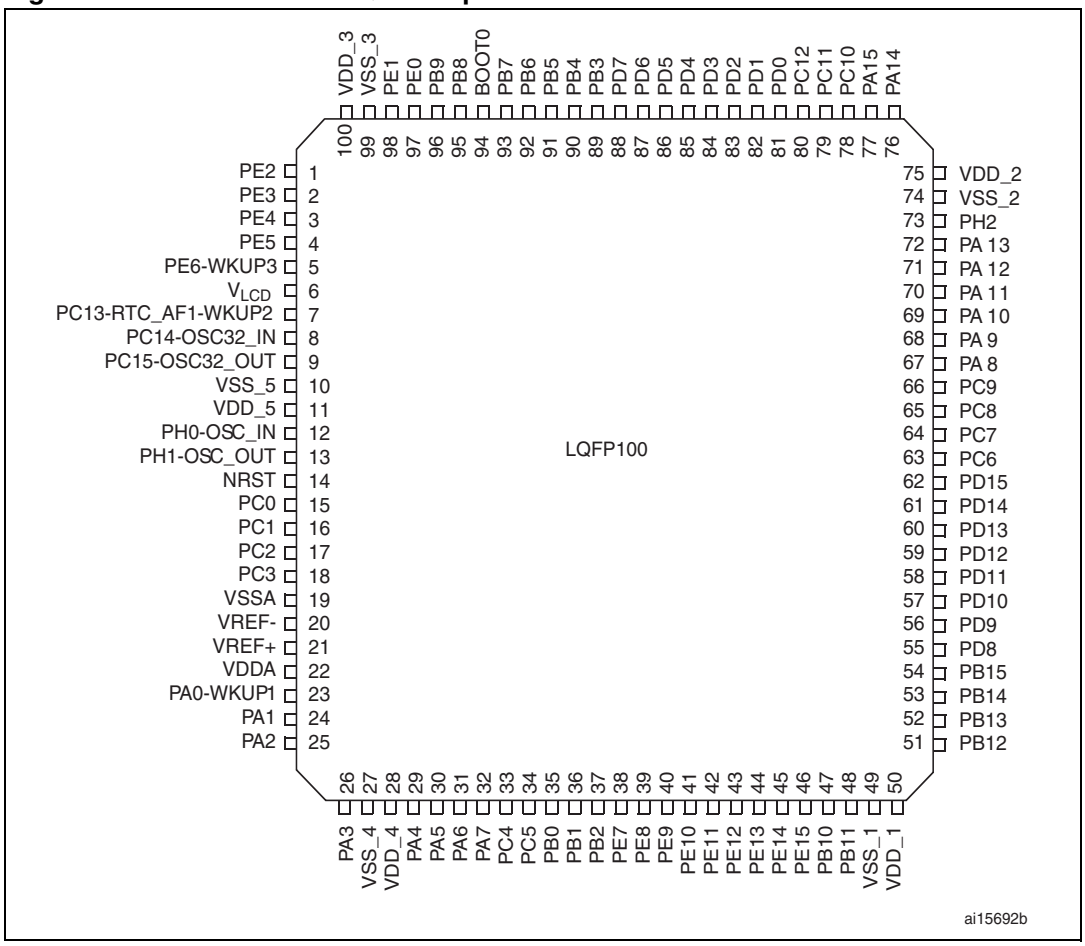


Figure 6. STM32L15xxx LQFP64 pinout

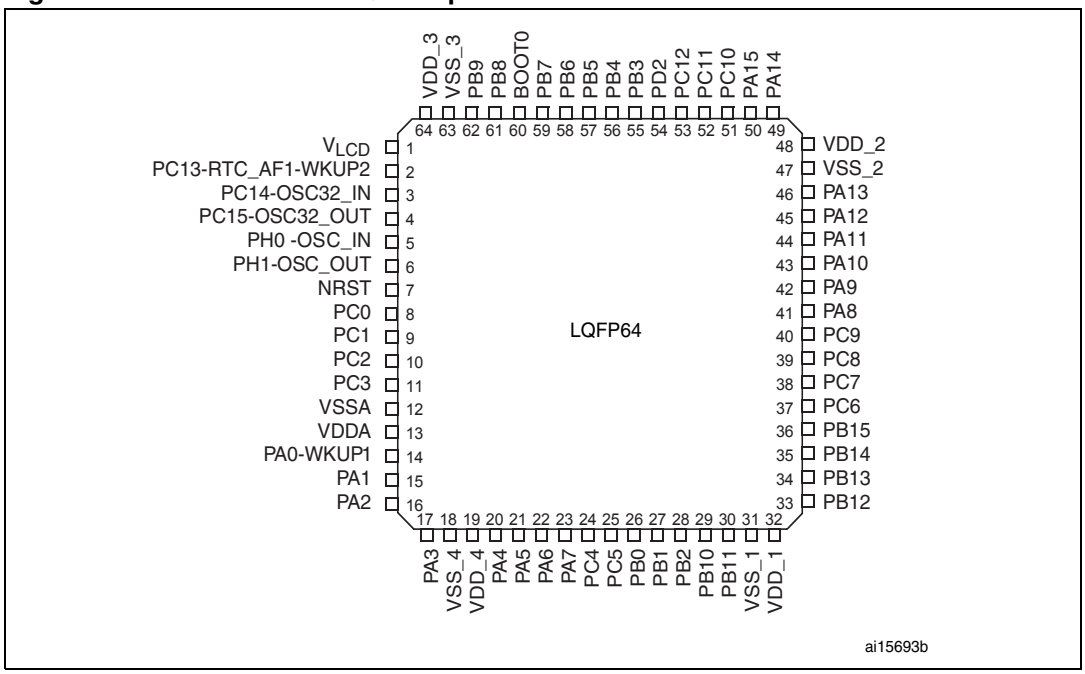


Figure 7. STM32L15xxx LQFP48 pinout

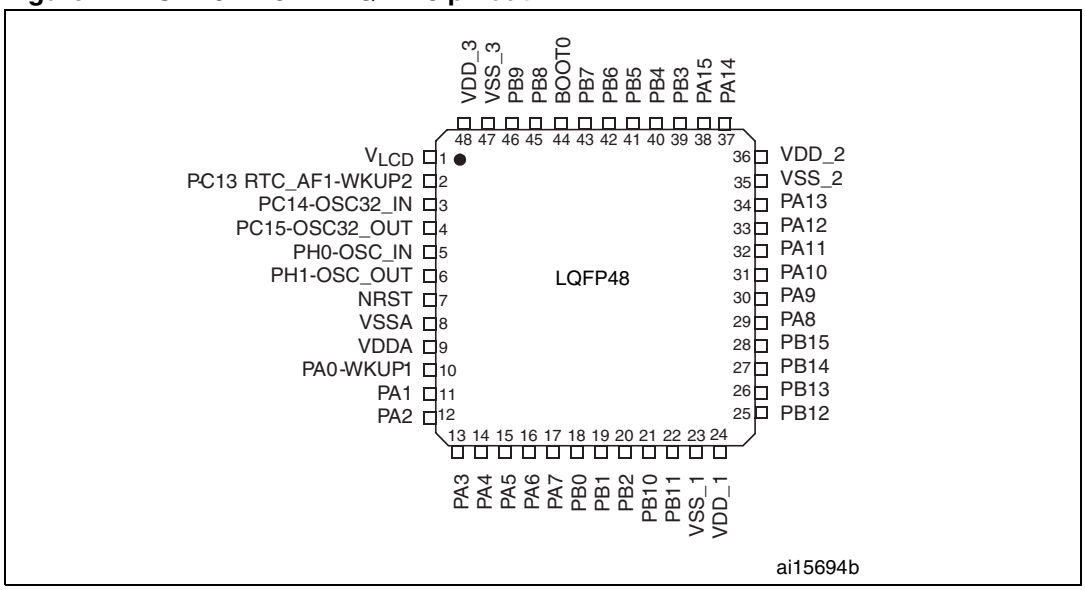


Figure 8. STM32L15xxx VFQFPN48 pinout

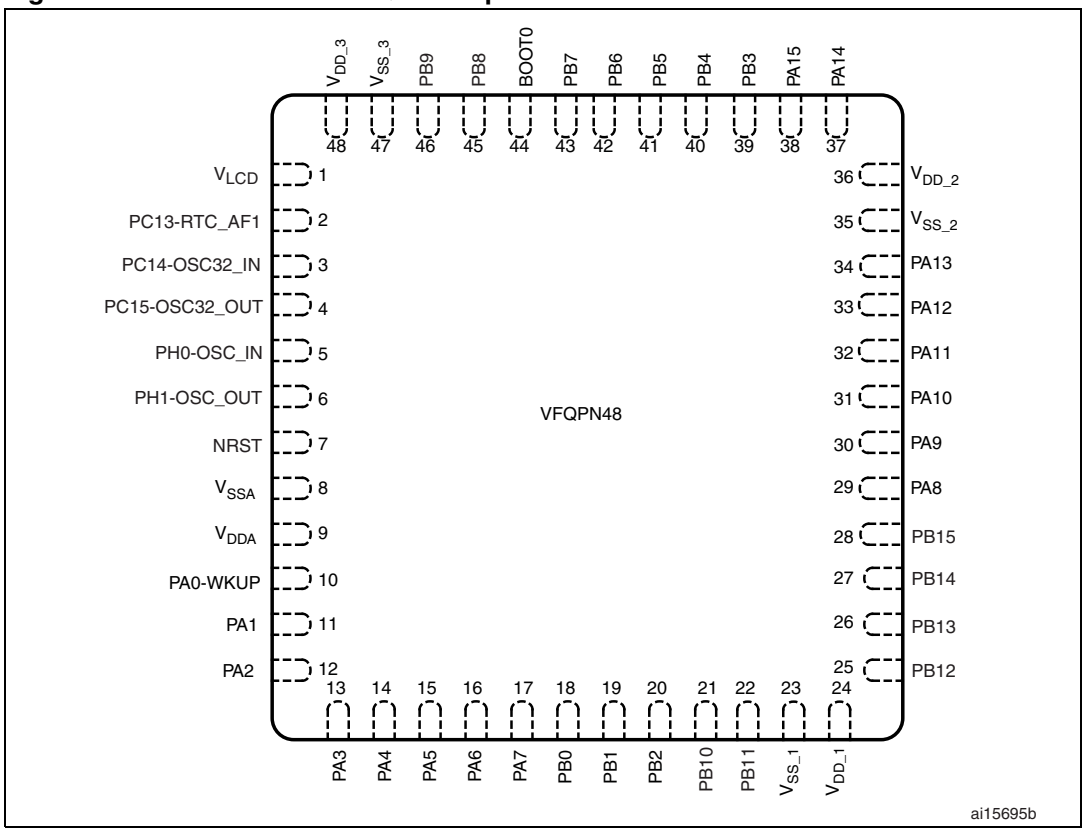


Table 4. STM32L15xxx pin definitions

Pins					Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or VFQFPN48					
1	-		B2	-	PE2	I/O	FT	PE2	TRACECK/LCD_SEG38/TIM3_ETR
2	-		A1	-	PE3	I/O	FT	PE3	TRACED0/LCD_SEG39/TIM3_CH1
3	-		B1	-	PE4	I/O	FT	PE4	TRACED1/TIM3_CH2
4	-		C2	-	PE5	I/O	FT	PE5	TRACED2/TIM9_CH1
5	-		D2	-	PE6	I/O	FT	PE6	TRACED3/WKUP3/TIM9_CH2
6	1	B2	E2	1	V_{LCD}(4)	S		V_{LCD}	
7	2	A2	C1	2	PC13-RTC_AF1	I/O	FT	PC13	RTC_AF1/WKUP2
8	3	A1	D1	3	PC14-OSC32_IN	I/O		PC14	OSC32_IN
9	4	B1	E1	4	PC15-OSC32_OUT	I/O		PC15	OSC32_OUT
10	-	-	F2	-	V_{SS_5}	S		V_{SS_5}	
11	-	-	G2	-	V_{DD_5}	S		V_{DD_5}	
12	5	C1	F1	5	PH0-OSC_IN(5)	I		OSC_IN	PH0
13	6	D1	G1	6	PH1-OSC_OUT	O		OSC_OUT	PH1
14	7	E1	H2	7	NRST	I/O		NRST	
15	8	E3	H1	-	PC0	I/O	FT	PC0	ADC_IN10/LCD_SEG18/ COMP1_INP
16	9	E2	J2	-	PC1	I/O	FT	PC1	ADC_IN11/LCD_SEG19/ COMP1_INP
17	10	F2	J3	-	PC2	I/O	FT	PC2	ADC_IN12/LCD_SEG20/ COMP1_INP
18	11	-(6)	K2	-	PC3	I/O	FT	PC3	ADC_IN13/LCD_SEG21/ COMP1_INP
19	12	F1	J1	8	V_{SSA}	S		V_{SSA}	
20	-	-	K1	-	V_{REF-}	S		V_{REF-}	
21	-	G1 (6)	L1	-	V_{REF+}	S		V_{REF+}	
22	13	H1	M1	9	V_{DDA}	S		V_{DDA}	
23	14	G2	L2	10	PA0-WKUP1	I/O	FT	PA0	WKUP1/USART2_CTS/ADC_IN0/TIM2_CH1_ETR/ COMP1_INP

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or VFQFPN48					
24	15	H2	M2	11	PA1	I/O	FT	PA1	USART2_RTS/ADC_IN1/ TIM2_CH2/LCD_SEG0/ COMP1_INP
25	16	F3	K3	12	PA2	I/O	FT	PA2	USART2_TX/ADC_IN2/ TIM2_CH3/TIM9_CH1/ LCD_SEG1/COMP1_INP
26	17	G3	L3	13	PA3	I/O	FT	PA3	USART2_RX/ADC_IN3/TIM2_CH4/TIM9_CH2/ LCD_SEG2/COMP1_INP
27	18	C2	E3	-	V_{SS_4}	S		V_{SS_4}	
28	19	D2	H3	-	V_{DD_4}	S		V_{DD_4}	
29	20	H3	M3	14	PA4	I/O		PA4	SPI1_NSS/ USART2_CK/ ADC_IN4/DAC_OUT1/COMP1_INP
30	21	F4	K4	15	PA5	I/O		PA5	SPI1_SCK/ADC_IN5/ DAC_OUT2/TIM2_CH1_ETR/COMP1_INP
31	22	G4	L4	16	PA6	I/O	FT	PA6	SPI1_MISO/ADC_IN6/TIM3_CH1/TIM1_BKIN/ LCD_SEG3/TIM10_CH1/ COMP1_INP
32	23	H4	M4	17	PA7	I/O	FT	PA7	SPI1_MOSI/ADC_IN7/TIM3_CH2/TIM1_CH1N/ LCD_SEG4/TIM11_CH1/COMP1_INP
33	24	H5	K5	-	PC4	I/O	FT	PC4	ADC_IN14/LCD_SEG22/COMP1_INP
34	25	H6	L5	-	PC5	I/O	FT	PC5	ADC_IN15/LCD_SEG23/COMP1_INP
35	26	F5	M5	18	PB0	I/O	FT	PB0	ADC_IN8/TIM3_CH3/LCD_SEG5/ COMP1_INP/VREF_OUT
36	27	G5	M6	19	PB1	I/O	FT	PB1	ADC_IN9/TIM3_CH4/LCD_SEG6/ COMP1_INP/VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/BOOT1	
38	-	-	M7	-	PE7	I/O		PE7	ADC_IN22/COMP1_INP
39	-	-	L7	-	PE8	I/O		PE8	ADC_IN23/COMP1_INP
40	-	-	M8	-	PE9	I/O		PE9	ADC_IN24/TIM2_CH1_ETR/COMP1_INP
41	-	-	L8	-	PE10	I/O		PE10	ADC_IN25/TIM2_CH2/COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or VFQFPN48					
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/TIM2_CH3/LCD_SEG10
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX/TIM2_CH4/LCD_SEG11
49	31	D6	F12	23	V_{SS_1}	S		V_{SS_1}	
50	32	E6	G12	24	V_{DD_1}	S		V_{DD_1}	
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/USART3_CK/LCD_SEG12/ ADC_IN18/COMP1_INP/TIM10_CH1
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/LCD_SEG13/ADC_IN19/ COMP1_INP/TIM9_CH1
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/LCD_SEG14/ADC_IN20/ COMP1_INP/TIM9_CH2
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N/LCD_SEG15/ADC_IN21/ COMP1_INP/TIM11_CH1/RTC_50_60Hz
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/LCD_SEG28
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/LCD_SEG29
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/LCD_SEG30
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/LCD_SEG31
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1 / USART3_RTS/ LCD_SEG32
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24
64	38	E7	E11		PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25
65	39	E8	E10		PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27
67	41	D7	D11	29	PA8	I/O	FT	PA8	USART1_CK/MCO/LCD_COM0
68	42	C7	D10	30	PA9	I/O	FT	PA9	USART1_TX / LCD_COM1
69	43	C6	C12	31	PA10	I/O	FT	PA10	USART1_RX / LCD_COM2
70	44	C8	B12	32	PA11	I/O	FT	PA11	USART1_CTS/ USBDM/SPI1_MISO
71	45	B8	A12	33	PA12	I/O	FT	PA12	USART1_RTS/USBDP/SPI1_MOSI
72	46	A8	A11	34	PA13	I/O	FT	JTMS/SWDIO	PA13

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or VFQFPN48					
73	-	-	C11	-	PH2	I/O	FT	PH2	I2C2_SMBA
74	47	D5	F11	35	V_{SS_2}	S		V_{SS_2}	
75	48	E5	G11	36	V_{DD_2}	S		V_{DD_2}	
76	49	A7	A10	37	PA14	I/O	FT	JTCK/SWCLK	PA14
77	50	A6	A9	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/ PA15/SPI1_NSS/LCD_SEG17
78	51	B7	B11	-	PC10	I/O	FT	PC10	USART3_TX/LCD_SEG28/LCD_SEG40/ LCD_COM4
79	52	B6	C10	-	PC11	I/O	FT	PC11	USART3_RX/LCD_SEG29/LCD_SEG41/LCD_COM5
80	53	C5	B10	-	PC12	I/O	FT	PC12	USART3_CK/LCD_SEG30/LCD_SEG42/LCD_COM6
81	5	C1	C9	5	PD0	I/O	FT	OSC_IN	SPI2_NSS/TIM9_CH1
82	6	D1	B9	6	PD1	I/O	FT	OSC_OUT	SPI2_SCK
83	54	B5	C8		PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31/LCD_SEG43/LCD_COM7
84	-	-	B8	-	PD3	I/O	FT	PD3	USART2_CTS/SPI2_MISO
85	-	-	B7	-	PD4	I/O	FT	PD4	USART2_RTS/SPI2_MOSI
86	-	-	A6	-	PD5	I/O	FT	PD5	USART2_TX
87	-	-	B6	-	PD6	I/O	FT	PD6	USART2_RX
88	-	-	A5	-	PD7	I/O	FT	PD7	USART2_CK/TIM9_CH2
89	55	A5	A8	39	PB3	I/O	FT	JTDO	TIM2_CH2 / PB3/TRACESWO SPI1_SCK/COMP2_INM/LCD_SEG7
90	56	A4	A7	40	PB4	I/O	FT	JNTRST	TIM3_CH1/ PB4/ SPI1_MISO/COMP2_INP/LCD_SEG8
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBAI/TIM3_CH2 /SPI1_MOSI/COMP2_INP/LCD_SEG9
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX/LCD_SEG8
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX/PVD_IN
94	60	B4	A4	44	BOOT0	I		BOOT0	
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL / LCD_SEG16/TIM10_CH1
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/LCD_COM3 / TIM11_CH1
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36 /TIM10_CH1

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or VFQFPN48					
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1
99	63	D4	D3	47	V_{SS_3}	S		V_{SS_3}	
100	64	E4	C4	48	V_{DD_3}	S		V_{DD_3}	

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 10*.
4. Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V_{DD}.
5. The pins number 5 and 6 in the LQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PH0 and PH1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32L15xxx reference manual (RM0038).
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 5. Alternate function input/output

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0															
NRST	NRST															
PA0-WKUP1	WKUP1	TIM2_CH1_ETR						USART2_CTS							TIMx_IC1	EVENTOUT
PA1		TIM2_CH2						USART2_RTS				[SEG0]			TIMx_IC2	EVENTOUT
PA2		TIM2_CH3		TIM9_CH1				USART2_TX				[SEG1]			TIMx_IC3	EVENTOUT
PA3		TIM2_CH4		TIM9_CH2				USART2_RX				[SEG2]			TIMx_IC4	EVENTOUT
PA4						SPI1_NSS		USART2_CK							TIMx_IC1	EVENTOUT
PA5		TIM2_CH1_ETR				SPI1_SCK									TIMx_IC2	EVENTOUT
PA6			TIM3_CH1	TIM10_CH1		SPI1_MISO						[SEG3]			TIMx_IC3	EVENTOUT
PA7			TIM3_CH2	TIM11_CH1		SPI1_MOSI						[SEG4]			TIMx_IC4	EVENTOUT
PA8	MCO							USART1_CK				[COM0]			TIMx_IC1	EVENTOUT
PA9								USART1_TX				[COM1]			TIMx_IC2	EVENTOUT
PA10								USART1_RX				[COM2]			TIMx_IC3	EVENTOUT
PA11						SPI1_MISO		USART1_CTS			DM				TIMx_IC4	EVENTOUT
PA12						SPI1_MOSI		USART1_RTS			DP				TIMx_IC1	EVENTOUT
PA13	JTMS-SWDAT														TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK														TIMx_IC3	EVENTOUT

Table 5. Alternate function input/output (continued)

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PA15	JTDI	TIM2_CH1_ETR				SPI1_NSS						SEG17			TIMx_IC4	EVENTOUT
PB0			TIM3_CH3									[SEG5]				EVENTOUT
PB1			TIM3_CH4									[SEG6]				EVENTOUT
PB2	BOOT1															EVENTOUT
PB3	JTDO	TIM2_CH2				SPI1_SCK						[SEG7]				EVENTOUT
PB4	JTRST		TIM3_CH1			SPI1_MISO						[SEG8]				EVENTOUT
PB5			TIM3_CH2		I2C1_SMBAI	SPI1_MOSI						[SEG9]				EVENTOUT
PB6			TIM4_CH1		I2C1_SCL			USART1_TX								EVENTOUT
PB7			TIM4_CH2		I2C1_SDA			USART1_RX								EVENTOUT
PB8			TIM4_CH3	TIM10_CH1*	I2C1_SCL							SEG16				EVENTOUT
PB9			TIM4_CH4	TIM11_CH1*	I2C1_SDA							[COM3]				EVENTOUT
PB10		TIM2_CH3			I2C2_SCL			USART3_TX				SEG10				EVENTOUT
PB11		TIM2_CH4			I2C2_SDA			USART3_RX				SEG11				EVENTOUT
PB12				TIM10_CH1	I2C2_SMBAI	SPI2_NSS		USART3_CK				SEG12				EVENTOUT
PB13				TIM9_CH1		SPI2_SCK		USART3_CTS				SEG13				EVENTOUT
PB14				TIM9_CH2		SPI2_MISO		USART3_RTS				SEG14				EVENTOUT
PB15	RTC 50/60 Hz			TIM11_CH1		SPI2_MOSI						SEG15				EVENTOUT
PC0												SEG18			TIMx_IC1	EVENTOUT

Table 5. Alternate function input/output (continued)

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PC1												SEG19			TIMx_IC2	EVENTOUT
PC2												SEG20			TIMx_IC3	EVENTOUT
PC3												SEG21			TIMx_IC4	EVENTOUT
PC4												SEG22			TIMx_IC1	EVENTOUT
PC5												SEG23			TIMx_IC2	EVENTOUT
PC6			TIM3_CH1									SEG24			TIMx_IC3	EVENTOUT
PC7			TIM3_CH2									SEG25			TIMx_IC4	EVENTOUT
PC8			TIM3_CH3									SEG26			TIMx_IC1	EVENTOUT
PC9			TIM3_CH4									SEG27			TIMx_IC2	EVENTOUT
PC10								USART3_TX				COM4 / SEG28 / SEG40			TIMx_IC3	EVENTOUT
PC11								USART3_RX				COM5 / SEG29 / SEG41			TIMx_IC4	EVENTOUT
PC12								USART3_CK				COM6 / SEG30 / SEG42			TIMx_IC1	EVENTOUT
PC13-RTC_AF1	RTC_AF1 / WKUP2														TIMx_IC2	EVENTOUT
PC14-OSC32_IN	OSC32_IN														TIMx_IC3	EVENTOUT
PC15-OSC32_OUT	OSC32_OUT														TIMx_IC4	EVENTOUT
PD0				TIM9_CH1		SPI2_NSS									TIMx_IC1	EVENTOUT
PD1						SPI2_SCK									TIMx_IC2	EVENTOUT

Table 5. Alternate function input/output (continued)

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PD2			TIM3_ETR									COM7 / SEG31 / SEG43			TIMx_IC3	EVENTOUT
PD3						SPI2_MISO		USART2_ CTS							TIMx_IC4	EVENTOUT
PD4						SPI2_MOSI		USART2_ RTS							TIMx_IC1	EVENTOUT
PD5								USART2_ TX							TIMx_IC2	EVENTOUT
PD6								USART2_ RX							TIMx_IC3	EVENTOUT
PD7				TIM9_CH2				USART2_ CK							TIMx_IC4	EVENTOUT
PD8								USART3_ TX				SEG28			TIMx_IC1	EVENTOUT
PD9								USART3_ RX				SEG29			TIMx_IC2	EVENTOUT
PD10								USART3_ CK				SEG30			TIMx_IC3	EVENTOUT
PD11								USART3_ CTS				SEG31			TIMx_IC4	EVENTOUT
PD12			TIM4_CH1					USART3_ RTS				SEG32			TIMx_IC1	EVENTOUT
PD13			TIM4_CH2									SEG33			TIMx_IC2	EVENTOUT
PD14			TIM4_CH3									SEG34			TIMx_IC3	EVENTOUT
PD15			TIM4_CH4									SEG35			TIMx_IC4	EVENTOUT
PE0			TIM4_ETR	TIM10_CH1								SEG36			TIMx_IC1	EVENTOUT
PE1				TIM11_CH1								SEG37			TIMx_IC2	EVENTOUT
PE2	TRACECK		TIM3_ETR									SEG 38			TIMx_IC3	EVENTOUT
PE3	TRACED0		TIM3_CH1									SEG 39			TIMx_IC4	EVENTOUT

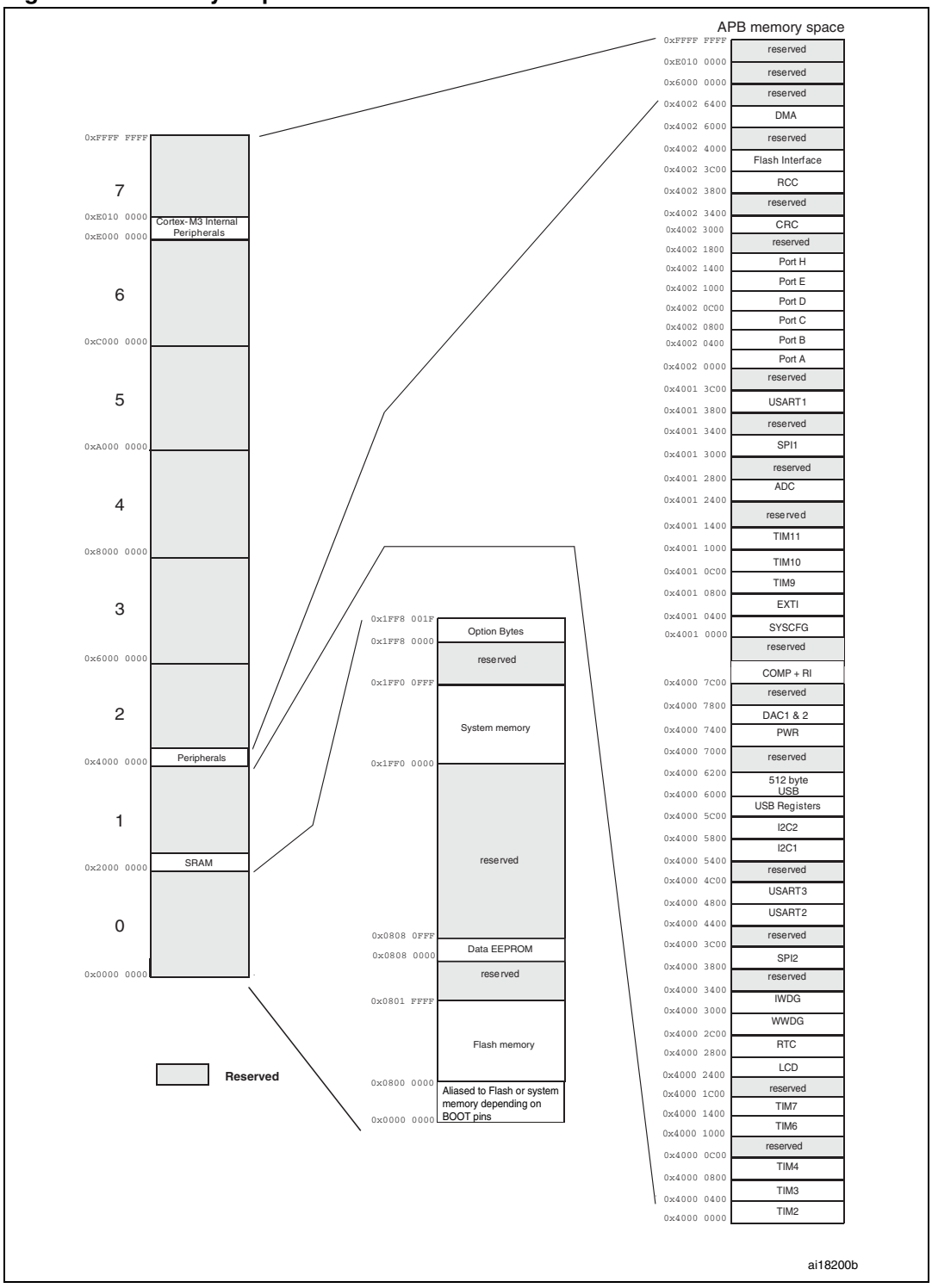
Table 5. Alternate function input/output (continued)

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PE4	TRACED1		TIM3_CH2												TIMx_IC1	EVENTOUT
PE5	TRACED2			TIM9_CH1*											TIMx_IC2	EVENTOUT
PE6	TRACED3 / WKUP3			TIM9_CH2*											TIMx_IC3	EVENTOUT
PE7															TIMx_IC4	EVENTOUT
PE8															TIMx_IC1	EVENTOUT
PE9		TIM2_CH1_ ETR													TIMx_IC2	EVENTOUT
PE10		TIM2_CH2													TIMx_IC3	EVENTOUT
PE11		TIM2_CH3													TIMx_IC4	EVENTOUT
PE12		TIM2_CH4				SPI1_NSS									TIMx_IC1	EVENTOUT
PE13						SPI1_SCK									TIMx_IC2	EVENTOUT
PE14						SPI1_MISO									TIMx_IC3	EVENTOUT
PE15						SPI1_MOSI									TIMx_IC4	EVENTOUT
PH0-OSC_IN	OSC_IN															
PH1-OSC_OUT	OSC_OUT															
PH2																EVENTOUT

5 Memory mapping

The memory map is shown in the following figure.

Figure 9. Memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.65 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

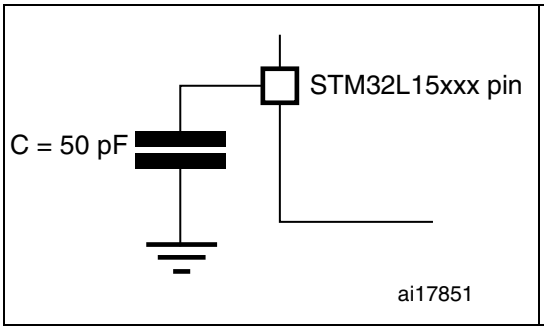
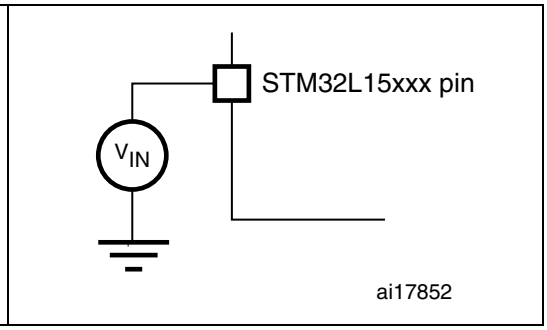
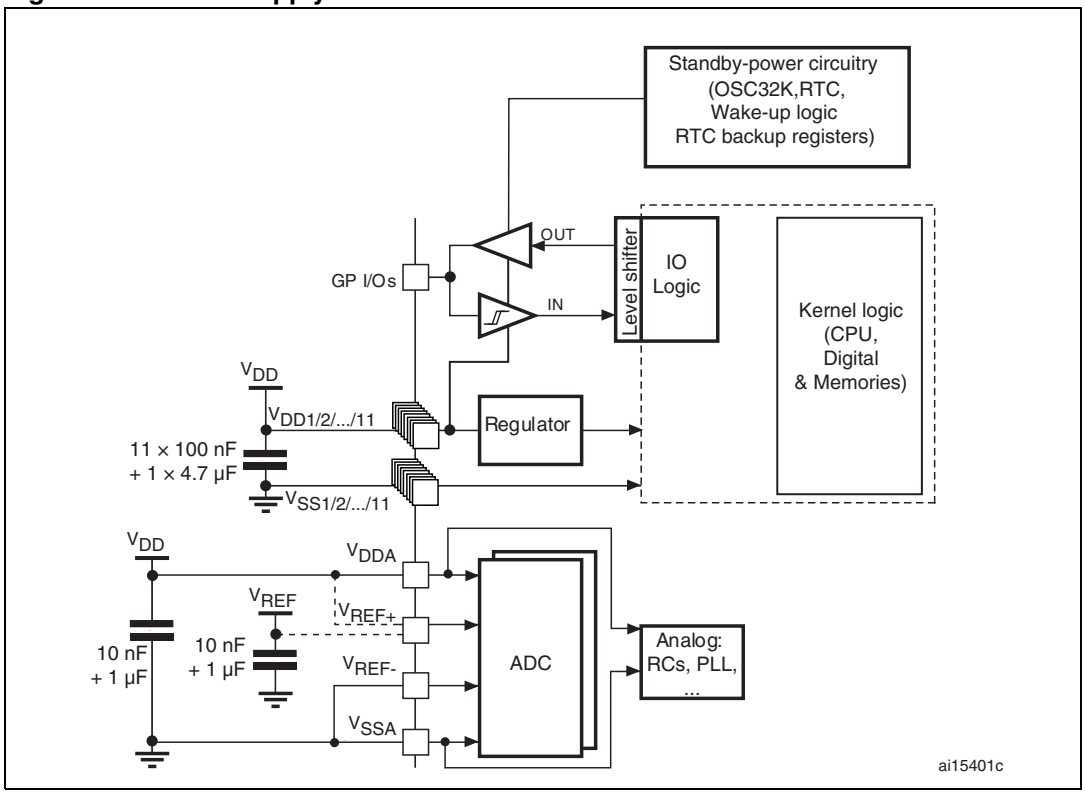


Figure 11. Pin input voltage



6.1.6 Power supply scheme

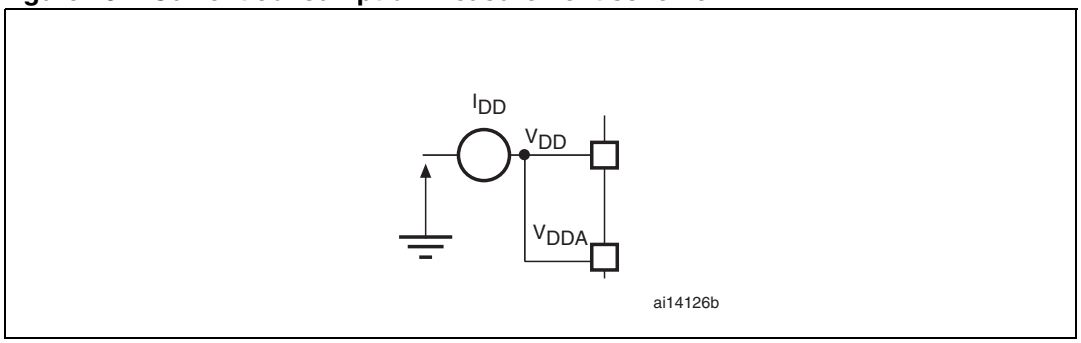
Figure 12. Power supply scheme



Caution: In this figure, the 4.7 µF capacitor must be connected to V_{DD2}.

6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin(3)	V_{SS} –0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.10*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Positive current injection is not possible on these I/Os. V_{IN} maximum must be respected. Negative current injection is possible and must not exceed $I_{INJ(PIN)}$.
3. $I_{INJ(PIN)}$ must never be exceeded (see *Table 7: Current characteristics*). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{IN}$max while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$I_{INJ(PIN)}$ (2)	Injected current on NRST pin(3)	± 5	
	Injected current on five-volt tolerant I/O(4)	+0 / -5	
	Injected current on any other pin (3)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.15*.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
4. Positive current injection is not possible on these I/Os. V_{IN} maximum must be respected. Negative current injection is possible and must not exceed $I_{INJ(PIN)}$.

5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	32	
f_{PCLK2}	Internal APB2 clock frequency		0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same voltage as V_{DD}(2)	1.65	3.6	V
	Analog operating voltage (ADC used)		1.8	3.6	
P_D	Power dissipation at T_A = 85 °C(3)	LQFP100		434	mW
		LQFP64		444	
		LQFP48		363	
		LFBGA108		TBD	
		TFBGA64		308	
		VFQFN48		TBD	
T_A	Temperature range	Maximum power dissipation	–40	85	°C
		Low power dissipation(4)	–40	105	
T_J	Junction temperature range	-40 °C ≤T_A ≤105 °C	–40	105	°C

1. When the ADC is used, refer to *Table 48: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 62: Thermal characteristics on page 101*).

4. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see *Table 62: Thermal characteristics on page 101*).

Table 10. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range				
Operating power supply range	**ADC operation**	**USB**	**V_{CORE}**	**Maximum CPU frequency (f_{CPU} max)**	**I/O operation**
V_{DD} = 1.65 to 1.8 V	Not functional	Not functional	Range 2 or range 3	16 MHz (1ws) 8MHz (0ws)	- Degraded speed performance - No I/O compensation
V_{DD} = 1.8 to 2.0 V	Conversion time up to 500 Ksps	Not functional	Range 2 or range 3	16 MHz (1ws) 8MHz (0ws)	- Degraded speed performance - No I/O compensation
V_{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional	Range 1, range 2 or range 3	32 MHz (1ws) 16MHz (0ws)	- Full-speed operation - I/O compensation works
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional	Range 1, range 2 or range 3	32 MHz (1ws) 16MHz (0ws)	- Full-speed operation - I/O compensation works

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

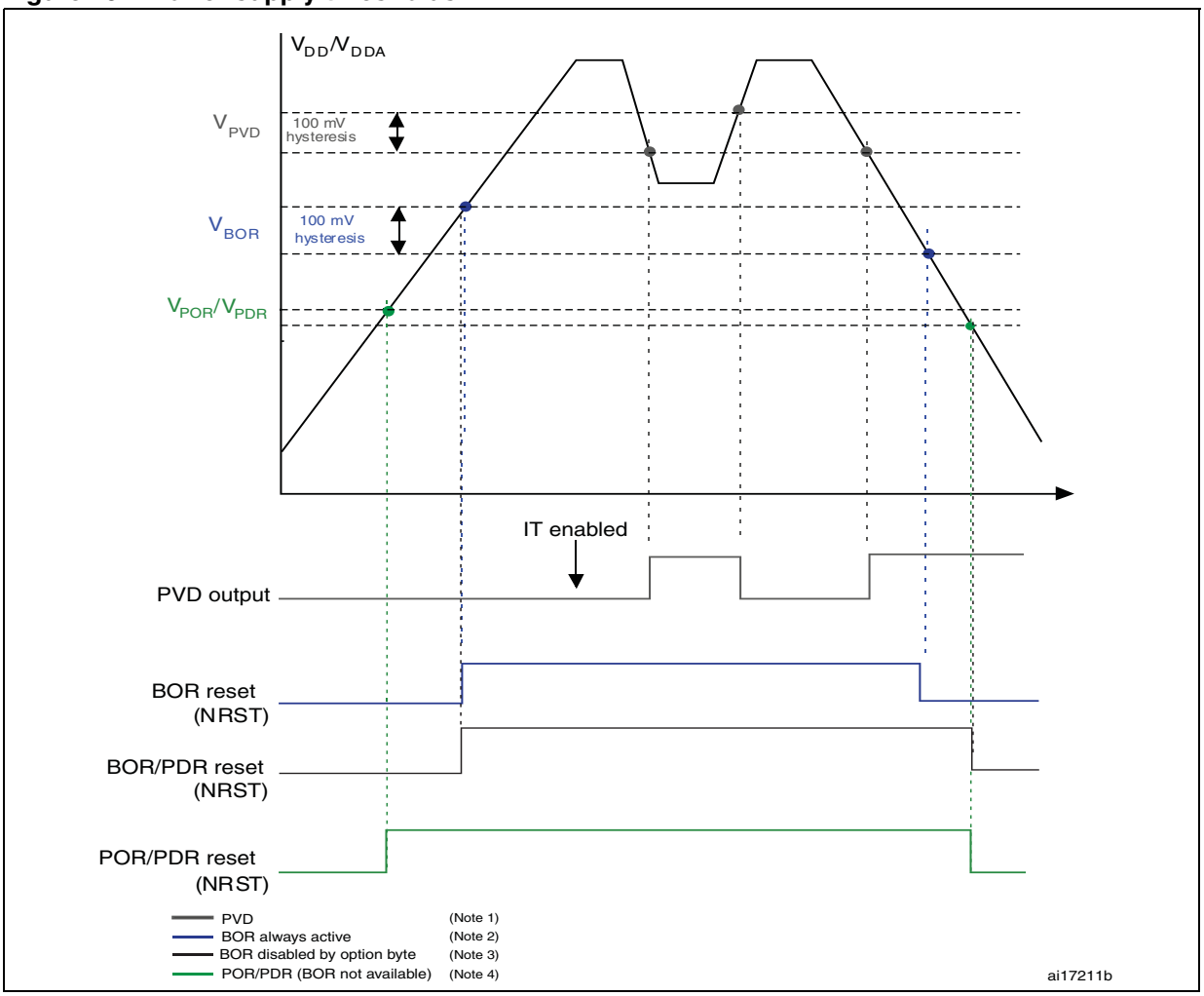
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)		∞	µs/V
		BOR detector disabled	TBD		TBD	
	V_{DD} fall time rate		0(1)		∞	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled		3.3	TBD	ms
		V_{DD} rising, BOR disabled		1.1	TBD	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	TBD	1.5	TBD	V
		Rising edge	TBD	1.5	TBD	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	TBD	1.7	TBD	
		Rising edge	TBD	1.76	TBD	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	TBD	1.93	TBD	
		Rising edge	TBD	2.03	TBD	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	TBD	2.30	TBD	
		Rising edge	TBD	2.41	TBD	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	TBD	2.55	TBD	
		Rising edge	TBD	2.66	TBD	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	TBD	2.8	TBD	
		Rising edge	TBD	2.9	TBD	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	TBD	1.85	TBD	
		Rising edge	TBD	1.94	TBD	
V_{PVD1}	PVD threshold 1	Falling edge	TBD	2.04	TBD	
		Rising edge	TBD	2.14	TBD	
V_{PVD2}	PVD threshold 2	Falling edge	TBD	2.24	TBD	
		Rising edge	TBD	2.34	TBD	
V_{PVD3}	PVD threshold 3	Falling edge	TBD	2.44	TBD	
		Rising edge	TBD	2.54	TBD	
V_{PVD4}	PVD threshold 4	Falling edge	TBD	2.64	TBD	
		Rising edge	TBD	2.74	TBD	
V_{PVD5}	PVD threshold 5	Falling edge	TBD	2.83	TBD	
		Rising edge	TBD	2.94	TBD	
V_{PVD6}	PVD threshold 6	Falling edge	TBD	3.05	TBD	
		Rising edge	TBD	3.15	TBD	

Table 11. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hyst}	Hysteresis voltage	BOR0 threshold		40		mV
		All BOR and PVD thresholds excepting BOR0		100		

1. Guaranteed by design, not tested in production.

Figure 10. Power supply thresholds



1. The PVD is available on all STM32L devices and it is enabled or disabled by software.
2. The BOR is available only on devices operating from 1.8 to 3.6 V, and unless disabled by option byte it will mask the POR/PDR threshold.
3. When the BOR is disabled by option byte, the reset is asserted when VDD goes below PDR level
4. For devices operating from 1.65 to 3.6 V, there is no BOR and the reset is released when VDD goes above POR level and asserted when VDD goes below PDR level

6.3.3 Embedded internal reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$	Internal reference voltage	–40 °C < T_J < +105 °C	TBD	1.224	TBD	V
I_{REFINT}	Internal reference current consumption			1.4	TBD	µA
$T_{VREFINT}$	Internal reference startup time			2	TBD	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	Built-in ADC	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values			±5	mV
V_{REFINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV			10	mV
T_{Coeff}(2)	Temperature coefficient			20	50	ppm/°C
A_{Coeff}(2)	Long-term stability	1000 hours, T= 25 °C			TBD	ppm
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5	10(2)	µs
T_{ADC_BUF}	Startup time of reference voltage buffer for ADC				TBD	µs
I_{BUF_ADC}	Consumption of reference voltage buffer for ADC			13.5	TBD	µA
I_{VREF_OUT}	VREF_OUT output current(3)				1	µA
C_{VREF_OUT}	VREF_OUT output load				50	pF
I_{LPBUF}	Consumption of reference voltage buffer for VREF_OUT and COMP			730	TBD	nA
V_{REFINT_DIV1}	1/4 reference voltage			25		% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage			50		
V_{REFINT_DIV3}	3/4 reference voltage			75		

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.
3. To guaranty less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- V_{DD} = 3.6V
- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted depending on f_{HCLK} frequency and voltage range
- Prefetch and 64-bit access are enabled in configurations with 1 wait state

The parameters given in *Table 13*, *Table 9* and *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 13. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	HSE = 16 MHz(2) (PLL ON for f_{HCLK} above 16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	234	TBD	TBD	TBD	µA
				2 MHz	427	TBD	TBD	TBD	
				4 MHz	813	TBD	TBD	TBD	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.97	TBD	TBD	TBD	mA
				8 MHz	1.87	TBD	TBD	TBD	
				16 MHz	3.8	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.16	TBD	TBD	TBD	
				16 MHz	4.57	TBD	TBD	TBD	
				32 MHz	9.5	TBD	TBD	TBD	
		HSI clock source (16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	4 MHz	TBD	TBD	TBD	TBD	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	TBD	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	TBD	TBD	TBD	TBD	
		MSI clock, 64 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	64 kHz	TBD	TBD	TBD	TBD	
		MSI clock, 512 kHz		512 kHz	TBD	TBD	TBD	TBD	
		MSI clock, 4 MHz		4 MHz	TBD	TBD	TBD	TBD	

1. Based on characterization, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 14. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	HSE = 16 MHz(2) (PLL ON for f_{HCLK} above 16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	204	TBD	TBD	TBD	µA
				2 MHz	380	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.9	TBD	TBD	TBD	mA
				8 MHz	1.73	TBD	TBD	TBD	
				16 MHz	3.5	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.01	TBD	TBD	TBD	
				16 MHz	4.21	TBD	TBD	TBD	
				32 MHz	8.68	TBD	TBD	TBD	
		HSI clock source (16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	4 MHz	TBD	TBD	TBD	TBD	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	TBD	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	TBD	TBD	TBD	TBD	
		MSI clock, 64 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	64 kHz	TBD	TBD	TBD	TBD	
		MSI clock, 512 kHz		512 kHz	TBD	TBD	TBD	TBD	
		MSI clock, 4 MHz		4 MHz	TBD	TBD	TBD	TBD	

1. Based on characterization, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
3. Data guaranteed, each individual device tested in production

Table 15. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	HSE = 16 MHz(2) (PLL ON for f_{HCLK} >16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	TBD	TBD	TBD	TBD	µA
				2 MHz	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	
		HSI clock source (16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	4 MHz	TBD	TBD	TBD	TBD	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	TBD	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	TBD	TBD	TBD	TBD	
		MSI clock, 64 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	64 kHz	TBD	TBD	TBD	TBD	
		MSI clock, 512 kHz		512 kHz	TBD	TBD	TBD	TBD	
		MSI clock, 4 MHz		4 MHz	TBD	TBD	TBD	TBD	
	Supply current in Sleep mode, code executed from Flash	HSE = 16 MHz(2) (PLL ON for f_{HCLK} above 16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	
				4 MHz	330	TBD	TBD	TBD	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	TBD	TBD	TBD	TBD	mA
				8 MHz	TBD	TBD	TBD	TBD	
				16 MHz	1.1	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	TBD	TBD	TBD	TBD	
				16 MHz	1.39	TBD	TBD	TBD	
				32 MHz	2.61	TBD	TBD	TBD	
		HSI clock source (16 MHz)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	4 MHz	TBD	TBD	TBD	TBD	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	1	TBD	TBD	TBD	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	2.16	TBD	TBD	TBD	

Table 15. Current consumption in Sleep mode (continued)

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)			Unit
						55 °C	85 °C	105 °C	
I_{DD} (Sleep)	Supply current in Sleep mode, code executed from Flash	MSI clock, 64 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	64 kHz	19	TBD	TBD	TBD	µA
		MSI clock, 512 kHz		512 kHz	36	TBD	TBD	TBD	
		MSI clock, 4 MHz		4 MHz	179	TBD	TBD	TBD	

1. Based on characterization, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
3. Data guaranteed, each individual device tested in production

Table 16. Current consumption in Low power run mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
$I_{DD\ (LP\ Run)}$	Supply current in Low power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 64 kHz f_{HCLK} = 32 kHz	T_A = 25°C	10.5		µA
			MSI clock, 64 kHz f_{HCLK} = 64 kHz	T_A = 25°C	15.8		
			MSI clock, 128 kHz f_{HCLK} = 128 kHz	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 64 kHz f_{HCLK} = 32 kHz	T_A = 25 °C	TBD		
			MSI clock, 64 kHz f_{HCLK} = 64 kHz	T_A = 25 °C	TBD		
			MSI clock, 128 kHz f_{HCLK} = 128 kHz	T_A = -40 °C to 25 °C	TBD	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
I_{DD} Max (LP Run)	Max current in Low power run mode	V_{DD} from 1.65 V to 3.6 V			TBD	TBD	

1. Based on characterization, not tested in production, unless otherwise specified.

Table 17. Current consumption in Low power sleep mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
$I_{DD\ (LP\ Sleep)}$	Supply current in Low power sleep mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 64 kHz f_{HCLK} = 32 kHz	T_A = 25 °C	4.07		µA
			MSI clock, 64 kHz f_{HCLK} = 64 kHz	T_A = 25 °C	4.55		
			MSI clock, 128 kHz f_{HCLK} = 128 kHz	T_A = -40 °C to 25 °C	7.69	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
		TIM9 and USART1 enabled, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 64 kHz f_{HCLK} = 32 kHz	T_A = 25 °C	4.85		
			MSI clock, 64 kHz f_{HCLK} = 64 kHz	T_A = 25 °C	5.66		
			MSI clock, 128 kHz f_{HCLK} = 128 kHz	T_A = -40 °C to 25 °C	9.85	TBD	
				T_A = 55 °C	TBD	TBD	
				T_A = 85 °C	TBD	TBD	
				T_A = 105 °C	TBD	TBD	
I_{DD} Max (LP Run)	Max current in Low power run mode	V_{DD} from 1.65 V to 3.6 V			TBD	TBD	

1. Based on characterization, not tested in production, unless otherwise specified.

Table 18. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions			Typ(1)	Max	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C	1.3		µA
				T_A = 55°C	TBD		
				T_A= 85°C	TBD		
				T_A = 105°C	TBD		
			LCD ON (static duty)(2)	T_A = -40°C to 25°C	3.3		
				T_A = 55°C	TBD		
				T_A= 85°C	TBD		
				T_A = 105°C	TBD		
			LCD ON (1/8 duty)(3)	T_A = -40°C to 25°C	7.6		
				T_A = 55°C	TBD		
				T_A= 85°C	TBD		
				T_A = 105°C	TBD		
		RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C	1.6	TBD	
				T_A = 55°C	TBD	TBD	
				T_A= 85°C	TBD	TBD	
				T_A = 105°C	TBD	TBD	
			LCD ON (static duty)(2)	T_A = -40°C to 25°C	3.6	TBD	
				T_A = 55°C	TBD	TBD	
				T_A= 85°C	TBD	TBD	
				T_A = 105°C	TBD	TBD	
			LCD ON (1/8 duty)(3)	T_A = -40°C to 25°C	7.6	TBD	
				T_A = 55°C	TBD	TBD	
				T_A= 85°C	TBD	TBD	
				T_A = 105°C	TBD	TBD	
I_{DD} (Stop)	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled		T_A = -40°C to 25°C	1.1		
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)		T_A = -40°C to 25°C	0.5	TBD	
				T_A = 55°C	TBD	TBD	
				T_A= 85°C	TBD	TBD	
				T_A = 105°C	TBD	TBD	
I_{DD} (WU from Stop)	Supply current during wake-up from Stop mode	MSI = 4 MHz		T_A = -40°C to 25°C	TBD		
		MSI = 1 MHz			TBD		
		MSI = 64 kHz			TBD		

1. Typical values are measured at T_A = 25 °C.

2. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected
3. LCD enabled with external VLCD, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.

Table 19. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ(1)	Max	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C	1.1		µA
			T_A = 55 °C	TBD		
			T_A= 85 °C	TBD		
			T_A = 105 °C	TBD		
		RTC clocked by LSE (no independent watchdog)	T_A = -40 °C to 25 °C	1.3	TBD	
			T_A = 55 °C	TBD	TBD	
			T_A= 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	
I_{DD} (Standby)	Supply current in Standby mode (RTC disabled)	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1		µA
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.3	TBD	
			T_A = 55 °C	TBD	TBD	
			T_A = 85 °C	TBD	TBD	
			T_A = 105 °C	TBD	TBD	
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode		T_A = -40 °C to 25 °C	TBD		

1. Typical values are measured at T_A = 25 °C.

Wakeup time from low-power mode

The wakeup times given in the following table are measured on a wakeup phase with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Deep sleep mode
- Standby mode: the clock source is the MSI oscillator running at 2 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 20. Typical and maximum timings in Low power modes

Symbol	Parameter	Conditions	Typ(1)	Max	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.35		µs
$t_{WUSLEEP\_LP}$(2)	Wakeup from Low power sleep mode f_{HCLK} = 128 kHz	f_{HCLK} = 128 kHz Flash enabled	TBD		
		f_{HCLK} = 128 kHz Flash switched OFF	TBD		
t_{WUSTOP}(1)	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{HSI}$ = 16 MHz	TBD		
	Wakeup from Stop mode, regulator in low power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1 and 2	7.9	TBD	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	7.9	TBD	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	10.2	TBD	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	TBD	TBD	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	TBD	TBD	
		f_{HCLK} = MSI = 64 kHz	TBD	TBD	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	f_{HCLK} = MSI = 2.1 MHz	57	TBD	

1. Typical values are measured at T_A = 25 °C.
2. Wakeup time until start of interrupt vector fetch. The first word of interrupt routine is fetched n CPU cycles after t_{WU}.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6: Voltage characteristics*.

Table 21. Peripheral current consumption(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low power sleep and run	
APB1	TIM2	TBD	TBD	TBD	TBD	µA/MHz
	TIM3	TBD	TBD	TBD	TBD	
	TIM4	TBD	TBD	TBD	TBD	
	TIM6	TBD	TBD	TBD	TBD	
	TIM7	TBD	TBD	TBD	TBD	
	LCD	TBD	TBD	TBD	TBD	
	WWDG	TBD	TBD	TBD	TBD	
	SPI2	TBD	TBD	TBD	TBD	
	USART2	TBD	TBD	TBD	TBD	
	USART3	TBD	TBD	TBD	TBD	
	I2C1	TBD	TBD	TBD	TBD	
	I2C2	TBD	TBD	TBD	TBD	
	USB	TBD	TBD	TBD	TBD	
	PWR	TBD	TBD	TBD	TBD	
	DAC	TBD	TBD	TBD	TBD	
	COMP	TBD	TBD	TBD	TBD	
	USB	TBD	TBD	TBD	TBD	

Table 21. Peripheral current consumption(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low power sleep and run	
APB2	SYSCFG & RI	TBD	TBD	TBD	TBD	µA/MHz
	TIM9	TBD	TBD	TBD	TBD	
	TIM10	TBD	TBD	TBD	TBD	
	TIM11	TBD	TBD	TBD	TBD	
	ADC1	TBD	TBD	TBD	TBD	
	SPI1	TBD	TBD	TBD	TBD	
	USART1	TBD	TBD	TBD	TBD	
AHB	GPIOA	TBD	TBD	TBD	TBD	
	GPIOB	TBD	TBD	TBD	TBD	
	GPIOC	TBD	TBD	TBD	TBD	
	GPIOD	TBD	TBD	TBD	TBD	
	GPIOE	TBD	TBD	TBD	TBD	
	GPIOF	TBD	TBD	TBD	TBD	
	CRC	TBD	TBD	TBD	TBD	
	FLASH	TBD	TBD	TBD	TBD	
	DMA1	TBD	TBD	TBD	TBD	
All enabled		TBD	TBD	TBD	TBD	
$I_{DD\ (RTC)}$		TBD				µA
$I_{DD\ (LCD)}$		TBD				
$I_{DD\ (ADC)}$(2)		TBD				
$I_{DD\ (DAC)}$(3)		TBD				
$I_{DD\ (COMP1)}$		TBD				
$I_{DD\ (COMP2)}$	Slow mode	TBD				
	Fast mode	TBD				
$I_{DD\ (PVD\ /\ BOR)}$(4)		TBD				
$I_{DD\ (IWDG}$		TBD				

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion

3. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}/2$. DAC output is left floating.
4. Including supply current of internal reference voltage.

6.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 22* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 22. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		TBD			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				TBD	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			2.6		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			TBD	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 23. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)		1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		TBD			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				TBD	
$C_{IN(LSE)}$	OSC32_IN input capacitance(1)			0.6		pF
$DuCy_{(LSE)}$	Duty cycle		TBD		TBD	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			TBD	µA

1. Guaranteed by design, not tested in production.

Figure 14. High-speed external clock source AC timing diagram

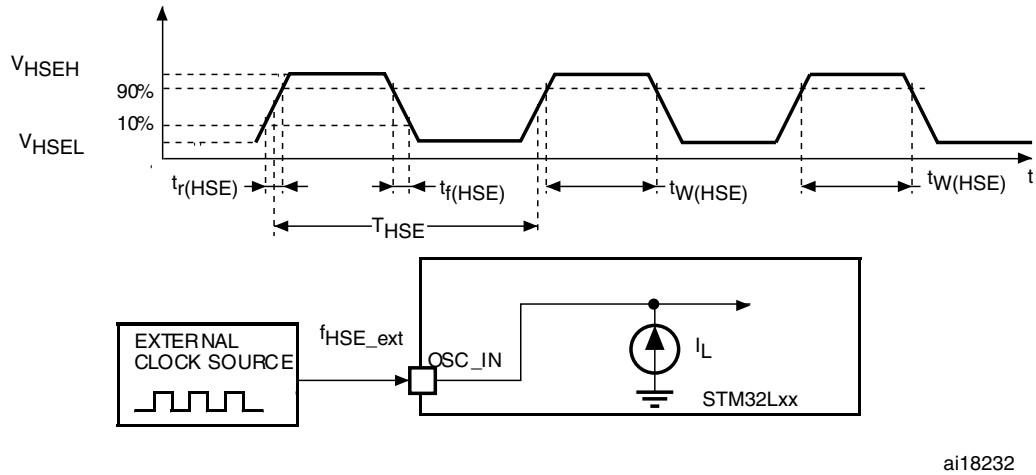
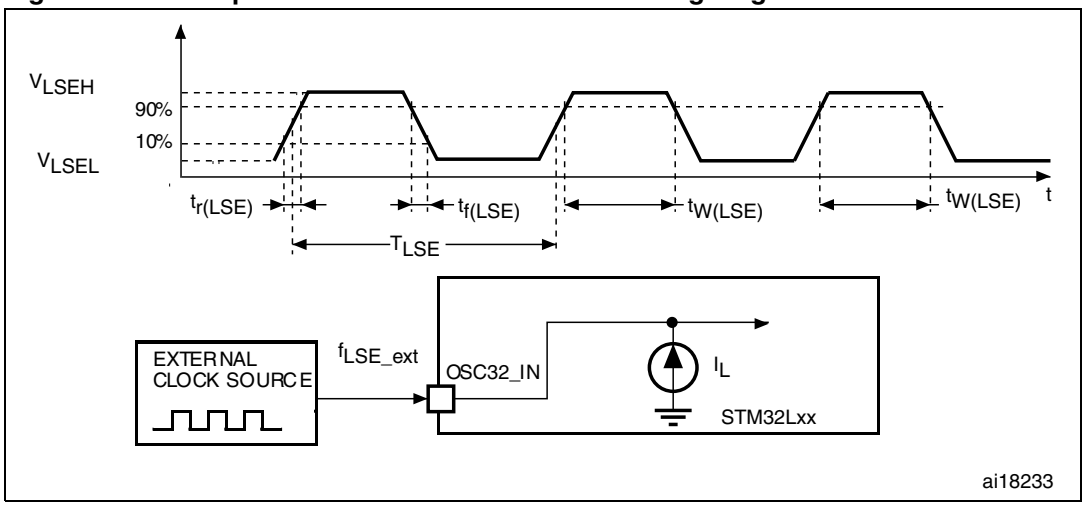


Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 24*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. HSE 1-24 MHz oscillator characteristics(1)(2)

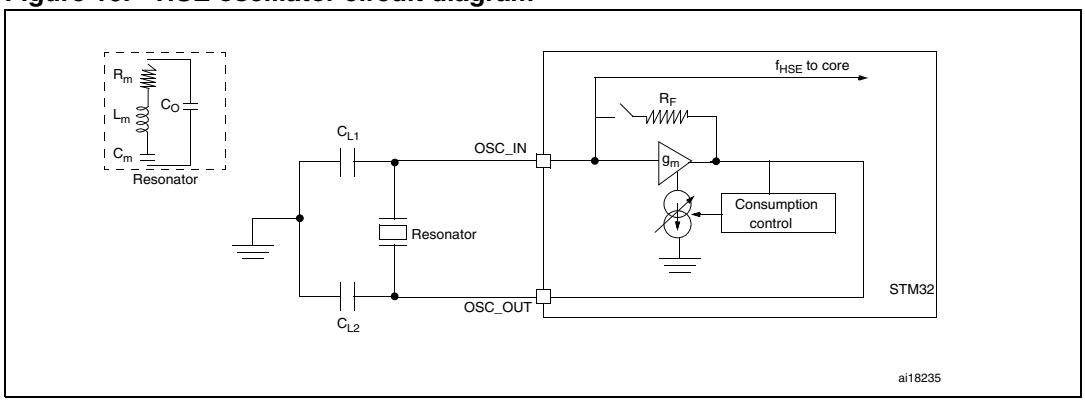
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		1		24	MHz
R_F	Feedback resistor			200		kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω		20		pF
i_2	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load			TBD	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz			TBD (startup) TBD (stabilized)(4)	mA
		C = 10 pF f_{OSC} = 16 MHz			TBD (startup) TBD (stabilized)	
g_m	Oscillator transconductance	Startup	3.5			mA /V
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stabilized		1		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.

3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. Data based on characterization. Not tested in production.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 16. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 25*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 25. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency			32.768		kHz
R_F	Feedback resistor			TBD		MΩ
C(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ			TBD	pF

Table 25. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1) (continued)

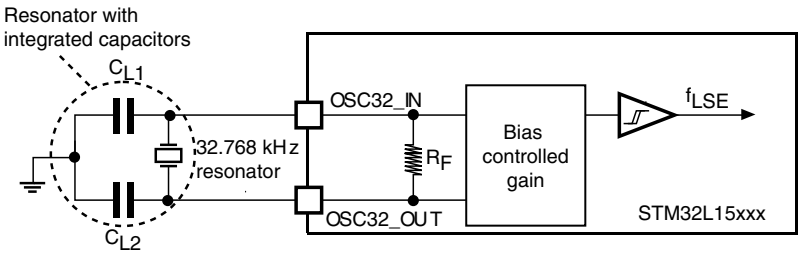
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}			TBD	µA
$I_{DD\ (LSE)}$	LSE oscillator current consumption	V_{DD} = 1.8 V		TBD		µA
		V_{DD} = 2.4 V		TBD		
		V_{DD} = 3.0 V		TBD		
		V_{DD} = 3.6V		TBD		
g_m	Oscillator transconductance		5			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized		TBD		s

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details;
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 17). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 17. Typical application with a 32.768 kHz crystal



6.3.6 Internal clock source characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 26. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V			16		MHz
TRIM	HSI user-trimmed resolution	-40 °C ≤T_A ≤105 °C			± 0.4	TBD	%
ACC_{HSI}	Accuracy of the HSI oscillator	Factory-calibrated(2)	T_A = - 40 to 105 °C	TBD	±1	TBD	%
			T_A = -10 to 85 °C	TBD	±1	TBD	%
			T_A = 0 to 70 °C	TBD	±1	TBD	%
			T_A = 25 °C	TBD	±1	TBD	%
$t_{SU(HSI)}$(2)	HSI oscillator startup time				3.7	TBD	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption				100	TBD	µA

1. 1.65 ≤V_{DD} ≤3.6 V, T_A = -40 to 105 °C unless otherwise specified
2. Based on characterization, not tested in production

Low-speed internal (LSI) RC oscillator

Table 27. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	LSI frequency	TBD	38	TBD	kHz
D_{LSI}	LSI oscillator frequency drift(3) 0°C ≤T_A ≤85°C	TDB		TDB	%
$t_{su(LSI)}$(4)	LSI oscillator startup time			200(5)	µs
$I_{DD(LSI)}$(4)	LSI oscillator power consumption		TBD	TBD	µA

1. V_{DD} = 3 V, T_A = -40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. This is a deviation for an individual part, once the initial frequency has been measured.
4. Guaranteed by design, not tested in production.
5. Guaranteed by design, not tested in production.

Multi-speed internal (MSI) RC oscillator

Table 28. MSI oscillator characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	TBD	65.5	TBD	kHz
		MSI range 1	TBD	131	TBD	
		MSI range 2	TBD	262	TBD	
		MSI range 3	TBD	524	TBD	
		MSI range 4	TBD	1.05	TBD	MHz
		MSI range 5	TBD	2.1	TBD	
		MSI range 6	TBD	4.2	TBD	
$D_{TEMP(MSI)}$	MSI oscillator frequency drift(2) 0 °C ≤T_A ≤85 °C			TBD		%
$D_{VOLT(MSI)}$	MSI oscillator frequency drift(3) 1.65 V ≤V_{DD} ≤3.6 V			TBD	TBD	%/V
$I_{DD(MSI)}$(4)	MSI oscillator power consumption	MSI range 0		TBD		µA
		MSI range 1		TBD		
		MSI range 2		TBD		
		MSI range 3		TBD		
		MSI range 4		TBD		
		MSI range 5		TBD		
		MSI range 6		TBD		

Table 28. MSI oscillator characteristics (1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0		TBD		µs
		MSI range 1		TBD		
		MSI range 2		TBD		
		MSI range 3		TBD		
		MSI range 4		TBD		
		MSI range 5		TBD		
		MSI range 6, Voltage range 1 and 2		TBD		
		MSI range 6, Voltage range 3		TBD		
$t_{STAB(MSI)}$	MSI oscillator stabilization time	MSI range 0			TBD	
		MSI range 1			TBD	
		MSI range 2			TBD	
		MSI range 3			TBD	
		MSI range 4			TBD	
		MSI range 5			TBD	
		MSI range 6, Voltage range 1 and 2			TBD	
		MSI range 3, Voltage range 3			TBD	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	MSI range 0 to range 5			TBD	f_{MSI}
		MSI range 0 to range 5 Voltage range 1 and 2			TBD	
		MSI range 0 to range 5 Voltage range 3			TBD	

1. $1.65 \leq V_{DD} \leq 3.6$ V, T_A = -40 to 105 °C unless otherwise specified.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. This is a deviation for an individual part, once the initial frequency has been measured.
4. Based on characterization, not tested in production.

6.3.7 PLL characteristics

The parameters given in *Table 29* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 29. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2		24	MHz
	PLL input clock duty cycle	TBD		TBD	%
f_{PLL_OUT}	PLL multiplier output clock	2		32	MHz
t_{LOCK}	PLL lock time			TBD	µs
Jitter	Cycle-to-cycle jitter			TBD	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}		TBD	TBD	µA
I_{DD}(PLL)	Current consumption on V_{DD}		TBD	TBD	

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.8 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 30. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.4			V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 31. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase		1.65		3.6	V
t_{prog}	Programming time for word or half-page	Erase word/half page			TBD	ms
		Programmed word/half page			TBD	
I_{DD}	Supply current during programming / erasing	T_A = 25 °C, V_{DD} = 3.0 V		TBD		mA
		T_A = 25 °C, V_{DD} = 1.8 V		TBD		mA

1. Guaranteed by design, not tested in production.

Table 32. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{CYC}	Erase / write cycles (program memory)	See notes(2)	TBD			kcycles
	Erase / write cycles (data memory)	See notes(3)	TBD			
t_{RET}	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +55 °C	TBD			Years
	Data retention (data memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +55 °C	TBD			
	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	TBD			

1. Based on characterization not tested in production.
2. Retention guaranteed after cycling is 10 years @ 55*°C
3. Retention guaranteed after cycling is 1 year @ 55*°C

6.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 33*. They are based on the EMS levels and classes defined in application note AN1709.

Table 33. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	TBD
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	TBD

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 34. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. voltage range			Unit
				4 MHz	16 MHz	32 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	TBD	TBD	TBD	dBµV
			30 to 130 MHz	TBD	TBD	TBD	
			130 MHz to 1GHz	TBD	TBD	TBD	
			SAE EMI Level	TBD	TBD	TBD	-

6.3.10 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 35. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	TBD	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 36. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	TBD

6.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 37. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports 2.7 V ≤V_{DD}≤3.6 V	V_{SS} - 0.3		0.8	V
V_{IH}	Standard I/O input high level voltage		2		V_{DD}+0.3	
	FT(1) I/O input high level voltage		2		5.5V	
V_{IL}	Input low level voltage	CMOS ports 1.65 V ≤V_{DD}≤ 3.6 V	–0.3		0.3 V_{DD}	
V_{IH}	Standard I/O Input high level voltage		0.7 V_{DD}(2)		V_{DD}+0.3	
	FT(3) I/O input high level voltage	CMOS ports 1.65 V ≤V_{DD}≤ 2.0 V			5.25	
		CMOS ports 2.0 V≤V_{DD}≤ 3.6 V			5.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(4)		10% V_{DD}(5)			
I_{lkg}	Input leakage current (6)	V_{SS} ≤V_{IN} ≤V_{DD} Standard I/Os			±50	nA

Table 37. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	TBD	45	TBD	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	TBD	45	TBD	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = 5V tolerant. To sustain a voltage higher than V_{DD} +0.5 the internal pull-up/pull-down resistors must be disabled.
2. $0.7V_{DD}$ for 5V-tolerant receiver
3. FT = Five-volt tolerant.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 200 mV. Based on characterization, not tested in production.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 38*.

in the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 38* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 38. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} =+ 4mA 1.65 V < V_{DD} < 2.7 V		0.45	
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.45		
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 4 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V		1.3	
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		V_{DD}-1.3		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 18* and *Table 39*, respectively.

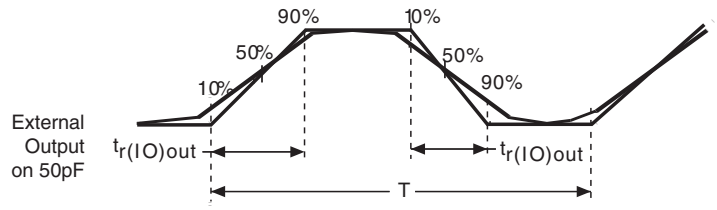
Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 39. I/O AC characteristics(1)

OSPEEDRx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		625(3)	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		125(3)	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
10	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		25(3)	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V		TBD(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		TBD		

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32L15xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 18*.
3. Guaranteed by design, not tested in production.

Figure 18. I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$) 2/3)T and if the duty cycle is (45-55%)
when loaded by 50 pF

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6.3.12 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 37*).

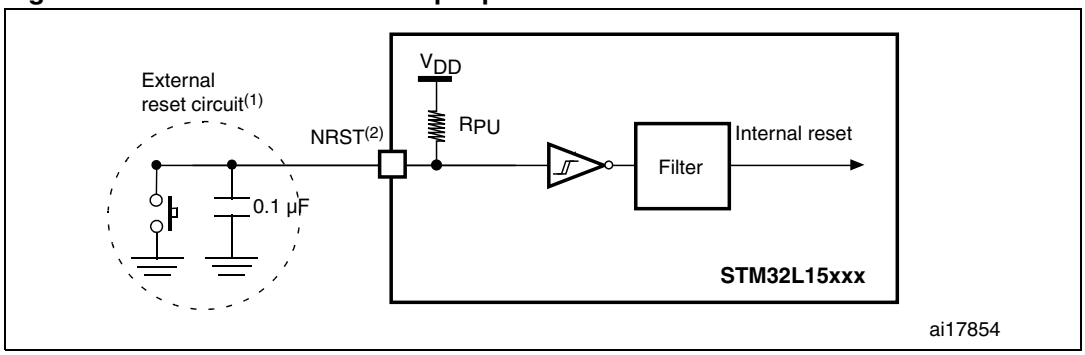
Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 40. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage		V_{SS}		0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage		1.4		V_{DD}	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V			0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V				
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		10%V_{DD}(2)			mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	TBD	45	TBD	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse				50	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse		350			ns

1. Guaranteed by design, not tested in production.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 40*. Otherwise the reset will not be taken into account by the device.

6.3.13 TIM timer characteristics

The parameters given in the following table are guaranteed by design.

Refer to *Section 6.3.11: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 41. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	36	MHz
Res_{TIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz		134.2	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

6.3.14 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

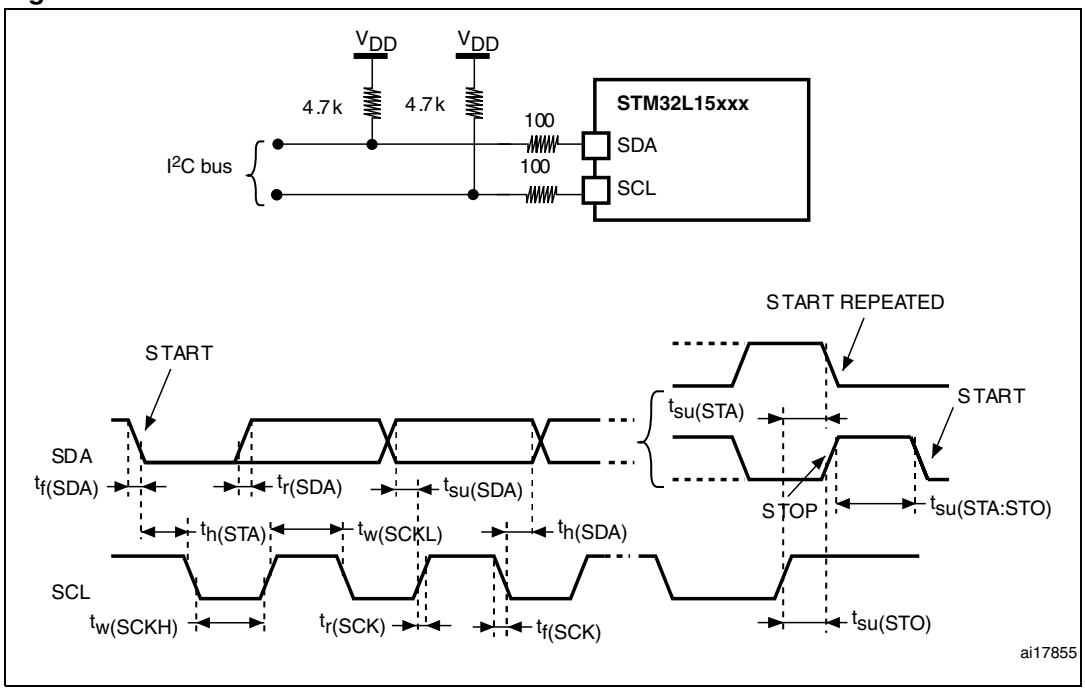
The I^2C characteristics are described in *Table 42*. Refer also to *Section 6.3.11: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 42. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve standard mode I²C frequencies. It must be higher than 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 20. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 43. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 6.3.11: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 44. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		16	MHz
		Slave mode		16	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		TBD	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	$2t_{PCLK}$		
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{PCLK} = 16 MHz, presc = 4	TBD	TBD	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$(2)	Data input hold time	Master mode	5		
$t_{h(SI)}$(2)		Slave mode	4		
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	TBD	TBD	
$t_{v(SO)}$(2)(1)	Data output valid time	Slave mode (after enable edge)		TBD	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		TBD	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	TBD		
$t_{h(MO)}$(2)		Master mode (after enable edge)	TBD		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

Figure 21. SPI timing diagram - slave mode and CPHA = 0

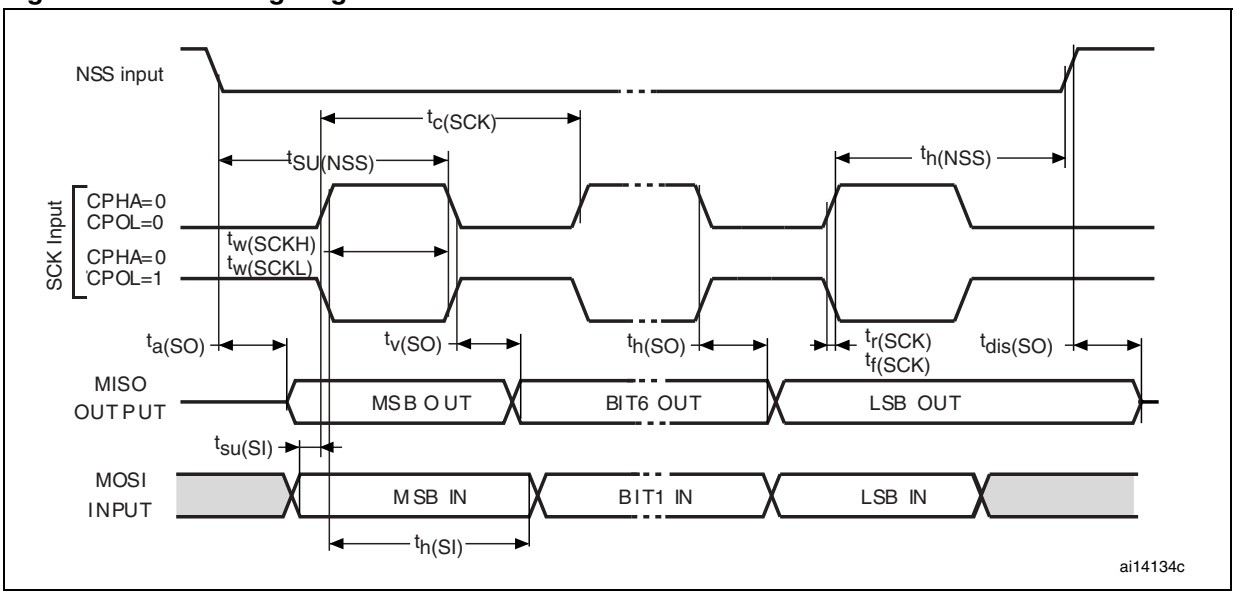
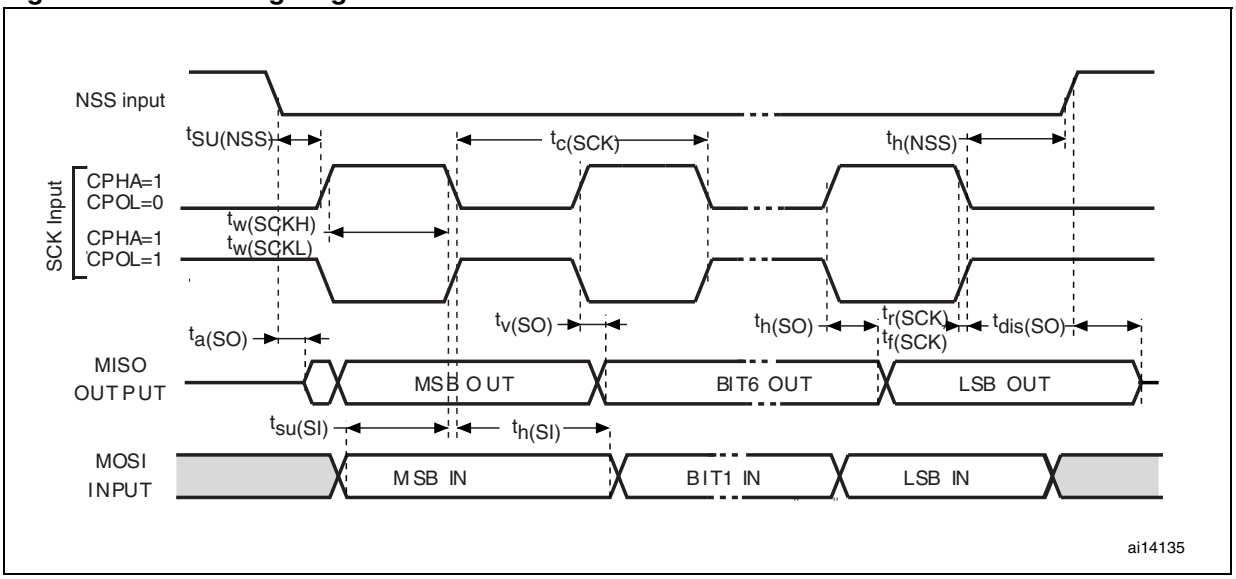
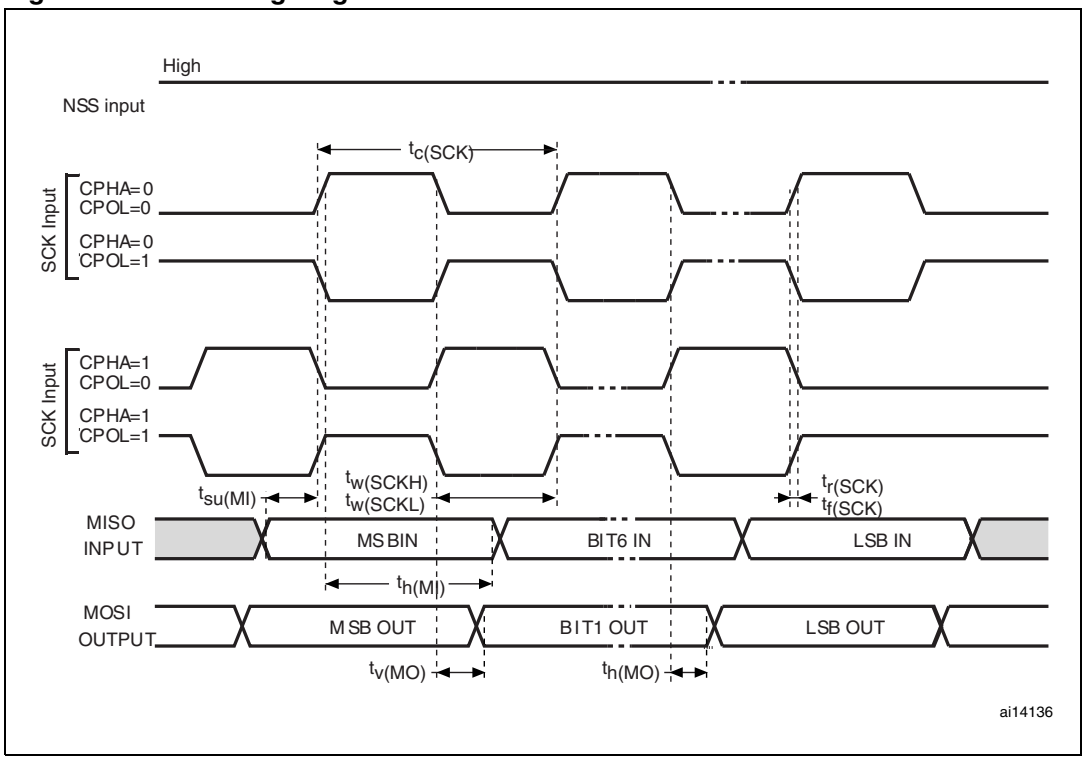


Figure 22. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 23. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 45. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 46. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)		0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32L15xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by characterization, not tested in production.
5. R_L is the load connected on the USB drivers.

Figure 24. USB timings: definition of data signal rise and fall time

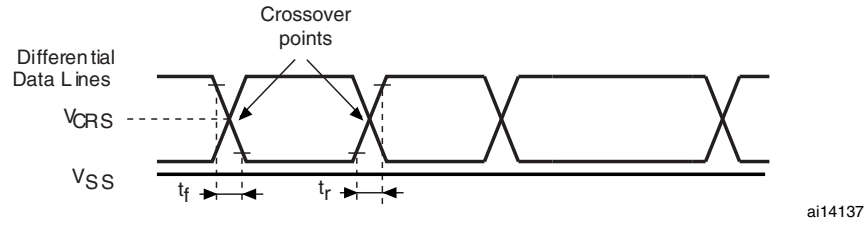


Table 47. USB: full-speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Table 48. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		1.8		3.6	V
V_{REF+}	Positive reference voltage	2.4 V ≤V_{DDA} ≤3.6 V	2.4		V_{DDA}	V
		1.8 V ≤V_{DDA} ≤2.4 V		V_{DDA}		
V_{REF-}	Negative reference voltage			V_{SSA}		
I_{VDDA}	Current on the V_{DDA} input pin			1000		µA
I_{VREF}	Current on the V_{REF} input pin			400(1)	TBD	
V_{AIN}	Conversion voltage range(2)		0(3)		V_{REF+}	V
f_{ADC}	ADC clock frequency	2.4 V ≤V_{DDA} ≤3.6V	0.320		16	MHz
		1.8 V ≤V_{DDA} ≤2.4V Voltage range 1 & 2	0.320		8	
		1.8 V ≤V_{DDA} ≤2.4V Voltage range 3	0.320		4	
f_S(4)	Sampling rate	Direct channels	0.02		1	Msps
		Multiplexed channels	0.02		TBD	
t_S	Sampling time	f_{ADC} = 16 MHz	0.107		17.1	µs
			4		384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1		24.75	µs
			4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
R_{ADC}	Sampling switch resistance	Direct channels			TBD	kΩ
		Multiplexed channels			TBD	
C_{ADC}	Internal sample and hold capacitor	Direct channels			TBD	pF
		Multiplexed channels			TBD	
f_{TRIG}	External trigger frequency	f_{ADC} = 16 MHz			TBD	kHz
					TBD	$1/f_{ADC}$
R_{AIN}(5)	External input impedance				TBD	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz			TBD	µs
					TBD	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz			TBD	µs
					TBD	$1/f_{ADC}$
t_{STAB}	Power-up time				3.5	µs

1. Based on characterization results, not tested in production.
2. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin description* for further details.
3. V_{SSA} or V_{REF-} must be tied to ground.
4. Guaranteed by design, not tested in production.
5. For 1 Msps, maximum Rext is 0.5 kΩ

Table 49. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error		±TBD	±TBD	LSB
EO	Offset error		±TBD	±TBD	
EG	Gain error		±TBD	±TBD	
ED	Differential linearity error		±TBD	±TBD	
EL	Integral linearity error		±TBD	±TBD	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative injection current: injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.11* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Table 50. ADC accuracy (1)(2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±TBD	±TBD	LSB
EO	Offset error		±TBD	±TBD	
EG	Gain error		±TBD	±TBD	
ED	Differential linearity error		±TBD	±TBD	
EL	Integral linearity error		±TBD	±TBD	
ENOB	Effective number of bits		±TBD	±TBD	bits
SINAD	Signal-to-noise and distortion ratio		±TBD	±TBD	dB
SNR	Signal-to-noise ratio		±TBD	±TBD	
THD	Total harmonic distortion		±TBD	±TBD	

1. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.11* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Figure 25. ADC accuracy characteristics

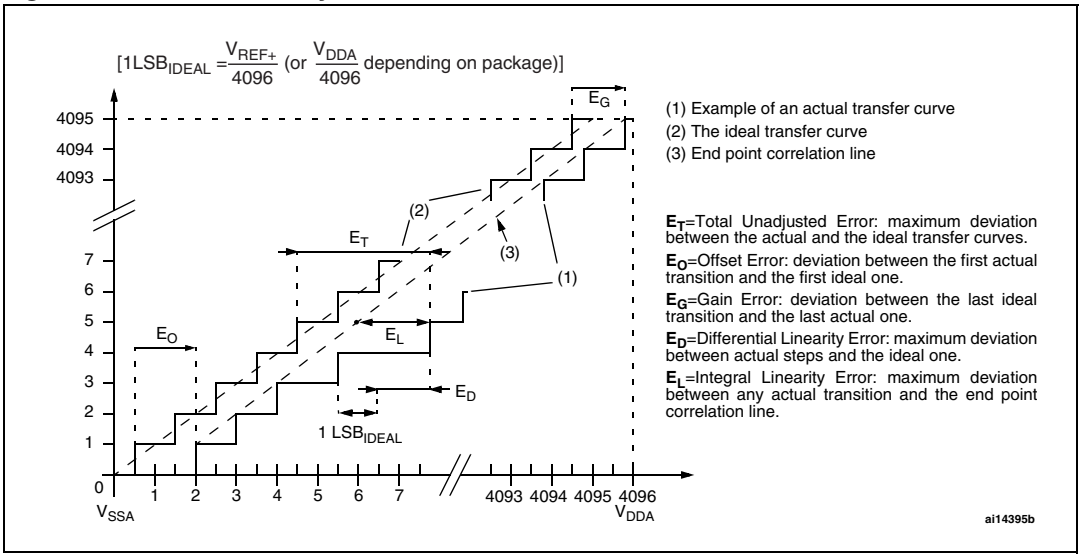
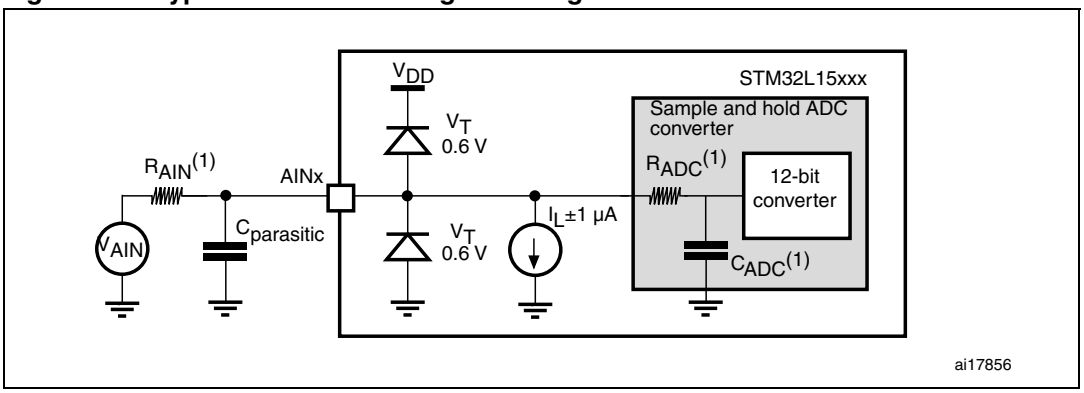


Figure 26. Typical connection diagram using the ADC

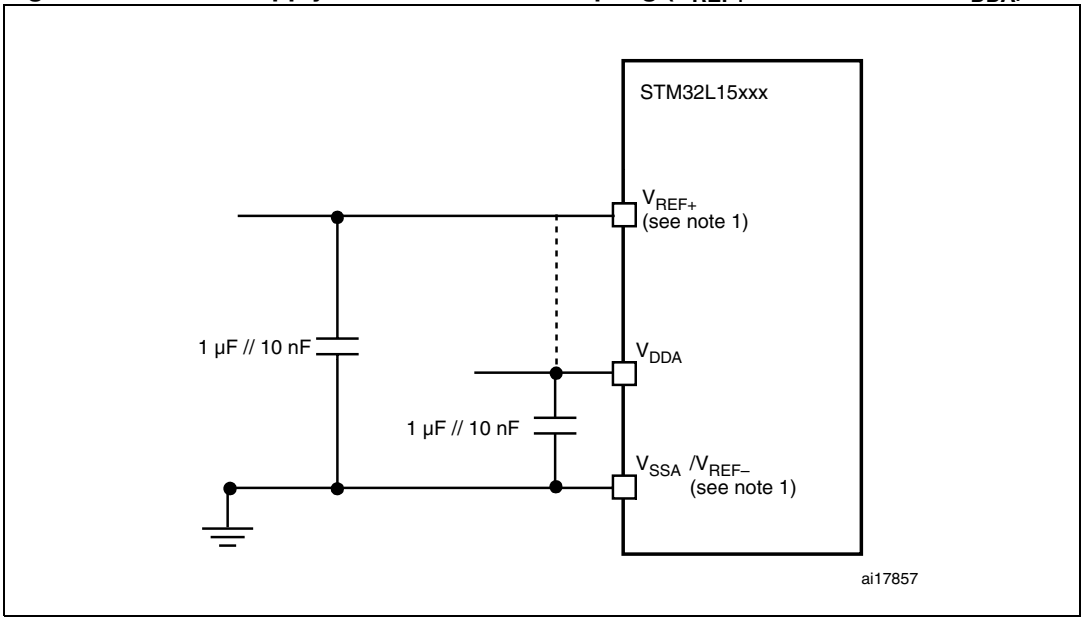


1. Refer to *Table 48* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

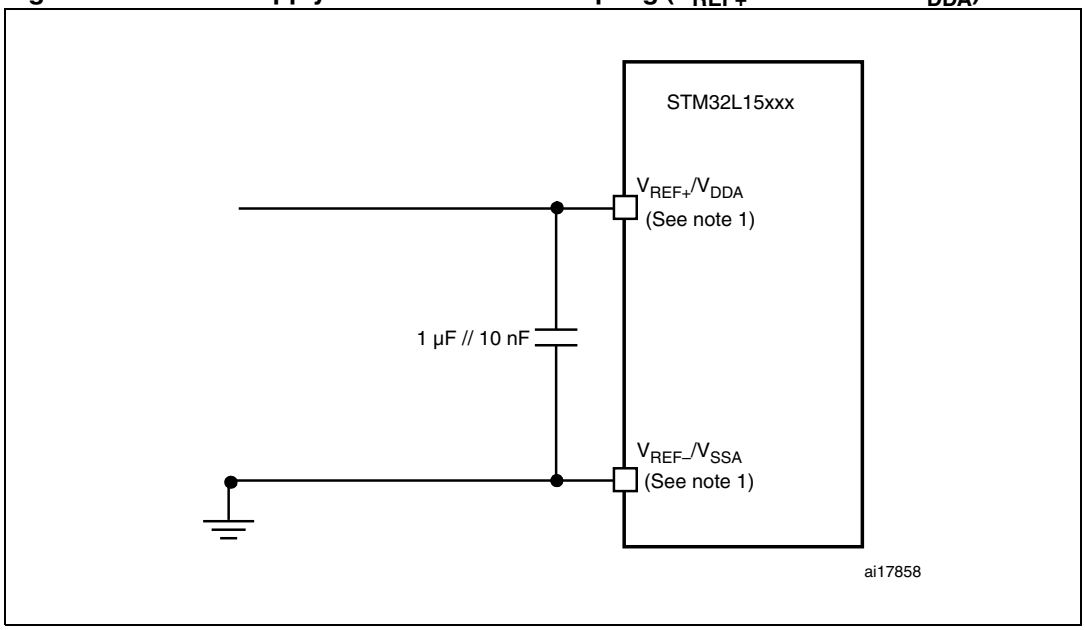
Power supply decoupling should be performed as shown in *Figure 27* or *Figure 28*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 27. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 28. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

6.3.16 DAC electrical specifications

Table 51. DAC characteristics

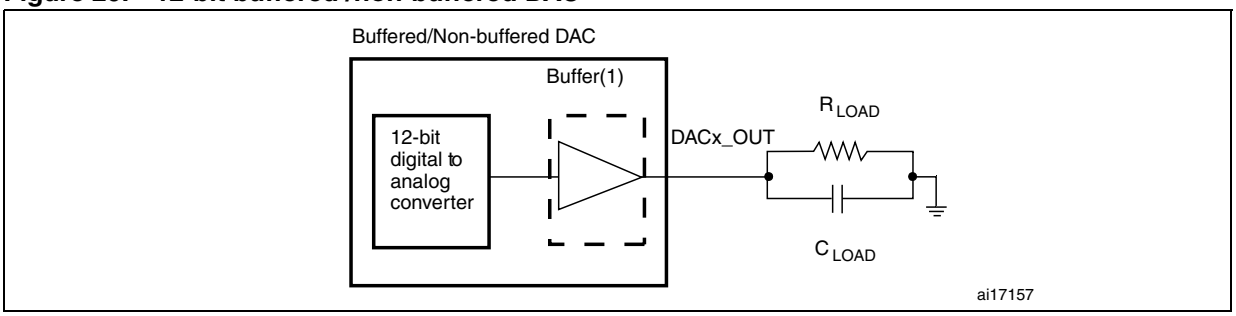
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		1.8		3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}	1.8		3.6	
V_{SSA}	Ground		0		0	
$I_{DDVREF+}$	Current consumption on V_{REF+} supply				210	µA
I_{DDA}	Current consumption on V_{DDA} supply	No load, middle code (0x800)		370	TBD	
		No load, worst code (0xF1C) with V_{REF+} = 3.6 V		500	TBD	
R_L(1)	Resistive load	DAC output buffer ON	5			kΩ
C_L(1)	Capacitive load				50	pF
R_O	Output impedance	DAC output buffer OFF			TBD	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2		V_{DDA} – 0.2	V
		DAC output buffer OFF	0.5		V_{REF+} – 1LSB	mV
DNL	Differential non linearity	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		±1	TBD	LSB
		$C_L \leq 50$ pF DAC output buffer OFF		TBD	TBD	
INL	Integral non linearity	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		±2	TBD	
		$C_L \leq 50$ pF DAC output buffer OFF		TBD	TBD	
Offset	Offset error (difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		±10		mV
		$C_L \leq 50$ pF DAC output buffer OFF		TBD	TBD	
Gain error	Gain error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		±0.5	TBD	%
		$C_L \leq 50$ pF DAC output buffer OFF		TBD	TBD	

Table 51. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TUE	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		TBD	TBD	LSB
		$C_L \leq 50$ pF DAC output buffer OFF		TBD	TBD	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ		7	TBD	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ			1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ		9	TBD	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ		-60	-35	dB

1. Connected between DAC_OUT and V_{SSA}.

Figure 29. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.17 Temperature sensor characteristics

Table 52. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature		±1	TBD	°C
Avg_Slope(1)	Average slope	TBD	1.62	TBD	mV/°C
V_{90}(1)	Voltage at 90°C ±5°C(2)	TBD	0.597	TBD	V
$I_{DDA(TEMP)}$	Current consumption		3.4	6	µA

Table 52. TS characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
t_{START}(3)	Startup time			10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature		5	10	

1. Guaranteed by characterization, not tested in production.
2. Measured at V_{DD} = 3 V ±10 mV. V90 ADC conversion result is stored in the TS_Factory_CONV_V90 byte.
3. Guaranteed by design, not tested in production.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 Comparator

Table 53. Comparator 1 characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	1.65		3.6	V
R_{400K}	R_{400K} value		400		kΩ
R_{10K}	R_{10K} value		10		
V_{IN}	Comparator 1 input voltage range	0		V_{DDA} - TBD	V
V_{REFINT}	Internal reference voltage		1.225		
t_{START}	Comparator startup time		7		µs
td	Propagation delay(2)		3		
Voffset	Comparator offset error		3		mV
I_{COMP1}	Current consumption(3)		160	TBD	nA

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 54. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage		1.65		3.6	V
V_{IN}	Comparator 2 input voltage range		0		V_{DDA}	V
t_{START}	Comparator startup time	Fast mode			TBD	µs
		Slow mode			TBD	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤V_{DDA} ≤2.7 V		TBD	TBD	
		2.7 V ≤V_{DDA} ≤3.6 V		TBD	TBD	
$t_{d\ fast}$	Propagation delay(3) in fast mode	1.65 V ≤V_{DDA} ≤2.7 V		TBD	TBD	
		2.7 V ≤V_{DDA} ≤3.6 V		TBD	TBD	

Table 54. Comparator 2 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{offset}	Comparator offset error			TBD		mV
I_{COMP2}	Current consumption(4)	Fast mode		TBD	TBD	µA
		Slow mode		TBD	TBD	

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
4. Comparator consumption only. Internal reference voltage not included.

6.3.19 LCD controller (STM32L152xx only)

The STM8L152xx embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 55. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage			3.6	V
V_{LCD0}	LCD internal reference voltage 0		2.6		
V_{LCD1}	LCD internal reference voltage 1		2.7		
V_{LCD2}	LCD internal reference voltage 2	0	2.8		
V_{LCD3}	LCD internal reference voltage 3		2.9		
V_{LCD4}	LCD internal reference voltage 4		3		
V_{LCD5}	LCD internal reference voltage 5		3.1		
V_{LCD6}	LCD internal reference voltage 6		3.2		
V_{LCD7}	LCD internal reference voltage 7		3.3		
C_{ext}	V_{LCD} external capacitance	0.1		2	µF
I_{LCD}(1)	Supply current at V_{DD} = 1.8 V		TBD		µA
	Supply current at V_{DD} = 1.8 V		TBD		
R_H	Low drive resistive network		TBD		MΩ
R_L	High drive resistive network		TBD		kΩ
V_{44}	Segment/Common highest level voltage			V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage		3/4 V_{LCD}		V
V_{23}	Segment/Common highest level voltage		2/3 V_{LCD}		
V_{12}	Segment/Common highest level voltage		1/2 V_{LCD}		
V_{13}	Segment/Common highest level voltage		1/3 V_{LCD}		

Table 55. LCD controller characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
V_{14}	Segment/Common highest level voltage		1/4 V_{LCD}		V
V_0	Segment/Common lowest level voltage	0			V

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected

7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 30. VFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline(1)

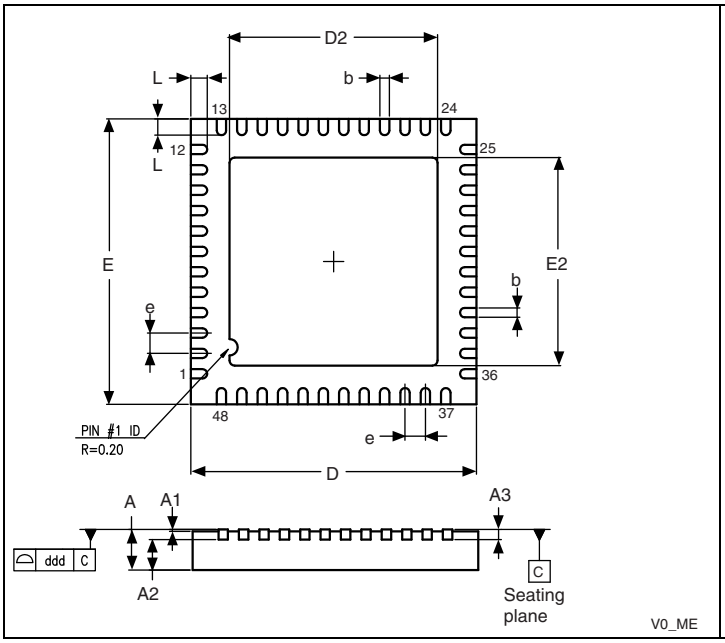
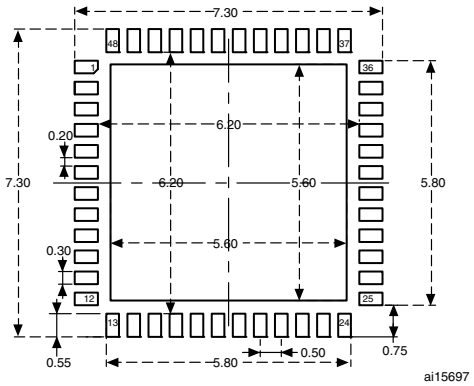


Figure 31. Recommended footprint (dimensions in mm)(1)



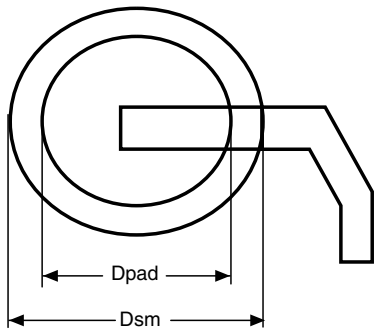
1. Drawing is not to scale.

Table 56. VFQFPN48 – very thin fine pitch quad flat pack nolead 7 × 7 mm, 0.5 mm pitch package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A	0.900	0.800	1.000	0.0354	0.0315	0.0394
A1	0.020		0.050	0.0008		0.0020
A2	0.650		1.000	0.0256		0.0394
A3	0.250			0.0098		
b	0.230	0.180	0.300	0.0091	0.0071	0.0118
D	7.000	6.850	7.150	0.2756	0.2697	0.2815
D2	4.700	2.250	5.250	0.1850	0.0886	0.2067
E	7.000	6.850	7.150	0.2756	0.2697	0.2815
E2	4.700	2.250	5.250	0.1850	0.0886	0.2067
e	0.500	0.450	0.550	0.0197	0.0177	0.0217
L	0.400	0.300	0.500	0.0157	0.0118	0.0197
ddd	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 32. Recommended PCB design rules for pads (0.5 mm pitch BGA)

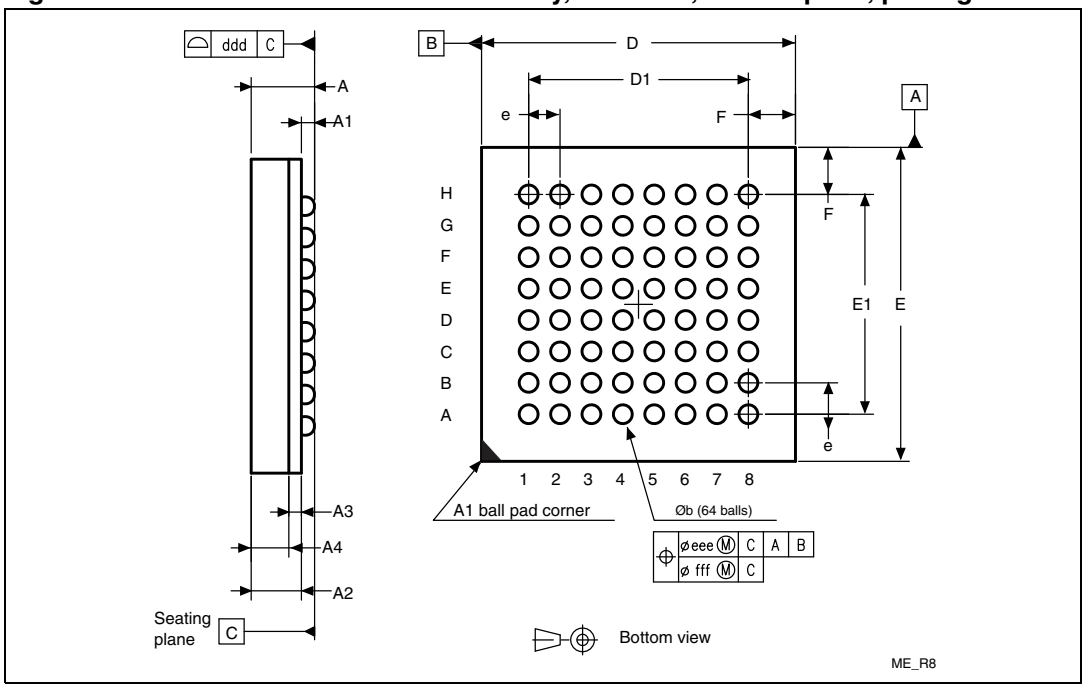


Pitch	0.5 mm
D pad	0.27 mm
Dsm	0.35 mm typ (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

ai15495

1. Non solder mask defined (NSMD) pads are recommended
2. 4 to 6 mils solder paste screen printing process

Figure 33. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package outline



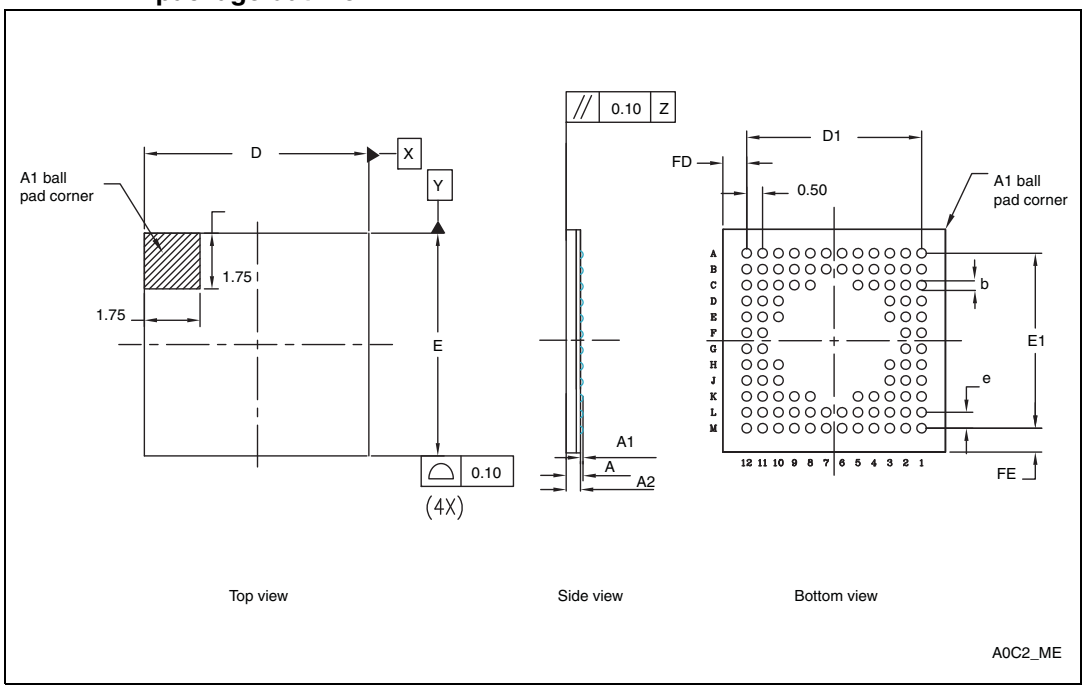
1. Drawing is not to scale.

Table 57. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1	0.150			0.0059		
A2		0.785			0.0309	
A3		0.200			0.0079	
A4			0.600			0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1		3.500			0.1378	
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1		3.500			0.1378	
e		0.500			0.0197	
F		0.750			0.0295	
ddd		0.080			0.0031	
eee		0.150			0.0059	
fff		0.050			0.0020	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. UFBGA100 - ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline



1. Drawing is not to scale.

Table 58. UFBGA100 - ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.46	0.53	0.6	0.0181	0.0209	0.0236
A1	0.06	0.08	0.1	0.0024	0.0031	0.0039
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D		7			0.2756	
D1		5.5			0.2165	
E		7			0.2756	
E1		5.5			0.2165	
e		0.5			0.0197	
FD		0.75			0.0295	
FE		0.75			0.0295	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline(1)

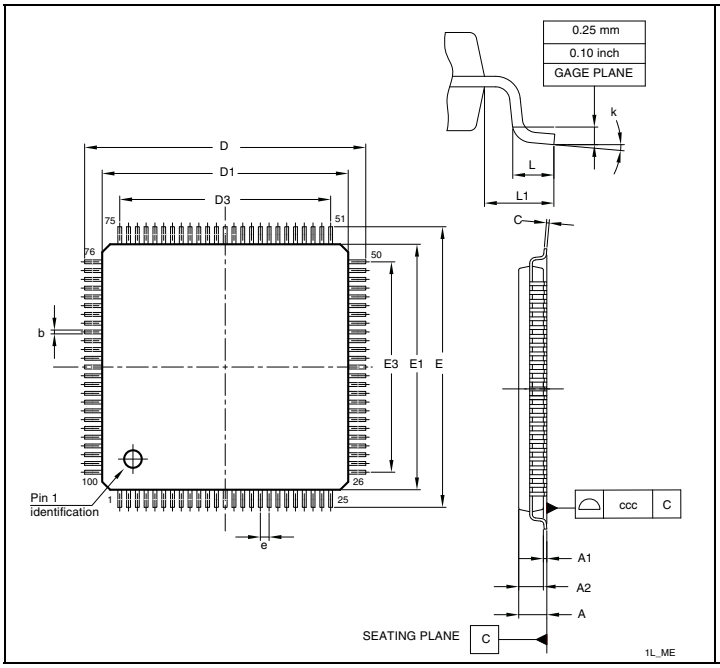
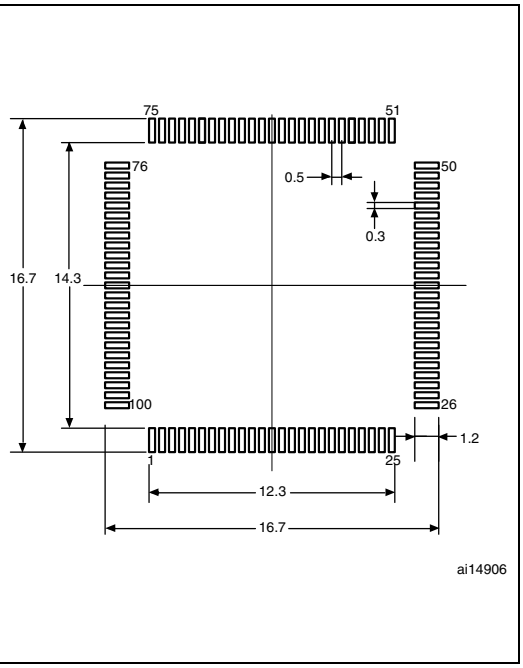


Figure 36. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 59. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.6			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.2	0.0035		0.0079
D	15.8	16	16.2	0.622	0.6299	0.6378
D1	13.8	14	14.2	0.5433	0.5512	0.5591
D3		12			0.4724	
E	15.8	16	16.2	0.622	0.6299	0.6378
E1	13.8	14	14.2	0.5433	0.5512	0.5591
E3		12			0.4724	
e		0.5			0.0197	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline(1)

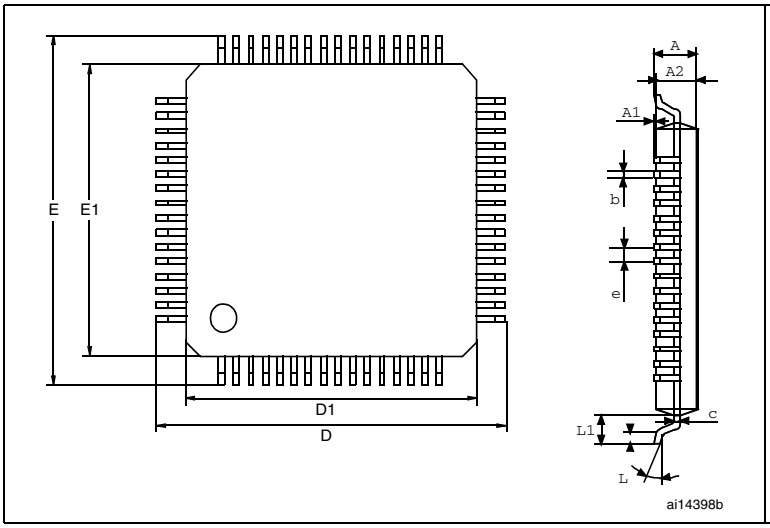
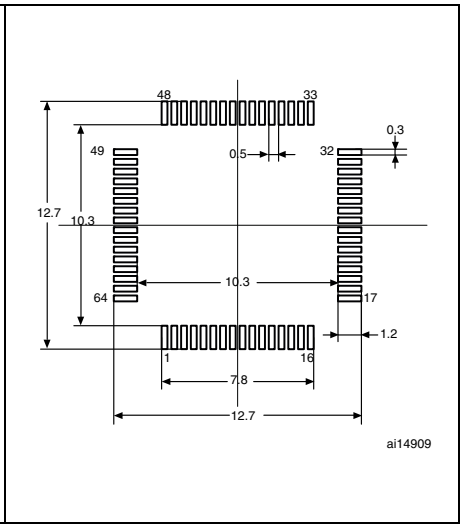


Figure 38. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 60. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline(1)

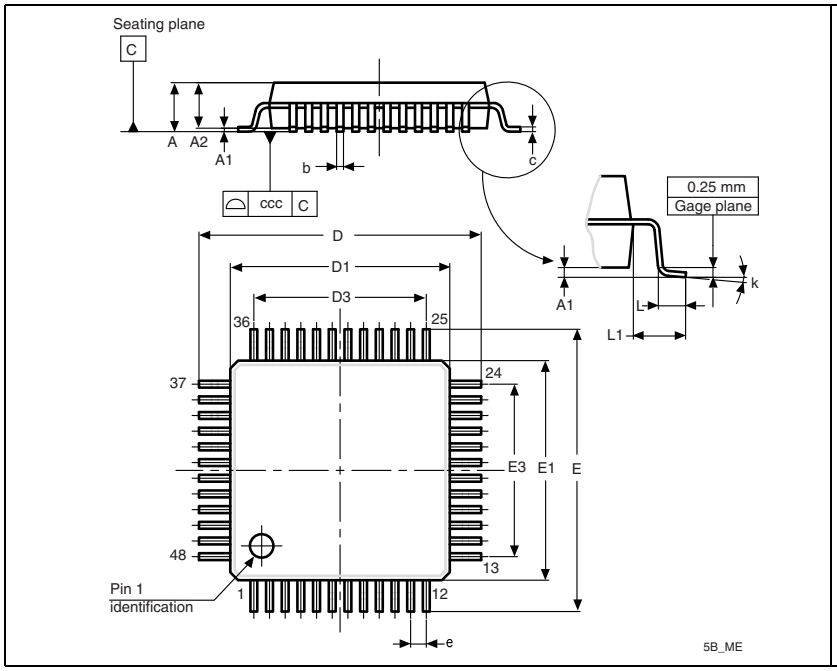
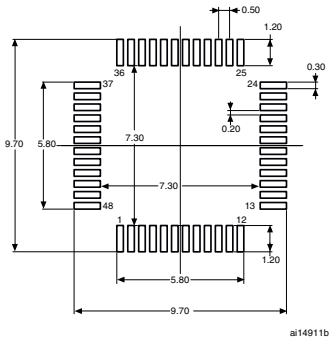


Figure 40. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 61. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
c		0.090	0.200		0.0035	0.0079
D	9.000	8.800	9.200	0.3543	0.3465	0.3622
D1	7.000	6.800	7.200	0.2756	0.2677	0.2835
D3	5.500			0.2165		
E	9.000	8.800	9.200	0.3543	0.3465	0.3622
E1	7.000	6.800	7.200	0.2756	0.2677	0.2835
E3	5.500			0.2165		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 62. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** BGA100 - 7 x 7 mm	TBD	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient VFQFPN48 - 7 x 7 mm / 0.5 mm pitch	16	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 63: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L15xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 62* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 63: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 62* T_{Jmax} is calculated as follows:

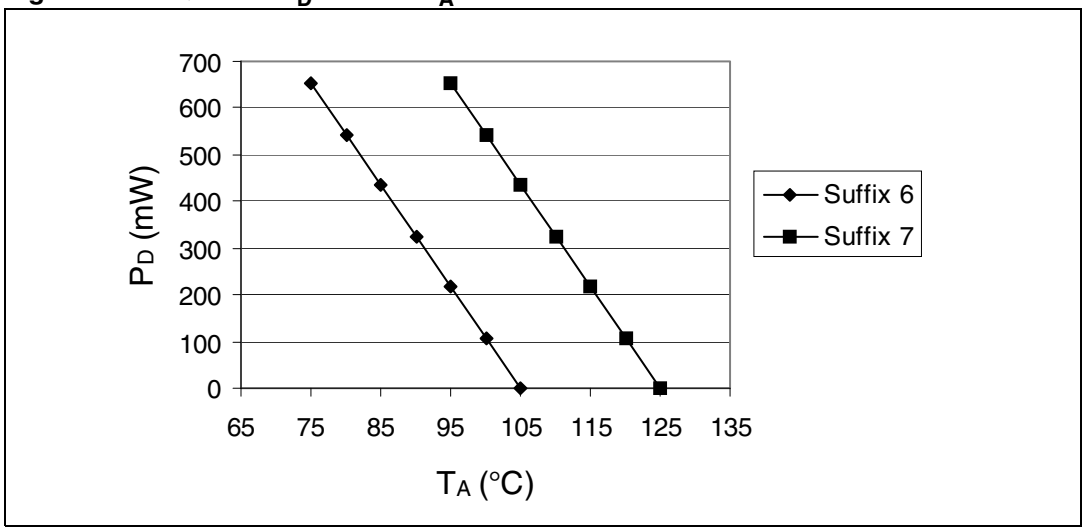
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 63: Ordering information scheme*).

Figure 41. LQFP100 P_D max vs. T_A



8 Ordering information scheme

Table 63. Ordering information scheme

Example: STM32 L 151 C 8 T 6 D xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

H = BGA

T = LQFP

U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 64. Document revision history

Date	Revision	Changes
02-Jul-2010	1	Initial release.

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