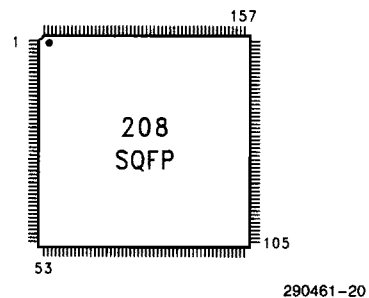
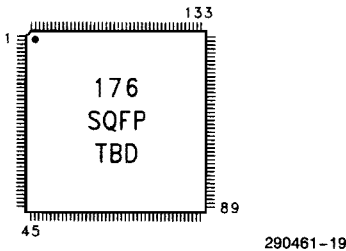


iFX8160

10 ns FLEXlogic FPGA WITH SRAM OPTION

- **High Performance FPGA (Field Programmable Gate Array)**
 - Deterministic 10 ns Pin-to-Pin Propagation Delays
 - 80 MHz System Clock Frequency
- **160 Complex Macrocells (7,000 Maximum Logic Gates) or up to 20,480 Bits of SRAM**
- **Any CFB can be either 24V10 Logic or SRAM Block**
 - 128 x 10 SRAM Configuration
 - CFB Selectable 3.3V or 5V Outputs
 - Open-Drain Output Option
- **Supports Partial Reconfigurability and Reprogrammability**
- **JTAG 1149.1 Compatible Test Port**
 - Supports Boundary Scan and In-Circuit Reconfiguration and Re-Programming
- **Supported by Industry Standard Design and Programming Tools**
- **Electrically Erasable 0.6 μ ETOX* IV CHMOS FLASH Technology**
 - Power Management Options Minimize Active Power Consumption (3 mA/MHz)
 - 1 mA Standby
- **High Drive I/O**
 - PCI Compliant
- **24V10 Macrocell Features**
 - Dual Feedback on All I/O Pins
 - Allocation Supports up to 16 Product Terms per Macrocell with No Performance Penalty
 - 12 Clocking Options
 - Flexible Preset/Clear Options
 - Selectable D/T Flip-Flops
 - Fast 12-Bit Identity Compare Option
- **Sixteen Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix**
 - Improves Fitting of Complex Designs
- **TQFP Thin Package Available**

2



Package Options

Pins	Package	Macrocells	I/O	Inputs	Clocks	JTAG/V _{PP}	V _{CC}	GND
176	TQFP	160	110	26	4	6	12	18
208	SQFP	160	120	48	4	6	12	18
225	BGA	160	120	54	4	6	17	24

*ETOX is a patented process of Intel Corporation.

INTRODUCTION

The iFX8160 is the third member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The iFX8160 consists of sixteen configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128 x 10 SRAM. This combination will provide approximately 7,000 gates of logic in either SQFP or BGA packages.

FLEXIBLE PERFORMANCE

The iFX8160 uses Intel's 0.6µ ETOX FLASH technology to provide an 80 MHz external clock frequency with predictable 10 ns pin-to-pin delays. This advanced process technology combined with power management options enables very low active and standby power consumption.

FLEXIBLE FEATURES

The unique combination of features available in the iFX8160 make it ideal for a wide variety of applications. For example, the high performance and flexible clock options provided are designed to support functions such as bus control, custom cache control, and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the iFX8160 to be used in mixed voltage appli-

cations such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication controllers or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design itself.

FLEXIBLE TESTING AND PROGRAMMING

The iFX8160 also provides dedicated JTAG 1149.1 compatible pins to support boundary scan, in-circuit reconfiguration/reprogramming, and programming modes. In-circuit reconfiguration/reprogramming not only allows the designer ultimate flexibility in prototyping new designs but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the iFX8160 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time. For more information on in-circuit reconfiguration and programming, refer to Application Brief AB-52.

FLEXIBLE TOOLS SUPPORT

The FLEXlogic FPGA family is supported by industry standard design entry/programming environments including Intel's PLDshell Plus software. This software runs on Intel386™ or higher PC-compatible platforms.

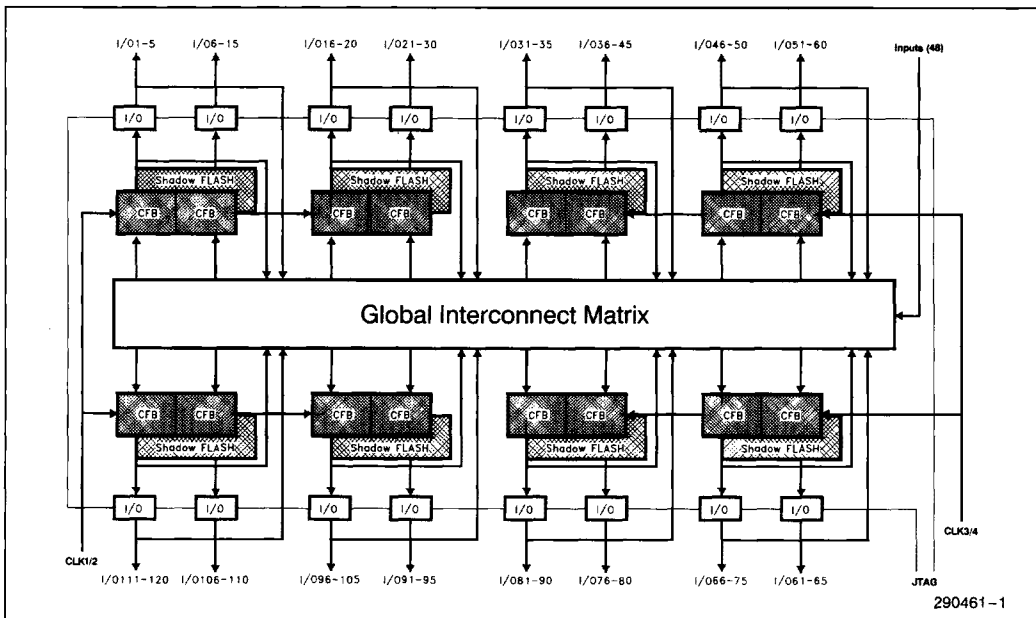


Figure 1. iFX8160 Architecture

INTERCONNECT

The Global Interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

Configurable Function Blocks

24V10 MODE

Each 24V10 block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a generous fan-in to macrocell ratio (2.4:1). This improves the fitting capacity of the iFX8160 architecture by providing more

available interconnect lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

MACROCELL CONFIGURATIONS

Each I/O of the device has dual (internal and pin) feedback paths (see Figure 2). This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Depending on the package used, some macrocell outputs may not be brought outside the package. These I/Os may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, a D-register. J/K and S/R registers are available via software emulations.

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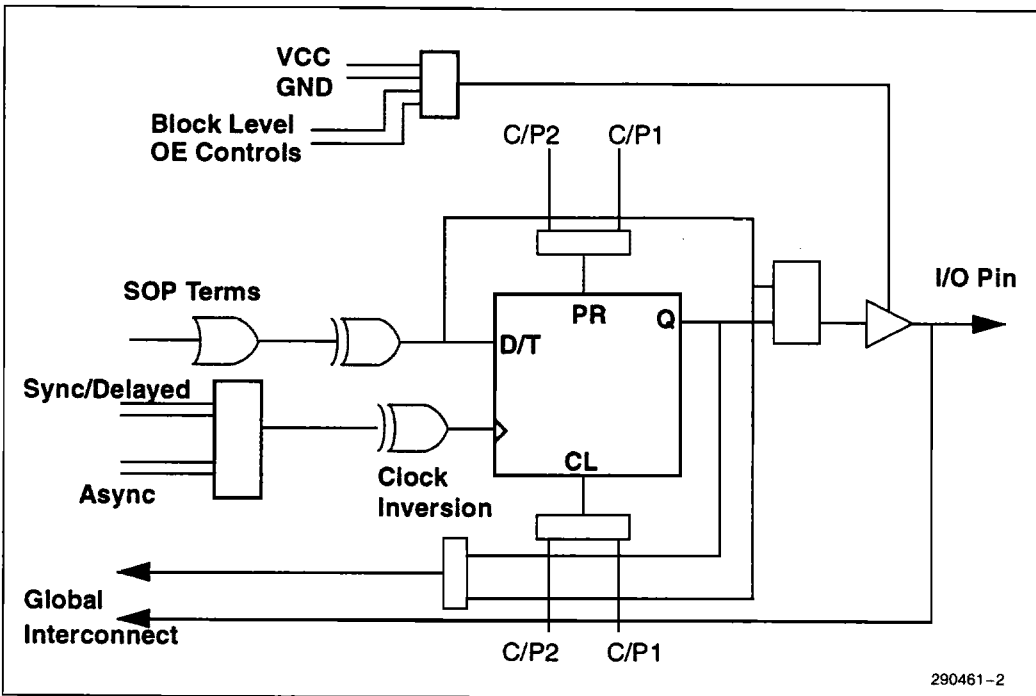


Figure 2. CFB as 24V10 Block

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CLOCKING MODES

There are three clocking modes available for every macrocell (see Figure 3): *synchronous*, *delayed*, *asynchronous*. Table 1 shows the different timing options each clock mode offers.

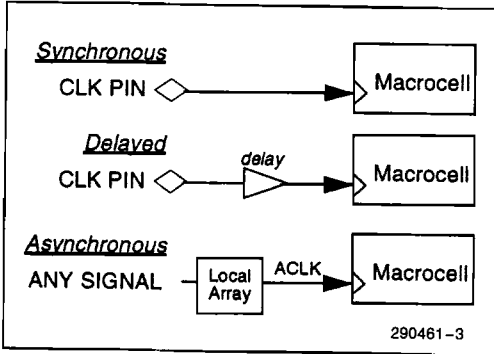


Figure 3. Clocking Modes

Synchronous is the standard clock mode where the register clock is driven directly from one of the two global clock pins.

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Table 1. Clock Mode Timings

Mode	T _{SU}	T _{HOLD}	T _{CO}
Synchronous	6.5	0	6
Delayed	5	2	8
Asynchronous	2	5	12

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

CONTROL SIGNALS

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Pre-set signals. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

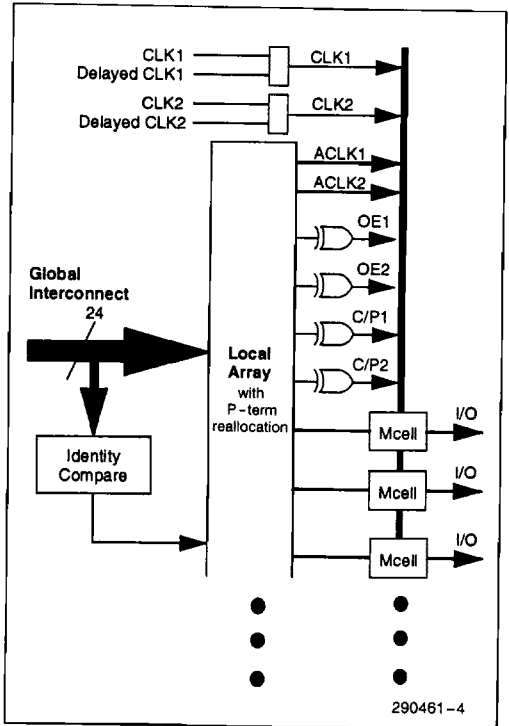


Figure 4. Control Signals

COMPARATOR LOGIC

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals, within the T_{PD} of the device.

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24 - 16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

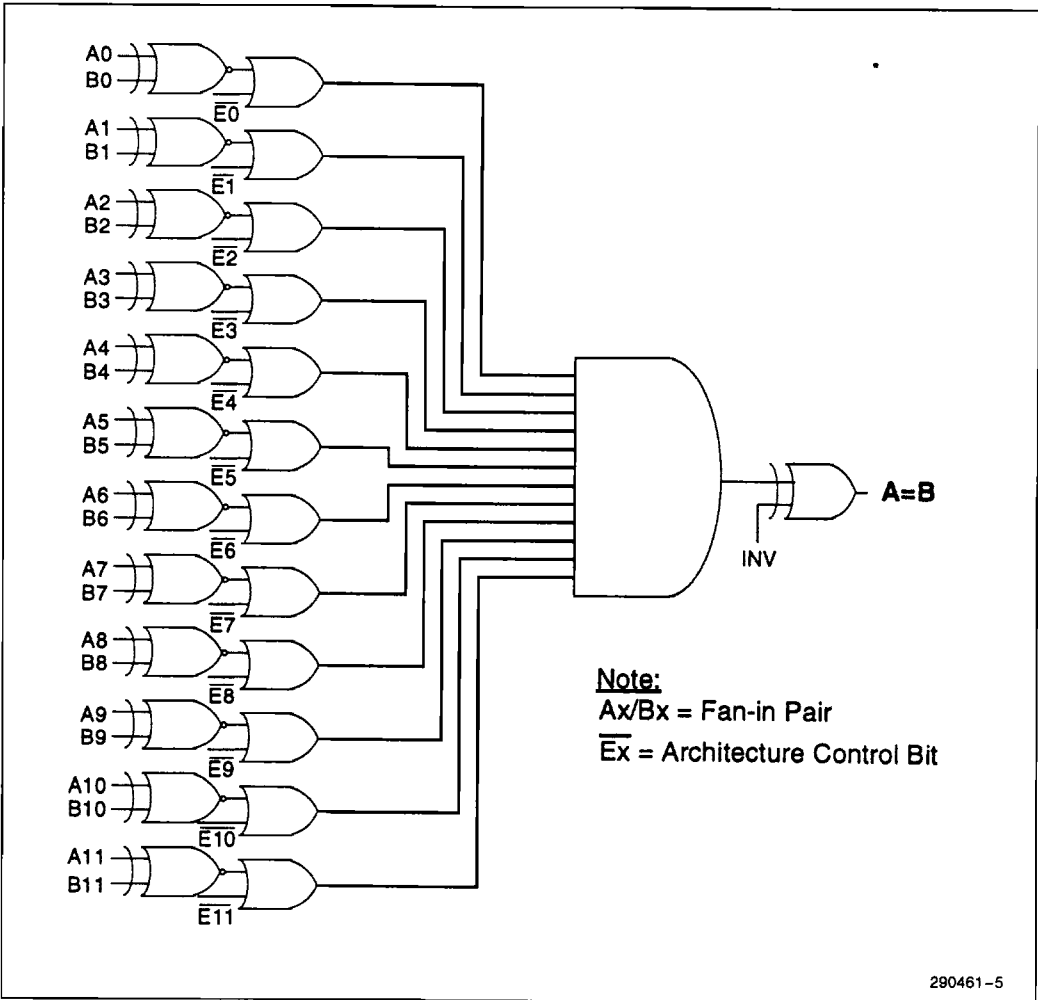


Figure 5. 12-Bit Identity Compare Logic

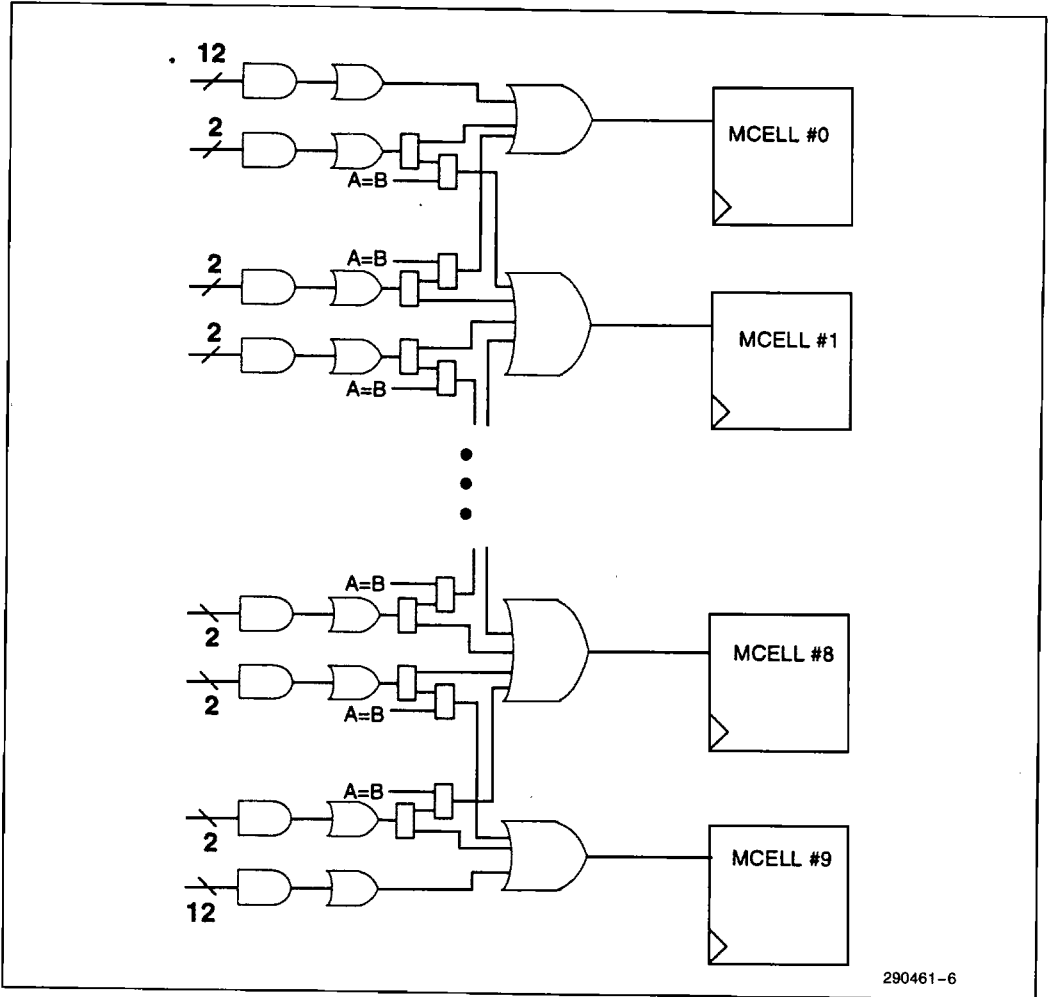


Figure 6. CFB Product Terms

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PRODUCT TERM ALLOCATION

The iFX8160 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to

16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 P-terms or 16 P-terms are being used.

SRAM Configuration

Each iFX8160 CFB block can be configured as a 128 x 10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for \overline{BE} (Block Enable), \overline{WE} , and \overline{OE} controls (see Table 2). SRAM control signals on the iFX8160 may be active-high or active low.

Table 2. SRAM Function Table

Inputs			Cycle	I/O Pins
BE	WE	OE		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	write	Disabled
0	0	0	write	Enabled

The SRAM memory bits are initialized by the on-chip FLASH cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the macrocells and p-terms have been converted to SRAM use.

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

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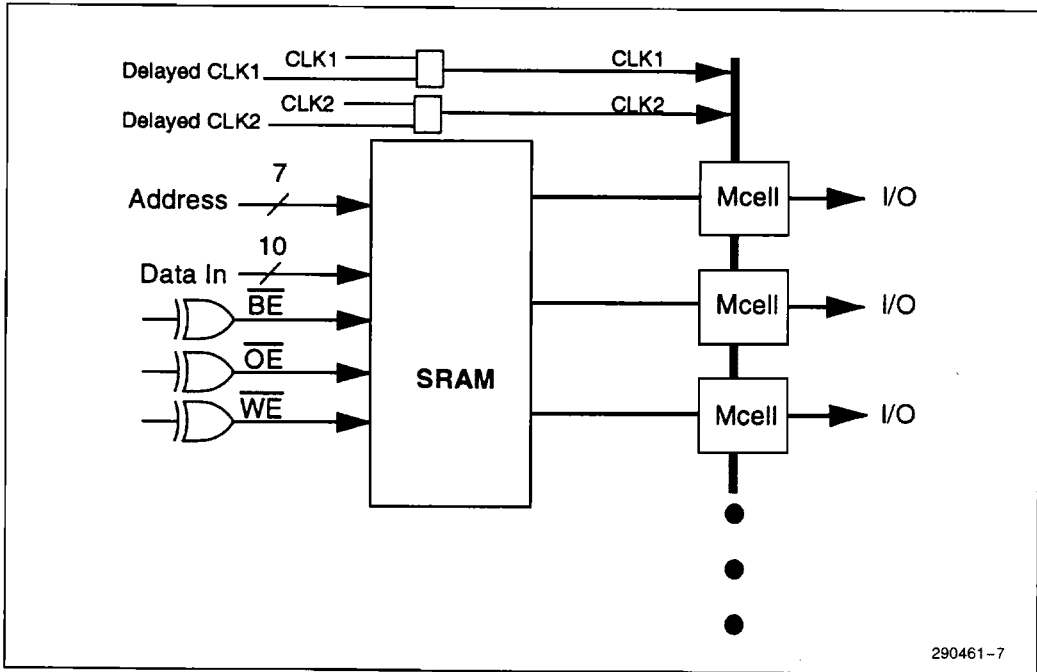


Figure 7. SRAM Overall Block Diagram

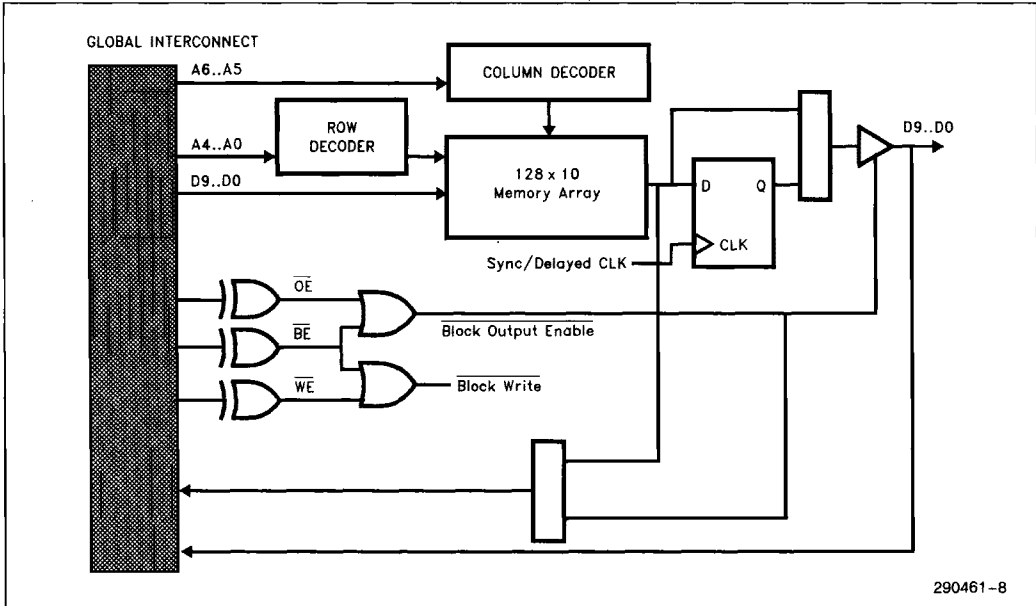


Figure 8. SRAM Functional Block Diagram

Input Configuration

Inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the "CMOS_LEVEL" and "TTL_LEVEL" keywords available in the PLDasm design language of PLDshell Plus. For 5V CMOS inputs, the "CMOS_LEVEL" keyword (the default condition for PLDasm) should be used. For TTL or 3.3V CMOS inputs, the "TTL_LEVEL" keyword should be used to minimize standby power consumption. Third party tools that support the FLEXlogic family provide input configuration in a method specific to each tool. For Additional information refer to Application Brief AB-27.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CC0} pins to a 3.3V power supply. While the iFX8160 still requires 5V V_{CC} for normal operation, the V_{CC0} pin associated with each CFB block may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block. This allows the iFX8160 to be used in mixed voltage

systems. For example, the iFX8160 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

OPEN DRAIN OUTPUT OPTION

The device can also be configured to enable an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

TTL VERSUS CMOS OUTPUTS

There is a weak pullup provided for CMOS-compatible outputs. This pullup is always active in both 3.3V and 5V modes.

HIGH DRIVE I/O

The iFX8160 output buffers are designed specifically for applications requiring high drive current. This allows the iFX8160 to drive a bus, like PCI, without the need for external buffers.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the iFX8160. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The iFX8160 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The boundary scan cells of the iFX8160 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the iFX8160 for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit programming.

Boundary Scan Instructions

The iFX8160 boundary scan Instruction Register (IR) supports public instruction opcodes, extended instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR OPCODE 00000 BINARY)

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the iFX8160 package, typically for printed circuit board interconnects.

BYPASS (IR OPCODE 11111 BINARY)

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR OPCODE 00001 BINARY)

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a snap-shot of the values of the pins of the iFX8160 in an unobtrusive manner and 2) preloads data to the iFX8160 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR OPCODE 00010 BINARY)

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the ID-code to be serially shifted out of TDO.

UESCODE (IR OPCODE 10110 BINARY)

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR OPCODE 01000 BINARY)

The HIZ instruction sets all I/Os to a high impedance state.

FERASE (IROPCODE TBD)

The FERASE instruction is used to erase the non-volatile shadow FLASH array before re-programming.

IN-CIRCUIT RECONFIGURATION AND REPROGRAMMING

The iFX8160 supports in-circuit reconfiguration through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device. This may be done as many times as desired in a prototyping scenario.

Once the final version of the design is confirmed it may be programmed into the FLASH cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pins (V_{PP}).

The iFX8160 FLASH cells are also electrically erasable and may be reprogrammed.

Partial reconfiguration and reprogrammability is also supported in the iFX8160. New configurations may be downloaded to either half of the iFX8160 during operation to reflect changes in system design.

SECURITY

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the non-volatile cells or the SRAM. The state of the non-volatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus includes several enhancements over earlier versions:

- Design Merge
- SRAM Configuration Support
- Compare Operation Support
- Simulation Support for Intel FPGA
- Vector Notation
- Full Mouse Support
- Device Selector

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel iFX8160. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA ARCHITECTURAL FEATURE SUPPORT

PLDshell Plus supports all of the innovative architectural features of the iFX8160 through the implementation of new language syntax such as:

- SRAM configuration
- Compare operation
- Buried macrocells
- Clocking options
- 3.3V and 5V options

FUNCTIONAL SIMULATION

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

PLDshell Plus provides the following simulation capabilities:

- Event-driven simulation of combinatorial, registered, and state machine designs
- Ability to set any input, preload any register, and compare any output against an expected value
- Ability to group signals together (form a vector) to simulate a bus
- Generation of test vectors from simulation results for inclusion in the JEDEC file
- Simulation history file with ability to output a subset of signals to a secondary trace file

DEVICE SELECTOR

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

SYSTEM REQUIREMENTS

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

- Intel 386 based PC compatible
- 4 MB RAM (minimum)
- VGA monitor/adaptor
- DOS 3.1 (or later)

THIRD-PARTY SUPPORT DESIGN SOFTWARE

Third party tools support is provided by the following vendors:

- Data I/O
 - ABEL: Design software allowing you to describe and implement logic designs.
- Logical Devices
 - CUPL: High level, universal design software package.
- Minc
 - PLDesigner-XL(R): Powerful design tool that can be used for all types of programmable logic with automatic device selection, automatic partitioning and functional simulation.
- OrCAD
 - PLD Tools and Schematic Design Tool: Software tool environment including schematic entry, test vector generation and multiple forms of input.

- Verification/Simulation Tool: Series of software tools for performing timing-based simulation of designs.
- Viewlogic
 - ViewPLD and Powerview: Integrated schematic capture and simulation environment.

DEVICE MODELS

Simulation models will be provided by the following vendors:

- Logic Modeling Corporation
 - Smart Model: Device model support for behavioral simulation through a variety of simulators.
- Viewlogic

PROGRAMMING SUPPORT

- Products in Motion (916) 363-5591
 - Flexlogic Programmer
- BP Microsystems
 - PLD 1100
- Data I/O
 - Unisite
 - 2900/3900
- Elan
 - Model 6000

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})⁽¹⁾ -2.0V to +7.0V
 Programming Supply
 Voltage (V_{PP})⁽¹⁾ -2.0V to +12.6V
 DC Input Voltage (V_I)^(1, 2) -0.5V to $V_{CC} + 0.5V$
 Storage Temperature (T_{stg}) -65°C to +150°C
 Ambient Temperature (T_{amb})⁽³⁾ ... -10°C to +85°C

NOTES:

1. Voltages with respect to ground.
2. Minimum DC input is -0.5V. During transitions, the inputs may undershoot to -2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply Voltage—5.0V	4.75	5.25	V
V_{CCO}	Output Supply Voltage—3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

DC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)(4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{IH}^{(5)}$	High Level Input Voltage	2.0		$V_{CC} + 0.3$	V	
$V_{IL}^{(5)}$	Low Level Input Voltage	-0.3		0.8	V	
$V_{OH}^{(7)}$	5V TTL High Level Output	2.4			V	I/O = -16.0 mA D.C., $V_{CC} = \text{Min.}$
	5V CMOS High Level Output	$V_{CCO} - 0.2$			V	I/O = -100 μA D.C., $V_{CC} = \text{Min.}$
	3V High Level Output Voltage	$V_{CCO} - 0.2$			V	I/O = -100 μA D.C., $V_{CC} = \text{Min.}$
$V_{OL}^{(7)}$	5V Low Level Output Voltage			0.45	V	I/O = 24.0 mA D.C., $V_{CC} = \text{Min.}$
	3V Low Level Output Voltage			0.2	V	I/O = 12 mA D.C., $V_{CC} = \text{Min.}$
$I_I^{(8)}$	Input Leakage Voltage			± 10	μA	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}
I_{OZ}	Output Leakage Current			± 50	μA	$V_{CC} = \text{Max.}$, $V_{OUT} = \text{GND}$ or V_{CC}
$I_{SC}^{(6)}$	Output Short Circuit Current	-30		-120	mA	$V_{CC} = \text{Max.}$, $V_{OUT} = 0.5\text{V}$
I_{SB}	Standby Power Supply Current		1		mA	$V_{IN} = V_{CC}$ or GND, Outputs Open
I_{CC} Active	Power Supply Current		3		mA per MHz	$V_{IN} = V_{CC}$ or GND, Outputs Open, Device Programmed as Eight 20-Bit Counters

NOTES:

4. Typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

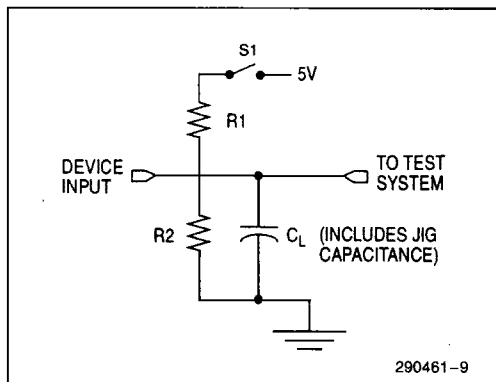
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.

6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

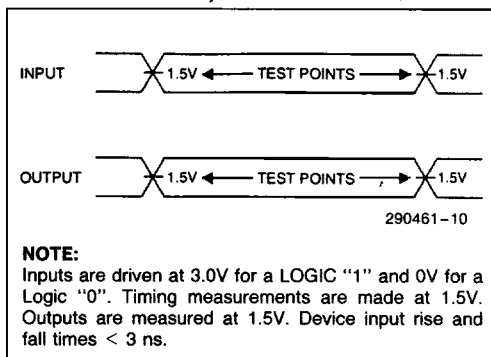
7. When driving an I/O pin under JTAG boundary scan, $I_{OH} = -4.0\text{ mA}$ and $I_{OL} = 12\text{ mA}$.

8. Input Leakage current on JTAG pins: $\pm 20\ \mu\text{A}$

AC TESTING LOAD CIRCUIT



AC TESTING INPUT, OUTPUT WAVEFORM



SWITCHING TEST CIRCUIT

Specification	S1	CL	Commercial		Measured Output Value
			R1	R2	
t _{PD}	Closed	35 pF	330Ω	200Ω	1.5V
t _{PZX}	Z → H: Open Z → L: Closed				1.5V
t _{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V _{OH} - 0.5V L → Z: V _{OL} + 0.5V

PIN CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)(7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C _{IN}	Input Capacitance	V _{IN} = 2V, f = 1.0 MHz				pF
C _{IO}	I/O Capacitance	V _{OUT} = 2V, f = 1.0 MHz				pF
C _{CLK}	Clock Pin Capacitance	V _{OUT} = 2V, f = 1.0 MHz				pF
C _{VPP}	V _{pp} Pin Capacitance	f = 1.0 MHz				pF

NOTE:

7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Symbol	Parameter	IFX8160-10			IFX8160-12			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or I/O to Output Valid			10			10	ns
$t_{PZX}^{(8)}$	Input or I/O to Output Enable			12			14	ns
$t_{PXZ}^{(8)}$	Input or I/O to Output Disable			12			14	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			15			18	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			10			12	ns

REGISTER MODE—IFX8160-10 CLOCK AC CHARACTERISTICS

 ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

2

Symbol	Parameter	Synchronous		Delayed Synchronous		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max. Counter Frequency $1/(t_{SU} + t_{CO1})$ —External Feedback	80		76.9		71.4		MHz
f_{CNT2}	Max. Counter Frequency $1/t_{CNT}$ —Internal Feedback	80		76.9		71.4		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/t_{CP}$ —No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6.5		5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6		8		12	ns
t_{CO2}	CLK to Output Valid Fed through Combinatorial Macrocell		16		18		22	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12.5		13		14	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

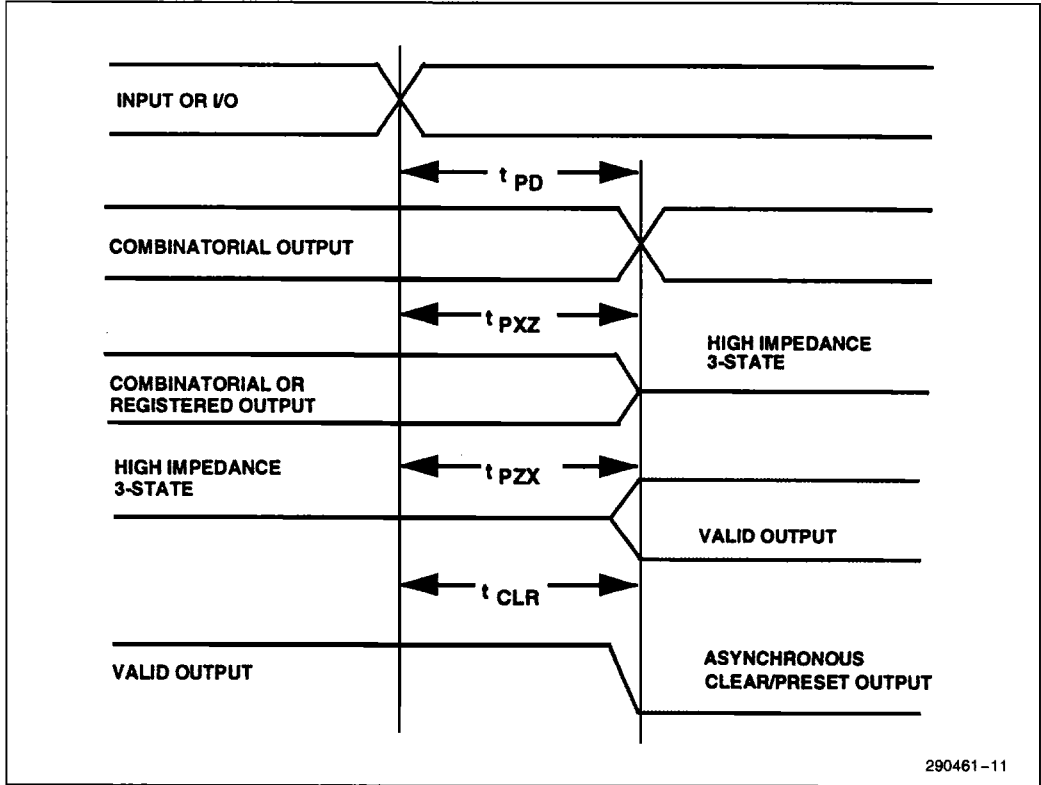
NOTE:

 8. t_{PZX} and t_{PXZ} are measured at $\pm 0.5\text{V}$ from steady state voltage as driven by specified output load. t_{PXZ} is measure with $C_L = 5\text{ pF}$. $Z \rightarrow H$ and $Z \rightarrow L$ are measured at 1.5V on output.

REGISTER MODE—IFX8160-12 CLOCK AC CHARACTERISTICS
 $(T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5.0\text{V} \pm 5\%)$

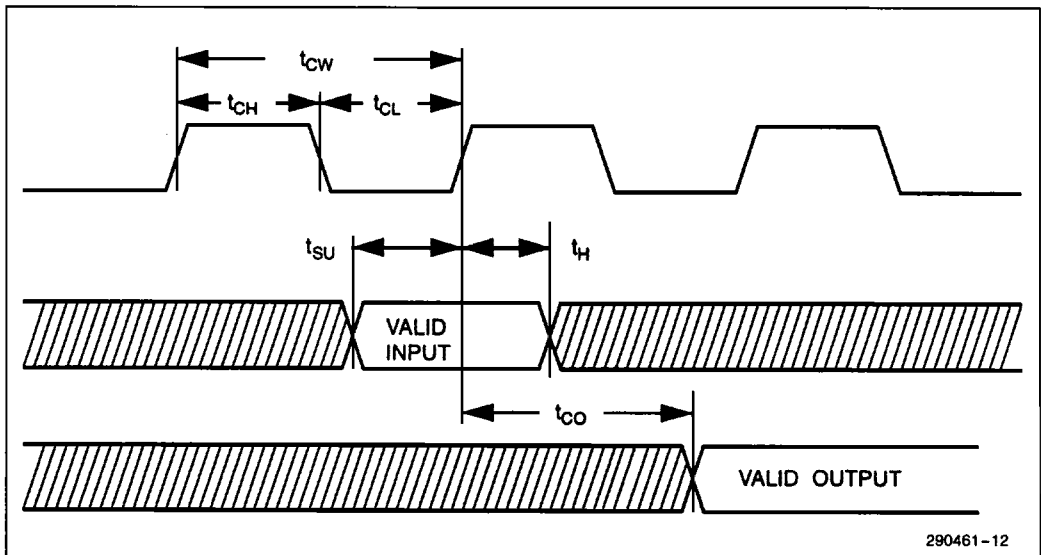
Symbol	Parameter	Synchronous		Delayed Synchronous		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max. Counter Frequency $1/(t_{\text{SU}} + t_{\text{CO1}})$ —External Feedback	64.5		64.5		58.8		MHz
f_{CNT2}	Max. Counter Frequency $1/t_{\text{CNT}}$ —Internal Feedback	64.5		64.5		58.8		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/t_{\text{CP}}$ —No Feedback	83.3		80		66.7		MHz
t_{SU}	Input or I/O Setup Time to CLK	8		6		2.5		ns
t_{H}	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		7.5		9.5		14.5	ns
t_{CO2}	CLK to Output Valid Fed through Combinatorial Macrocell		19.5		21.5		26.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		15.5		15.5		17	ns
t_{CL}	CLK Low Time	5.5		5.5		5.5		ns
t_{CH}	CLK High Time	5.5		5.5		5.5		ns
t_{CP}	CLK Period	12		12.5		15		ns

COMBINATORIAL MODE WAVEFORMS



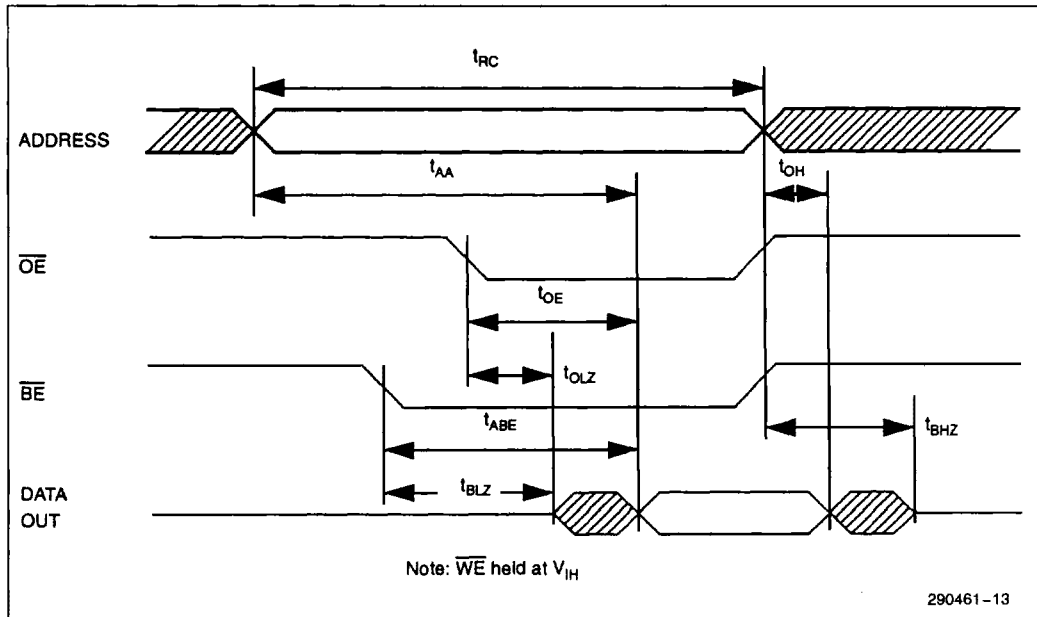
2

REGISTERED MODE WAVEFORMS



SRAM READ—AC CHARACTERISTICS ($T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Symbol	Parameter	iFX8160-10		iFX8160-12		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		18		ns
t_{AA}	Address Access Time		15		18	ns
t_{ABE}	Block Enable Access Time		15		18	ns
$t_{OE}^{(1)}$	Output Enable to Output Valid		12		14.5	ns
t_{OH}	Output Hold from Address Change	2		3		ns
$t_{BLZ}^{(1)}$	Block Enable to Output in Low Z	3		4		ns
$t_{BHZ}^{(1, 2)}$	Block Disable to Output in High Z		10		12	ns
$t_{OLZ}^{(1)}$	Output Enable to Output in Low Z	3		4		ns

TIMING WAVEFORM OF READ CYCLE


SRAM WRITE—AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

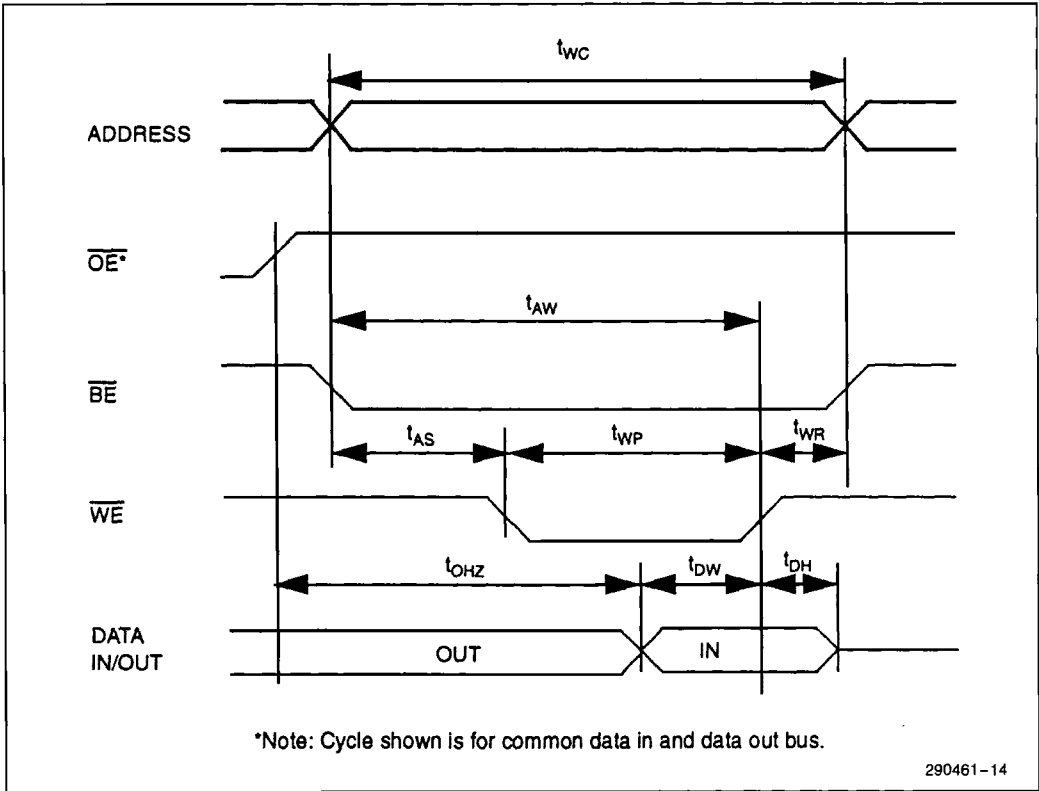
Symbol	Parameter	IFX8160-10		IFX8160-12		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		18		ns
t_{BW}	Block Enable to End of Write	10		12		ns
t_{AW}	Address Valid to End of Write	13		15.5		ns
t_{AS}	Address Set-up Time	3		4		ns
t_{WP}	Write Pulse Width	10		12		ns
t_{WR}	Write Recovery Time	2		3		ns
t_{DW}	Data Valid to End of Write	10		12		ns
t_{DH}	Data Hold Time	2		3		ns
$t_{OHZ}^{(1, 2, 3)}$	Output Disable to Valid Data In	10		12		ns

2

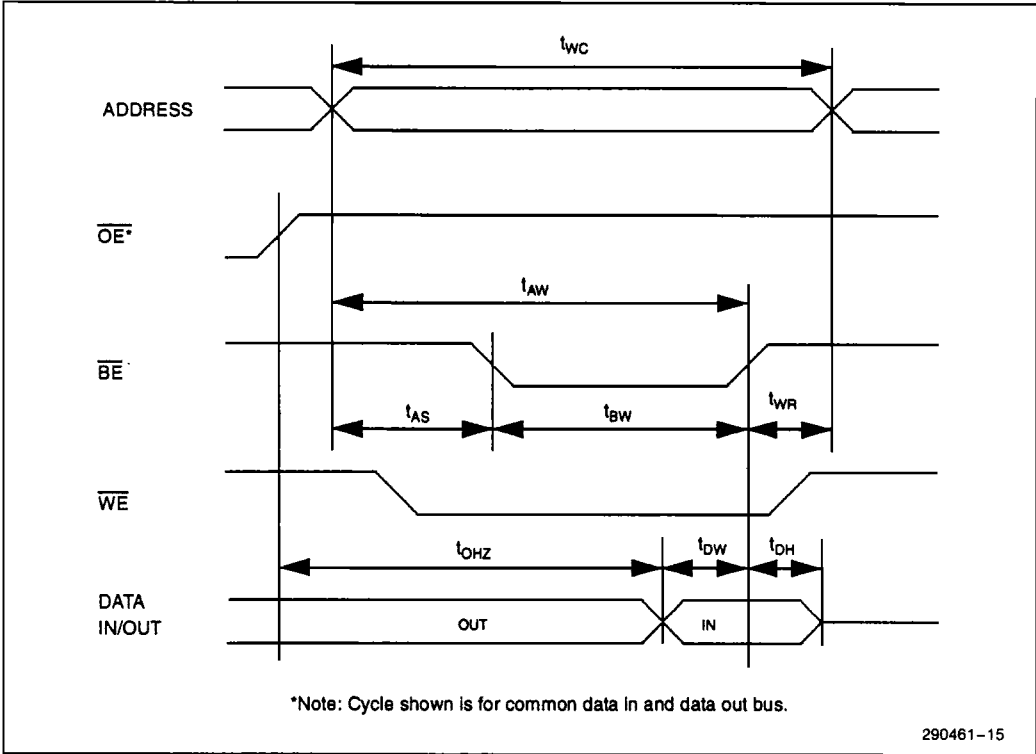
NOTES:

1. These signals are measured at $\pm 0.5\text{V}$ from steady state voltage as driven by specified output load. $Z \rightarrow H$ and $Z \rightarrow L$ are measured at 1.5V on output.
2. These signals are measured with $C_L = 5\text{ pF}$.
3. Does not apply for separate data in and data out buses.

TIMING WAVEFORM OF WRITE CYCLE #1 (\overline{WE} Controlled Timing)

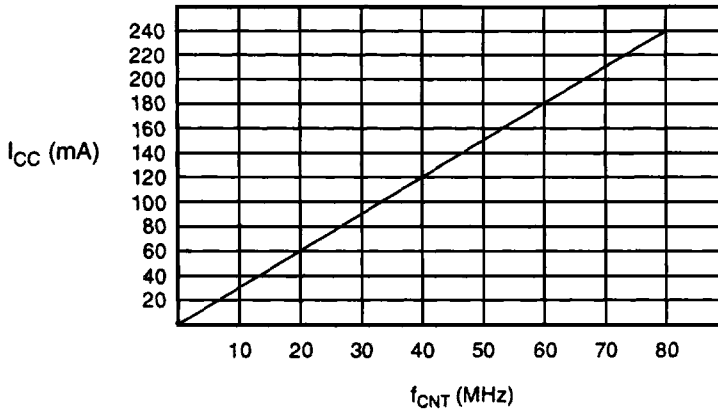


TIMING WAVEFORM OF WRITE CYCLE #2 (\overline{BE} Controlled Timing)



2

I_{CC} VERSUS FREQUENCY



Conditions: TA = +25°C, VCC = 5V
 (Note: Eight 20-bit counters)

290461-16

POWER-UP RESET

Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic. The power-up cycle is complete within a delay of t_{PR} after V_{CC} reaches the V_{ON} value.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state. The outputs on an unprogrammed device will power-up in a high impedance state.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t _{PR}	Power-Up Reset Time	100 μs Max
V _{ON}	Turn-On Voltage	4.75V Min

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

Pin Name	Description
V _{CC} ⁽¹⁾	Supply voltage for the iFX8160. All must be connected to 5V.
V _{SS}	Ground connections for the iFX8160. All must be connected to GND.
V _{PP} ⁽¹⁾	Programming voltage for the iFX8160. During programming, 12V must be supplied to this pin. When not in programming mode, this pin may be connected to V _{CC} , V _{PP} or left floating (not GND).
INx	Input only pins. These pins may not be available on all packages. Unused inputs should be connected to V _{CC} or GND.
TDI	The Testability Data Input is the boundary scan serial data input to the iFX8160. JTAG instructions and data are shifted into the iFX8160 on the TDI input pin on the rising edge of TCK. TDI may be left floating if unused.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX8160. JTAG instructions and data are shifted out of the iFX8160 on the TDO output on the falling edge of TCK.
TCK	The Testability Clock input provides the boundary scan clock for the iFX8160. TCK is used to clock state information and data into and out of the iFX8160 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz. TCK may be left floating if unused.
TMS	The Testability Control input is the boundary scan test mode select for the iFX8160. TMS may be left floating if unused.

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Table 5 lists the user-defined pin names and descriptions.

Table 5. User-Defined Pins

Pin Name	Description
V _{CC0x} ⁽¹⁾	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals. These pins must always be connected to the desired output drive voltage.
CLKx	Global clocks.
I/Oxx	Pins that can be configured either as an input or an output. Unused I/O pins should be connected to V _{CC} or GND.

NOTES:

1. Proper power decoupling is required on all power pins. A 0.01 μF decoupling capacitor is recommended between the power pin and ground.