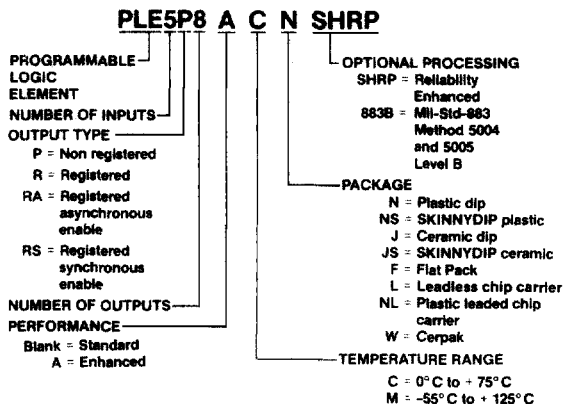# Programmable Logic Element PLE™ Family

Features/Benefits

- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- Expedites and simplifies prototyping and board layout
- Saves space with .3 inch SKINNYDIP® packages
- Programmed on standard PROM programmers
- Test and simulation made simple with PLEASM software
- Low-current PNP inputs
- Three-state outputs
- Reliable Ti-W fuses guarantee >98% programming yield

Ordering Information

PLE5P8 A C N SHRP

PROGRAMMABLE LOGIC ELEMENT

NUMBER OF INPUTS

OUTPUT TYPE
- P = Non registered
- R = Registered
- RA = Registered asynchronous enable
- RS = Registered synchronous enable

NUMBER OF OUTPUTS

PERFORMANCE
- Blank = Standard
- A = Enhanced

OPTIONAL PROCESSING
- SHRP = Reliability Enhanced
- 883B = Mil-Std-883 Method 5004 and 5005 Level B

PACKAGE
- N = Plastic dip
- NS = SKINNYDIP plastic
- J = Ceramic dip
- JS = SKINNYDIP ceramic
- F = Flat Pack
- L = Leadless chip carrier
- NL = Plastic leaded chip carrier
- W = Cerpak

TEMPERATURE RANGE
- C = 0°C to +75°C
- M = –55°C to +125°C

PLE Selection Guide

PART NUMBER	INPUTS	OUTPUTS	PRODUCT TERMS	OUTPUT REGISTERS	t_{PD} (ns) MAX *
PLE5P8	5	8	32		25
PLE5P8A	5	8	32		15
PLE8P4	8	4	256		30
PLE8P8	8	8	256		28
PLE9P4	9	4	512		35
PLE9P8	9	8	512		30
PLE10P4	10	4	1024		35
PLE11P4	11	4	2048		35
PLE11P8	11	8	2048		35
PLE12P4	12	4	4096		35
PLE12P8	12	8	4096		40
PLE9R8	9	8	512	8	15
PLE10R8	10	8	1024	8	15
PLE11RA8	11	8	2048	8	15
PLE11RS8	11	8	2048	8	15

* Clock to output time for registered outputs.

NOTE: Commercial limits specified.

PLE means Programmable Logic Element

Joining the world of IdeaLogic™ is a new generation of high-speed PROMs which the designer can use as *Programmable Logic Elements*. The combination of PLEs as logic elements with PALs can greatly enhance system speed while providing almost unlimited design freedom.

Basically, PLEs are ideal when a large number of product terms is required. On the other hand, a PAL is best suited for situations when many inputs are needed.

The PLE transfer function is the familiar OR of products. Like the PAL, the PLE has a single array of fusible links. Unlike the PAL, the PLE circuits have a programmable OR array driven by a fixed AND array (the PAL is a programmed AND array driving a fixed OR array).

PRODUCT TERM AND INPUT LINES

	PLE	PAL
Product Terms	32 to 4096	2 to 16
Input Lines	5 to 12	10 to 20

The PLE family features common electrical parameters and programming algorithm, low-current PNP inputs, full Schottky clamping and three-state outputs.

The entire PLE family is programmed on conventional PROM programmers with the appropriate personality cards and socket adapters.

Registered PLEs

The registered PLEs have on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{ES}$) enables are Low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{E}$ to a High or if $\overline{ES}$ is High when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

A flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin Low, one of the 16 initialize words, addressed through pins 5, 6, 7 and 8 will be set in the output registers independent of all other input pins. The unprogrammed state of $\overline{IS}$ words are Low, presenting a CLEAR with $\overline{IS}$ pin Low. With all $\overline{IS}$ column words (A3-A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed High a PRESET function is performed.

The PLE9R8 has asynchronous PRESET and CLEAR functions. With the chip enabled, a Low on the $\overline{PR}$ input will cause all outputs to be set to the High state. When the $\overline{CLR}$ input is set Low the output registers are reset and all outputs will be set to the Low state. The $\overline{PR}$ and $\overline{CLR}$ functions are common to all output registers and independent of all other data input states.

	AND	OR	OUTPUT OPTIONS
PLE	Fixed	Prog	TS, Registered Outputs, Fusible Polarity
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	Prog	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback I/O
PAL	Prog	Fixed	TS, Registered Feedback I/O Fusible Polarity

PLEASM™

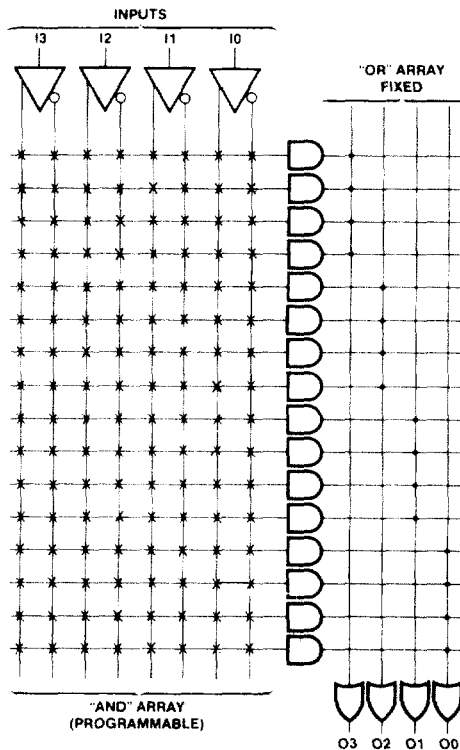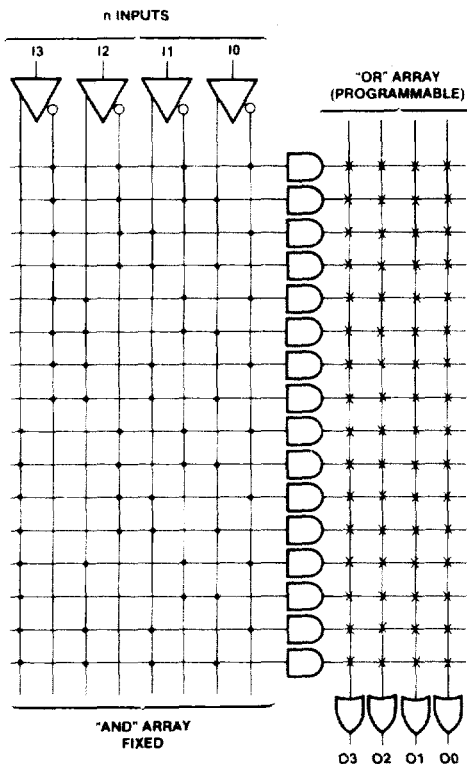### Software that makes programmable logic easy.

Monolithic Memories has developed a software tool to assist in designing and programming PROMs as PLEs. This package called "PLEASM" (PLE Assembler) is available for several computers including the VAX/VMS and IBM PC/DOS. PLEASM converts design equation (Boolean and arith-metic) into truth tables and formats compatible with PROM programmers. A simulator is also provided to test a design using a Function Table before actually programming the PLE.

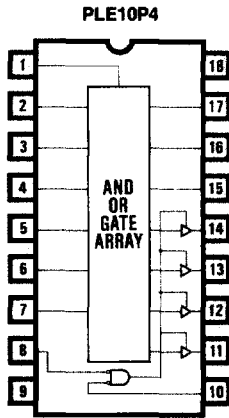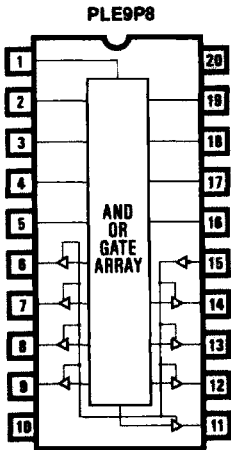PLEASM may be requested through the Monolithic Memories IdeaLogic Exchange.

PLE (PROM)

PAL

Note: ● = Hardwired connection
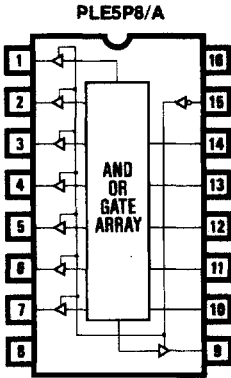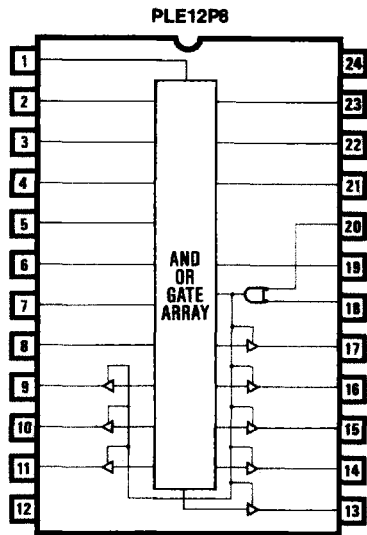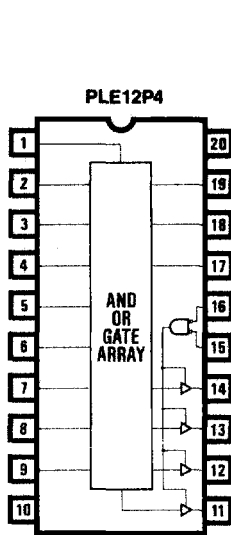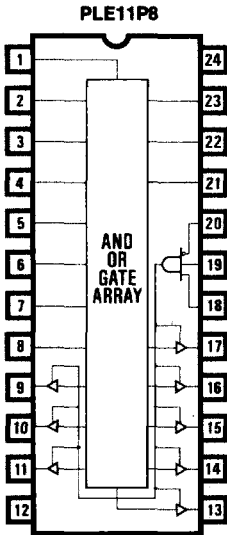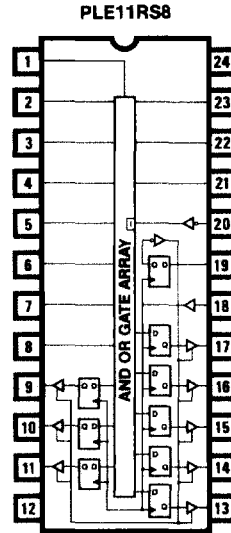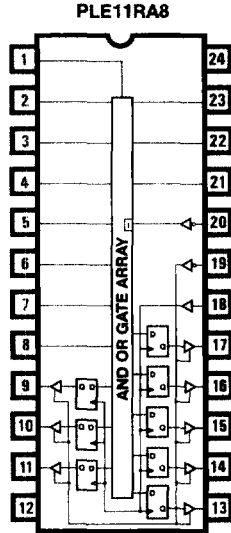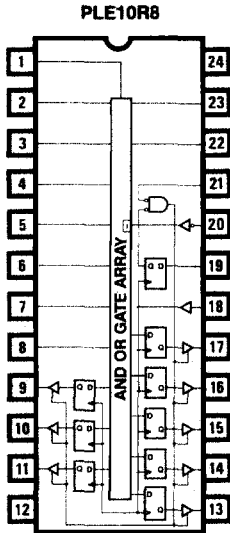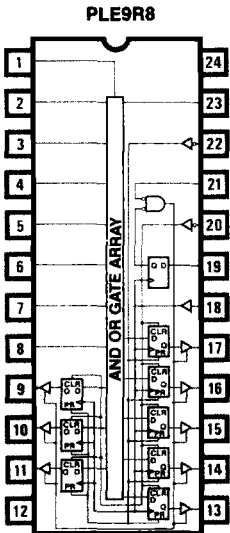X = Programmable fuse with a diode

Logic Symbols

PLE5P8/A

PLE8P4

PLE8P8

PLE9P4

PLE9P8

PLE10P4

PLE10P8

PLE11P4

Logic Symbols

PLE11P8

PLE12P4

PLE12P8

PLE9R8

PLE10R8

PLE11RA8

PLE11RS8
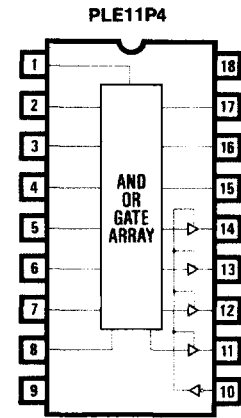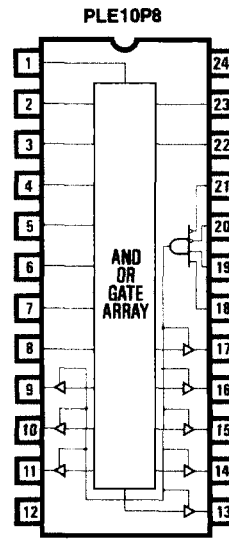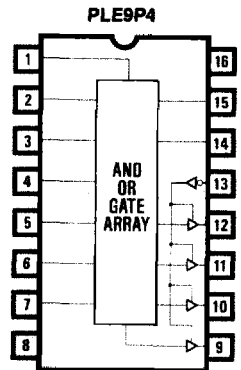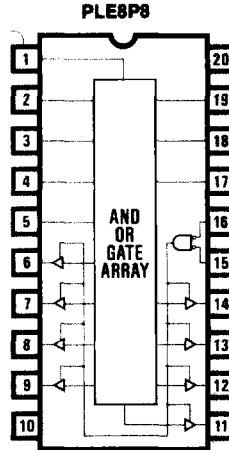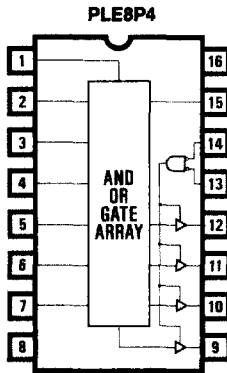
Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			MILITARY			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating free-air temperature	0	25	75	−55	25	125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP*	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	$V_I = V_{CC}$				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA	Com		0.3	.45	V
				Mil		0.3	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	Com I_{OH} = −3.2 mA		2.4	2.9		V
			Mil I_{OH} = −2 mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				−40	μA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5 V	V_O = 0 V		−20	−50	−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs TTL; all outputs open	5P8			90	125	mA
			5P8A			90	125	
			8P4			80	130	
			8P8			90	140	
			9P4			90	130	
			9P8			104	155	
			10P4			95	140	
			11P4			110	150	
			11P8			135	185	
			12P4			130	175	
			12P8			150	190	
			9R8			130	180	
			10R8			130	180	
			11RA8			140	185	
			11RS8			140	185	

* Typical at 5.0 V V_{CC} and 25° C T_A.

Switching Characteristics Over Military Operating Conditions

DEVICE TYPE	t_{PD} (ns) PROPAGATION DELAY MAX	t_{PZX} AND t_{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8AC	15	20
5P8C	25	20
8P4C	30	20
8P8C	28	25
9P4C	35	20
9P8C	30	25
10P4C	35	25
11P4C	35	25
11P8C	35	25
12P4C	35	25
12P8C	40	30

Switching Characteristics Over Commercial Operating Conditions

DEVICE TYPE	t_{PD} (ns) PROPAGATION DELAY MAX	t_{PZX} AND t_{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8M	35	30
8P4M	40	30
8P8M	40	30
9P4M	45	30
9P8M	40	30
10P4M	50	30
11P4M	50	30
11P8M	50	30
12P4M	50	30
12P8M	50	35

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN TYP* MAX			MILITARY MIN TYP* MAX			UNIT
t_w	Width of clock (High or Low)	20	10		20	10		ns
t_{prw} t_{clrw}	Width of preset or clear (Low) to Output (High or Low)	20	10		20	10		ns
t_{prr} t_{clrr}	Recovery from preset or clear (Low) to clock High	20	11		25	11		ns
t_{su}	Setup time from input to clock	30	22		35	22		ns
$t_s(\overline{ES})$	Setup time from $\overline{ES}$ to clock	10	7		15	7		ns
t_h	Hold time from input to clock	0	-5		0	-5		ns
$t_h(\overline{ES})$	Hold time from $\overline{ES}$ to clock	5	-3		5	-3		ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COMMERCIAL MIN TYP* MAX			MILITARY MIN TYP* MAX			UNIT
t_{CLK}	Clock to output delay		11	15		11	20	ns
t_{PR}	Preset to output delay		15	25		15	25	ns
t_{CLR}	Clear to output delay		18	25		18	35	ns
t_{PZX} (CLK)	Clock to output enable time		14	25		14	30	ns
t_{PXZ} (CLK)	Clock to output disable time		14	25		14	30	ns
t_{PZX}	Input to output enable time		10	20		10	25	ns
t_{PXZ}	Input to output disable time		10	20		10	25	ns

* Typical at 5.0 V V_{CC} and 25°C T_A.

Monolithic Memories

Definition of Waveforms

NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.

3. Input access measured at the 1.5 V level.

4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{PXZ} and t_{PZX}.

5. t_{PZX} and $t_{PZX(CLK)}$ are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			MILITARY			UNIT
		MIN	TYP*	MAX	MIN	TYP*	MAX	
t_W	Width of clock (High or Low)	20	10		20	10		ns
t_{su}	Setup time from input to clock (10R8)	30	25		40	25		ns
t_{su}	Setup time from input to clock (11RA8, 11RS8)	35	28		40	28		ns
t_s ($\overline{ES}$)	Setup time from $\overline{ES}$ to clock	15	7		15	7		ns
t_s ($\overline{IS}$)	Setup time from $\overline{IS}$ to clock	25	20		30	20		ns
t_h	Hold time input to clock	0	-5		0	-5		ns
t_h ($\overline{ES}$)	Hold time ($\overline{ES}$)	5	-3		5	-3		ns
t_h ($\overline{IS}$)	Hold time ($\overline{IS}$)	0	-5		0	-5		ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

| SYMBOL	PARAMETER	COMMERCIAL			MILITARY			UNIT
		MIN	TYP*	MAX	MIN	TYP*	MAX	
t_{CLK}	Clock to output delay		10	15		10	20	ns
t_{PZX} (CLK)	Clock to output enable time		17	25		17	30	ns
t_{PXZ} (CLK)	Clock to output disable time		17	25		17	30	ns
t_{PZX}	Input to output enable time		17	25		17	30	ns
t_{PXZ}	Input to output disable time		17	25		17	30	ns

* Typical at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms
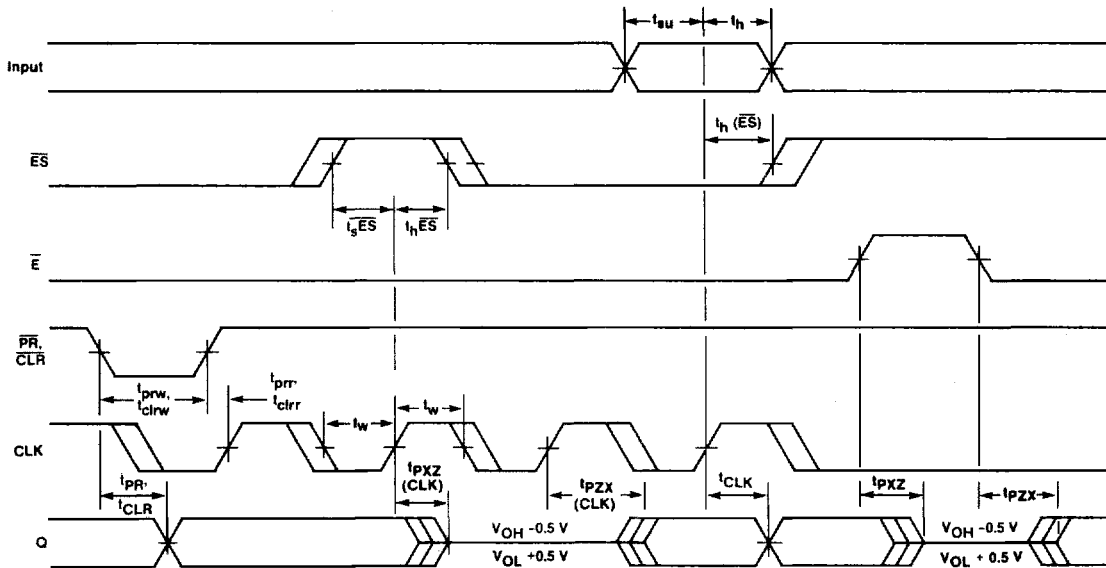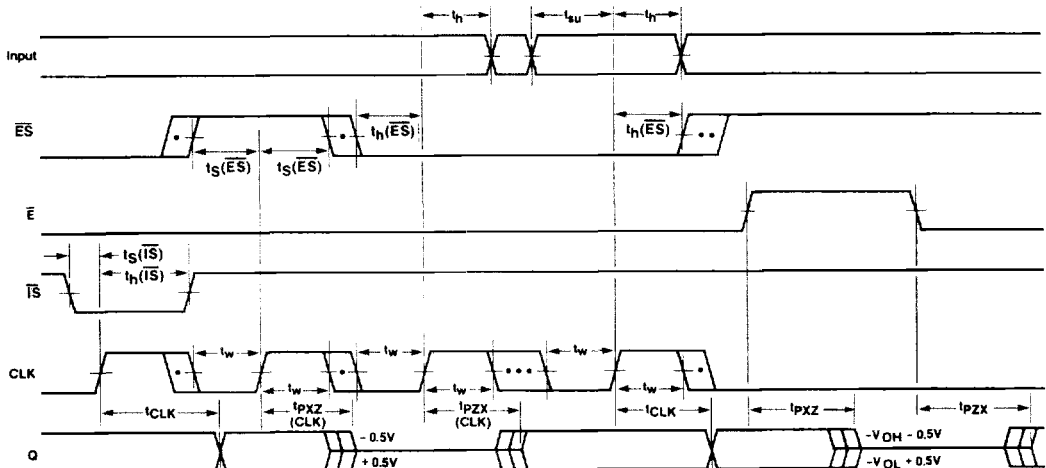
NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
3. Input access measured at the 1.5 V level.
4. Switch S_1 is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except t_{PZX} and t_{PXZ}.
5. t_{PZX} and $t_{PZX(CLK)}$ are measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5 V output level. S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5 V output level.
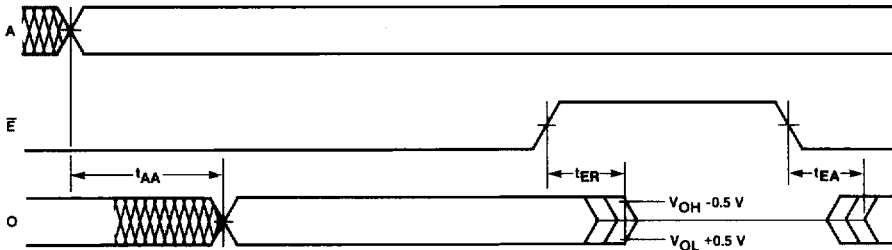
Switching Test Load
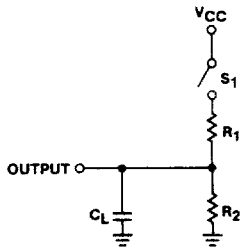
Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms

NOTES: Apply to electrical and switching characteristics

Typical at 5.0 V V_{CC} and 25° C T_A.

Measurements are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise.
In all PLE devices unused inputs must be tied to either ground or V_{CC}. The series resistor required for unused inputs on standard TTL is NOT required for PLE devices, thus using less parts.

*Not more than on output should be shorted at a time and duration of the short-circuit should not exceed one second.

1. For commercial operating range R_1 = 200Ω, R_2 = 390Ω. For military operating range R_1 = 300Ω. R_2 = 600Ω.

2. Input pulse amplitude 0 V to 3.0 V.

3. Input rise and fall times 2-5 ns from 0.8 to 2.0 V.

4. Input access measured at the 1.5 V level.

5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.

6. t_{PZX} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.
t_{PXZ} is measured C_L = 5 pF. S_1 is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high-impedance test measured at V_{OL} + 0.5 V output level.

PLE™ Family
Programming Instructions

Device Description

All of the members of the PLE family are manufactured with all outputs LOW in all storage locations. To produce a HIGH at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PLE only one output at a time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5 KΩ resistors.

Unless specified, Inputs should be at VIL.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100 ns or greater must be allowed between steps. The enabling pulse must not occur less than 100 ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/μs.

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. Following verification, apply five additional programming pulses to the bit being programmed.

Programming Parameters Do not test these parameters or you may program the device

SYMBOL	PARAMETER	RECOMMENDED			UNIT
		MIN	VALUE	MAX	
V_{CCP}	Required V_{CC} for programming	11.5	11.75	12.0	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μS
I_{CCP}	Current limit of V_{CCP} supply	800	1200		mA
I_{OP}	Current limit of V_{OP} supply	15	20		mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μS
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}		25	25	%
t_D	Delay time between programming steps	100	120		ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

Programming Equipment Suppliers

Monolithic Memories PLEs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine,

ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PLEs available can be made unreliable by improper programming techniques.

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson, TX 75081

4

Block Diagrams

PLE5P8/A
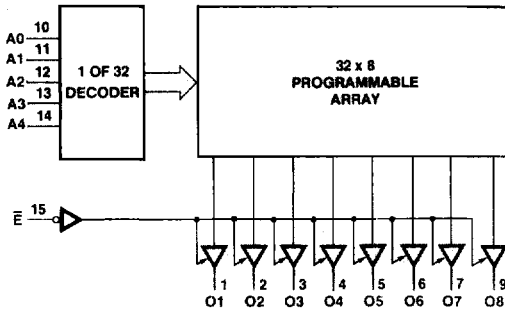
PLE8P4
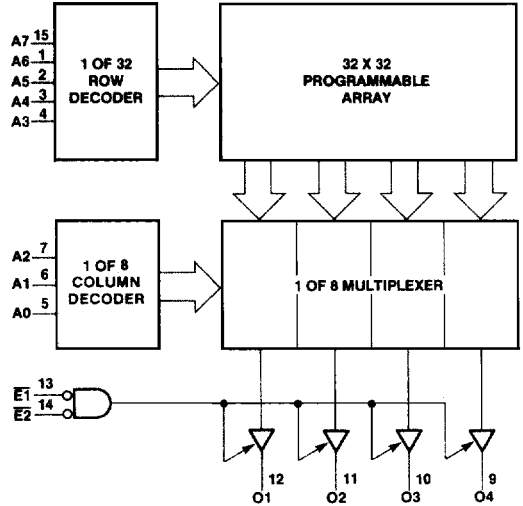
PLE8P8
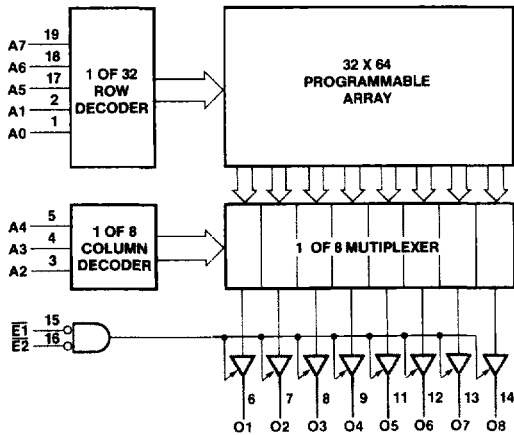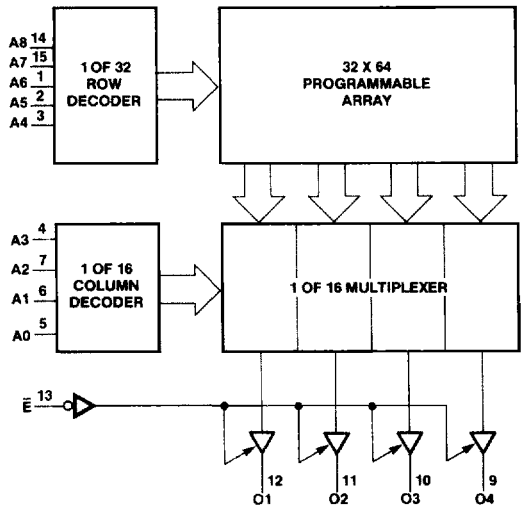
PLE9P4

Block Diagrams

PLE9P8

PLE10P4

PLE10P8

PLE11P4

Block Diagrams

PLE11P8

A10 21
A9 22
A8 23
A7 1
A6 2
A5 3
A4 4

1 OF 128 ROW DECODER

128x128 PROGRAMMABLE ARRAY

A3 5
A2 6
A1 7
A0 8

1 OF 16 COLUMN DECODER

1 OF 16 MULTIPLEXER

$\overline{E1}$ 20
E2 19
E3 18

9 10 11 13 14 15 16 17
O1 O2 O3 O4 O5 O6 O7 O8

PLE12P4

A11 17
A10 18
A9 19
A8 1
A7 2
A6 3
A5 4

1 OF 128 ROW DECODER

128 X 128 PROGRAMMABLE ARRAY

A4 5
A3 6
A2 7
A1 8
A0 9

1 OF 32 COLUMN DECODER

1 OF 32 MULTIPLEXER

$\overline{E1}$ 15
$\overline{E2}$ 16

14 13 12 11
O1 O2 O3 O4

PLE12P8

A11 19
A10 21
A9 22
A8 23
A7 1
A6 2
A5 3

1 OF 128 ROW DECODER

128 x 256 PROGRAMMABLE ARRAY

A4 4
A3 5
A2 6
A1 7

1 OF 16 COLUMN DECODER

2 OF 32 MULTIPLEXER

A0 8

1 OF 2 Z DECODER

Z MULTIPLEXER

$\overline{E1}$ 20
E2 18

9 10 11 13 14 15 16 17
O1 O2 O3 O4 O5 O6 O7 O8

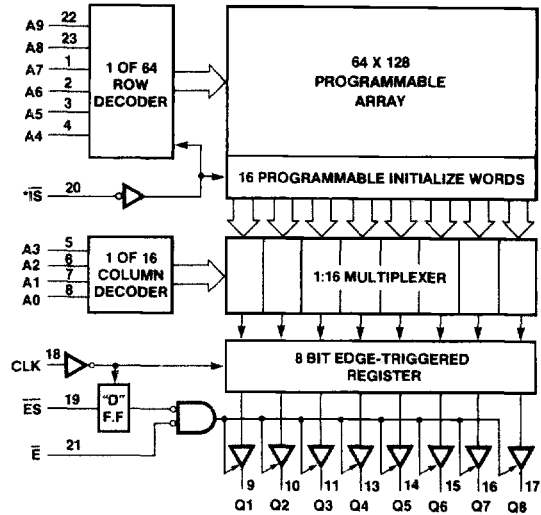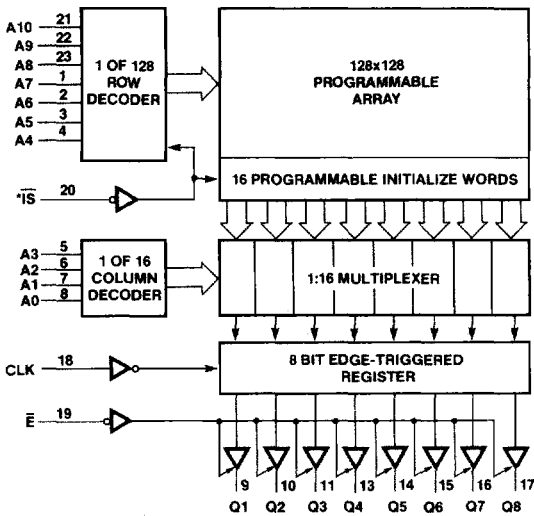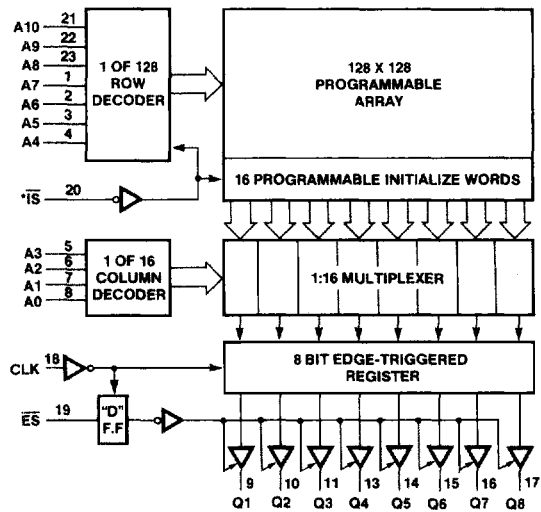## Block Diagrams

PLE9R8

PLE10R8

PLE11RA8

PLE11RS8

*IS selects 1:16 programmable initialization words.