

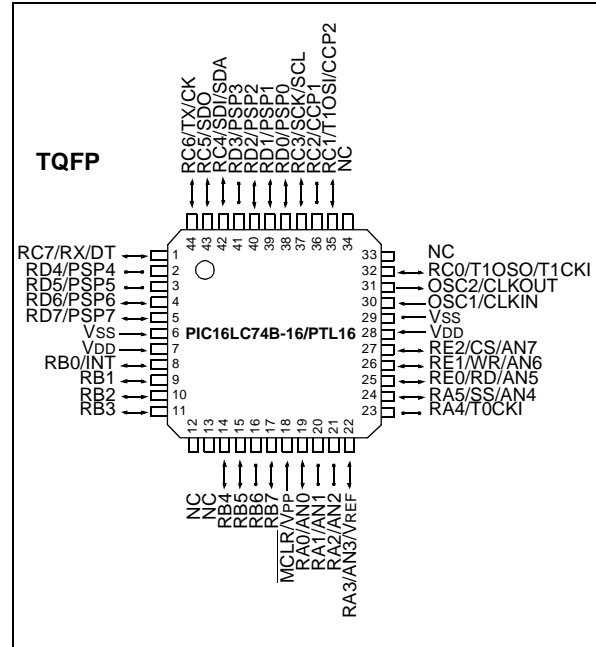
## 8-Bit CMOS Microcontrollers with A/D Converter

### PIC16LC74B-16/PTL16 Microcontroller Core

#### Features:

- High-performance RISC CPU
- Specially tested
  - 16MHz @ 3V
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 16 MHz clock input  
DC - 250 ns instruction cycle
- 4K x 14 words of Program Memory,  
192 x 8 bytes of Data Memory (RAM)
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM technology
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current 25/25 mA
- Commercial, Industrial and Automotive temperature ranges
- Low-power consumption:
  - < 5 mA @ 5V, 4 MHz
  - 23  $\mu$ A typical @ 3V, 32 kHz
  - < 3  $\mu$ A typical standby current

### Pin Diagram:



### Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module(s)
  - Capture is 16 bit, max. resolution is 15.6 ns
  - Compare is 16 bit, max. resolution is 250 ns
  - PWM max. resolution is 10 bit
- 8-bit multichannel analog-to-digital converter
- Synchronous Serial Port (SSP) with SPI™ and I<sup>2</sup>C™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP), 8-bits wide, with external RD, WR and CS controls
- Brown-out detection circuitry for Brown-out Reset (BOR) Pin Diagrams

# PIC16LC74B-16/PTL16

---

## Table of Contents

1.0 General Description .....	3
2.0 Electrical Characteristics.....	5
3.0 DC and AC Characteristics Graphs and Tables.....	27
4.0 Packaging Information .....	29
Index .....	33
On-Line Support.....	35
Reader Response .....	36
Product Identification System.....	37

### *To Our Valued Customers*

#### **Most Current Data Sheet**

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number. e.g., DS3000A is version A of document DS3000.

#### **Errata**

An errata sheet may exist for current devices, describing minor operational differences (from the data sheet) and recommended workarounds. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (602) 786-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

#### **Corrections to this Data Sheet**

We constantly strive to improve the quality of all our products and documentation. We have spent a great deal of time to ensure that this document is correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please:

- Fill out and mail in the reader response form in the back of this data sheet.
- E-mail us at [webmaster@microchip.com](mailto:webmaster@microchip.com).

We appreciate your assistance in making this a better document.

## 1.0 GENERAL DESCRIPTION

This data sheet covers the PIC16LC74B-16/PTL16 device. The functional characteristics of this device are identical to the PIC16LC74B. For electrical specifications, see the electrical specifications contained within this document. For all other information about this device, see the PIC16C63A/65B/73B/74B data sheet (DS30605).

# PIC16LC74B-16/PTL16

---

NOTES:

## 2.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Ambient temperature under bias .....	-55°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on any pin with respect to V <sub>SS</sub> (except V <sub>DD</sub> , $\overline{\text{MCLR}}$ , and RA4).....	-0.3V to (V <sub>DD</sub> + 0.3V)
Voltage on V <sub>DD</sub> with respect to V <sub>SS</sub> .....	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V <sub>SS</sub> (Note 2).....	0V to +13.25V
Voltage on RA4 with respect to V <sub>SS</sub> .....	0V to +8.5V
Total power dissipation (Note 1) .....	1.0W
Maximum current out of V <sub>SS</sub> pin .....	300 mA
Maximum current into V <sub>DD</sub> pin .....	250 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> ).....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> ) .....	±20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin .....	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined).....	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) .....	200 mA
Maximum current sunk by PORTC and PORTD (combined) .....	200 mA
Maximum current sourced by PORTC and PORTD (combined) .....	200 mA

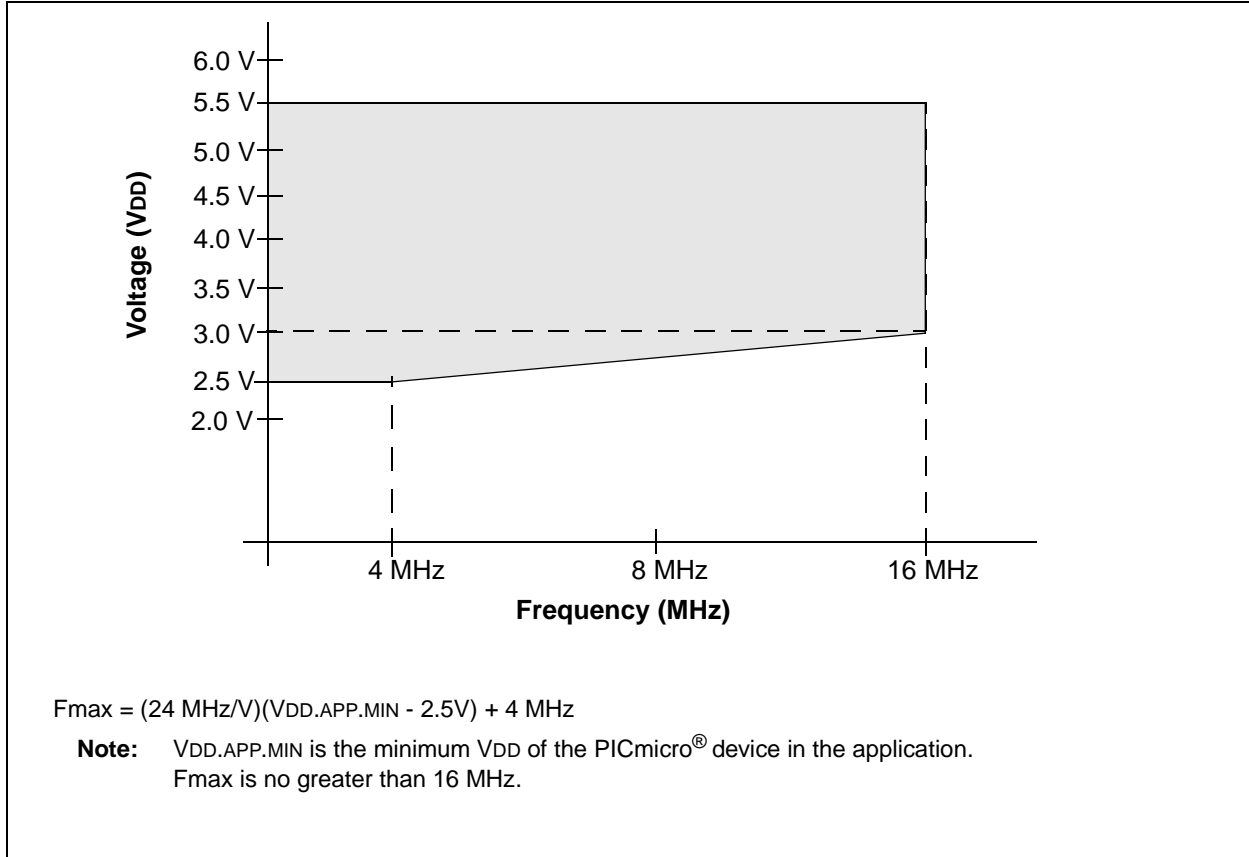
**Note 1:** Power dissipation is calculated as follows:  $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum \{V_{OL} \times I_{OL}\}$

**Note 2:** Voltage spikes below V<sub>SS</sub> at the  $\overline{\text{MCLR}}$ /V<sub>PP</sub> pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the  $\overline{\text{MCLR}}$ /V<sub>PP</sub> pin rather than pulling this pin directly to V<sub>SS</sub>.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device, at those or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC16LC74B-16/PTL16

FIGURE 2-1: PIC16LC74B-16/PTL16 VOLTAGE-FREQUENCY GRAPH



# PIC16LC74B-16/PTL16

## 2.1 DC Characteristics: PIC16LC74B-16/PTL-04 (Commercial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature 0°C ≤ TA ≤ +70°C for commercial					
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	<b>Supply Voltage</b>	2.5 VBOR*	- -	5.5 5.5	V V	RC, LP, XT, HS osc modes (DC - 4 MHz) BOR enabled (Note 7)
D002*	VDR	<b>RAM Data Retention Voltage</b> (Note 1)	-	TBD	-	V	
D003	VPOR	<b>VDD Start Voltage</b> to ensure internal Power-on Reset signal	-	VSS	-	V	
D004*	SVDD	<b>VDD Rise Rate</b> to ensure internal Power-on Reset signal	0.05	-	-	V/mS	PWRT enabled ( $\overline{\text{PWRT}}\text{E}$ bit clear)
D004A*			TBD	-	-	V/mS	PWRT disabled ( $\overline{\text{PWRT}}\text{E}$ bit set)
D005	VBOR	<b>Brown-out Reset</b> voltage trip point	3.65	-	4.35	V	BODEN bit set
D010	IDD	<b>Supply Current</b> (Note 2, 5)	-	2.0	3.8	mA	XT, RC osc modes FOSC = 4 MHz, VDD = 3.0V (Note 4)
			-	3.0	6.0	mA	HS oscillator mode Fosc = 16MHz, VDD = 3.0V
D010A			-	22.5	48	μA	LP osc mode FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D021	IPD	<b>Power-down Current</b> (Note 3, 5)	-	0.9	5	μA	VDD = 3.0V, WDT disabled, 0°C to +70°C
		<b>Module Differential Current</b> (Note 6)					
D022*	ΔIWDT	Watchdog Timer	-	6.0	20	μA	WDTE bit set, VDD = 4.0V
D022A*	ΔIBOR	Brown-out Reset	-	350	425	μA	BODEN bit set, VDD = 5.0V

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

**4:** For RC osc mode, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{ext}$  (mA) with Rext in kOhm.

**5:** Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

**6:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**7:** When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

# PIC16LC74B-16/PTL16

## 2.2 DC Characteristics: PIC16LC74B-16/PTL-04 (Commercial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial					
		Operating voltage $V_{DD}$ range as described in DC spec Section 2.1					
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033	$V_{IL}$	<b>Input Low Voltage</b> I/O ports with TTL buffer with Schmitt Trigger buffer $\overline{\text{MCLR}}$ , OSC1 (in RC mode) OSC1 (in XT, HS and LP modes)	$V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$	- - - - -	$0.15V_{DD}$ $0.8\text{V}$ $0.2V_{DD}$ $0.2V_{DD}$ $0.3V_{DD}$	V V V V V	For entire $V_{DD}$ range $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ Note1
D040 D040A D041 D042 D042A D043	$V_{IH}$	<b>Input High Voltage</b> I/O ports with TTL buffer with Schmitt Trigger buffer $\overline{\text{MCLR}}$ OSC1 (XT, HS and LP modes) OSC1 (in RC mode) <b>Input Leakage Current</b> (Notes 2, 3)	2.0 $0.25V_{DD} + 0.8\text{V}$ $0.8V_{DD}$ $0.8V_{DD}$ $0.7V_{DD}$ $0.9V_{DD}$	- - - - - -	$V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$	V V V V V V	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ For entire $V_{DD}$ range For entire $V_{DD}$ range Note1
D060 D061 D063	$I_{IL}$	I/O ports $\overline{\text{MCLR}}$ , RA4/T0CKI OSC1	- - -	- - -	$\pm 1$ $\pm 5$ $\pm 5$	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	$V_{SS} \leq V_{PIN} \leq V_{DD}$ , Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$ , XT, HS and LP osc modes
D070	IPURB	<b>PORTB weak pull-up current</b>	50	250	400	$\mu\text{A}$	$V_{DD} = 5\text{V}$ , $V_{PIN} = V_{SS}$
D080 D083	$V_{OL}$	<b>Output Low Voltage</b> I/O ports OSC2/CLKOUT (RC osc mode)	- - -	- - -	0.6 0.6 0.6 0.6	V V V V	$I_{OL} = 8.5\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $I_{OL} = 7.0\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ $I_{OL} = 1.6\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $I_{OL} = 1.2\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
D090	$V_{OH}$	<b>Output High Voltage</b> I/O ports (Note 3)	$V_{DD}-0.7$	-	-	V	$I_{OH} = -3.0\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the device be driven with external clock in RC mode.
- 2:** The leakage current on the  $\overline{\text{MCLR}}$ / $V_{PP}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.



## 2.2 DC Characteristics: PIC16LC74B-16/PTL-04 (Commercial) (Cont'd)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage $V_{DD}$ range as described in DC spec Section 2.1					
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D092		OSC2/CLKOUT (RC osc mode)	$V_{DD}-0.7$	-	-	V	$I_{OH} = -2.5\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
			$V_{DD}-0.7$	-	-	V	$I_{OH} = -1.3\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
			$V_{DD}-0.7$	-	-	V	$I_{OH} = -1.0\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
D150*	V <sub>OD</sub>	<b>Open-Drain High Voltage</b>	-	-	8.5	V	RA4 pin
		<b>Capacitive Loading Specs on Output Pins</b>					
D100	C <sub>osc2</sub>	OSC2 pin	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	C <sub>IO</sub>	All I/O pins and OSC2 (in RC mode)	-	-	50	pF	
D102	C <sub>b</sub>	SCL, SDA in I <sup>2</sup> C mode	-	-	400	pF	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the device be driven with external clock in RC mode.

**2:** The leakage current on the  $\overline{\text{MCLR}}/V_{PP}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

# PIC16LC74B-16/PTL16

## 2.3 AC (Timing) Characteristics

### 2.3.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

- |             |           |  |
|-------------|-----------|--|
| 1. TppS2ppS | 3. Tcc:ST | (I <sup>2</sup> C specifications only) |
| 2. TppS     | 4. Ts     | (I <sup>2</sup> C specifications only) |

<b>T</b>			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

<b>pp</b>			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

<b>S</b>			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
<b>I<sup>2</sup>C only</b>			
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:ST (I<sup>2</sup>C specifications only)

<b>CC</b>			
HD	Hold	SU	Setup
<b>ST</b>			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

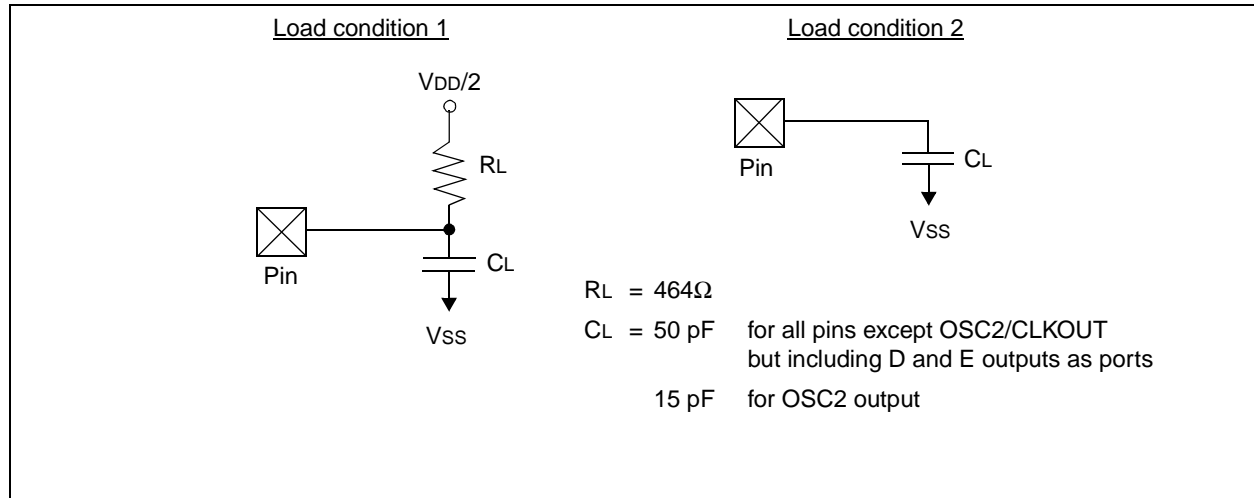
## 2.3.2 TIMING CONDITIONS

The temperature and voltages specified in Table 2-1 apply to all timing specifications unless otherwise noted. Figure 2-2 specifies the load conditions for the timing specifications.

**TABLE 2-1: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC**

<b>AC CHARACTERISTICS</b>	<b>Standard Operating Conditions (unless otherwise stated)</b>
	Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial
	Operating voltage $V_{DD}$ range as described in DC spec Section 2.1.
	LC parts operate for commercial/industrial temp's only.

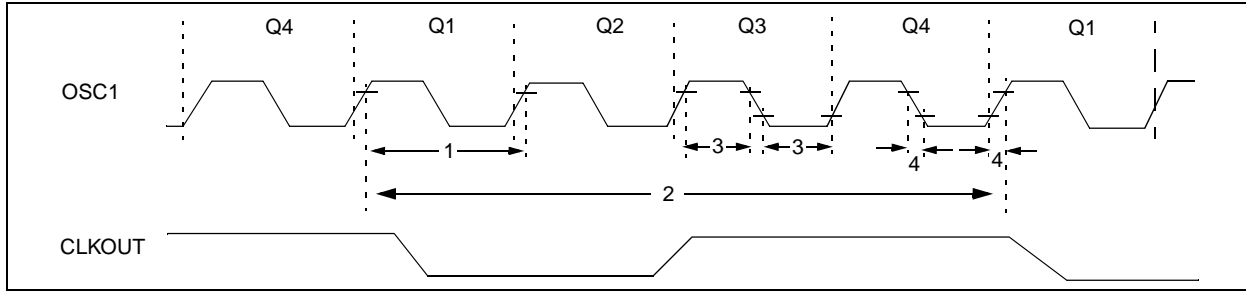
**FIGURE 2-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**



# PIC16LC74B-16/PTL16

## 2.3.3 TIMING DIAGRAMS AND SPECIFICATIONS

**FIGURE 2-3: EXTERNAL CLOCK TIMING**



**TABLE 2-2: EXTERNAL CLOCK TIMING REQUIREMENTS**

Param No.	Sym	Characteristic	Min (Note 2)	Typ†	Max (Note 3)	Units	Conditions
1A	Fosc	<b>External CLKIN Frequency</b> (Note 1)	DC	—	4	MHz	RC and XT osc modes
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		<b>Oscillator Frequency</b> (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	<b>External CLKIN Period</b> (Note 3)	250	—	—	ns	RC and XT osc modes
			250	—	—	ns	HS osc mode (-04)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
		<b>Oscillator Period</b> (Note 3)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			50	—	250	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
2	Tcy	<b>Instruction Cycle Time</b> (Note 1)	200	—	DC	ns	Tcy = 4/FOSC
3*	TosL, TosH	<b>External Clock in (OSC1) High or Low Time</b>	100	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR, TosF	<b>External Clock in (OSC1) Rise or Fall Time</b>	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

\* These parameters are characterized but not tested.

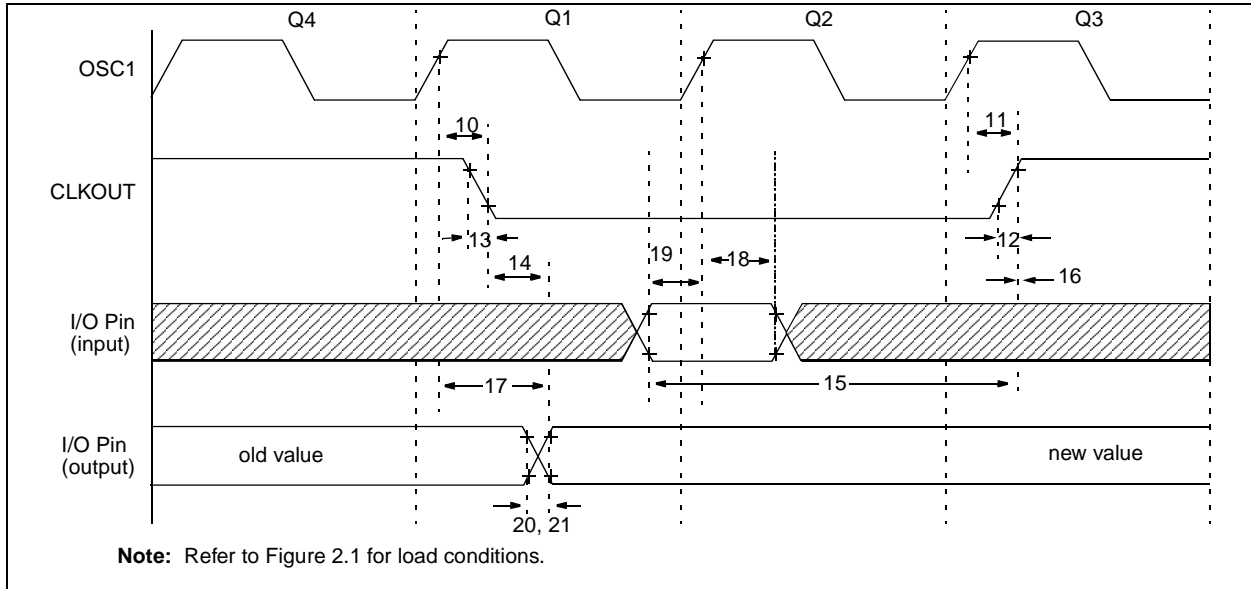
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

**2:** All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.

**3:** When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

**FIGURE 2-4: CLKOUT AND I/O TIMING**



**TABLE 2-3: CLKOUT AND I/O TIMING REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	Tosc + 200	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150	ns	
18A*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20A*	TioR	Port output rise time	—	—	80	ns	
21A*	TioF	Port output fall time	—	—	80	ns	
22††*	Tinp	INT pin high or low time	TCY	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time	TCY	—	—	ns	

\* These parameters are characterized but not tested.

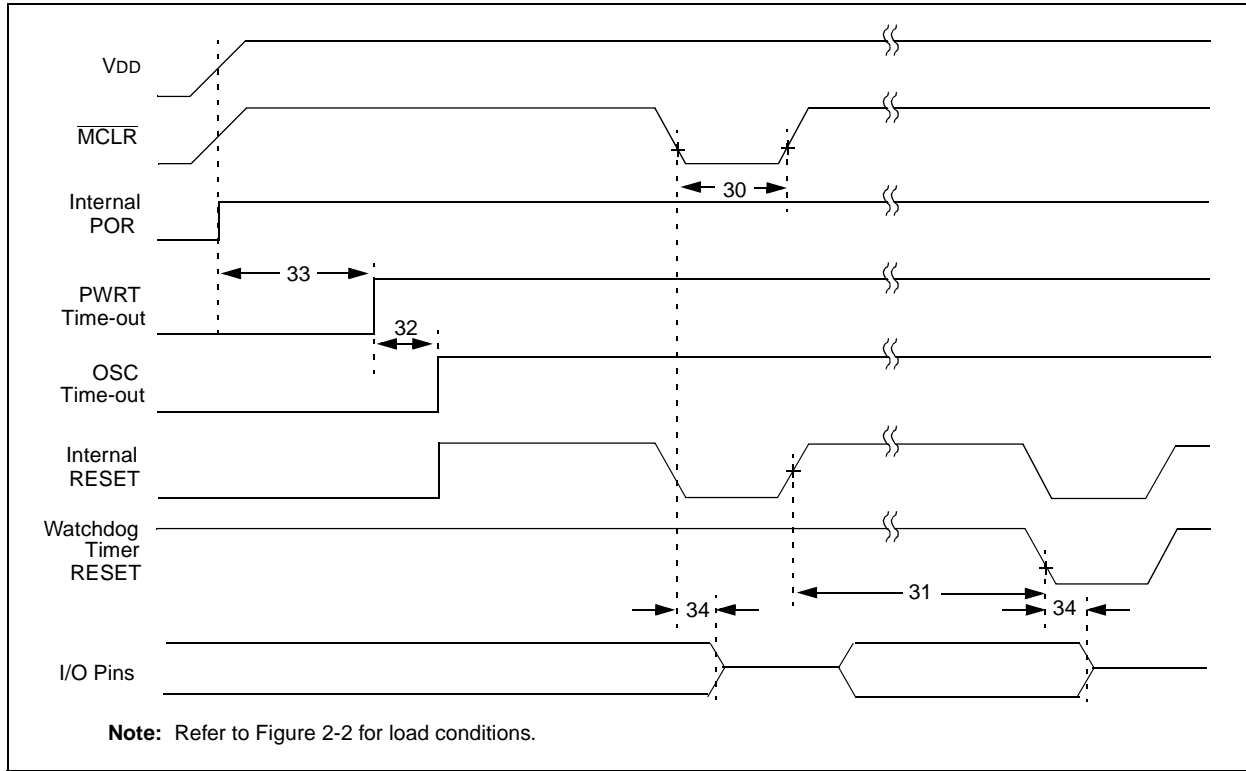
† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

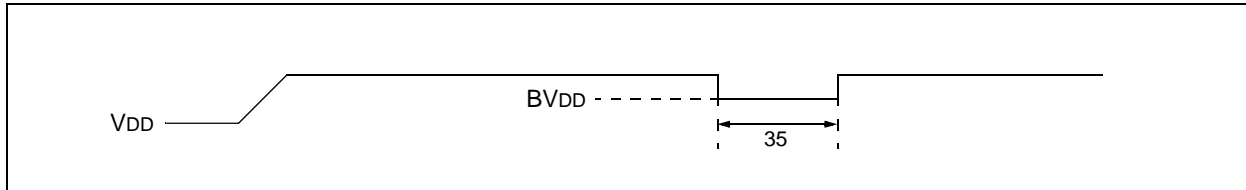
**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

# PIC16LC74B-16/PTL16

**FIGURE 2-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**FIGURE 2-6: BROWN-OUT RESET TIMING**



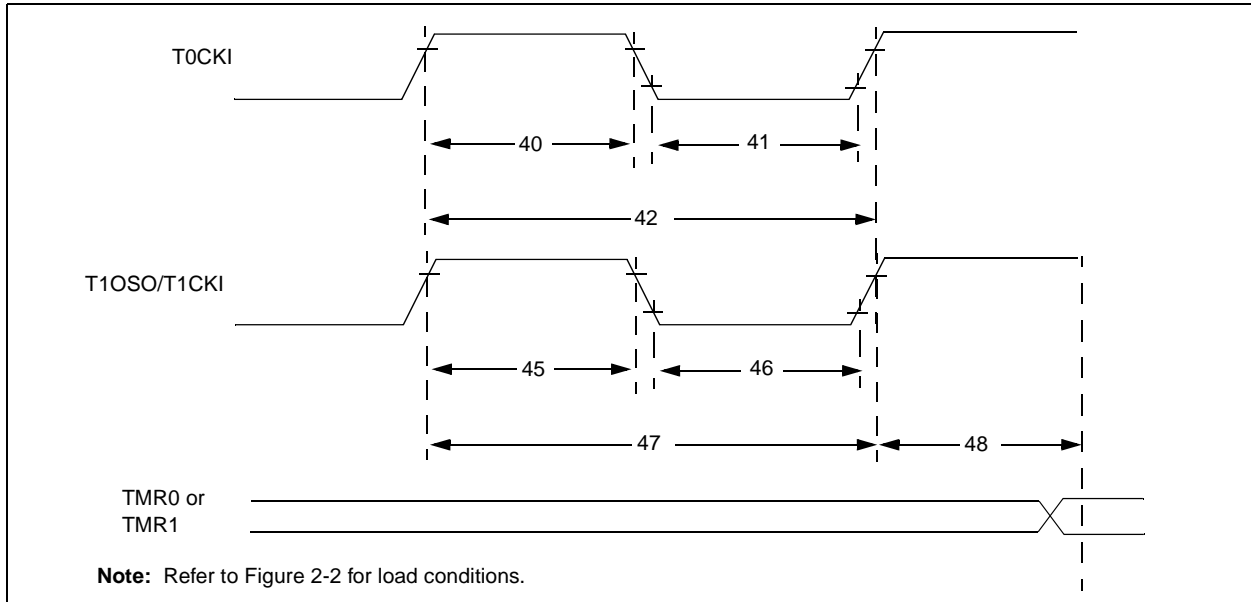
**TABLE 2-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from MCLR Low or WDT reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μs	VDD ≤ BVDD (D005)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 2-7: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS**



**TABLE 2-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS**

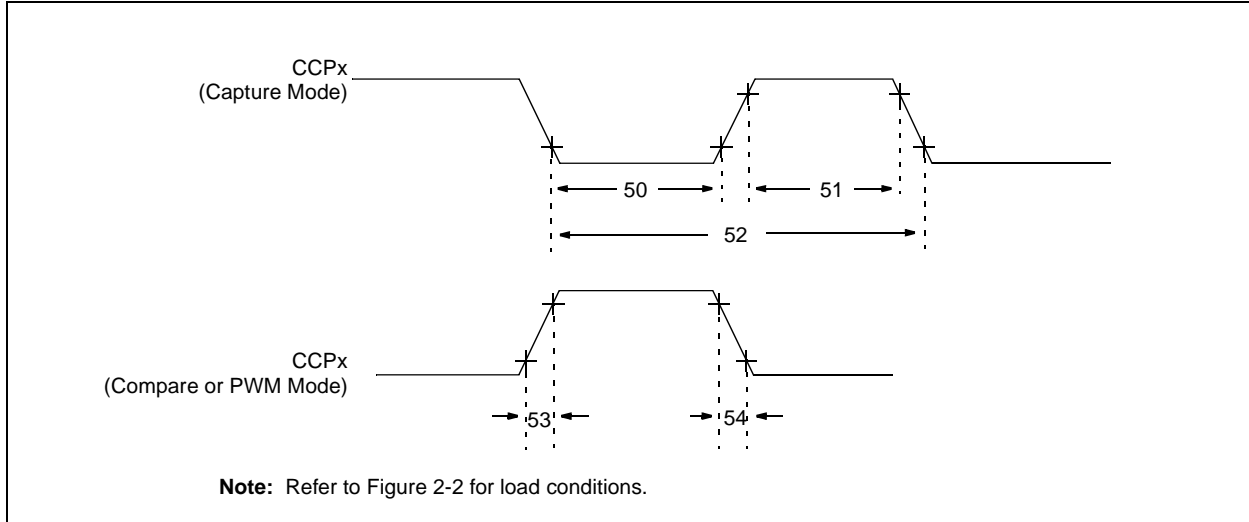
Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period	No Prescaler	$T_{CY} + 40$	—	—	ns	N = prescale value (2, 4, ..., 256)
			With Prescaler	Greater of: $20$ or $\frac{T_{CY} + 40}{N}$	—	—	ns	
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2, 4, 8	25	—	—	ns	
			Asynchronous	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2, 4, 8	25	—	—	ns	
			Asynchronous	50	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	Greater of: $50$ or $\frac{T_{CY} + 40}{N}$				N = prescale value (1, 2, 4, 8)
			Asynchronous	100	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment		$2T_{osc}$	—	$7T_{osc}$	—	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16LC74B-16/PTL16

**FIGURE 2-8: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)**



**TABLE 2-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)**

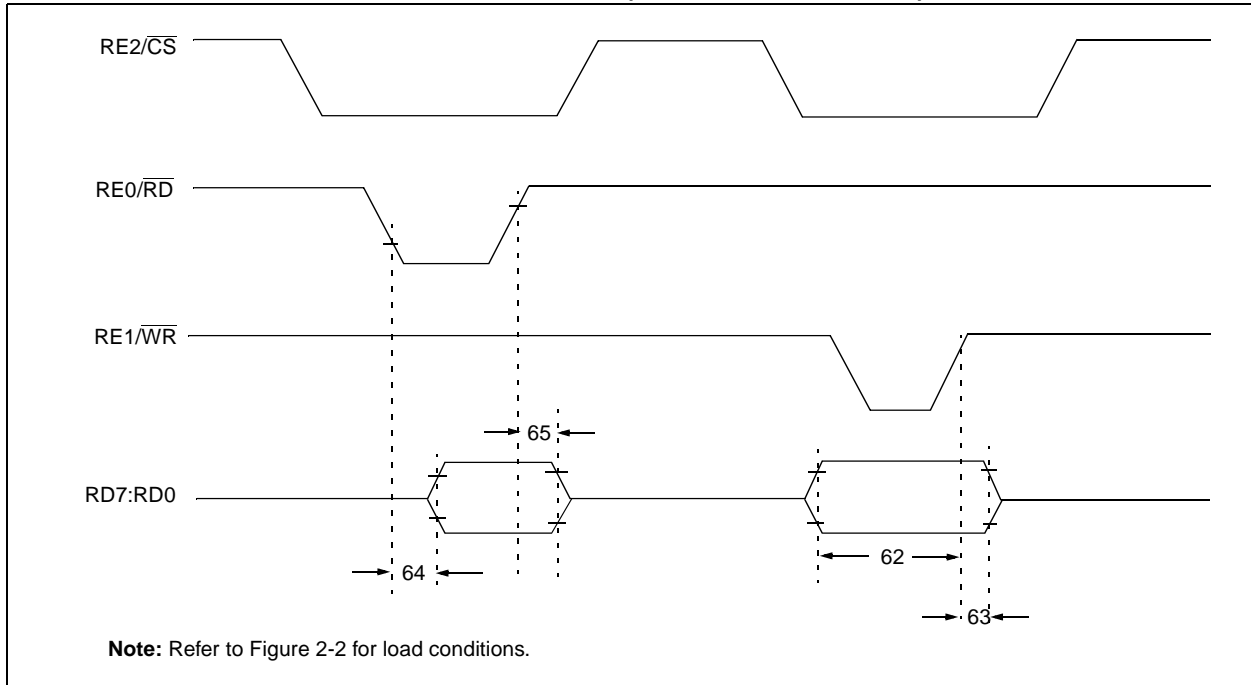
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2 input low time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns
		With Prescaler	20	—	—	ns	
51*	TccH	CCP1 and CCP2 input high time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns
		With Prescaler	20	—	—	ns	
52*	TccP	CCP1 and CCP2 input period	$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 and CCP2 output rise time	—	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time	—	25	45	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



**FIGURE 2-9: PARALLEL SLAVE PORT TIMING (PIC16LC74B-16/PTL16)**



**TABLE 2-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16LC74B-16/PTL16)**

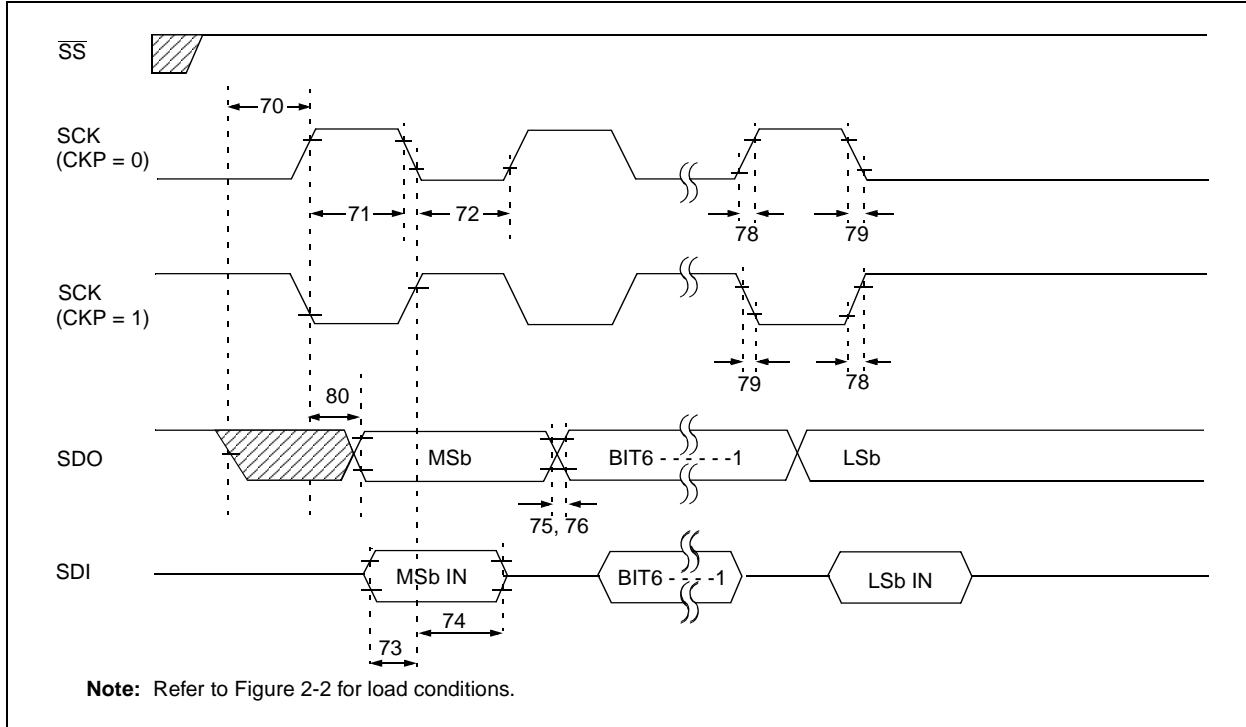
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time)	20	—	—	ns	
63*	TwrH2dtI	$\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data-in invalid (hold time)	35	—	—	ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data-out valid	—	—	80	ns	
65*	TrdH2dtI	$\overline{RD}\uparrow$ or $\overline{CS}\uparrow$ to data-out invalid	10	—	30	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16LC74B-16/PTL16

**FIGURE 2-10: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)**



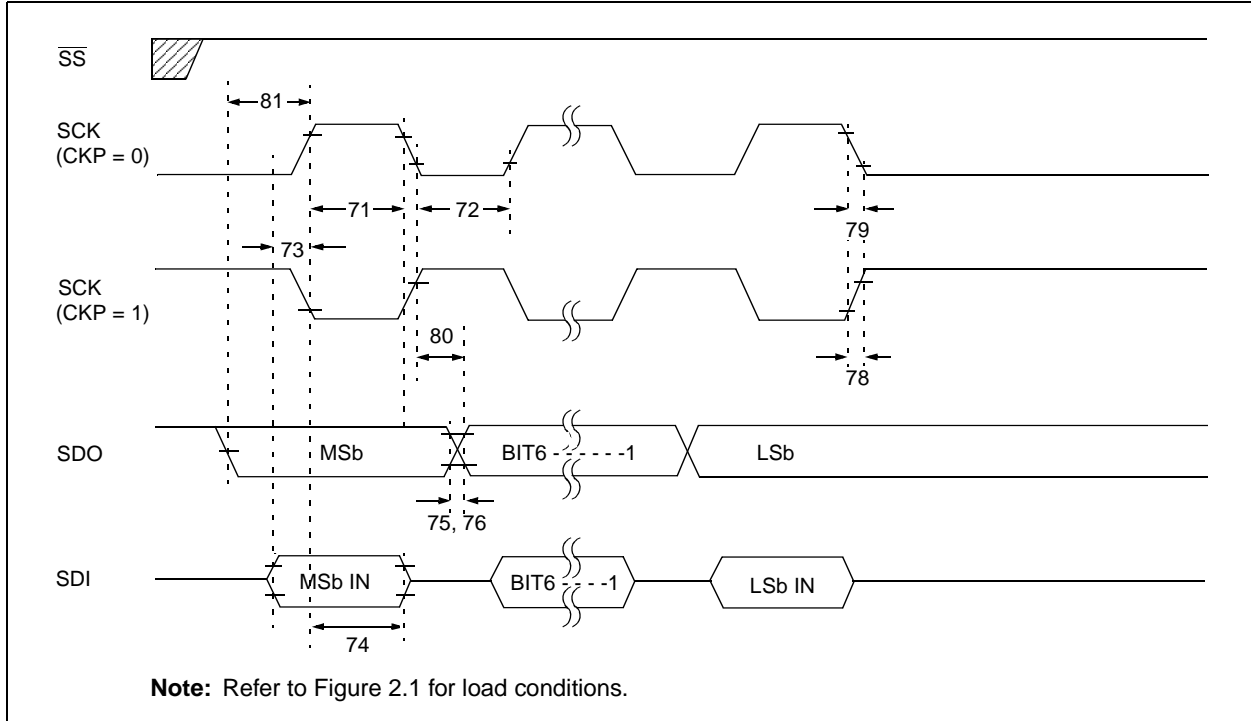
**TABLE 2-8: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)**

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions	
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	T <sub>CY</sub>	—	—	ns		
71	TscH	SCK input high time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns		
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5T <sub>CY</sub> + 40	—	—	ns	Note 1	
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns		
75	TdoR	SDO data output rise time	—	20	45	ns		
76	TdoF	SDO data output fall time	—	10	25	ns		
78	TscR	SCK output rise time (master mode)	—	20	45	ns		
79	TscF	SCK output fall time (master mode)	—	10	25	ns		
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	—	100	ns		

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

**FIGURE 2-11: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)**



**TABLE 2-9: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)**

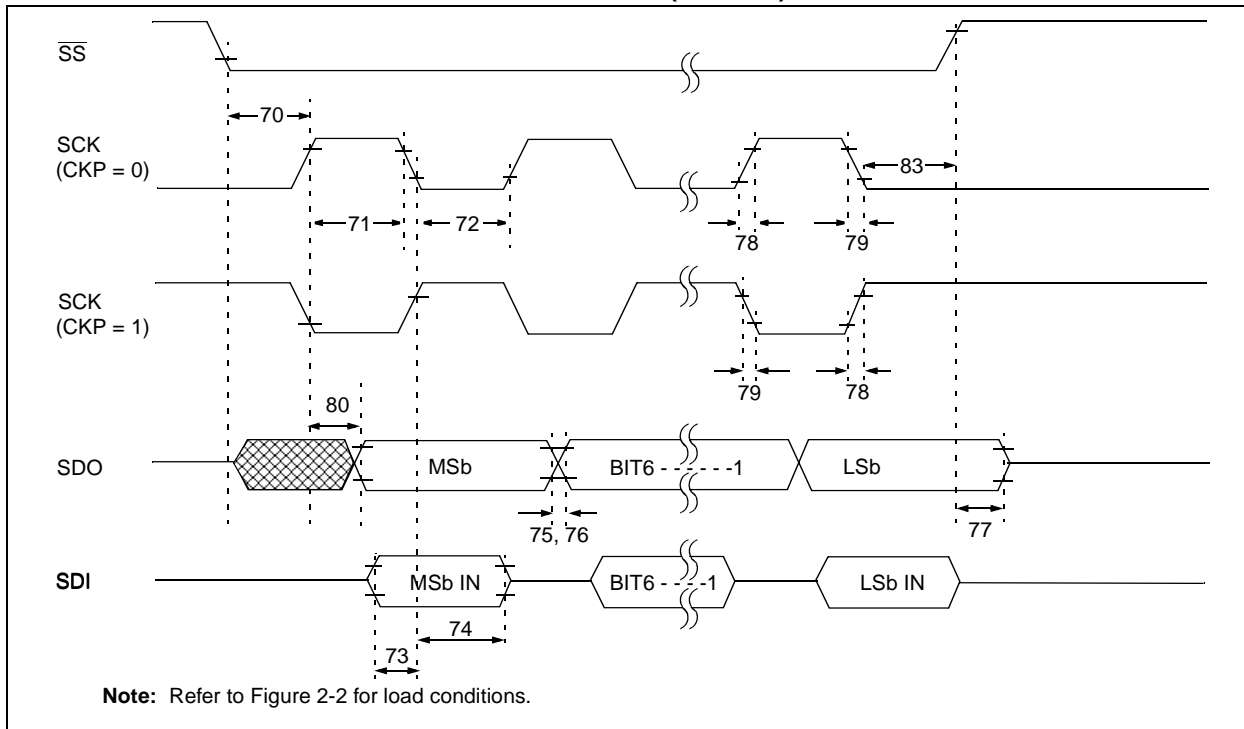
Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
71	Tsch	SCK input high time	1.25T <sub>CY</sub> + 30	—	—	ns	
71A		(slave mode)					
		Continuous	1.25T <sub>CY</sub> + 30	—	—	ns	
		Single Byte	40	—	—	ns	Note 1
72	Tscl	SCK input low time	1.25T <sub>CY</sub> + 30	—	—	ns	
72A		(slave mode)					
		Continuous	1.25T <sub>CY</sub> + 30	—	—	ns	
		Single Byte	40	—	—	ns	Note 1
73	TdiV2sch, TdiV2scl	Setup time of SDI data input to SCK edge	100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5T <sub>CY</sub> + 40	—	—	ns	Note 1
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75	TdoR	SDO data output rise time	—	20	45	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
78	TscR	SCK output rise time (master mode)	—	20	45	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	—	100	ns	
81	TdoV2sch, TdoV2scl	SDO data output setup to SCK edge	T <sub>CY</sub>	—	—	ns	

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

# PIC16LC74B-16/PTL16

**FIGURE 2-12: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)**



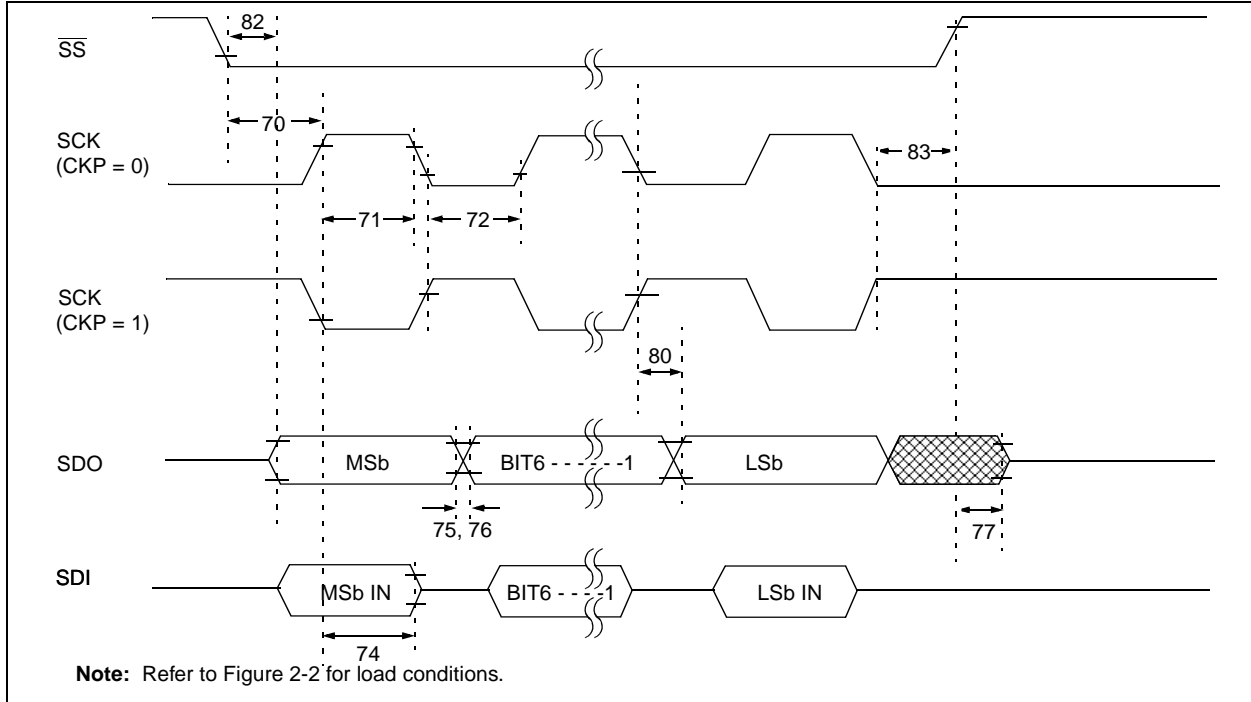
**TABLE 2-10: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0))**

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions	
70	TssL2sch, TssL2scl	SS↓ to SCK↓ or SCK↑ input	T <sub>CY</sub>	—	—	ns		
71	Tsch	SCK input high time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2sch, TdiV2scl	Setup time of SDI data input to SCK edge	100	—	—	ns		
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5T <sub>CY</sub> + 40	—	—	ns	Note 1	
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns		
75	TdoR	SDO data output rise time	—	20	45	ns		
76	TdoF	SDO data output fall time	—	10	25	ns		
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	—	50	ns		
78	TscR	SCK output rise time (master mode)	—	20	45	ns		
79	TscF	SCK output fall time (master mode)	—	10	25	ns		
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	—	100	ns		
83	Tsch2ssH, TscL2ssH	SS↑ after SCK edge	1.5T <sub>CY</sub> + 40	—	—	ns		

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

**FIGURE 2-13: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)**



**TABLE 2-11: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)**

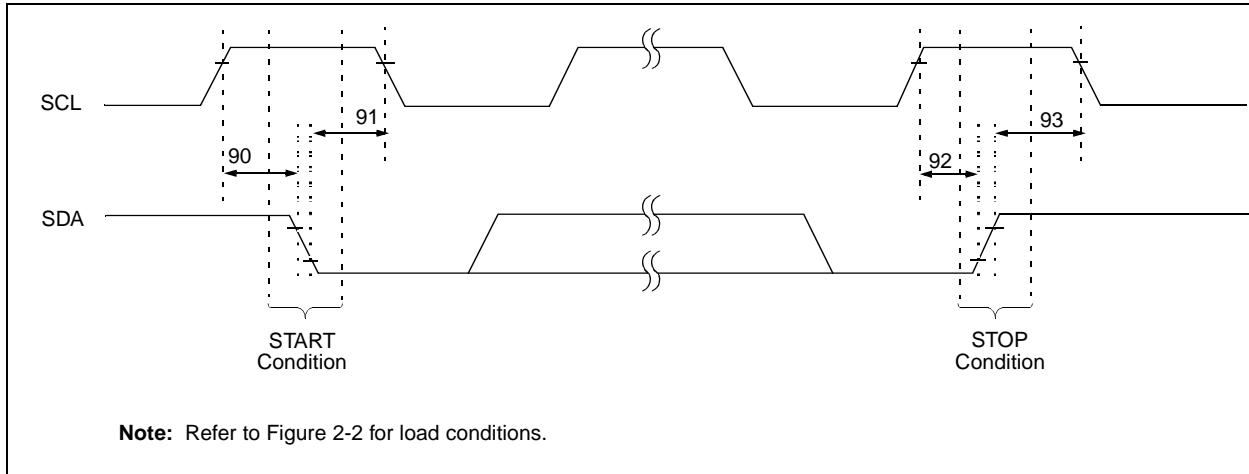
Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2sch, TssL2scL	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	$T_{CY}$	—	—	ns	
71	Tsch	SCK input high time (slave mode)	Continuous	$1.25T_{CY} + 30$	—	—	ns
71A			Single Byte	40	—	—	ns
72	TscL	SCK input low time (slave mode)	Continuous	$1.25T_{CY} + 30$	—	—	ns
72A			Single Byte	40	—	—	ns
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	$1.5T_{CY} + 40$	—	—	ns	Note 1
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75	TdoR	SDO data output rise time	—	20	45	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	—	20	45	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	—	100	ns	
82	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	—	—	100	ns	
83	Tsch2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge	$1.5T_{CY} + 40$	—	—	ns	

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

# PIC16LC74B-16/PTL16

**FIGURE 2-14: I<sup>2</sup>C BUS START/STOP BITS TIMING**

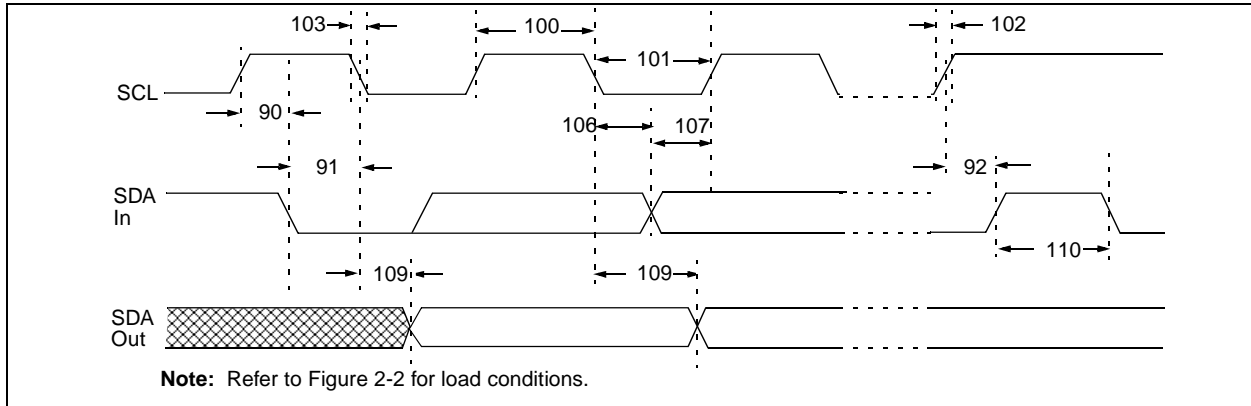


**TABLE 2-12: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
90*	T <sub>SU:STA</sub>	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91*	T <sub>HD:STA</sub>	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92*	T <sub>SU:STO</sub>	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	T <sub>HD:STO</sub>	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

\* These parameters are characterized but not tested.

**FIGURE 2-15: I<sup>2</sup>C BUS DATA TIMING**



**TABLE 2-13: I<sup>2</sup>C BUS DATA REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Max	Units	Conditions	
100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	μs	
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
	Cb	Bus capacitive loading	—	400	pF		

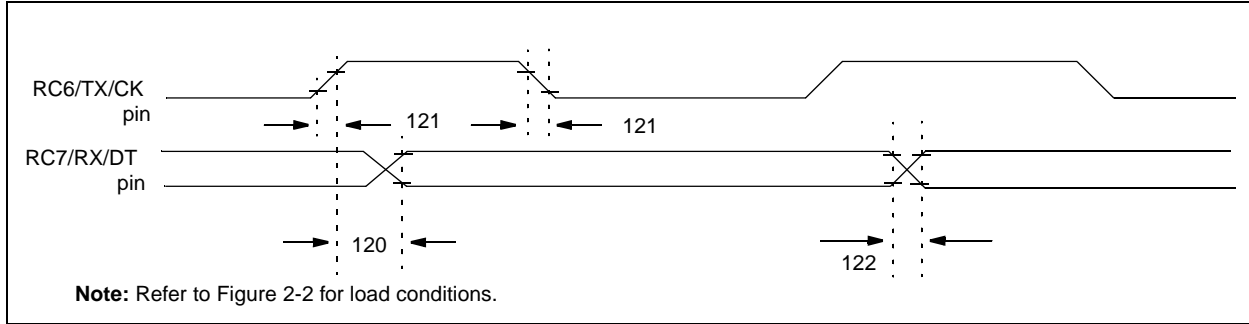
\* These parameters are characterized but not tested.

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**2:** A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line Tr max.+tsu; DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

# PIC16LC74B-16/PTL16

**FIGURE 2-16: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**



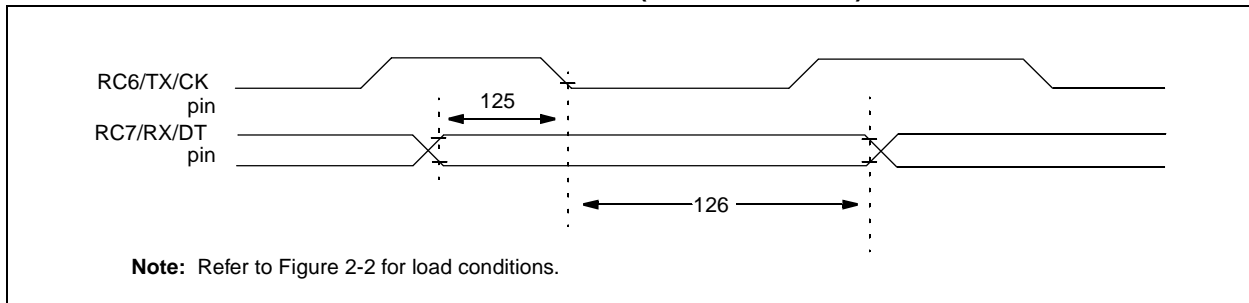
**TABLE 2-14: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	—	—	100	ns	
121*	Tckrf	Clock out rise time and fall time (Master Mode)	—	—	50	ns	
122*	Tdtrf	Data out rise time and fall time	—	—	50	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 2-17: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**



**TABLE 2-15: USART SYNCHRONOUS RECEIVE REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	—	—	ns	
126*	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



**TABLE 2-16: A/D CONVERTER CHARACTERISTICS: PIC16LC74B-16/PTL16-04 (COMMERCIAL)**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	8 bits	bit	VREF = VDD
A02	EABS	Total Absolute error	—	—	< ± 1	LSb	VREF = VDD VSS ≤ VAIN ≤ VREF
A03	EIL	Integral linearity error	—	—	< ± 1	LSb	VREF = VDD VSS ≤ VAIN ≤ VREF
A04	EDL	Differential linearity error	—	—	< ± 1	LSb	VREF = VDD VSS ≤ VAIN ≤ VREF
A05	EFS	Full scale error	—	—	< ± 1	LSb	VREF = VDD VSS ≤ VAIN ≤ VREF
A06	EOFF	Offset error	—	—	< ± 1	LSb	VREF = VDD VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity (Note 3)	—	guaranteed	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage	2.5V	—	VDD + 0.3	V	
A25	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	—	90	—	μA	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD
			—	—	10	μA	During A/D Conversion cycle

\* These parameters are characterized but not tested.

†Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

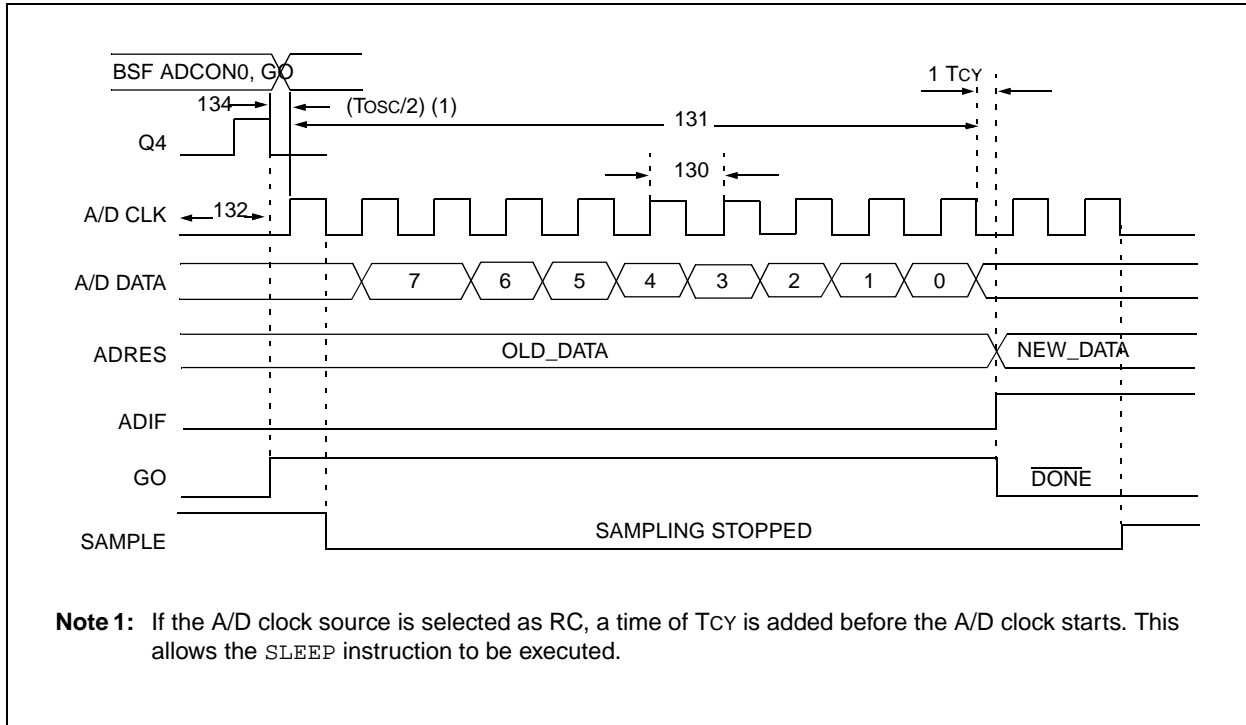
**Note 1:** When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

**2:** VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

**3:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

# PIC16LC74B-16/PTL16

**FIGURE 2-18: A/D CONVERSION TIMING**



**TABLE 2-17: A/D CONVERSION REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	2.0	—	—	$\mu\text{s}$	TOSC based, $V_{REF}$ full range
			3.0	6.0	9.0	$\mu\text{s}$	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)	11 Note 2	— 16	11 —	TAD $\mu\text{s}$	$V_{DD} = 3.0\text{V}$ , Temp. = $100^\circ\text{C}$ , $R_s = 10\text{K}\Omega$
132	TACQ	Acquisition time	5*	—	—	$\mu\text{s}$	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start	—	TOSC/2	—	—	If the A/D clock source is selected as RC, a time of $T_{CY}$ is added before the A/D clock starts. This allows the <code>SLEEP</code> instruction to be executed.
135	TSWC	Switching from convert $\rightarrow$ sample time	1.5 §	—	—	TAD	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V,  $25^\circ\text{C}$  unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** ADRES register may be read on the following  $T_{CY}$  cycle.

**Note 2:** See A/D section for minimum requirements.

## 3.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs and Tables not available at this time.

# PIC16LC74B-16/PTL16

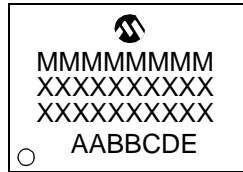
---

NOTES:

## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

44-Lead TQFP



Example

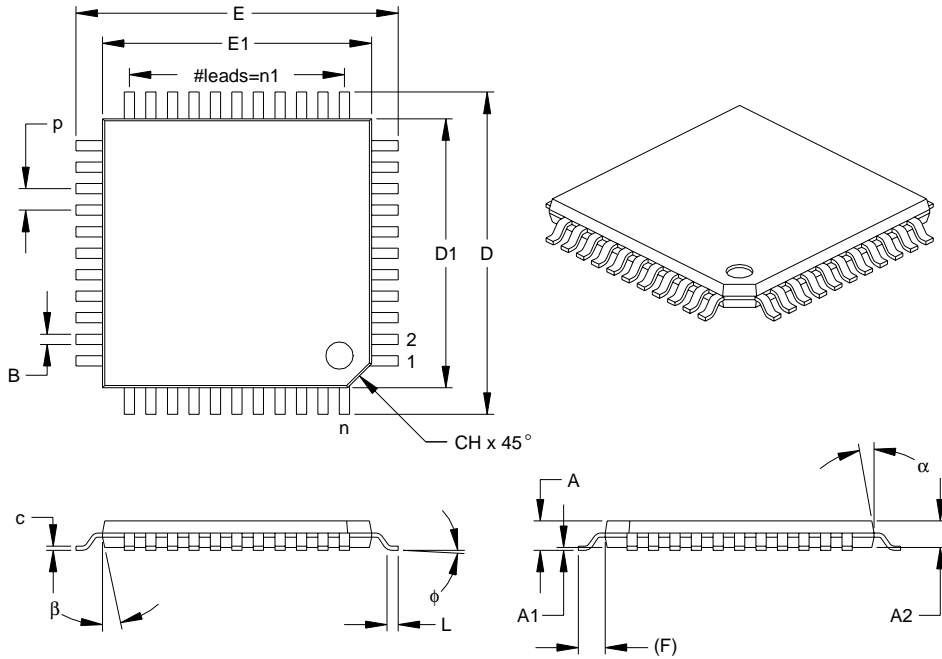


<b>Legend:</b>	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured
		O = Outside Vendor
		C = 5" Line
		S = 6" Line
		H = 8" Line
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

\* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

# PIC16LC74B-16/PTL16

## 44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	A	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039		1.00		
Foot Angle	$\phi$	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	$\alpha$	5	10	15	5	10	15
Mold Draft Angle Bottom	$\beta$	5	10	15	5	10	15

\*Controlling Parameter

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-026

Drawing No. C04-076

## APPENDIX A: REVISION HISTORY

Version	Date	Revision Description
A	6/99	This is a new data sheet providing the electrical specifications for the 3V, 16 MHz device. For all other information, see the PIC16C63A/65B/73B/74B data sheet (DS30605).

# PIC16LC74B-16/PTL16

---

NOTES:



## INDEX

### A

A/D	
Converter Characteristics .....	25
Timing Diagram .....	26
Absolute Maximum Ratings .....	5

### B

Brown-out Reset (BOR)	
Timing Diagram .....	14

### C

Capture/Compare/PWM (CCP)	
Timing Diagram .....	16

### D

DC Characteristics .....	8
--------------------------	---

### E

Electrical Characteristics .....	5
Errata .....	2

### G

General Description .....	3
---------------------------	---

### I

I <sup>2</sup> C (SSP Module)	
Timing Diagram, Data .....	23
Timing Diagram, Start/Stop Bits .....	22

### P

Packaging .....	29
Parallel Slave Port (PSP)	
Timing Diagram .....	17
Power-on Reset (POR)	
Timing Diagram .....	14
Product Identification System .....	37

### R

Reset	
Timing Diagram .....	14
Revision History .....	31

### T

Timer0	
Timing Diagram .....	15
Timer1	
Timing Diagram .....	15
Timing Diagrams and Specifications .....	12
A/D Conversion .....	26
Brown-out Reset (BOR) .....	14
Capture/Compare/PWM (CCP) .....	16
CLKOUT and I/O .....	13
External Clock .....	12
I <sup>2</sup> C Bus Data .....	23
I <sup>2</sup> C Bus Start/Stop Bits .....	22
Oscillator Start-up Timer (OST) .....	14
Parallel Slave Port (PSP) .....	17
Power-up Timer (PWRT) .....	14
Reset .....	14
Timer0 and Timer1 .....	15
USART Synchronous Receive ( Master/Slave) .....	24
USART Synchronous Transmission ( Master/Slave) ..	24
Watchdog Timer (WDT) .....	14

### U

USART	
Synchronous Master Mode	
Timing Diagram, Synchronous Receive .....	24
Timing Diagram, Synchronous Transmission ....	24

### W

Watchdog Timer (WDT)	
Timing Diagram .....	14
WWW, On-Line Support .....	2

# PIC16LC74B-16/PTL16

---

## ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

### Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

**[www.microchip.com](http://www.microchip.com)**

The file transfer site is available by using an FTP service to connect to:

**<ftp://ftp.microchip.com>**

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

## Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-602-786-7302 for the rest of the world.

981103

**Trademarks:** The Microchip name, logo, PIC, PICmicro, PICSTART, PICMASTER and PRO MATE are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries. *FlexROM*, *MPLAB* and *fuzzy-LAB* are trademarks and *SQTP* is a service mark of Microchip in the U.S.A.

All other trademarks mentioned herein are the property of their respective companies.

# PIC16LC74B-16/PTL16

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (602) 786-7578.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager Total Pages Sent  
RE: Reader Response  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: **PIC16LC74B-16/PTL16** Literature Number: **DS30026A**

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this data sheet easy to follow? If not, why?

---

---

4. What additions to the data sheet do you think would enhance the structure and subject?

---

---

5. What deletions from the data sheet could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

8. How would you improve our software, systems, and silicon products?

---

---

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-XX</u>	<u>X</u>	<u>/XX</u>	<u>L16</u>
Device	Frequency Range	Temperature Range	Package	Pattern
Device	PIC16LC7X <sup>(1)</sup> , PIC16LC7XT <sup>(2)</sup> ; V <sub>DD</sub> range 2.5V to 5.5V			
Frequency Range	04 = 4 MHz 16 = 16 MHz 20 = 20 MHz			
Temperature Range	blank = 0°C to 70°C (Commercial)			
Package	PT = TQFP (Thin Quad Flatpack)			
Pattern	QTP, SQTP, Code or Special Requirements L16 = 3V, 16 MHz			

**Examples:**

a) PIC16LC74B-16/PTL16 = Commercial temp., TQFP package, 16 MHz, low voltage V<sub>DD</sub> limits, QTP pattern #301.

**Note 1:** LC = Low Voltage CMOS  
**2:** T = in tape and reel - PLCC, QFP, TQFP packages only.

\* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

# PIC16LC74B-16/PTL16

---

NOTES:

NOTES:

---

---

**Note the following details of the code protection feature on PICmicro® MCUs.**

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

---

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*





# MICROCHIP

## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200 Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: <http://www.microchip.com>

#### Rocky Mountain

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7966 Fax: 480-792-7456

#### Atlanta

500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770-640-0034 Fax: 770-640-0307

#### Boston

2 Lan Drive, Suite 120  
Westford, MA 01886  
Tel: 978-692-3848 Fax: 978-692-3821

#### Chicago

333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 630-285-0071 Fax: 630-285-0075

#### Dallas

4570 Westgrove Drive, Suite 160  
Addison, TX 75001  
Tel: 972-818-7423 Fax: 972-818-2924

#### Detroit

Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250 Fax: 248-538-2260

#### Kokomo

2767 S. Albright Road  
Kokomo, Indiana 46902  
Tel: 765-864-8360 Fax: 765-864-8387

#### Los Angeles

18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888 Fax: 949-263-1338

#### New York

150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

#### China - Beijing

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Beijing Liaison Office  
Unit 915  
Bei Hai Wan Tai Bldg.  
No. 6 Chaoyangmen Beidajie  
Beijing, 100027, No. China  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Chengdu Liaison Office  
Rm. 2401, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-6766200 Fax: 86-28-6766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Fuzhou Liaison Office  
Unit 28F, World Trade Plaza  
No. 71 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7503506 Fax: 86-591-7503521

#### China - Shanghai

Microchip Technology Consulting (Shanghai)  
Co., Ltd.  
Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### China - Shenzhen

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Shenzhen Liaison Office  
Rm. 1315, 13/F, Shenzhen Kerry Centre,  
Renminnan Lu  
Shenzhen 518001, China  
Tel: 86-755-2350361 Fax: 86-755-2366086

#### Hong Kong

Microchip Technology Hongkong Ltd.  
Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaugnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-334-8870 Fax: 65-334-8850

### Taiwan

Microchip Technology Taiwan  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

Microchip Technology Nordic ApS  
Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
Tel: 45 4420 9895 Fax: 45 4420 9910

#### France

Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

01/18/02