



Micro Power Systems

MP7541

CMOS

Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- Full Four Quadrant Multiplication
- 12-Bit Linearity
- Guaranteed Monotonic; All Grades; All Temperatures.
- TTL/CMOS Compatible
- Stable, More Accurate Decoded Architecture
 - 2.0 ppm/°C Typ. Gain Error Tempco
 - 0.2 ppm/°C Max. Linearity Tempco
 - Lowest Sensitivity to Output Amplifier Offset
- Latch-Up Free
- PDIP, CDIP, SOIC Packages Available
- Use MP7541B for New Designs

APPLICATIONS

- Industrial Automation
- Automatic Test Equipment
- Disk Drive Servo Systems
- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratioetric A/D Conversion
- Function Generation
- Digitally Controlled Filters

GENERAL DESCRIPTION

The MP7541 is a 12-Bit Digital-to-Analog Converter which is manufactured using Micro Power Systems patented advanced thin film resistor and double metal CMOS process. The MP7541 incorporates a bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7541's outstanding features are:

Stability: Both Integral-Non-Linearity and Differential-Non-Linearity are rated at 0.2 ppm/°C maximum. Monotonicity is

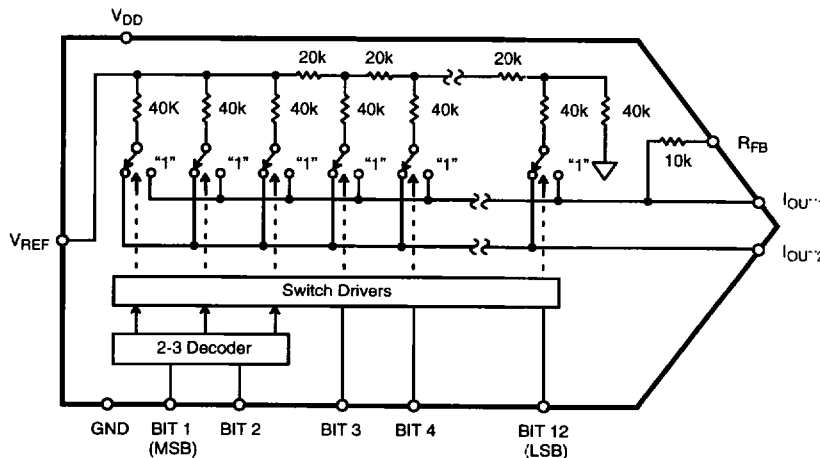
guaranteed over the entire temperature range. Gain Temperature Coefficient (TCGE) is 2.0 ppm/°C typical.

Lower Sensitivity to Output Amplifier Offset: Multiplying DACs provide an output current into a virtual ground of the output op amp. Additional linearity error caused by the op amp is reduced by a factor of 2 in the MP7541 versus conventional R-2R DACs.

Specified for operation over the commercial industrial (-40 to +85°C) and military (-55 to +125°C) temperature ranges, the MP7541 is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line and Surface Mount (SOIC) packages.

4

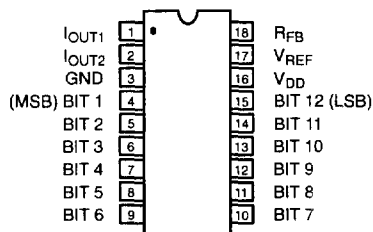
SIMPLIFIED BLOCK DIAGRAM



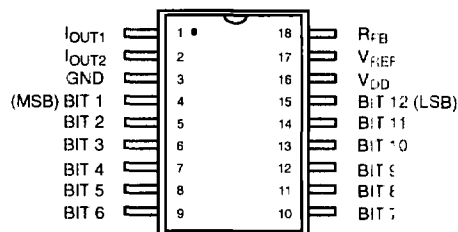
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSH)
Plastic Dip	-40 to +85°C	MP7541JN	±1	±1	±0.4
Plastic Dip	-40 to +85°C	MP7541KN	±1/2	±1	±0.4
SOIC	-40 to +85°C	MP7541JS	±1	±1	±0.4
SOIC	-40 to +85°C	MP7541KS	±1/2	±1	±0.4
Ceramic Dip	-40 to +85°C	MP7541AD	±1	±1	±0.4
Ceramic Dip	-40 to +85°C	MP7541BD	±1/2	±1	±0.4
Ceramic Dip	-55 to +125°C	MP7541SD	±1	±1	±0.4
Ceramic Dip	-55 to +125°C	MP7541SD/883	±1	±1	±0.4
Ceramic Dip	-55 to +125°C	MP7541TD	±1/2	±1	±0.4
Ceramic Dip	-55 to +125°C	MP7541TD/883	±1/2	±1	±0.4

PIN CONFIGURATIONS



18 Pin PDIP, CDIP (0.300")
N18, D18



18 Pin SOIC (Jedec, 0.300")
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I _{OUT1}	Current Output 1
2	I _{OUT2}	Current Output 2
3	GND	Ground
4	BIT1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6

PIN NO.	NAME	DESCRIPTION
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12 (LSB)
16	V _{DD}	Positive Power Supply
17	V _{REF}	Reference Input voltage
18	R _{FB}	Internal Feedback Resistor



ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C			T _{min} to T _{max}		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
STATIC PERFORMANCE (1)								
Resolution (All Grades)	N	12			12		Bits	FSR = Full Scale Range
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1			±1	
K, B, T				±1/2			±1/2	
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range
J, A, S				±1			±1	
K, B, T				±1			±1	
Non-Linearity Tempco (2)							±0.2	ppm/°C
Gain Error	GE			±0.4			±0.4	% FSR Using Internal R _{FB}
Gain Temperature Coefficient (2)	TC _{GE}						±2	ppm/°C ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100			±200	ppm/% ΔGain/ΔV _{DD} ΔV _{DD} = ±5%
Output Leakage Current	I _{OUT}			±50			±200	nA
DYNAMIC PERFORMANCE (2)								
Current Settling Time	I _S		0.5	1			μs	Full Scale Change to 1/2 LSB
AC Feedthrough at I _{OUT1}	F _T			1			mV p-p	V _{REF} = 10kHz, 20 th p-p sinewave
REFERENCE INPUT								
Input Resistance	R _{IN}	5		20	5	20	kΩ	
DIGITAL INPUTS (3)								
Logical "1" Voltage	V _{IH}	2.4			2.4			V
Logical "0" Voltage	V _{IL}			0.8		0.8		V
Input Leakage Current	I _{LKG}			±1		±1		μA
Input Capacitance (2) Data	C _{IN}			8				pF
ANALOG OUTPUTS								
Output Capacitance (2)	C _{OUT1}			52				pF
	C _{OUT1}			26				pF
	C _{OUT2}			13				pF
	C _{OUT2}			45				pF
POWER SUPPLY (4)								
Functional Voltage Range (2)	V _{DD}	4.5		16	4.5	16		V
Supply Current	I _{DD}			2		2		mA

4

NOTES:

- (1) Full Scale Range (FSR) is 10V for unipolar mode.
- (2) Guaranteed but not production tested.
- (3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- (4) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

MP7541



ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

V _{DD} to GND	+17 V	Storage Temperature	-65°C to +150°C
Digital Input Voltage to GND	GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds)	+300°C
I _{OUT1} , I _{OUT2} to GND	GND -0.5 to V _{DD} +0.5 V	Package Power Dissipation Rating to 75°C		
V _{REF} to GND	±25 V	CDIP, PDIP, SOIC	850mW
V _{RFB} to GND	±25 V	Derates above 75°C	11mW/°C

NOTES:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 20mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information