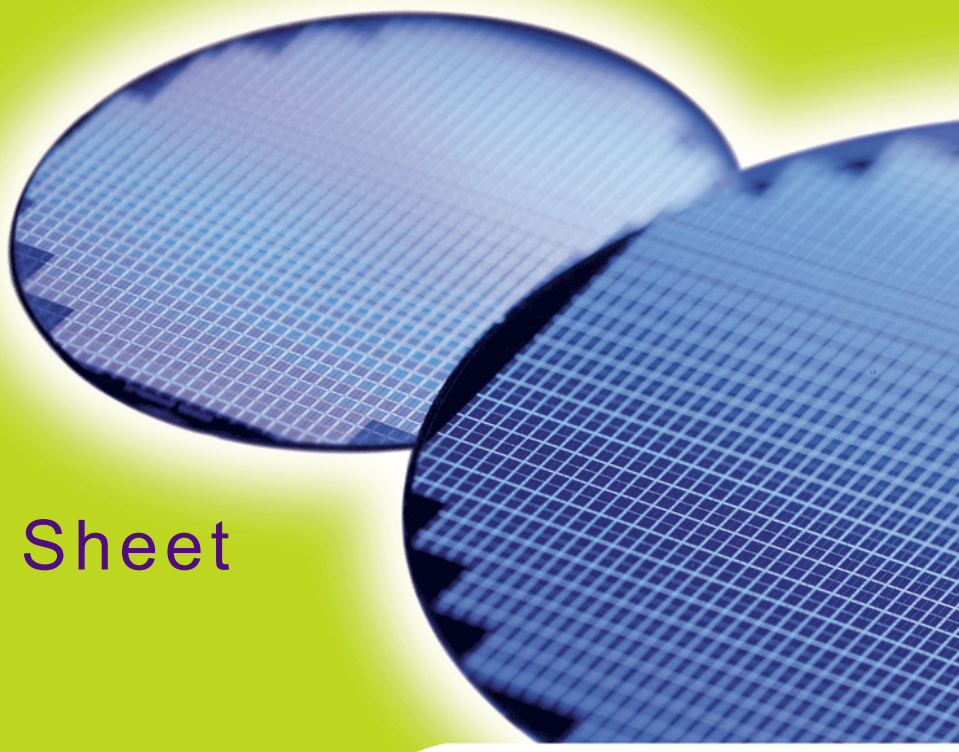
January 2008

IMSH4GP12A1F2C
IMSH4GP23A1F2C
IMSH8GP22A1F2C

240-Pin DDR3 Registered Modules with Parity bit
4 GByte and 8 GByte
RoHS compliant



Advance

Internet Data Sheet

Rev. 0.50

www.qimonda.com

IMSH4GP12A1F2C, IMSH4GP23A1F2C, IMSH8GP22A1F2C Revision History: 2008-01, Rev. 0.50	
Page	**Subjects (major changes since last revision)**
All	New Document.

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1 Overview

This chapter gives an overview of the 240–pin Registered DDR3 Dual-In-Line Memory Modules product family with parity bit for address and control bus and describes its main characteristics.

1.1 Features

- 240-pin 8-Byte DDR3 SDRAM Registered Dual-In-Line Memory Modules with parity bit for address and control bus.
- Module organization: two rank 512Mb × 72 and four rank 1024Mb × 72
  Chip organization: 2 × 256Mb × 4, 2 × 128Mb × 8.
- PC3-10600, PC3-8500 and PC3-6400 module speed grades.
- 8GB, 4GB modules built with 2Gb (1Gb dual-die) DDR3 SDRAMs in packages PG-TFBGA-78
- DDR3 SDRAMs with a single 1.5 V (± 0.075 V) power supply.
- Asynchronous Reset.
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.
- Serial Presence Detect with EEPROM.
- On-DIMM Thermal Sensor functionality.
- RDIMM dimensions: 133.35 mm x 30 mm.
- Based on standard reference raw cards: 'D', 'F' and 'G'.
- RoHS compliant products[1].

TABLE 1
Performance Table for DDR3–1333

Qimonda Speed Code		**–13G**	**–13H**	**Unit**	**Note** [1]
Module Speed Bin	**PC3**	**–10600G**	**–10600H**		
Device Speed Bin	**DDR3**	**–1333G**	**–1333H**		
CL-n_{RCD}-n_{RP}		**8-8-8**	**9-9-9**		
CL and CWL settings for maximum clock frequency		CL = 8 CWL = 7	CL = 9 CWL = 7	MHz	
Maximum Clock Frequency and Data Rate with above CL and CWL settings		667 1333	667 1333	MHz Mb/s	
Minimum Clock Frequency and Data Rate with above CL and CWL settings		533 1066	533 1066	MHz Mb/s	

1) The available CL and CWL settings depend on the SDRAM device speed bin. The CL setting and CWL setting result in maximum but also minimum clock frequency requirements. When making a selection of operating clock frequency, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting. For details, refer to **Chapter 4.1** Speed Bins.

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 2
Performance Table for DDR3–1066 and DDR3–800

Qimonda Speed Code		–10F	–10G	–08D	–08E	Unit	Note 1)
Module Speed Bin	PC3	–8500F	–8500G	–6400D	–6400E		
Device Speed Bin	DDR3	–1066F	–1066G	–800D	–800E		
CL-n_{RCD}-n_{RP}		7-7-7	8-8-8	5-5-5	6-6-6		
CL and CWL settings for maximum clock frequency		CL = 7 CWL = 6	CL = 8 CWL = 6	CL = 5 CWL = 5	CL = 6 CWL = 5	MHz	
Maximum Clock Frequency and Data Rate with above CL and CWL settings		533 1066	533 1066	400 800	400 800	MHz Mb/s	
Minimum Clock Frequency and Data Rate with above CL and CWL settings		400 800	400 800	300 600	300 600	MHz Mb/s	

1) The available CL and CWL settings depend on the SDRAM device speed bin. The CL setting and CWL setting result in maximum but also minimum clock frequency requirements. When making a selection of operating clock frequency, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting. For details, refer to **Chapter 4.1** Speed Bins.

1.2 Description

The Qimonda IMSH[4G/8G]PxxA1F2C are Registered DIMM (RDIMM) family with 30 mm height based on DDR3 SDRAM technology. DIMMs are available ECC modules in 512Mb × 72 (4GB), 1024Mb × 72 (8GB) organization and density, intended for mounting into 240 pin connector sockets.

The memory array is designed with 2Gb (1Gb dual-die) Double Data Rate (DDR3) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. De-coupling capacitors, stub resistors, calibration resistors and termination resistors are mounted on the PCB board. The DIMMs feature serial presence detect based on a 256 byte serial EEPROM device using the 2-pin I^2C protocol. The first 176 bytes are programmed with module specific SPD data.

green Product

TABLE 3
Product Information for Modules without Heat Spreader

Qimonda Part Number	Compliance Code	Description
4096 MByte Registered DIMM IMSH4GP12A1F2C		
IMSH4GP12A1F2C-08D	4GB 2R×4 PC3–6400P–5–XX–D0	240-pin 4096 MByte DDR3 registered DIMM with two rank and On-DIMM Thermal Sensor. The memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card D is used on this assembly **Used DDR3 SDRAM Component** Part Number: ISSH2G-12A1F2C Density: 2Gbit (1Gbit Dual Die) Organization: 2 × 256Mbit × 4 Address Bits (Row/Column/Bank): 14/11/3
IMSH4GP12A1F2C-08E	4GB 2R×4 PC3–6400P–6–XX–D0	
IMSH4GP12A1F2C-10F	4GB 2R×4 PC3–8500P–7–XX–D0	
IMSH4GP12A1F2C-10G	4GB 2R×4 PC3–8500P–8–XX–D0	
IMSH4GP12A1F2C-13G	4GB 2R×4 PC3–10600P–8–XX–D0	
IMSH4GP12A1F2C-13H	4GB 2R×4 PC3–10600P–9–XX–D0	
4096 MByte Registered DIMM IMSH4GP23A1F2C		
IMSH4GP23A1F2C-08D	4GB 4R×8 PC3–6400P–5–XX–G0	240-pin 4096 MByte DDR3 registered DIMM with four ranks and On-DIMM Thermal Sensor. Each memory rank consists of nine DDR3 components in x8 organization. Standard reference card G is used on this assembly **Used DDR3 SDRAM Component** Part Number: ISSH2G-13A1F2C Density: 2Gbit (1Gbit Dual Die) Organization: 2 × 128Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH4GP23A1F2C-08E	4GB 4R×8 PC3–6400P–6–XX–G0	
IMSH4GP23A1F2C-10F	4GB 4R×8 PC3–8500P–7–XX–G0	
IMSH4GP23A1F2C-10G	4GB 4R×8 PC3–8500P–8–XX–G0	
IMSH4GP23A1F2C-13G	4GB 4R×8 PC3–10600P–8–XX–G0	
IMSH4GP23A1F2C-13H	4GB 4R×8 PC3–10600P–9–XX–G0	
8192 MByte Registered DIMM IMSH8GP22A1F2C		
IMSH8GP22A1F2C-08D	8GB 4R×4 PC3–6400P–5–XX–F0	240-pin 8192 MByte DDR3 registered DIMM with four rank and On-DIMM Thermal Sensor. The memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card F is used on this assembly **Used DDR3 SDRAM Component** Part Number: ISSH2G-12A1F2C Density: 2Gbit (1Gbit Dual Die) Organization: 2 × 256Mbit × 4 Address Bits (Row/Column/Bank): 14/11/3
IMSH8GP22A1F2C-08E	8GB 4R×4 PC3–6400P–6–XX–F0	
IMSH8GP22A1F2C-10F	8GB 4R×4 PC3–8500P–7–XX–F0	
IMSH8GP22A1F2C-10G	8GB 4R×4 PC3–8500P–8–XX–F0	
IMSH8GP22A1F2C-13G	8GB 4R×4 PC3–10600P–8–XX–F0	
IMSH8GP22A1F2C-13H	8GB 4R×4 PC3–10600P–9–XX–F0	

TABLE 4
Product Information for Modules with Heat Spreader

Qimonda Part Number	Compliance Code	Description
4096 MByte Registered DIMM IMHH4GP12A1F2C		
IMHH4GP12A1F2C-08D	4GB 2R×4 PC3–6400P–5–XX–D0	240-pin 4096 MByte DDR3 registered DIMM with two rank and On-DIMM Thermal Sensor. The memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card D is used on this assembly **Used DDR3 SDRAM Component** Part Number: ISSH2G-12A1F2C Density: 2Gbit (1Gbit Dual Die) Organization: 2 × 256Mbit × 4 Address Bits (Row/Column/Bank): 14/11/3
IMHH4GP12A1F2C-08E	4GB 2R×4 PC3–6400P–6–XX–D0	
IMHH4GP12A1F2C-10F	4GB 2R×4 PC3–8500P–7–XX–D0	
IMHH4GP12A1F2C-10G	4GB 2R×4 PC3–8500P–8–XX–D0	
IMHH4GP12A1F2C-13G	4GB 2R×4 PC3–10600P–8–XX–D0	
IMHH4GP12A1F2C-13H	4GB 2R×4 PC3–10600P–9–XX–D0	
4096 MByte Registered DIMM IMHH4GP23A1F2C		
IMHH4GP23A1F2C-08D	4GB 4R×8 PC3–6400P–5–XX–G0	240-pin 4096 MByte DDR3 registered DIMM with four ranks and On-DIMM Thermal Sensor. Each memory rank consists of nine DDR3 components in x8 organization. Standard reference card G is used on this assembly **Used DDR3 SDRAM Component** Part Number: ISSH2G-13A1F2C Density: 2Gbit (1Gbit Dual Die) Organization: 2 × 128Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMHH4GP23A1F2C-08E	4GB 4R×8 PC3–6400P–6–XX–G0	
IMHH4GP23A1F2C-10F	4GB 4R×8 PC3–8500P–7–XX–G0	
IMHH4GP23A1F2C-10G	4GB 4R×8 PC3–8500P–8–XX–G0	
IMHH4GP23A1F2C-13G	4GB 4R×8 PC3–10600P–8–XX–G0	
IMHH4GP23A1F2C-13H	4GB 4R×8 PC3–10600P–9–XX–G0	

2 Configuration

2.1 Pin Configuration

TABLE 5
Pin Configuration of DDR3 RDIMM - 240 Pins

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
Clock Signals					
CK0	ck0_t	184	I	SSTL	**Differnetial Clock Inputs [1:0]**
$\overline{CK0}$	ck0_c	185	I	SSTL	
CK1	ck1_t	63	I	SSTL	
$\overline{CK1}$	ck1_c	64	I	SSTL	
Control Signals					
CKE0	cke0	50	I	SSTL	**Clock Enable [1:0]**
CKE1/NC	cke1	169	I	SSTL	
ODT0	odt0	195	I	SSTL	**On-Die Termination [1:0]**
ODT1/NC	odt1	77	I		
$\overline{S0}$	s0_n	193	I	SSTL	**Chip Select [3:0]**
$\overline{S1}$	s1_n	76	I	SSTL	
$\overline{S2}$	s2_n	79	I	SSTL	
$\overline{S3}$	s3_n	198	I	SSTL	
Command Signals					
$\overline{RAS}$	ras_n	192	I	SSTL	**Row Address Strobe**
$\overline{CAS}$	cas_n	74	I	SSTL	**Column Address Strobe**
$\overline{WE}$	we_n	73	I	SSTL	**Write Enable**
Bank Address Signals					
BA0	ba0	71	I	SSTL	**Bank Address Bus[2:0]**
BA1	ba1	190	I	SSTL	
BA2	ba2	52	I	SSTL	
Address Signals					
A0	a0	188	I	SSTL	**Address Bus [15:0]**
A1	a1	181	I	SSTL	
A2	a2	61	I	SSTL	

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
A3	a3	180	I	SSTL	**Address Bus [15:0]**
A4	a4	59	I	SSTL	
A5	a5	58	I	SSTL	
A6	a6	178	I	SSTL	
A7	a7	56	I	SSTL	
A8	a8	177	I	SSTL	
A9	a9	175	I	SSTL	
A10/AP	a10	70	I	SSTL	
A11	a11	55	I	SSTL	
A12/$\overline{BC}$	a12	174	I	SSTL	
A13	a13	196	I	SSTL	
A14	a14	172	I	SSTL	
A15	a15	171	I	SSTL	
Data Signals					
DQ0	dq0	3	I/O	SSTL	**Data Bus [63:0]**
DQ1	dq1	4	I/O	SSTL	
DQ2	dq2	9	I/O	SSTL	
DQ3	dq3	10	I/O	SSTL	
DQ4	dq4	122	I/O	SSTL	
DQ5	dq5	123	I/O	SSTL	
DQ6	dq6	128	I/O	SSTL	
DQ7	dq7	129	I/O	SSTL	
DQ8	dq8	12	I/O	SSTL	
DQ9	dq9	13	I/O	SSTL	
DQ10	dq10	18	I/O	SSTL	
DQ11	dq11	19	I/O	SSTL	
DQ12	dq12	131	I/O	SSTL	
DQ13	dq13	132	I/O	SSTL	
DQ14	dq14	137	I/O	SSTL	
DQ15	dq15	138	I/O	SSTL	
DQ16	dq16	21	I/O	SSTL	
DQ17	dq17	22	I/O	SSTL	
DQ18	dq18	27	I/O	SSTL	
DQ19	dq19	28	I/O	SSTL	
DQ20	dq20	140	I/O	SSTL	
DQ21	dq21	141	I/O	SSTL	
DQ22	dq22	146	I/O	SSTL	
DQ23	dq23	147	I/O	SSTL	
DQ24	dq24	30	I/O	SSTL	

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
DQ25	dq25	31	I/O	SSTL	**Data Bus [63:0]**
DQ26	dq26	36	I/O	SSTL	
DQ27	dq27	37	I/O	SSTL	
DQ28	dq28	149	I/O	SSTL	
DQ29	dq29	150	I/O	SSTL	
DQ30	dq30	155	I/O	SSTL	
DQ31	dq31	156	I/O	SSTL	
DQ32	dq32	81	I/O	SSTL	
DQ33	dq33	82	I/O	SSTL	
DQ34	dq34	87	I/O	SSTL	
DQ35	dq35	88	I/O	SSTL	
DQ36	dq36	200	I/O	SSTL	
DQ37	dq37	201	I/O	SSTL	
DQ38	dq38	206	I/O	SSTL	
DQ39	dq39	207	I/O	SSTL	
DQ40	dq40	90	I/O	SSTL	
DQ41	dq41	91	I/O	SSTL	
DQ42	dq42	96	I/O	SSTL	
DQ43	dq43	97	I/O	SSTL	
DQ44	dq44	209	I/O	SSTL	
DQ45	dq45	210	I/O	SSTL	
DQ46	dq46	215	I/O	SSTL	
DQ47	dq47	216	I/O	SSTL	
DQ48	dq48	99	I/O	SSTL	
DQ49	dq49	100	I/O	SSTL	
DQ50	dq50	105	I/O	SSTL	
DQ51	dq51	106	I/O	SSTL	
DQ52	dq52	218	I/O	SSTL	
DQ53	dq53	219	I/O	SSTL	
DQ54	dq54	224	I/O	SSTL	
DQ55	dq55	225	I/O	SSTL	
DQ56	dq56	108	I/O	SSTL	
DQ57	dq57	109	I/O	SSTL	
DQ58	dq58	114	I/O	SSTL	
DQ59	dq59	115	I/O	SSTL	
DQ60	dq60	227	I/O	SSTL	
DQ61	dq61	228	I/O	SSTL	
DQ62	dq62	233	I/O	SSTL	
DQ63	dq63	234	I/O	SSTL	

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
CB0	cb0	39	I/O	SSTL	**Check Bit [7:0]**
CB1	cb1	40	I/O	SSTL	
CB2	cb2	45	I/O	SSTL	
CB3	cb3	46	I/O	SSTL	
CB4	cb4	158	I/O	SSTL	
CB5	cb5	159	I/O	SSTL	
CB6	cb6	164	I/O	SSTL	
CB7	cb7	165	I/O	SSTL	
DQS0	dqs0_t	7	I/O	SSTL	**Data Strobe Signals [17:0]**
$\overline{\text{DQS0}}$	dqs0_c	6	I/O	SSTL	
DQS1	dqs1_t	16	I/O	SSTL	
$\overline{\text{DQS1}}$	dqs1_c	15	I/O	SSTL	
DQS2	dqs2_t	25	I/O	SSTL	
$\overline{\text{DQS2}}$	dqs2_c	24	I/O	SSTL	
DQS3	dqs3_t	34	I/O	SSTL	
$\overline{\text{DQS3}}$	dqs3_c	33	I/O	SSTL	
DQS4	dqs4_t	85	I/O	SSTL	
$\overline{\text{DQS4}}$	dqs4_c	84	I/O	SSTL	
DQS5	dqs5_t	94	I/O	SSTL	
$\overline{\text{DQS5}}$	dqs5_c	93	I/O	SSTL	
DQS6	dqs6_t	103	I/O	SSTL	
$\overline{\text{DQS6}}$	dqs6_c	102	I/O	SSTL	
DQS7	dqs7_t	112	I/O	SSTL	
$\overline{\text{DQS7}}$	dqs7_c	111	I/O	SSTL	
DQS8	dqs8_t	43	I/O	SSTL	
$\overline{\text{DQS8}}$	dqs8_c	42	I/O	SSTL	
(T)DQS9	dqs9_t	125	I/O	SSTL	
$\overline{\text{(T)DQS9}}$	dqs9_c	126	I/O	SSTL	
(T)DQS10	dqs10_t	134	I/O	SSTL	
$\overline{\text{(T)DQS10}}$	dqs10_c	135	I/O	SSTL	
(T)DQS11	dqs11_t	143	I/O	SSTL	
$\overline{\text{(T)DQS11}}$	dqs11_c	144	I/O	SSTL	
(T)DQS12	dqs12_t	152	I/O	SSTL	
$\overline{\text{(T)DQS12}}$	dqs12_c	153	I/O	SSTL	
(T)DQS13	dqs13_t	203	I/O	SSTL	
$\overline{\text{(T)DQS13}}$	dqs13_c	204	I/O	SSTL	
(T)DQS14	dqs14_t	212	I/O	SSTL	
$\overline{\text{(T)DQS14}}$	dqs14_c	213	I/O	SSTL	
(T)DQS15	dqs15_t	221	I/O	SSTL	

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
(T)DQS15	dqs15_c	222	I/O	SSTL	**Data Strobe Signals [17:0]**
(T)DQS16	dqs16_t	230	I/O	SSTL	
(T)DQS16	dqs16_c	231	I/O	SSTL	
(T)DQS17	dqs17_t	161	I/O	SSTL	
(T)DQS17	dqs17_c	162	I/O	SSTL	
EEPROM and Thermal Sensor					
SCL	scl	118	I	CMOS	**Serial Bus Clock**
SDA	sda	238	I/O	OD	**Serial Data Bus**
SA0	sa0	117	I	CMOS	**Serial Address Select Bus [2:0]**
SA1	sa1	237	I	CMOS	
SA2	sa2	119	I	CMOS	
Power Supply					
V_{DD}	vdd	51, 54, 57, 60, 62, 65, 66, 69, 72, 75, 78, 170, 173, 176, 179, 182, 183, 186, 189, 191, 194, 197	PWR	-	**Power Supply**

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
V_{SS}	vss	2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 80, 83, 86, 89,92, 95, 98, 101, 104, 107, 110, 113, 116, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 199, 202, 205, 208, 211, 214, 217, 220, 223, 226, 229, 232, 235, 239	GND	-	**Ground**
$V_{REF.DQ}$	vrefdq	1	AI	-	**Reference Voltage**
$V_{REF.CA}$	vrefca	67	AI	-	**Reference Voltage**
V_{TT}	vtt	48, 49, 120 , 240	PWR	-	**Termination Voltage**
V_{DDSPD}	vddspd	236		-	**EEPROM and Thermal Sensor Power Supply**
Other Pins					
$\overline{\text{RESET}}$	reset_n	168	I		**Asynchronous Reset**
$\overline{\text{Err\_Out}}$	err_out_n	53	O	OD	**$\overline{\text{Err\_Out}}$**
Par_In	par_in	68	I		**Par_In**

Pin Name	EDA Signal Name[1)]	Pin No.	Pin Type	Buffer Type	Function
$\overline{\text{EVENT}}$	event_n	187	O	OD	**$\overline{\text{EVENT}}$**
NC	nc	79, 126, 135, 144, 153, 162, 167, 198, 204, 213, 222, 231,	-	-	**Not Connected**

1) The EDA (Electronic Design Automation) Signal Name is used in Qimonda Simulation Models such as EBD (Electronic Board Description).

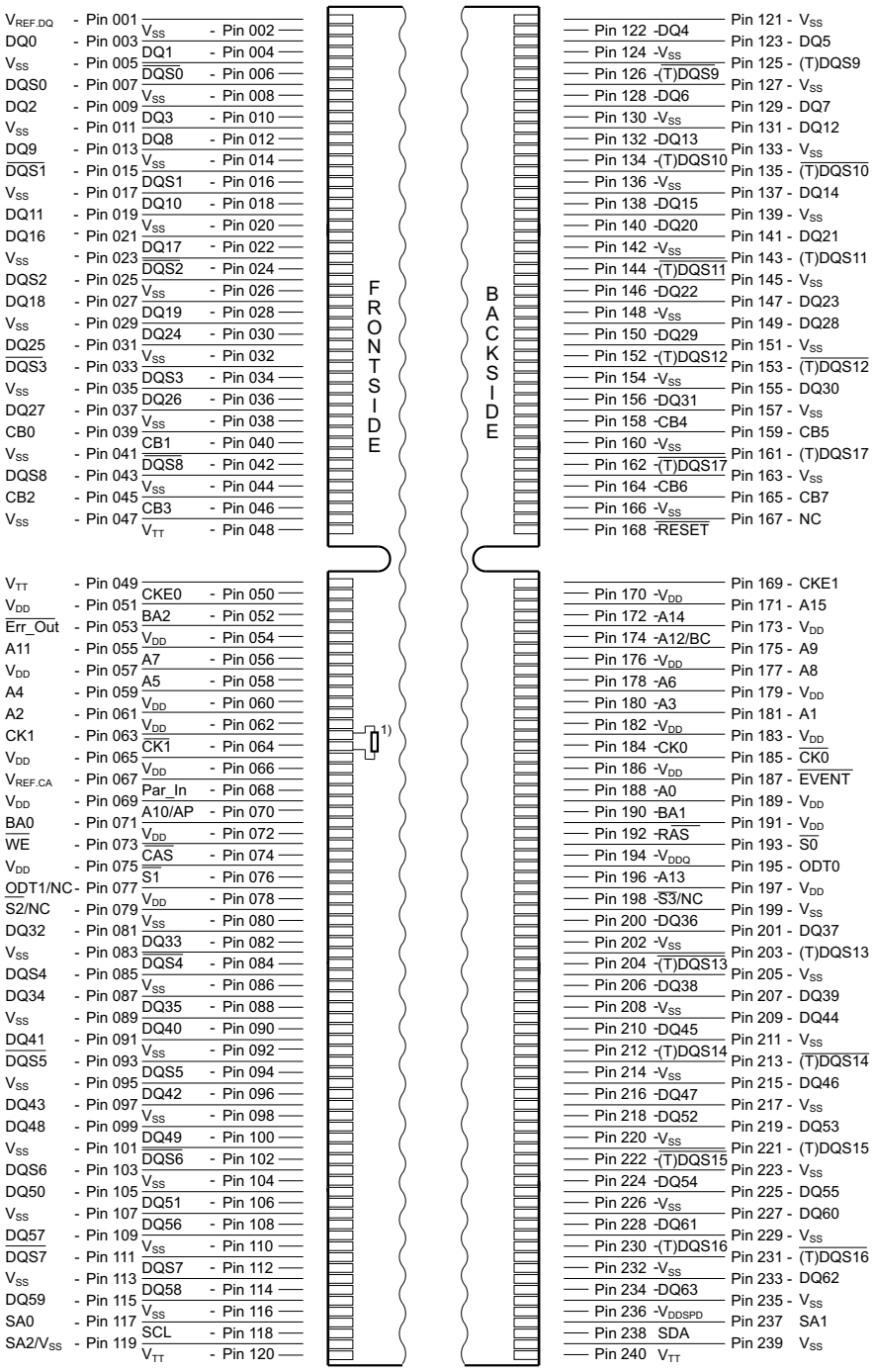
TABLE 6
Abbreviations for Pin Type

Abbreviation	Description
I	Standard Input pin only. Digital levels.
O	Standard Output pin only - Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input - Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration RDIMM - 240 Pin



1) Pin 63 and Pin 64 terminated with 120 Ω

(T) : For x8 DRAM only

MPPH0250

3 Operating Conditions

3.1 Absolute Maximum Ratings

TABLE 8
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	–0.4	+1.975	V	1)
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	–0.4	+1.975	V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	+1.975	V	

1) V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{REFDQ} and V_{REFCA} must not be greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500 mV, V_{REFDQ} and V_{REFCA} may be equal or less than 300 mV.

TABLE 9
Environmental Parameters

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Operating Temperature	T_{OPR}	–	–	°C	1)
Operating Humidity (relative)	H_{OPR}	10	90	%	
Storage Temperature	T_{STG}	–50	+100	°C	2)
Storage Humidity (without condensation)	H_{STG}	5	95	%	
Barometric Pressure (Operating and Storage)	P_{Bar}	69	105	KPascal	3)

1) Device designer must meet the case temperature specification for individual module components.
2) Storage Temperature is the case surface temperature on the center/top side of the SDRAM mentioned in Qimonda component datasheet.
3) Up to 9850 ft.

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 10
DRAM Component Operating Temperature Range

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Normal Operating Temperature Range	T_{OPER}	0	85	°C	1)2)
Extended Temperature Range		85	95	°C	1)3)

1) Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the SDRAM mentioned..
2) The Normal Temperature Range specifies the temperatures where all SDRAM specification will be supported.
3) Some application require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C operating temperature. For more details please refer to Qimonda Component datasheet.

3.2 Recommended DC Operating Conditions

TABLE 11
DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.425	1.5	1.575	V	1)2)
Supply Voltage for EEPROM and Thermal Sensor	$V_{DD.SPD}$	3.0	3.3	3.6	V	1)2)
Supply Voltage for Output	V_{DDQ}	1.425	1.5	1.575	V	1)2)
Reference Voltage for DQ, DM inputs	$V_{REFDQ.DC}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3)4)
Reference Voltage for ADD, CMD inputs	$V_{REFCA.DC}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3)4)
Terminal Voltage	V_{TT}	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	
External Calibration Resistor connected from ZQ pin to ground	R_{ZQ}	237.6	240.0	242.4	Ω	5)

1) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together
2) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
3) The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF.DC}$ by more than ±1% V_{DD} (for reference: approx. ± 15 mV).
4) For reference: approx. $V_{DD}/2$ ± 15 mV.
5) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.

4 Speed Bins and Timing Parameters

AC timings are provided with CK/$\overline{CK}$ and DQS/$\overline{DQS}$ differential slew rate of 2.0 V/ns. Timings are further provided for calibrated OCD drive strength. The CK/$\overline{CK}$ input reference level (for timing referenced to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.The DQS/$\overline{DQS}$ reference level (for timing referenced to DQS/$\overline{DQS}$) is the point at which DQS and $\overline{DQS}$ cross.Inputs are not recognized as valid until V_{REF} stabilizes. During the period before $V_{REF.CA}$ and V_{REFDQ} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low. The output timing reference voltage level is V_{TT}.For details of all relevant AC timing parameters see the QIMONDA DDR3 component datasheet.

4.1 Speed Bins

The following tables show DDR3 speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter.

General Notes for Speed Bins:

- The CL setting and CWL setting result in $t_{CK.AVG.MIN}$ and $t_{CK.AVG.MAX}$ requirements. When making a selection of $t_{CK.AVG}$, both need to be fulfiled: Requirements from CL setting as well as requirements from CWL setting.
- $t_{CK.AVG.MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be provided. An application should use the next smaller standard $t_{CK.AVG}$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = t_{AA} [ns] / $t_{CK.AVG}$ [ns], rounding up to the next 'Supported CL'.
- $t_{CK.AVG.MAX}$ limits: Calculate $t_{CK.AVG}$ = $t_{AA.MAX}$ / CLSELECTED and round the resulting $t_{CK.AVG}$ down to the next valid speed bin limit (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.25 ns). This result is $t_{CK.AVG.MAX}$ corresponding to CLSELECTED.

The absolute specification for all speed bins is T_{OPER} and V_{DD} = V_{DDQ} = 1.5 V +/-0.075 V. In addition the following general notes apply.

- 'Reserved' settings are not allowed. User must program a different value.
- Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization.

TABLE 12
DDR3–800 Speed Bins

Speed Bin		DDR3-800D		DDR3-800E		Unit	Note
CL-n_{RCD}-n_{RP}		5-5-5		6-6-6			
QAG Partnumber Extension		-08D		-08E			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	12.5	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	12.5	—	15.0	—	ns	1)
PRE command period	t_{RP}	12.5	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	50.0	—	52.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6		6		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5		5		n_{CK}	1)

Speed Bin		DDR3-800D		DDR3-800E		Unit	Note
CL-n_{RCD}-n_{RP}		5-5-5		6-6-6			
QAG Partnumber Extension		-08D		-08E			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**		
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

TABLE 13
DDR3–1066 Speed Bins

Speed Bin		DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL-n_{RCD}-n_{RP}		6-6-6		7-7-7		8-8-8			
QAG Partnumber Extension		-10E		-10F		-10G			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	11.25	20.0	13.125	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	11.25	—	13.125	—	15.0	—	ns	1)
PRE command period	t_{RP}	11.25	—	13.125	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.75	—	50.625	—	52.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6		5, 6		5, 6		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

TABLE 14
DDR3–1333 Speed Bins

Speed Bin		DDR3-1333G		DDR3-1333H		DDR3-1333J		Unit	Note
CL-n_{RCD}-n_{RP}		8-8-8		9-9-9		10-10-10			
QAG Partnumber Extension		-13G		-13H		-13J			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	12.0	20.0	13.5	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	12.0	—	13.5	—	15.0	—	ns	1)
PRE command period	t_{RP}	12.0	—	13.5	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.0	—	49.5	—	51.0	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8, 9, 10		6, 8, 9, 10		6, 8, 10		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 7	$t_{CK.AVG.CL05.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 7	$t_{CK.AVG.CL06.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 7	$t_{CK.AVG.CL07.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 8; CWL = 7	$t_{CK.AVG.CL08.CWL07}$	1.5	1.875	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 5	$t_{CK.AVG.CL09.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 6	$t_{CK.AVG.CL09.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 7	$t_{CK.AVG.CL09.CWL07}$	1.5	1.875	1.5	1.875	RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 5	$t_{CK.AVG.CL10.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 6	$t_{CK.AVG.CL10.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 7	$t_{CK.AVG.CL10.CWL07}$	1.5	1.875	1.5	1.875	1.5	1.875	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

5 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 15
IMSH4GP12A1F2C

TBD

TABLE 16
IMSH4GP23A1F2C

TBD

TABLE 17
IMSH8GP22A1F2C

TBD

TABLE 18
IMHH4GP12A1F2C

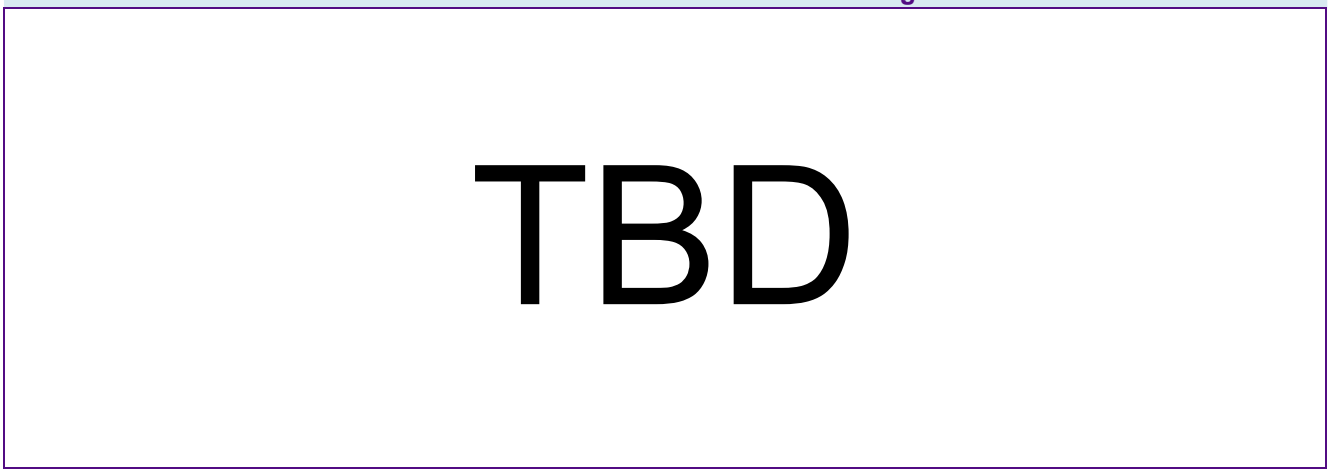
TBD

TABLE 19
IMHH4GP23A1F2C

TBD

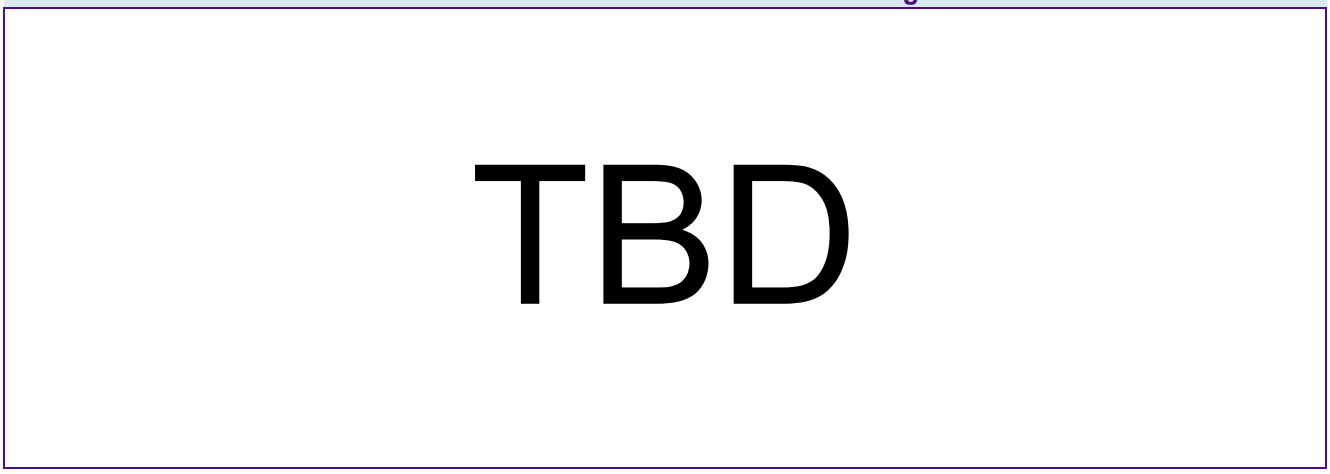
6 Package Outline Diagrams

FIGURE 2
Package Outline LG-DIM-240-094 R/C D



Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.

FIGURE 3
Package Outline LG-DIM-240-095 R/C F



Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.

FIGURE 4
Package Outline LG-DIM-240-096 R/C G

Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.

7 Product Type Nomenclature

For reference the applicable Qimonda DDR3 DIMM module nomenclature is listed in this chapter.

TABLE 20
Example: DDR3 1GByte Registered Module

Field Number	1+2	3	4	5+6	7	8	9	10+11	12+13	14	15	16+17	18
Qimonda Product Type	IM	S	H	4G	P	1	2	A1	F2	C	–	08	E

TABLE 21
DDR3 DIMM Nomenclature

Field	Description	Value	Coding
1+2	Qimonda Identifier	IM	Qimonda Memory modules
3	Power or Application	S	Standard
		H	Heat Spreader
		L	Low Power
4	Product Family	H	DDR3
5+6	Density	51	512 MBytes
		1G	1024 MBytes
		2G	2048 MBytes
		4G	4096 MBytes
7	Module Type / ECC Support	U	240 pin unbuffered DIMMs - Non-ECC
		E	240 pin unbuffered DIMMs - ECC
		S	204 pin Small Outline DIMMs - Non-ECC
		R	240 pin Registered DIMMs - ECC
		P	240 pin Registered DIMMs with Parity Bit - ECC
8	Number of Ranks	0	One Rank of SDRAMs
		1	Two Ranks of SDRAMs
		2	Four Ranks of SDRAMs
9	DRAM Device Number of IOs	2	×4 components (2^2)
		3	×8 components (2^3)
		4	×16 components (2^4)
10+11	Die Revision	A1	First
12+13	Package	F1	Planar FBGA, lead- and halogen-free
		F2	Dual Die FBGA, lead- and halogen-free
14	Temperature Range	C	Commercial (0 °C - 95 °C)
15	Thermal Sensor	T	Modules with Thermal Sensor

Field	Description	Value	Coding
16+17	Band Width	08	PC3–6400, 6.4 GB/s, t_{CK} = 2.5 ns, f_{CK} =400 MHz
		10	PC3–8500, 8.5 GB/s, t_{CK} = 1.875 ns, f_{CK} =533 MHz
		13	PC3–10600, 10,66 GB/s, t_{CK} = 1.5 ns, f_{CK} =667 MHz
		16	PC3–12800, 12,8 GB/s, t_{CK} = 1.25 ns, f_{CK} =800 MHz
18	Latencies	D	CL–RCD–RP = 5–5–5
		E	CL–RCD–RP = 6–6–6
		F	CL–RCD–RP = 7–7–7
		G	CL–RCD–RP = 8–8–8
		H	CL–RCD–RP = 9–9–9
		J	CL–RCD–RP = 10–10–10

Contents

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