HARRIS HSP43891/883

May 1991

Digital Filter

Features

- This Circuit is Processed In Accordance to Mil-Std-883C and is Fully Conformant Under the Provisions of Paragraph 1.2.1
- 0 to 25.6MHz Sample Rate
- Eight Filter Cells
- 9-Bit Coefficients and Signal Data
- Low Power CMOS Operation
  - I_{CCSB} = 500µA Maximum
  - I_{CCOP} = 160µA Maximum @ 20MHz
- 26-Bit Accumulator per Stage
- Filter Lengths Up to 1032 Taps
- Shift-and-Add Output Stage for Combining Filter Outputs
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

Applications

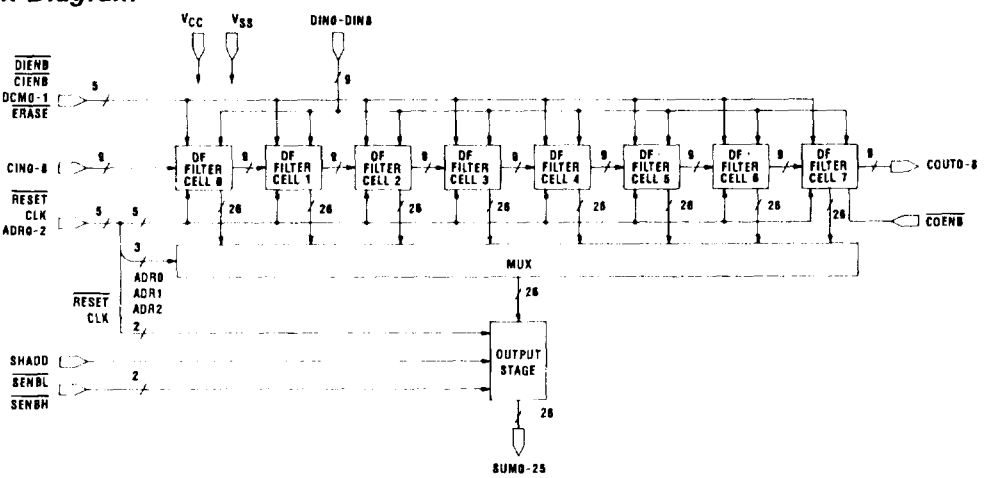
- 1-D and 2-D FIR Filters
- Radar/Sonar
- Digital Video and Audio
- Adaptive Filters
- Echo Cancellation
- Correlation/Convolution
- Complex Multiply-Add
- Butterfly Computation
- Matrix Multiplication
- Sample Rate Converters

Description

The HSP43891/883 is a video-speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 9x9 two's complement multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8 bits. The HSP43891/883 has a maximum sample rate of 25.6MHz. The effective multiply-accumulate (mac) rate is 204MHz. The HSP43891/883 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or 9-bit two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three re-sampling or decimation registers which permit output sample rate reduction at rates of 1/2, 1/3 or 1/4 the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and NxN spatial correlations/convolutions for image processing applications.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2451.1**

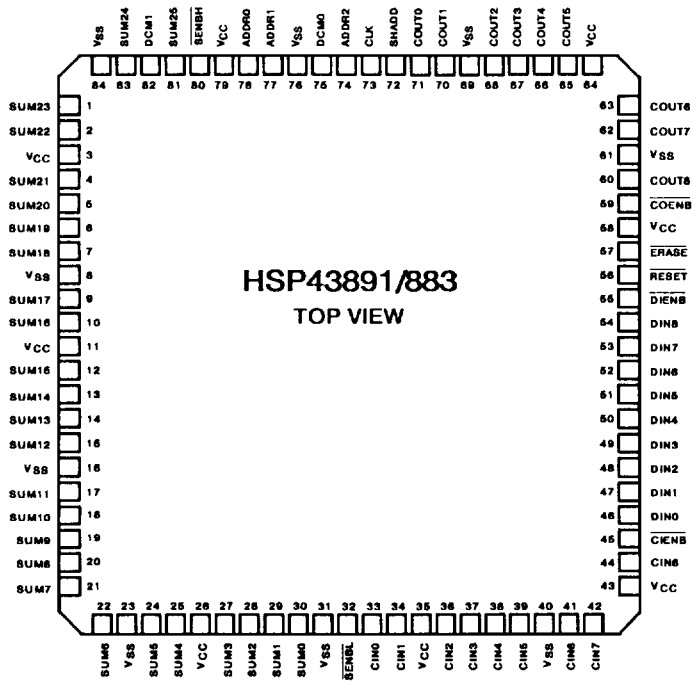
Pinouts

85 PIN GRID ARRAY (PGA)

	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	$\overline{COENB}$	V_{CC}	$\overline{RESET}$	DIN7	DIN6	DIN5	DIN0	CIN6	V_{CC}	V_{SS}
B	V_{CC}	COUT7	COUT6	$\overline{ERASE}$	DIN8	DIN1	DIN2	$\overline{CIENB}$	CIN7	CIN6	CIN4
C	COUT5	COUT6	ALIGN PIN		$\overline{DIENB}$	DIN5	DIN4			CIN5	CIN3
D	COUT3	COUT4		HSP43891/883 TOP VIEW PINS DOWN						CIN2	V_{CC}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{SENBL}$
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
K	$\overline{SENBH}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9

	1	2	3	4	5	6	7	8	9	10	11
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9
K	$\overline{SENBH}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
H	ADR1	ADR0								SUM5	SUM4
G	ADR2	DCM0	CLK	HSP43891/883 BOTTOM VIEW PINS UP					SUM1	SUM3	SUM2
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{SENBL}$
D	COUT3	COUT4								CIN2	V_{CC}
C	COUT5	COUT6	ALIGN PIN		$\overline{DIENB}$	DIN5	DIN4			CIN5	CIN3
B	V_{CC}	COUT7	COUT6	$\overline{ERASE}$	DIN6	DIN1	DIN2	$\overline{CIENB}$	CIN7	CIN6	CIN4
A	V_{SS}	$\overline{COENB}$	V_{CC}	$\overline{RESET}$	DIN7	DIN6	DIN3	DIN0	CIN6	V_{CC}	V_{SS}

84 PIN CERAMIC QUAD FLATPACK



Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output Voltage Applied ..... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
Ceramic PGA Package ..... 34.66°C/W 7.78°C/W
Maximum Package Power Dissipation at +125°C
Ceramic PGA Package ..... 1.44 Watt
Gate Count ..... 17762 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HSP43891/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Output Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	V_{CC}-0.8	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V, Outputs Open	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz V_{CC} = 5.5V (Note 2)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	160.0	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	

NOTES: 1. Interchanging of force and sense conditions is permitted.

2. Operating Supply Current is proportional to frequency, typical rating is 8mA/MHz.

3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V, V_{IHC} = V_{CC} -0.4V, and V_{ILC} = 0.4V.

TABLE 2. HSP43891/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T_{CP}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	39	-	ns
Clock Low	T_{CL}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Clock High	T_{CH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	16	-	ns
Input Setup	T_{IS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	17	-	ns
Input Hold	T_{IH}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
CLK to Coefficient Output Delay	T_{ODC}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	24	-	20	ns
Output Enable Delay	T_{OED}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
CLK to SUM Output Delay	T_{ODS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	31	-	25	ns

NOTE: 1. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 3. HSP43891/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-20 (20MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC}=Open, f=1MHz All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	15	-	15	pF
Output Disable Delay	T_{ODD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	-	15	ns
Output Rise Time	T_{OR}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns
Output Fall Time	T_{OF}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	7	-	6	ns

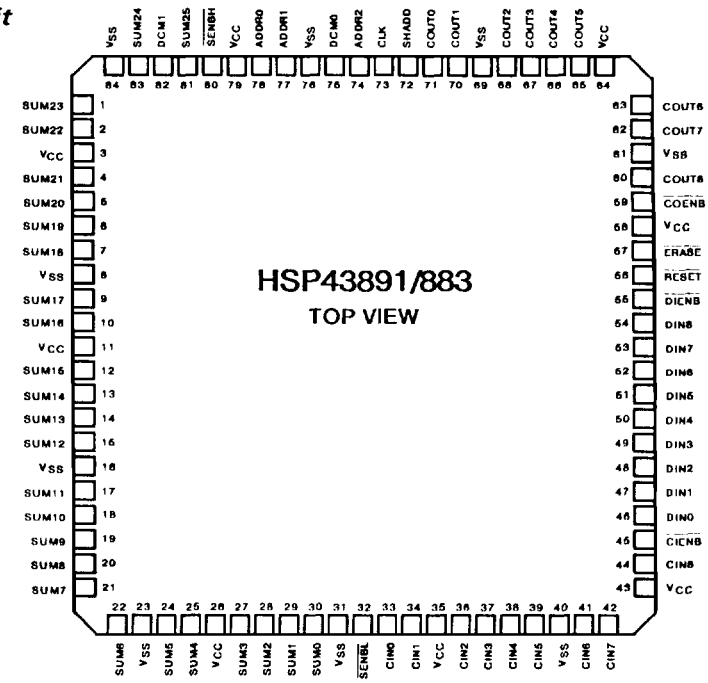
NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Loading is as specified in the test load circuit, C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

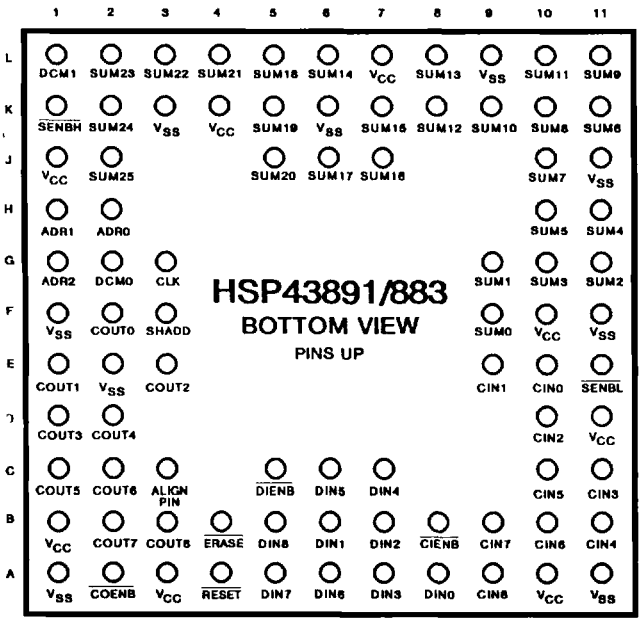
Burn-In Circuit



QFP LEAD	PIN NAME	BURN-IN SIGNAL	QFP LEAD	PIN NAME	BURN-IN SIGNAL	QFP LEAD	PIN NAME	BURN-IN SIGNAL	QFP LEAD	PIN NAME	BURN-IN SIGNAL
1	SUM23	$V_{CC}/2$	22	SUM6	$V_{CC}/2$	43	V_{CC}	V_{CC}	64	V_{CC}	V_{CC}
2	SUM22	$V_{CC}/2$	23	V_{SS}	GND	44	CIN8	F9	65	COUT5	$V_{CC}/2$
3	V_{CC}	V_{CC}	24	SUM5	$V_{CC}/2$	45	$\overline{CIENB}$	F10	66	COUT4	$V_{CC}/2$
4	SUM21	$V_{CC}/2$	25	SUM4	$V_{CC}/2$	46	DIN0	F0	67	COUT3	$V_{CC}/2$
5	SUM20	$V_{CC}/2$	26	V_{CC}	V_{CC}	47	DIN1	F1	68	COUT2	$V_{CC}/2$
6	SUM19	$V_{CC}/2$	27	SUM3	$V_{CC}/2$	48	DIN2	F2	69	V_{SS}	GND
7	SUM18	$V_{CC}/2$	28	SUM2	$V_{CC}/2$	49	DIN3	F3	70	COUT1	$V_{CC}/2$
8	V_{SS}	GND	29	SUM1	$V_{CC}/2$	50	DIN4	F4	71	COUT0	$V_{CC}/2$
9	SUM17	$V_{CC}/2$	30	SUM0	$V_{CC}/2$	51	DIN5	F5	72	SHADD	F9
10	SUM16	$V_{CC}/2$	31	V_{SS}	GND	52	DIN6	F6	73	CLK	F0
11	V_{CC}	V_{CC}	32	$\overline{SENBL}$	F10	53	DIN7	F8	74	ADDR2	F2
12	SUM15	$V_{CC}/2$	33	CIN0	F0	54	DIN8	F7	75	DCM0	F5
13	SUM14	$V_{CC}/2$	34	CIN1	F1	55	$\overline{DIENB}$	F10	76	V_{SS}	GND
14	SUM13	$V_{CC}/2$	35	V_{CC}	V_{CC}	56	$\overline{RESET}$	F11	77	ADDR1	F1
15	SUM12	$V_{CC}/2$	36	CIN2	F2	57	$\overline{ERASE}$	F10	78	ADDR0	F0
16	V_{SS}	GND	37	CIN3	F3	58	V_{CC}	V_{CC}	79	V_{CC}	V_{CC}
17	SUM11	$V_{CC}/2$	38	CIN4	F4	59	$\overline{COENB}$	F10	80	$\overline{SENBH}$	F10
18	SUM10	$V_{CC}/2$	39	CIN5	F5	60	COUT8	$V_{CC}/2$	81	SUM25	$V_{CC}/2$
19	SUM9	$V_{CC}/2$	40	V_{SS}	GND	61	V_{SS}	GND	82	DCM1	F6
20	SUM8	$V_{CC}/2$	41	CIN6	F6	62	COUT7	$V_{CC}/2$	83	SUM24	$V_{CC}/2$
21	SUM7	$V_{CC}/2$	42	CIN7	F7	63	COUT6	$V_{CC}/2$	84	V_{SS}	GND

NOTES:
1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1µF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%

Burn-In Circuit



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	V_{SS}	GND	C1	COUT5	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K4	V_{CC}	V_{CC}
A2	$\overline{COENB}$	F10	C2	COUT6	$V_{CC}/2$	F11	V_{SS}	GND	K5	SUM19	$V_{CC}/2$
A3	V_{CC}	V_{CC}	C3	ALIGN	NC	G1	ADR2	F2	K6	V_{SS}	GND
A4	$\overline{RESET}$	F11	C5	$\overline{DIENB}$	F10	G2	DCM0	F5	K7	SUM15	$V_{CC}/2$
A5	DIN7	F8	C6	DIN5	F5	G3	CLK	F0	K8	SUM12	$V_{CC}/2$
A6	DIN6	F6	C7	DIN4	F4	G9	SUM1	$V_{CC}/2$	K9	SUM10	$V_{CC}/2$
A7	DIN3	F3	C10	CIN5	F5	G10	SUM3	$V_{CC}/2$	K10	SUM8	$V_{CC}/2$
A8	DIN0	F0	C11	CIN3	F3	G11	SUM2	$V_{CC}/2$	K11	SUM6	$V_{CC}/2$
A9	CIN8/TCCI	F8	D1	COUT3	$V_{CC}/2$	H1	ADR1	F1	L1	DCM1	F6
A10	V_{CC}	V_{CC}	D2	COUT4	$V_{CC}/2$	H2	ADR0	F0	L2	SUM23	$V_{CC}/2$
A11	V_{SS}	GND	D10	CIN2	F2	H10	SUM5	$V_{CC}/2$	L3	SUM22	$V_{CC}/2$
B1	V_{CC}	V_{CC}	D11	V_{CC}	V_{CC}	H11	SUM4	$V_{CC}/2$	L4	SUM21	$V_{CC}/2$
B2	COUT7	$V_{CC}/2$	E1	COUT1	$V_{CC}/2$	J1	V_{CC}	V_{CC}	L5	SUM18	$V_{CC}/2$
B3	COUT8/ TCCO	$V_{CC}/2$	E2	V_{SS}	GND	J2	SUM25	$V_{CC}/2$	L6	SUM14	$V_{CC}/2$
			E3	COUT2	$V_{CC}/2$	J5	SUM20	$V_{CC}/2$	L7	V_{CC}	V_{CC}
B4	$\overline{ERASE}$	F10	E9	CIN1	F1	J6	SUM17	$V_{CC}/2$	L8	SUM13	$V_{CC}/2$
B5	DIN8/TCS	F7	E10	CIN0	F0	J7	SUM16	$V_{CC}/2$	L9	V_{SS}	GND
B6	DIN1	F1	E11	$\overline{SENBL}$	F10	J10	SUM7	$V_{CC}/2$	L10	SUM11	$V_{CC}/2$
B7	DIN2	F2	F1	V_{SS}	GND	J11	V_{SS}	GND	L11	SUM9	$V_{CC}/2$
B8	$\overline{CIENB}$	F10	F2	CUT0	$V_{CC}/2$	K1	$\overline{SENBH}$	F10			
B9	CIN7	F7	F3	SHADD	F9	K2	SUM24	$V_{CC}/2$			
B10	CIN6	F6	F9	SUM0	$V_{CC}/2$	K3	V_{SS}	GND			
B11	CIN4	F4									

NOTES:
1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1μF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . . . , F11 = F10/2, 40% - 60% Duty Cycle.
6. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ±10%

Metallization Topology

DIE DIMENSIONS:
328 x 283 x 19 ±1 mils

METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

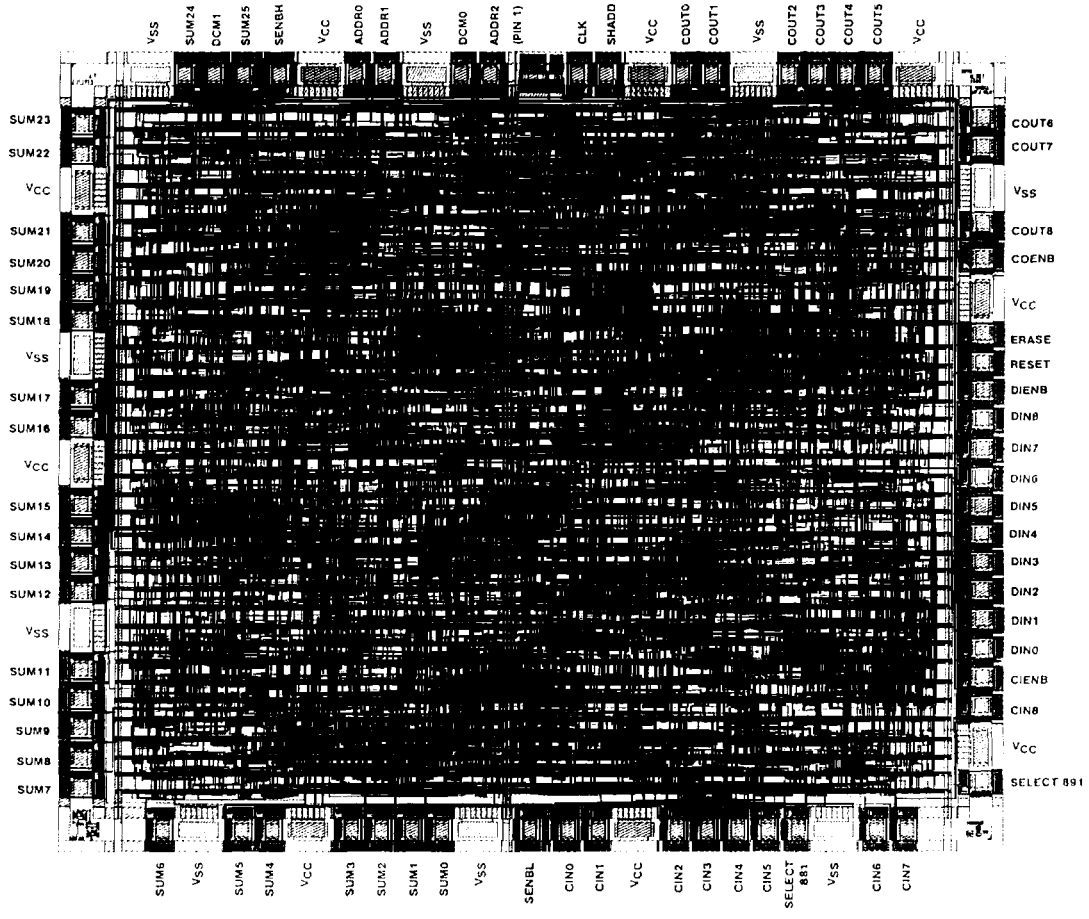
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy (PGA)
Silver/Glass (QFP)

WORST CASE CURRENT DENSITY:
$1.2 \times 10^5 A/cm^2$

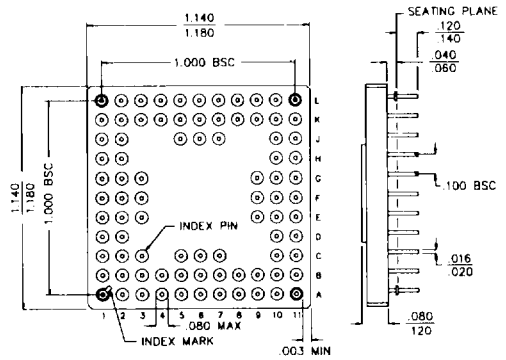
Metallization Mask Layout

HSP43891/883



Packaging†

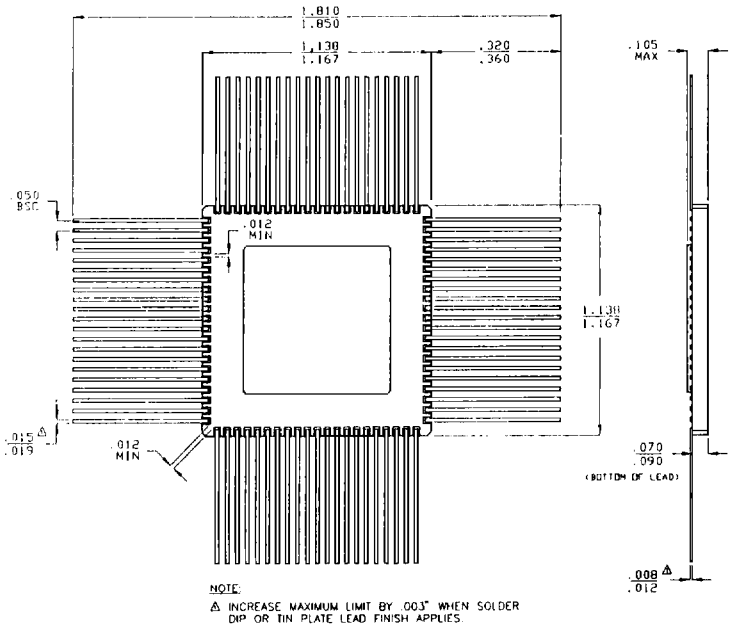
85 PIN GRID ARRAY (PGA)



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510P-AC

84 PIN QUAD FLATPACK (QFP)



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510C-G6

NOTE: All Dimensions are Min/Max, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.