DENSE-PAC
MICROSYSTEMS

32 Megabit CMOS SRAM
DP3S1MX32PY5

ADVANCED INFORMATION

DESCRIPTION:

The DP3S1MX32PY5 is a 1M x 32 SRAM module that utilizes the new and innovative space saving TSOP stacking technology. The module is constructed of two 1M x 16 SRAM's that are configured as a 1M x 32.

The DP3S1MX32PY5 module features high speed access times with common data inputs and outputs.

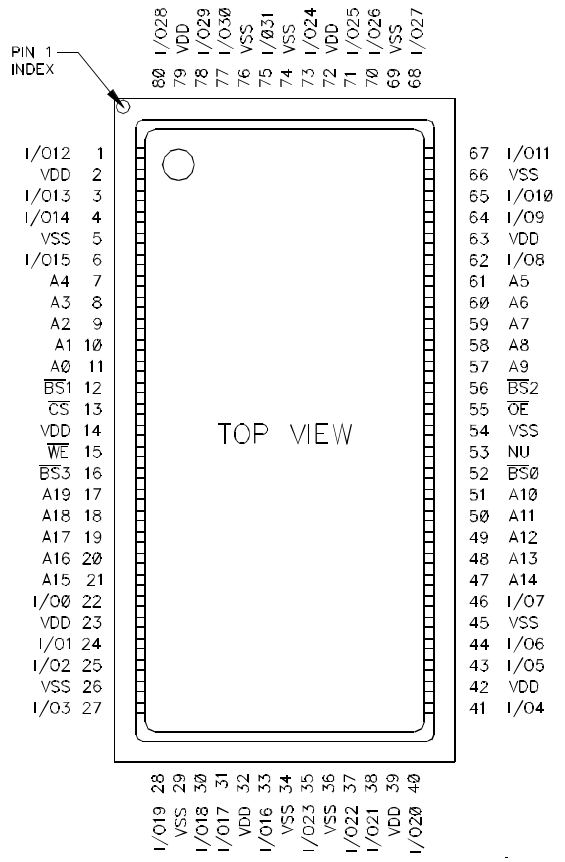
FEATURES:

- Organizations Available: 1M x 32
- Access Times: 10*, 12, 15, 20ns
- 3.3 ± 0.3** Volt Power Requirement
- Fully Static Operation - No clock or refresh required
- TTL-compatible Inputs and Outputs
- 80-Pin Surface Mount LP-Stack ™

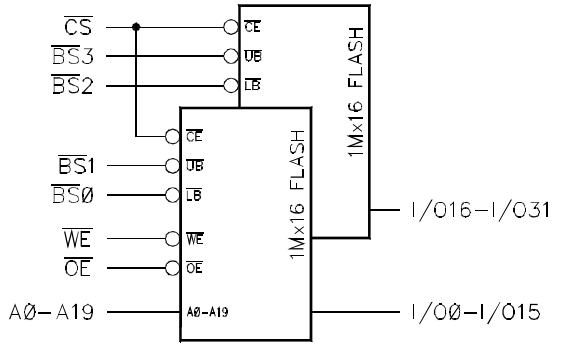
PIN NAMES	
A0 - A19	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CS}$	Stack Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{BS0}$	Byte Select I/O0 - I/O7
$\overline{BS1}$	Byte Select I/O8 - I/O15
$\overline{BS2}$	Byte Select I/O16 - I/O23
$\overline{BS3}$	Byte Select I/O24 - I/O31
V_{DD}	Power (+3.3V)
V_{SS}	Ground
NU.	Not Usable

* 0°-70° only.
** 5% for 10ns only.

PIN-OUT DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING RANGE [4]						
Symbol	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	Supply Voltage	10ns	3.135	3.3	3.465	V
		12, 15, 20ns	3.0	3.3	3.6	
V_{IH}	Input HIGH Voltage		2.0		$V_{DD}+0.3$[3]	V
V_{IL}	Input LOW Voltage		-0.3[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		CI	-40	+25	+85	

CAPACITANCE [5]: T_A = 25°C, F = 1.0MHz				
Symbol	**Parameter**	**Max.**	**Unit**	**Condition**
C_{ADR}	Address Input	20	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	20		
C_{BS}	Byte Select	15		
C_{WE}	Write Enable	20		
C_{OE}	Output Enable	20		
$C_{I/O}$	Data Input/Output	15		

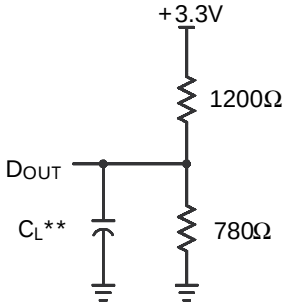
DC OUTPUT CHARACTERISTICS					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Unit**
V_{OH}	HIGH Voltage	I_{OH} = -2mA	2.4		V
V_{OL}	LOW Voltage	I_{OL} = +2mA		0.4	V

ABSOLUTE MAXIMUM RATINGS [4]			
Symbol	**Parameter**	**Value**	**Unit**
T_{STC}	Storage Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +4.6	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to +4.6	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	2ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	30pF	except t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

Figure 1. Output Load
** Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges					
Symbol	**Characteristics**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}, V_{DD} = max.	-2	+2	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, V_{DD} = max., $\overline{CE}$ = V_{IH}	-1	+1	µA
I_{CC}	Dynamic Operating Current	$\overline{CE}$ = V_{IL}, V_{DD} = max. I_{OUT} = 0mA, f = f max.		900	mA
I_{SB1}	Full Standby Supply Current (CMOS)	f = 0, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE} \geq V_{DD}$ -0.2V		8	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, f = f max.		210	mA
V_{OL}	Output Low Voltage	I_{OUT} = +2.0mA		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -2.0mA	2.4		V

ADVANCED INFORMATION

TRUTH TABLE												
Mode	**$\overline{CS}$**	**$\overline{OE}$**	**$\overline{WE}$**	**$\overline{BS0}$**	**$\overline{BS1}$**	**$\overline{BS2}$**	**$\overline{BS3}$**	**I/O0-I/O7**	**I/O8-I/O15**	**I/O16-I/O23**	**I/O24-I/O31**	**Supply Current**
Read	L	L	H	L	L	L	L	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Active
				H	L	L	L	High-Z	D_{OUT}	D_{OUT}	D_{OUT}	
				L	H	L	L	D_{OUT}	High-Z	D_{OUT}	D_{OUT}	
				L	L	H	L	D_{OUT}	D_{OUT}	High-Z	D_{OUT}	
				L	L	L	H	D_{OUT}	D_{OUT}	D_{OUT}	High-Z	
Write	L	X	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Active
				H	L	L	L	High-Z	D_{IN}	D_{IN}	D_{IN}	
				L	H	L	L	D_{IN}	High-Z	D_{IN}	D_{IN}	
				L	L	H	L	D_{IN}	D_{IN}	High-Z	D_{IN}	
				L	L	L	H	D_{IN}	D_{IN}	D_{IN}	High-Z	
Output Data	L	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Active
	L	X	X	H	H	H	H	High-Z	High-Z	High-Z	High-Z	
Standby	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Standby

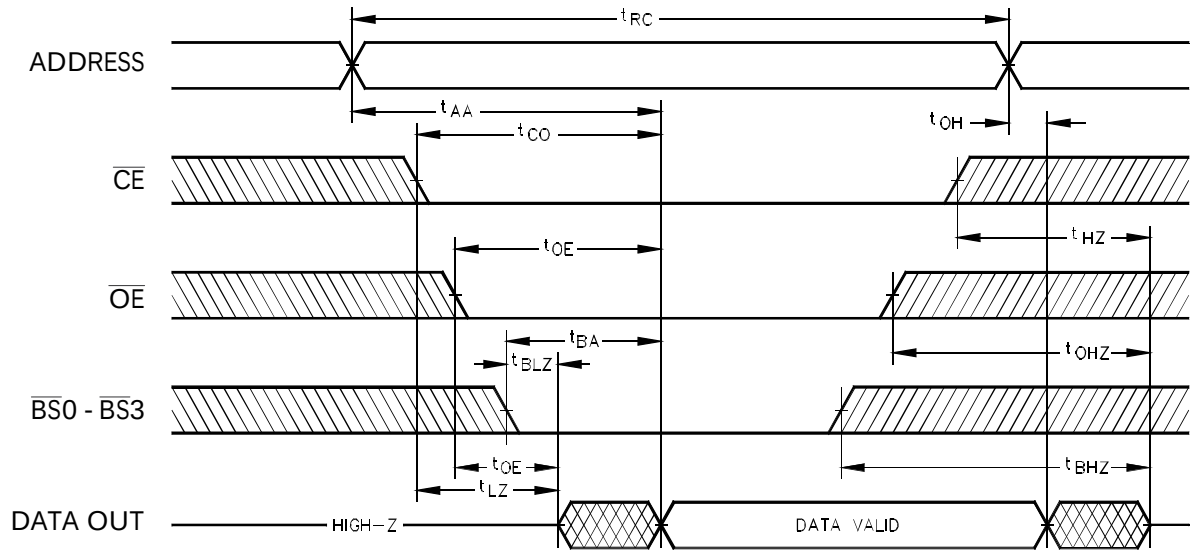
H = HIGH L = LOW X = Don t Care

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	**Symbol**	**Parameter**	**10ns**		**12ns**		**15ns**		**20ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	10		12		15		20		ns
2	t_{AA}	Address Access Time		10		12		15		20	ns
3	t_{CO}	$\overline{CE}$ to Output Valid		10		12		15		20	ns
4	t_{OE}	Output Enable to Output Valid		5		6		8		9	ns
5	t_{BA}	Byte Enable Access Time		5		6		8		9	ns
6	t_{LZ}	$\overline{CE}$ to Output in LOW-Z [5, 6]	3		3		3		3		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [5, 6]	1		1		1		1		ns
8	t_{BLZ}	Byte Enable to Output in LOW-Z	1		1		1		1		ns
9	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [5, 6]		6		7		8		9	ns
10	t_{OHZ}	Output Enable to Output in HIGH-Z [5, 6]		6		7		8		9	ns
11	t_{BHZ}	Byte Enable to Output in HIGH-Z		6		7		8		9	ns
12	t_{OH}	Output Hold from Address Change	3		3		3		3		ns

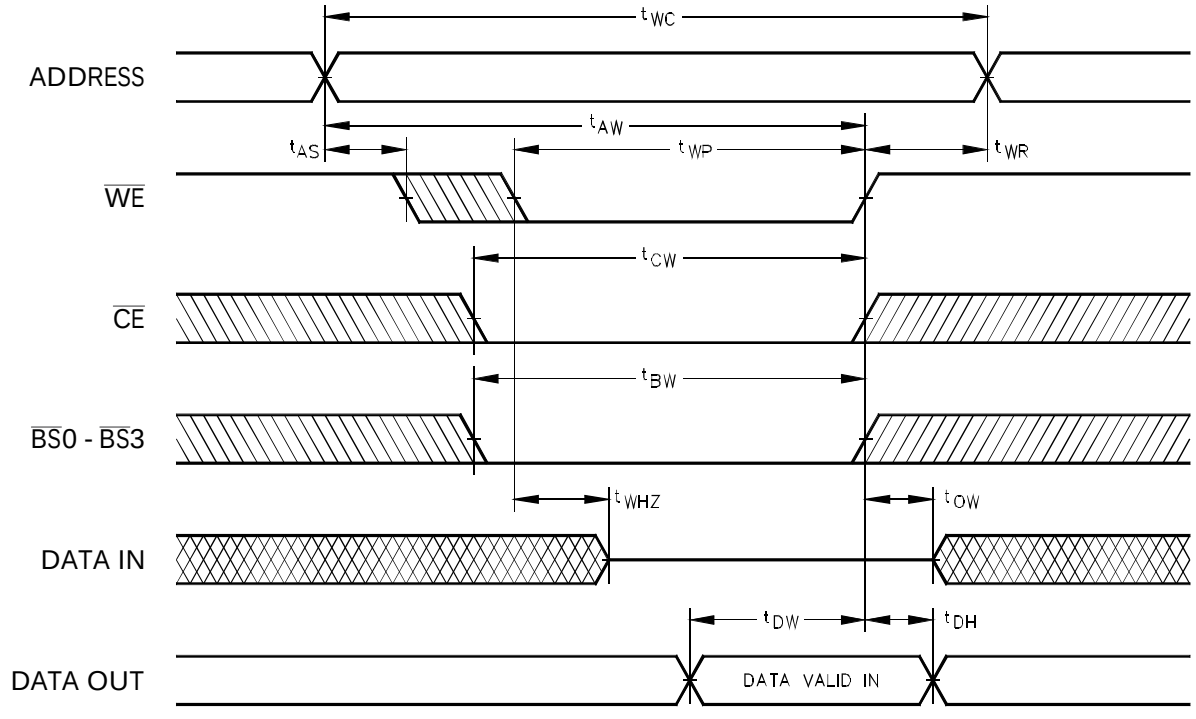
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [7, 8]**:** Over operating ranges											
No.	**Symbol**	**Parameter**	**10ns**		**12ns**		**15ns**		**20ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
13	t_{WC}	Write Cycle Time	10		12		15		20		ns
14	t_{AW}	Address Valid to End of Write	8.5		9		11		15		ns
15	t_{CW}	Chip Enable to End of Write	8.5		9		11		15		ns
16	t_{BW}	Byte Enable to End of Write	8.5		9		11		15		ns
17	t_{AS}	Address Set-Up Time *	0		0		0		0		ns
18	t_{WP}	Write Pulse Width ($\overline{OE}$ High)	7		8		10		12		ns
19	t_{WR}	Write Recovery Time, $\overline{CE}$, $\overline{WE}$	0		0		0		0		ns
20	t_{WHZ}	Write Enable to Output in HIGH-Z [5, 6]		6		7		8		10	ns
21	t_{DW}	Data to Write Time Overlap	6		7		8		10		ns
22	t_{DH}	Data Hold from Write Time	0		0		0		0		ns
23	t_{OW}	Output Active from End of Write	1		1		1		1		ns

* Valid for both Read and Write Cycles.

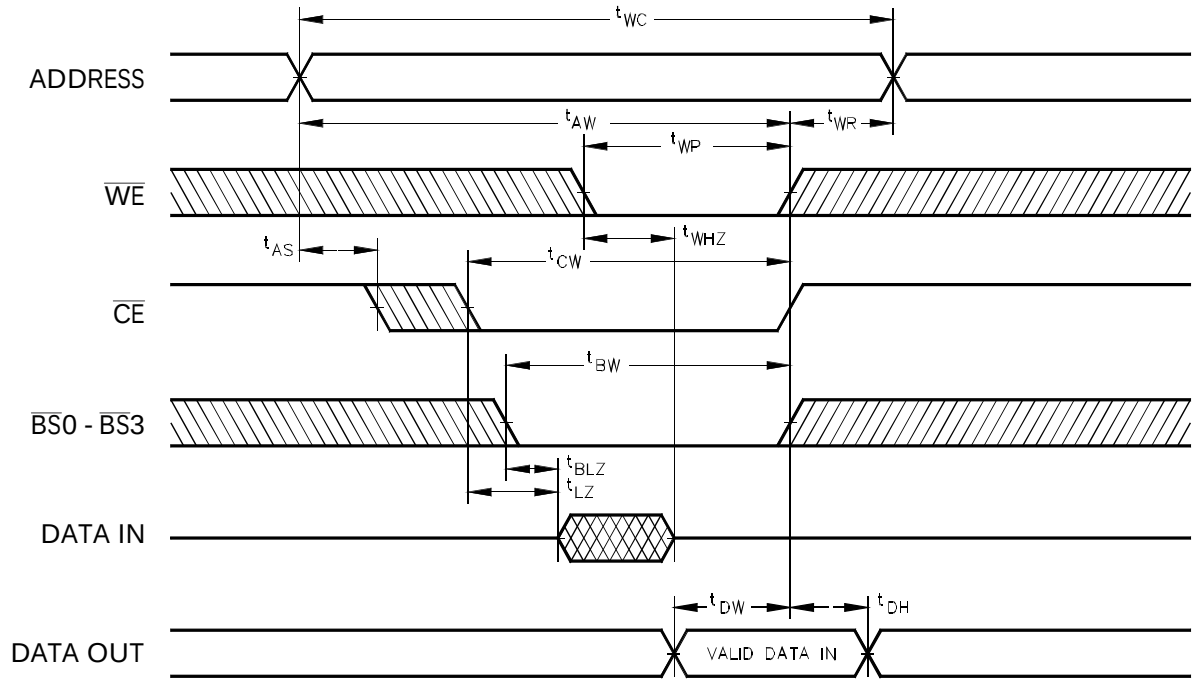
READ CYCLE



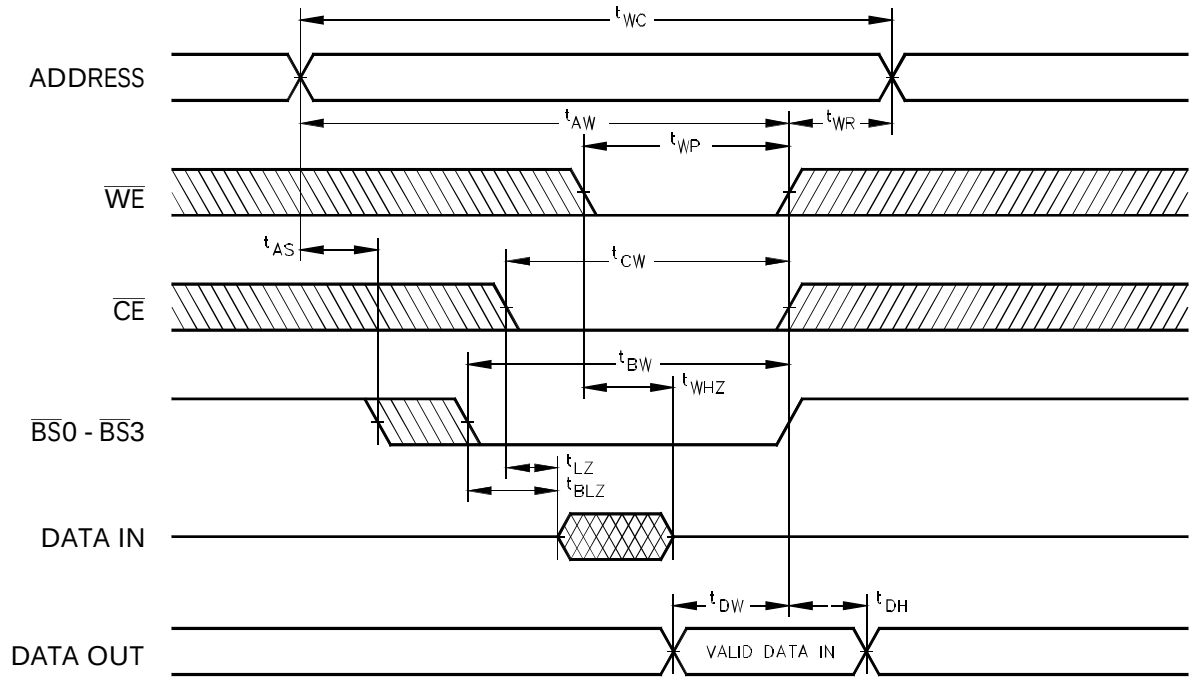
WRITE CYCLE 1: $\overline{WE}$ Controlled.



WRITE CYCLE 2: $\overline{CE}$ Controlled.

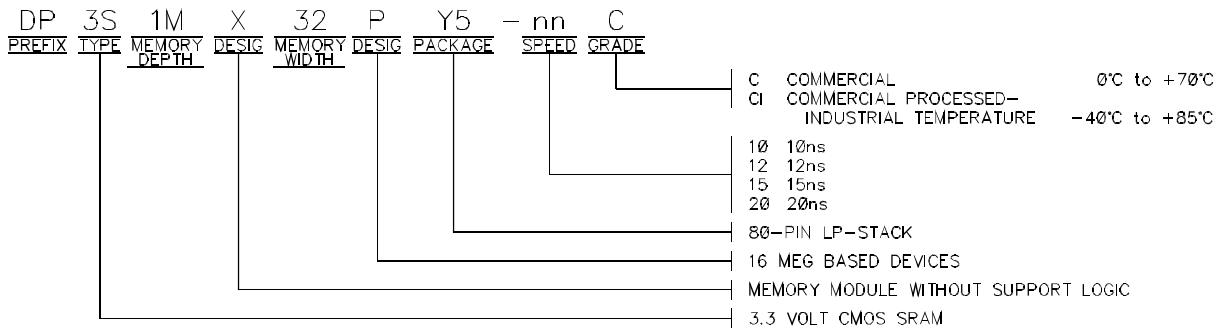


WRITE CYCLE 3: $\overline{UB}$, $\overline{LB}$ Controlled.



ADVANCED INFORMATION

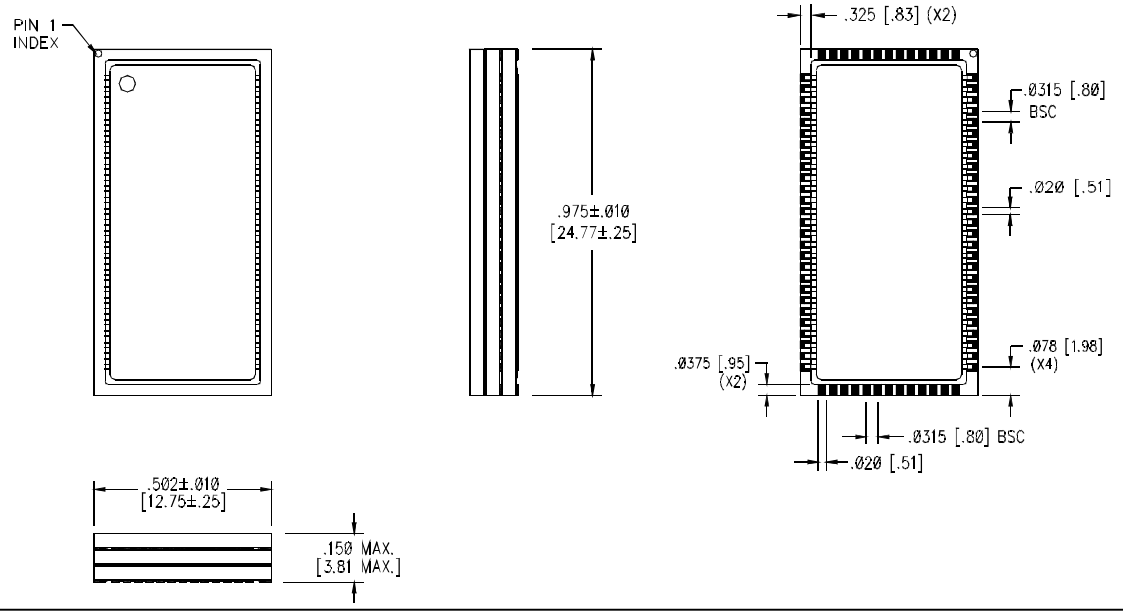
ORDERING INFORMATION



NOTES:

1. All voltages are with respect to V_{SS}.
2. -1.5V min. (Pulse Width ≤ 4ns) for I ≤ 20mA.
3. V_{IH} (max.) = V_{DD} + 1.5Vdc (Pulse Width ≤ 4ns) for I ≤ 20mA.
4. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. This parameter is guaranteed and not 100% tested.
6. Transition is measured at the point of ±500mV from steady state voltage.
7. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
9. Chip Enable and Write Enable can initiate and terminate WRITE Cycle.

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way, Garden Grove, California 92841-1431
(714) 898-0007 ◆ (800) 642-4477 ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com