

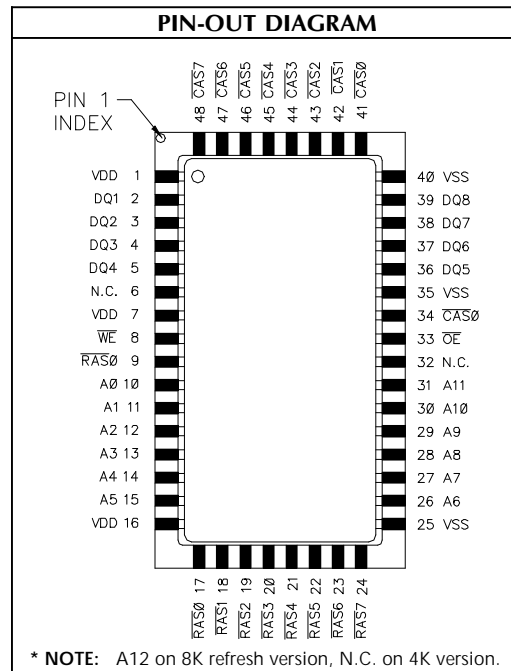
DESCRIPTION:

The *M-Densus* series is a family of interchangeable memory modules. The 64 Megabit DRAM is a member of this family which utilizes the new and innovative space saving TSOP technology. The modules are constructed with 8 Meg x 8 DRAM's available in 512, 256 and 128 Megabits.

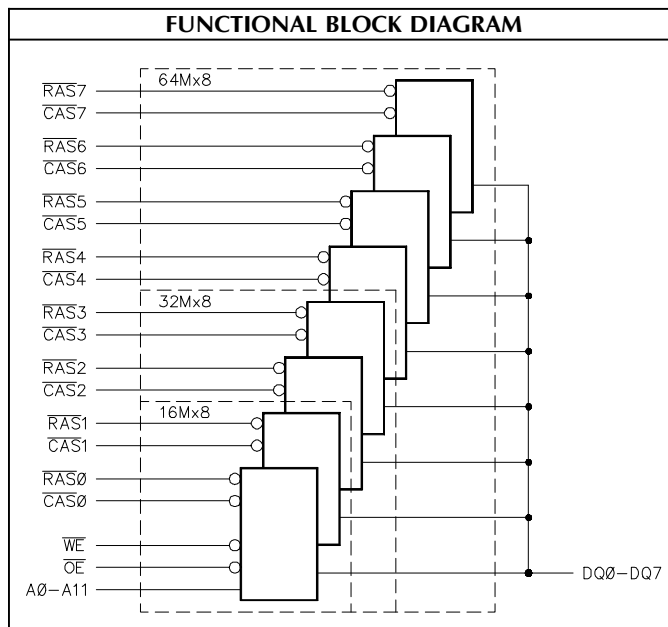
The 64 Megabit based *M-Densus* modules have been designed to fit in the same footprint as the 8 Meg x 8 DRAM TSOP monolithic and are backward compatible with the 16 Megabit based family of *M-Densus* modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

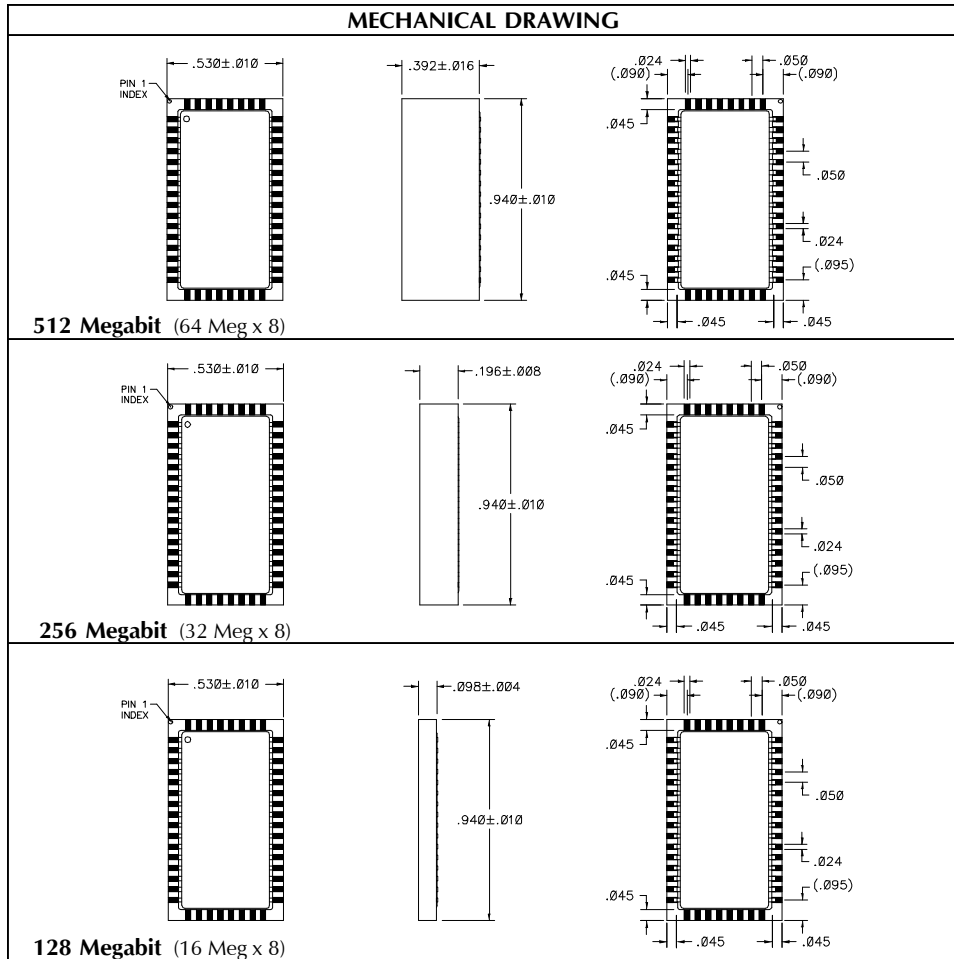
- Configurations Available:
 - 512 Megabit: 64 Meg x 8
 - 256 Megabit: 32 Meg x 8
 - 128 Megabit: 16 Meg x 8
- Access Times: 50, 60, 70ns (max.)
- 5.0V or 3.3V Supply
- Common Data Inputs and Outputs
- EDO or Fast Page Mode Capability
- 4096 Cycles / 64 ms
- 3 Variations of Refresh:
 - \overline{RAS} only Refresh
 - \overline{CAS} before \overline{RAS} Refresh
 - Hidden Refresh
- Package: Leadless TSOP Module



PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A11 Refresh Address: A0 - A11
DQ0 - DQ7	Data In / Data Out
$\overline{CAS0} - \overline{CAS7}$	Column Address Strobes
$\overline{RAS0} - \overline{RAS7}$	Row Address Enables
\overline{WE}	Data Write Enable
\overline{OE}	Data Output Enable
VDD	Power Supply (+5V/3.3V)
VSS	Ground
N.C.	No Connect



ORDERING INFORMATION										
DP	n	n	D	nM	X	8	R	Y5	-nn	C
PREFIX	DESIG	DESIG	TYPE	MEMORY	DESIG	MEMORY	DESIG	PACKAGE	SPEED	GRADE
				DEPTH		WIDTH				
										C COMMERCIAL 0°C to +70°C
									50	50ns
									60	60ns
									70	70ns
								Y5		STACKABLE TSOP (T-STACK)
							R			64 MEGABIT BASED
										MEMORY MODULE WITHOUT SUPPORT LOGIC
									64	64 MEG
									32	32 MEG
									16	16 MEG
										CMOS DRAM
										BLANK FAST PAGE
										E EDO
										BLANK 5.0 VOLT
										3 3.3 VOLT



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