



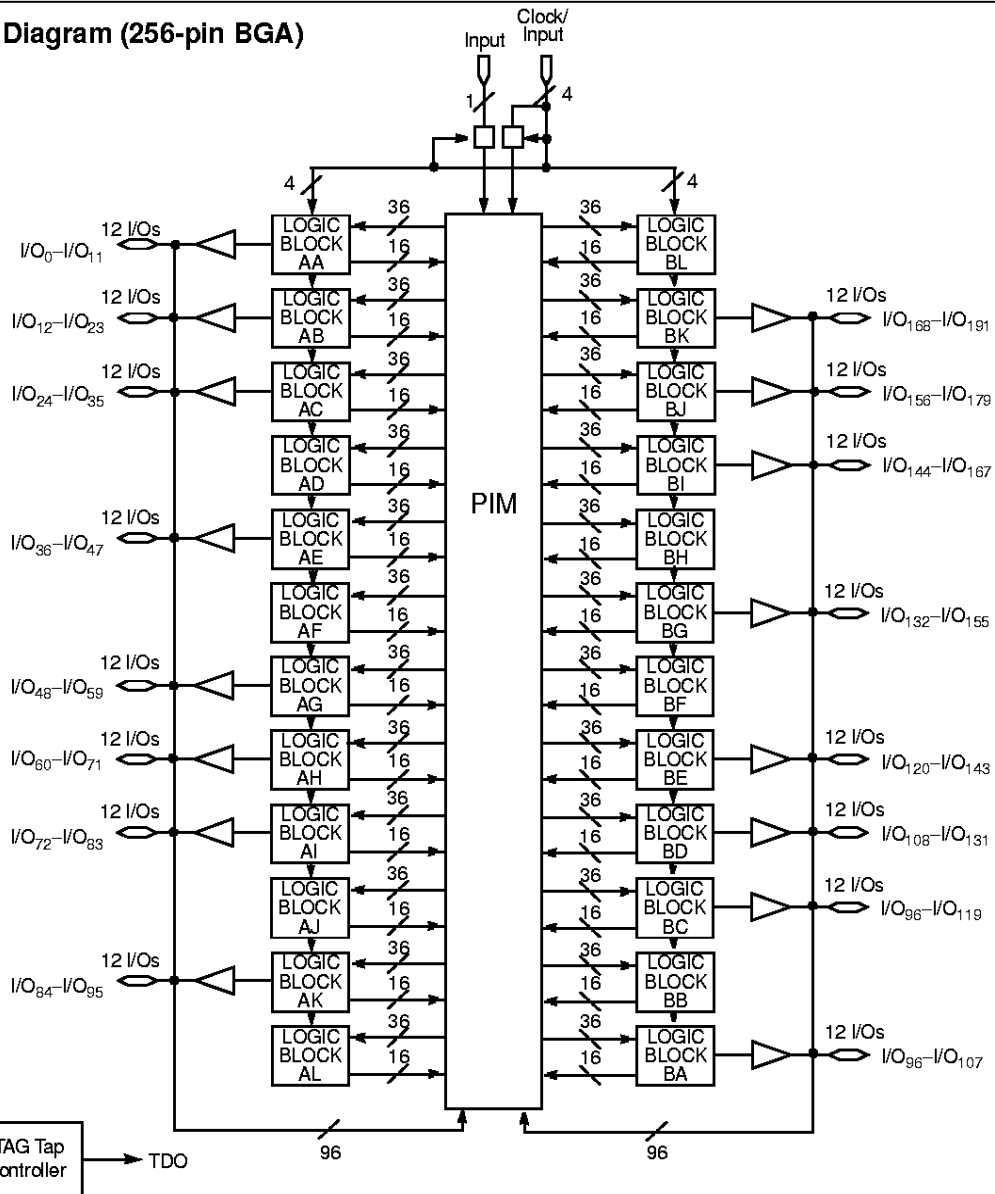
UltraLogic™ 384-Macrocell ISR™ CPLD

Features

- 384 macrocells in 24 logic blocks
- In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- Up to 192 I/Os
  - plus 5 dedicated inputs including 4 clock inputs
- High speed
  - $f_{MAX} = 125 \text{ MHz}$
  - $t_{PD} = 10 \text{ ns}$

- $t_S = 5.5 \text{ ns}$
- $t_{CO} = 6 \text{ ns}$
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- 5V and 3.3V I/O capability
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant
- Available in 208-pin PQFP and 256-lead BGA packages
- Pinout compatible with the CY37384V, CY37256/37256V, CY37512/37512V

Logic Block Diagram (256-pin BGA)



37384-1



## Selection Guide

	CY37384-154	CY37384-143	CY37384-125	CY37384-83
Maximum Propagation Delay, $t_{PD}$ (ns)	7.5	8.5	10	15
Minimum Set-Up, $t_S$ (ns)	5	5.0	5.5	8.0
Maximum Clock to Output, $t_{CO}$ (ns)	4.5	6.0	6.5	8.0
Typical Supply Current, $I_{CC}$ (mA) in Low Power Mode	120	180	180	180

Shaded areas contain advance information.

## Functional Description

The CY37384 is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37384 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

# of Pins	# Buried Macrocells	# I/O Macrocells	Package Types
208	224	160	PQFP
256	192	192	BGA

For a more detailed description of the architecture and features of the CY37384 see the Ultra37000 family data sheet.

### Fully Routable with 100% Logic Utilization

The CY37384 is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

### Simple Timing Model

The CY37384 features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

### Low Power Operation

Each Logic Block of the CY37384 can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes approximately 50% less power and slows down by  $t_{LP}$ .

### Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added

noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

### 3.3V or 5V I/O Operation

The CY37384 operates with a 5V supply, and can support 5V or 3.3V I/O levels.  $V_{CCO}$  connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the  $V_{CCO}$  pins to 5V the user insures 5V TTL levels on the outputs. If  $V_{CCO}$  is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. A nominal timing delay is incurred on output buffers when  $V_{CCO}$  is set to 3.3V. This device requires 5V ISR Programming.

### In System Reprogramming

The CY37384 can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37384 can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3™* programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to InSRkit: ISR programming data sheet (CY3600i).

### User-Programmable Bus Hold

All outputs of the CY37384 can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

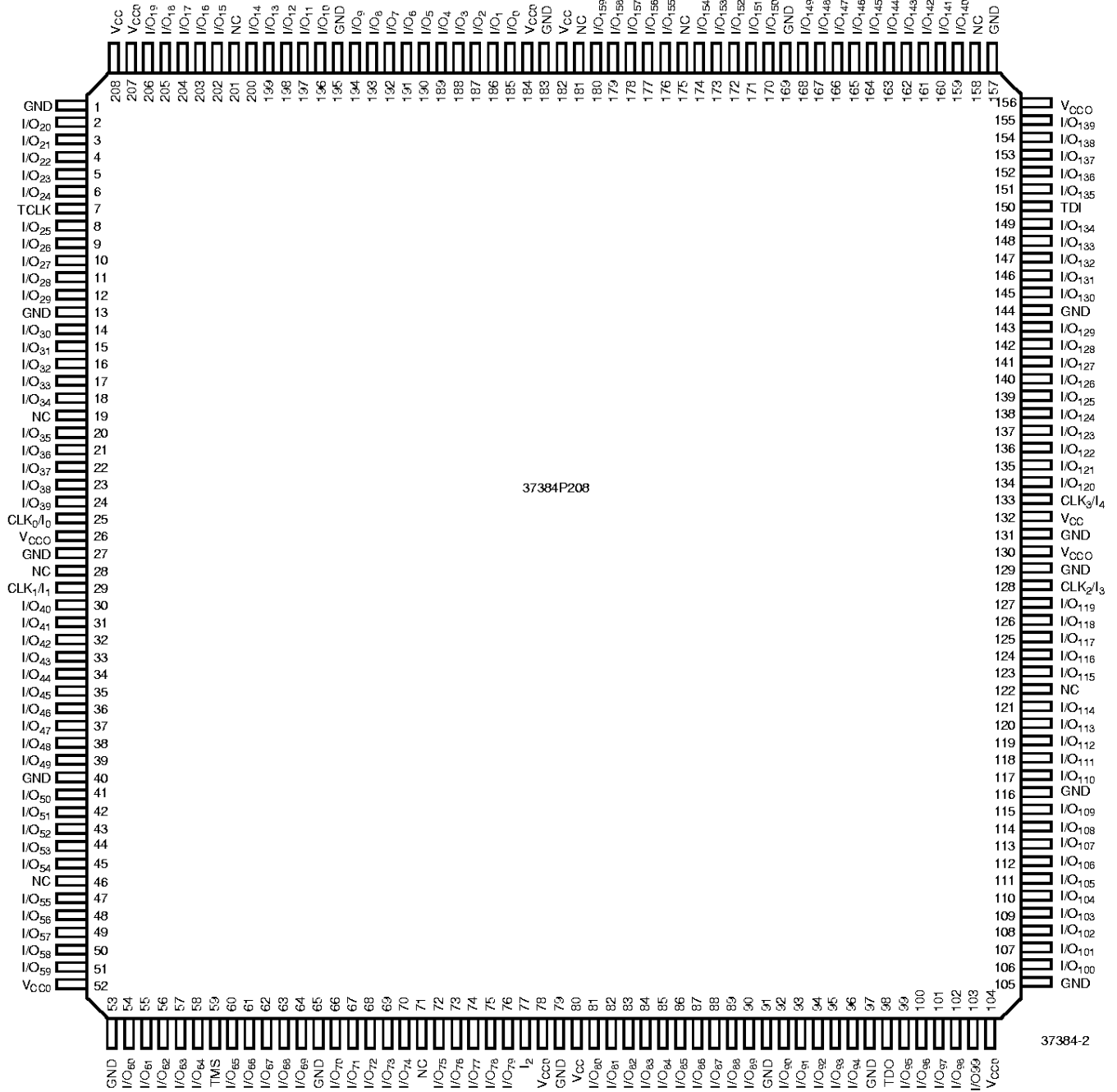
### Design Tools

Development software for the CY37384 is available from Cypress's *Warp™* or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.



Pin Configurations

208-pin PQFP  
Top View





Pin Configurations (continued)

256-ball BGA  
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O <sub>21</sub>	NC	I/O <sub>16</sub>	I/O <sub>12</sub>	I/O <sub>9</sub>	I/O <sub>7</sub>	I/O <sub>4</sub>	I/O <sub>0</sub>	I/O <sub>190</sub>	I/O <sub>189</sub>	I/O <sub>186</sub>	I/O <sub>182</sub>	NC	I/O <sub>178</sub>	I/O <sub>175</sub>	NC	NC	I/O <sub>169</sub>	I/O <sub>168</sub>	A
B	I/O <sub>23</sub>	I/O <sub>20</sub>	I/O <sub>19</sub>	I/O <sub>18</sub>	I/O <sub>15</sub>	I/O <sub>11</sub>	I/O <sub>8</sub>	I/O <sub>5</sub>	I/O <sub>1</sub>	I/O <sub>191</sub>	I/O <sub>187</sub>	I/O <sub>185</sub>	I/O <sub>181</sub>	NC	NC	I/O <sub>174</sub>	I/O <sub>171</sub>	I/O <sub>170</sub>	NC	I/O <sub>166</sub>	B
C	NC	NC	I/O <sub>22</sub>	NC	I/O <sub>17</sub>	I/O <sub>14</sub>	I/O <sub>10</sub>	I/O <sub>6</sub>	I/O <sub>2</sub>	NC	I/O <sub>188</sub>	I/O <sub>184</sub>	I/O <sub>180</sub>	I/O <sub>179</sub>	I/O <sub>176</sub>	I/O <sub>173</sub>	I/O <sub>172</sub>	I/O <sub>167</sub>	I/O <sub>165</sub>	I/O <sub>162</sub>	C
D	I/O <sub>24</sub>	NC	NC	GND	NC	V <sub>CC0</sub>	I/O <sub>13</sub>	GND	I/O <sub>3</sub>	NC	V <sub>CC</sub>	I/O <sub>183</sub>	GND	I/O <sub>177</sub>	V <sub>CC0</sub>	NC	GND	I/O <sub>164</sub>	TDI	I/O <sub>160</sub>	D
E	I/O <sub>27</sub>	I/O <sub>26</sub>	I/O <sub>25</sub>	NC													I/O <sub>183</sub>	I/O <sub>161</sub>	I/O <sub>159</sub>	I/O <sub>156</sub>	E
F	I/O <sub>30</sub>	TCK	I/O <sub>28</sub>	V <sub>CC0</sub>													V <sub>CC0</sub>	I/O <sub>158</sub>	NC	I/O <sub>154</sub>	F
G	I/O <sub>33</sub>	I/O <sub>32</sub>	I/O <sub>31</sub>	I/O <sub>29</sub>													I/O <sub>157</sub>	I/O <sub>155</sub>	I/O <sub>153</sub>	I/O <sub>152</sub>	G
H	I/O <sub>35</sub>	NC	I/O <sub>34</sub>	GND													GND	I/O <sub>151</sub>	I/O <sub>150</sub>	I/O <sub>149</sub>	H
J	I/O <sub>39</sub>	I/O <sub>38</sub>	I/O <sub>37</sub>	I/O <sub>36</sub>													I/O <sub>148</sub>	I/O <sub>147</sub>	I/O <sub>146</sub>	I/O <sub>145</sub>	J
K	I/O <sub>42</sub>	I/O <sub>40</sub>	I/O <sub>41</sub>	V <sub>CC</sub>													I/O <sub>144</sub>	CLK <sub>3</sub> /I <sub>4</sub>	NC	NC	K
L	I/O <sub>43</sub>	I/O <sub>44</sub>	I/O <sub>45</sub>	I/O <sub>46</sub>													V <sub>CC</sub>	CLK <sub>2</sub> /I <sub>3</sub>	I/O <sub>143</sub>	NC	L
M	I/O <sub>47</sub>	CLK <sub>0</sub> /I <sub>0</sub>	CLK <sub>1</sub> /I <sub>1</sub>	I/O <sub>48</sub>													I/O <sub>139</sub>	I/O <sub>140</sub>	I/O <sub>141</sub>	I/O <sub>142</sub>	M
N	I/O <sub>49</sub>	I/O <sub>50</sub>	I/O <sub>51</sub>	GND													GND	I/O <sub>136</sub>	I/O <sub>137</sub>	I/O <sub>138</sub>	N
P	I/O <sub>52</sub>	I/O <sub>53</sub>	I/O <sub>55</sub>	I/O <sub>58</sub>													I/O <sub>131</sub>	I/O <sub>133</sub>	I/O <sub>134</sub>	I/O <sub>135</sub>	P
R	I/O <sub>54</sub>	I/O <sub>56</sub>	I/O <sub>59</sub>	V <sub>CC0</sub>													V <sub>CC0</sub>	I/O <sub>130</sub>	NC	I/O <sub>132</sub>	R
T	I/O <sub>57</sub>	I/O <sub>60</sub>	I/O <sub>62</sub>	I/O <sub>65</sub>													I/O <sub>124</sub>	I/O <sub>127</sub>	I/O <sub>128</sub>	I/O <sub>129</sub>	T
U	I/O <sub>61</sub>	I/O <sub>63</sub>	I/O <sub>66</sub>	GND	I/O <sub>76</sub>	V <sub>CC0</sub>	I/O <sub>82</sub>	GND	I/O <sub>91</sub>	V <sub>CC</sub>	I/O <sub>98</sub>	I/O <sub>102</sub>	GND	I/O <sub>112</sub>	V <sub>CC0</sub>	NC	GND	I/O <sub>123</sub>	I/O <sub>122</sub>	I/O <sub>126</sub>	U
V	I/O <sub>64</sub>	I/O <sub>67</sub>	I/O <sub>69</sub>	I/O <sub>75</sub>	I/O <sub>78</sub>	I/O <sub>81</sub>	I/O <sub>85</sub>	I/O <sub>88</sub>	I/O <sub>92</sub>	I <sub>2</sub>	I/O <sub>97</sub>	I/O <sub>101</sub>	I/O <sub>105</sub>	I/O <sub>109</sub>	I/O <sub>113</sub>	TDO	I/O <sub>114</sub>	I/O <sub>117</sub>	I/O <sub>121</sub>	I/O <sub>125</sub>	V
W	I/O <sub>68</sub>	I/O <sub>70</sub>	I/O <sub>72</sub>	I/O <sub>74</sub>	I/O <sub>79</sub>	I/O <sub>83</sub>	I/O <sub>86</sub>	I/O <sub>89</sub>	I/O <sub>93</sub>	I/O <sub>95</sub>	I/O <sub>96</sub>	I/O <sub>100</sub>	I/O <sub>104</sub>	I/O <sub>107</sub>	I/O <sub>110</sub>	NC	NC	I/O <sub>115</sub>	I/O <sub>118</sub>	I/O <sub>120</sub>	W
Y	I/O <sub>71</sub>	I/O <sub>73</sub>	I/O <sub>77</sub>	TMS	I/O <sub>80</sub>	I/O <sub>84</sub>	I/O <sub>87</sub>	I/O <sub>90</sub>	I/O <sub>94</sub>	NC	NC	I/O <sub>99</sub>	I/O <sub>103</sub>	I/O <sub>106</sub>	I/O <sub>108</sub>	I/O <sub>111</sub>	NC	NC	I/O <sub>116</sub>	I/O <sub>119</sub>	Y

\*NOTE: Center pins must be connected to GND to aid thermal dissipation.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to +7.0V  
 DC Program Voltage ..... 4.5V to 5.5V  
 Current into Outputs ..... 16 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range<sup>[1]</sup>**

Range	Ambient Temperature <sup>[1]</sup>	Junction Temperature	Output Condition	V <sub>CC</sub>	V <sub>CCO</sub>
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	-40°C to +85°C	-40°C to +125°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

**Note:**

1. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.



**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min. I <sub>OH</sub> = -3.2 mA (Com'I/Ind) <sup>[2]</sup>	2.4			V
V <sub>OHZ</sub>	Output HIGH Voltage with Output Disabled <sup>[6]</sup>	V <sub>CC</sub> = Max. I <sub>OH</sub> = 0 μA (Com'I/Ind) <sup>[3]</sup>			4.0	V
		I <sub>OH</sub> = -50 μA (Com'I/Ind) <sup>[3]</sup>			3.6	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. I <sub>OL</sub> = 16 mA (Com'I/Ind) <sup>[2]</sup>			0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs <sup>[4]</sup>	2.0		V <sub>CCmax</sub>	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs <sup>[4]</sup>	-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	V <sub>I</sub> = GND OR V <sub>CC</sub>	-10		10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>O</sub> = GND or V <sub>CC</sub> , Output Disabled	-50		50	μA
		V <sub>CC</sub> = Max., V <sub>O</sub> = 3.3V, Output Disabled <sup>[3]</sup>	0	-70	-125	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[5, 6]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V	-30		-160	mA
I <sub>BHL</sub>	Input Bus Hold LOW Sustaining Current	V <sub>CC</sub> = Min., V <sub>IL</sub> = 0.8V	+75			μA
I <sub>BHH</sub>	Input Bus Hold HIGH Sustaining Current	V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V	-75			μA
I <sub>BHLO</sub>	Input Bus Hold LOW Overdrive Current	V <sub>CC</sub> = Max.			+500	μA
I <sub>BHHO</sub>	Input Bus Hold HIGH Overdrive Current	V <sub>CC</sub> = Max.			-500	μA

**Inductance<sup>[6]</sup>**

Parameter	Description	Test Conditions	208-lead BGA	Unit
L	Maximum Pin Inductance	V <sub>IN</sub> = 5.0V at f = 1 MHz	11	nH

**Capacitance<sup>[6]</sup>**

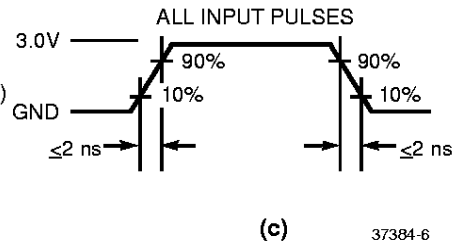
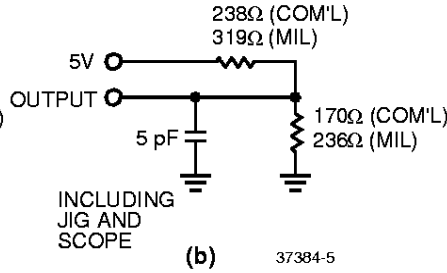
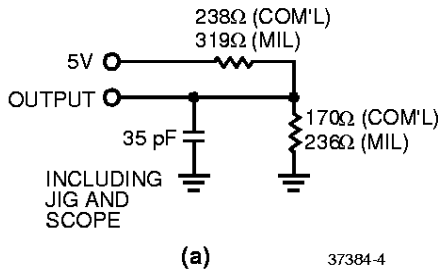
Parameter	Description	Test Conditions	Max.	Unit
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz at T <sub>A</sub> = 25°C	8	pF
C <sub>CLK</sub>	Clock Signal Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz at T <sub>A</sub> = 25°C	12	pF

**Endurance Characteristics<sup>[6]</sup>**

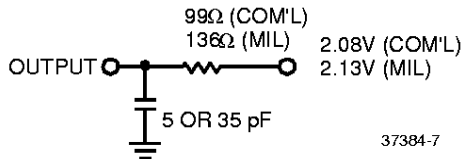
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions <sup>[1]</sup>	1,000	10,000	Cycles

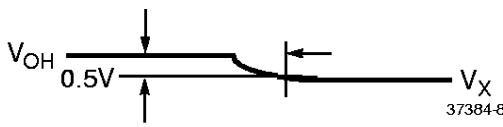
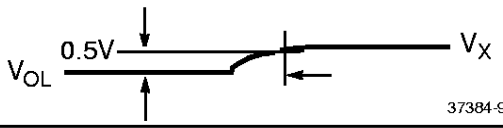
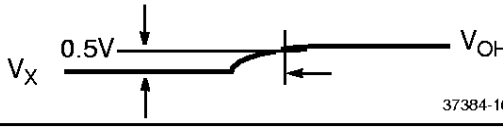
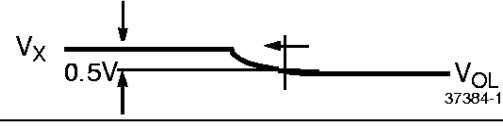
**Notes:**

- I<sub>OH</sub> = -2 mA, I<sub>OL</sub> = 2 mA for TDO.
- When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT



Parameter <sup>[7]</sup>	$V_X$	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	$V_{the}$	

**(d) Test Waveforms**
**Note:**

 7.  $t_{ER}$  measured with 5-pF AC Test Load and  $t_{EA}$  measured with 35-pF AC Test Load.



Switching Characteristics Over the Operating Range<sup>[8]</sup>

Parameter	Description	37384-154		37384-143		37384-125		37384-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Combinatorial Mode Parameters</b>										
$t_{PD}^{[9, 10, 11]}$	Input to Combinatorial Output		7.5		8.5		10		15	ns
$t_{PDL}^{[9, 10, 11]}$	Input to Output Through Transparent Input or Output Latch		12		12		13		18	ns
$t_{PDLL}^{[9, 10, 11]}$	Input to Output Through Transparent Input and Output Latches		13		13.5		15		19	ns
$t_{EA}^{[9, 10, 11]}$	Input to Output Enable		11		13		14		19	ns
$t_{ER}^{[9]}$	Input to Output Disable		11		13		14		19	ns
<b>Input Register Parameters</b>										
$t_{WL}$	Clock or Latch Enable Input LOW Time <sup>[6]</sup>	2.5		2.5		3		4		ns
$t_{WH}$	Clock or Latch Enable Input HIGH Time <sup>[6]</sup>	2.5		2.5		3		4		ns
$t_{IS}$	Input Register or Latch Set-Up Time	2		2		2		3		ns
$t_{IH}$	Input Register or Latch Hold Time	2		2		2		3		ns
$t_{ICO}^{[9, 10, 11]}$	Input Register Clock or Latch Enable to Combinatorial Output		11		12.5		12.5		19	ns
$t_{ICOL}^{[9, 10, 11]}$	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		12		14		16		21	ns
<b>Synchronous Clocking Parameters</b>										
$t_{CO}^{[10, 11]}$	Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Output		4.5		6		6.5		8	ns
$t_S^{[9]}$	Set-Up Time from Input to Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable	5		5		5.5		8		ns
$t_H$	Register or Latch Data Hold Time	0		0		0		0		ns
$t_{CO2}^{[9, 10, 11]}$	Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		11		12		14		19	ns
$t_{SCS}^{[9]}$	Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable (Through Logic Array)	6.5		7		8		12		ns
$t_{SL}^{[9]}$	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable	8.5		9		10		15		ns
$t_{HL}$	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable	0		0		0		0		ns
<b>Product Term Clocking Parameters</b>										
$t_{COPT}^{[9, 10, 11]}$	Product Term Clock or Latch Enable (PTCLK) to Output		10		13		13		15	ns
$t_{SPT}$	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	2.5		3		3		4.5		ns

Shaded areas contain advance information.

Notes:

- 8. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
- 9. Logic Blocks operating in low power mode, add  $t_{LP}$  to this spec.
- 10. Outputs using Slow Output Slew Rate, add  $t_{SLEW}$  to this spec.
- 11. When  $V_{CC0} = 3.3V$ , add  $t_{3.3V0}$  to this spec.



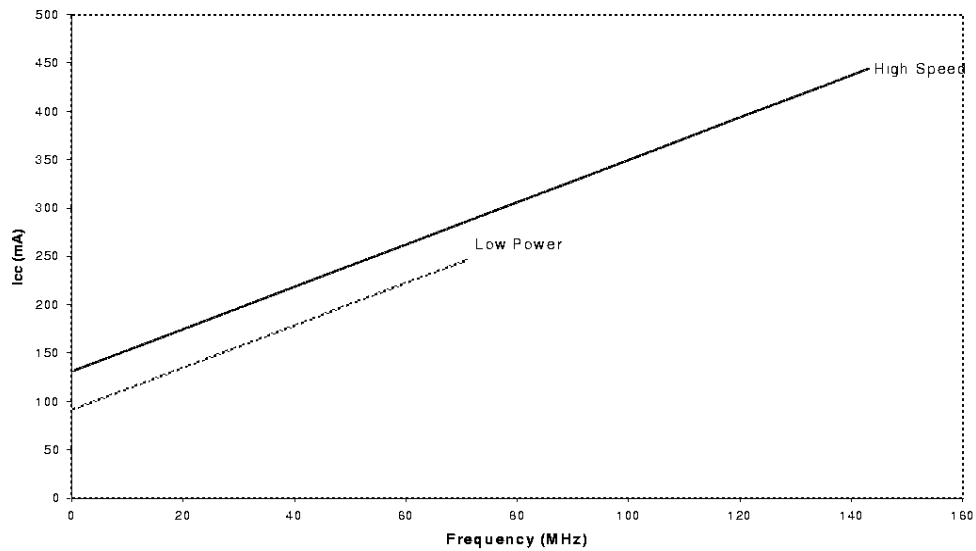


Switching Characteristics Over the Operating Range<sup>[8]</sup> (continued)

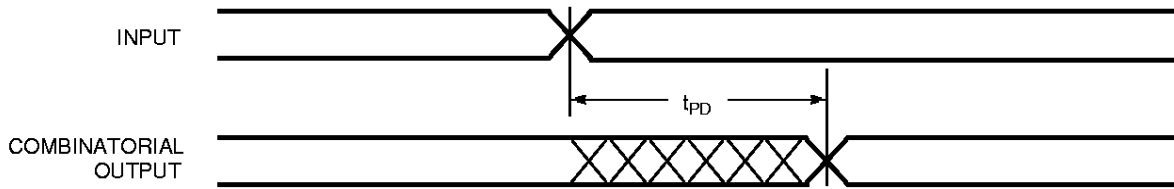
Parameter	Description	37384-154		37384-143		37384-125		37384-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HPT</sub>	Register or Latch Data Hold Time	2.5		3		3		4.5		ns
t <sub>ISPT</sub> <sup>[9]</sup>	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		-2		-2		-2		-2	ns
t <sub>IHPT</sub>	Buried Register Used as an Input Register or Latch Data Hold Time		6.5		7.5		9		14	ns
t <sub>CO2PT</sub> <sup>[9, 10, 11]</sup>	Product Term Clock or Latch Enable (PT-CLK) to Output Delay (Through Logic Array)		15		19		19		24	ns
<b>Pipelined Mode Parameters</b>										
t <sub>ICS</sub> <sup>[9]</sup>	Input Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) to Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> )	6		7		8		12		ns
<b>Operating Frequency Parameters</b>										
f <sub>MAX1</sub>	Maximum Frequency with Internal Feedback (Lesser of 1/t <sub>SCS</sub> , 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> ) <sup>[6]</sup>	154		143		125		83		MHz
f <sub>MAX2</sub>	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> )	200		167		158		125		MHz
f <sub>MAX3</sub>	Maximum Frequency with External Feedback (Lesser of 1/(t <sub>CO</sub> + t <sub>S</sub> ) or 1/(t <sub>WL</sub> + t <sub>WH</sub> ))	105		91		83		67		MHz
f <sub>MAX4</sub>	Maximum Frequency in Pipelined Mode (Lesser of 1/(t <sub>CO</sub> + t <sub>IS</sub> ), 1/t <sub>ICS</sub> , 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>IS</sub> + t <sub>IH</sub> ), or 1/t <sub>SCS</sub> )	143		125		125		67		MHz
<b>Reset/Preset Parameters</b>										
t <sub>RW</sub>	Asynchronous Reset Width <sup>[6]</sup>	8		8		10		15		ns
t <sub>RR</sub> <sup>[9]</sup>	Asynchronous Reset Recovery Time <sup>[6]</sup>	10		10		12		17		ns
t <sub>RO</sub> <sup>[9, 10, 11]</sup>	Asynchronous Reset to Output		12		14		15		21	ns
t <sub>PW</sub>	Asynchronous Preset Width <sup>[6]</sup>	8		8		10		15		ns
t <sub>PR</sub> <sup>[9]</sup>	Asynchronous Preset Recovery Time <sup>[6]</sup>	10		10		12		17		ns
t <sub>PO</sub> <sup>[9, 10, 11]</sup>	Asynchronous Preset to Output		12		14		15		21	ns
<b>User Option Parameters</b>										
t <sub>LP</sub>	Low Power Adder		4		4		4		4	ns
t <sub>SLEW</sub>	Slow Output Slew Rate Adder		2		2		2		2	ns
t <sub>3.3IO</sub>	3.3V I/O Mode Timing Adder		0.1		0.1		0.1		0.1	ns
<b>JTAG Timing Parameters</b>										
t <sub>S JTAG</sub>	Set-Up Time from TDI and TMS to TCK	0		0		0		0		ns
t <sub>H JTAG</sub>	Hold Time on TDI and TMS	20		20		20		20		ns
t <sub>CO JTAG</sub>	Falling Edge of TCK to TDO		20		20		20		20	ns
f <sub>JTAG</sub>	Maximum JTAG Tap Controller Frequency		20		20		20		20	MHz

Shaded areas contain advance information.

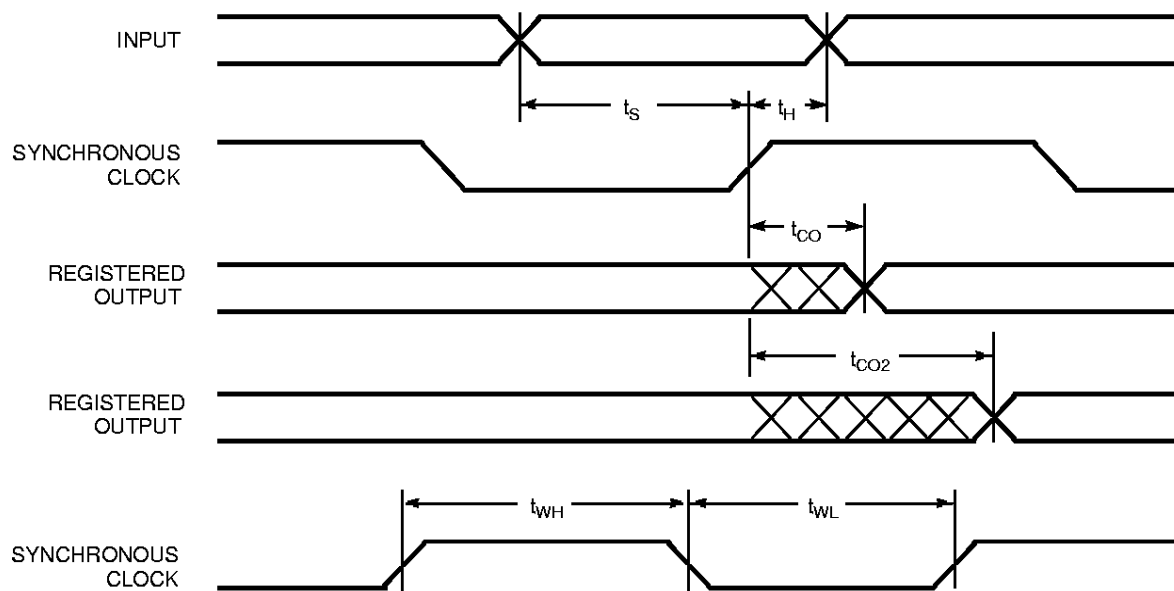
## Typical $I_{CC}$ Characteristics



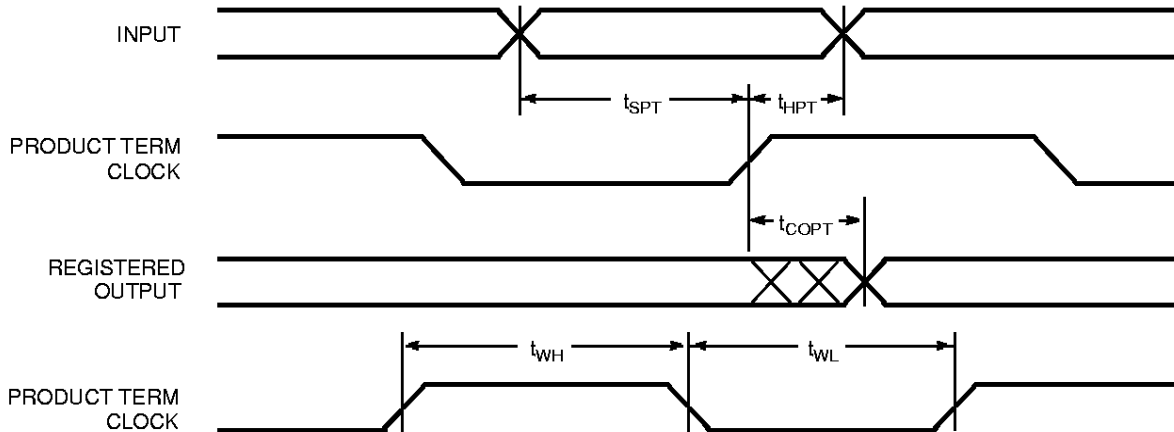
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 5.0V$ ,  $T_A = \text{Room Temperature}$

**Switching Waveforms**
**Combinatorial Output**


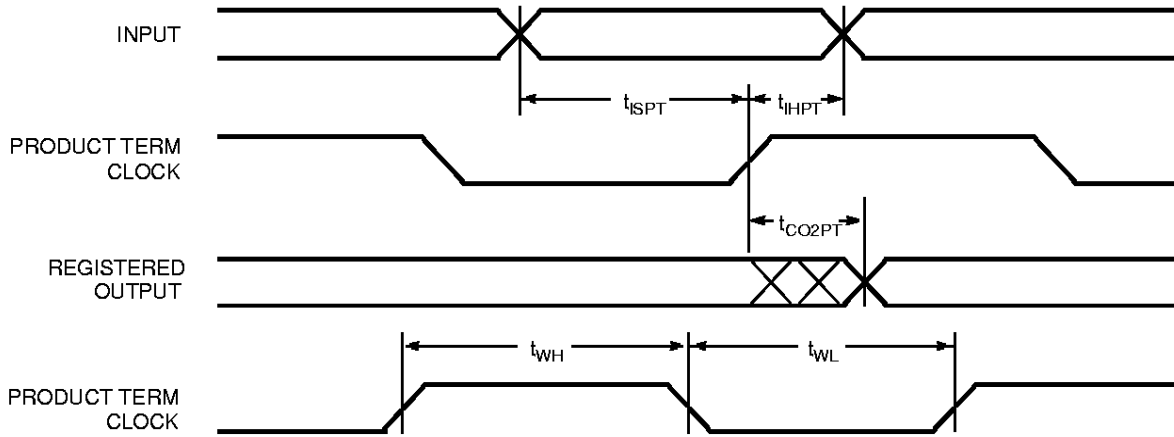
37384-13

**Registered Output with Synchronous Clocking**


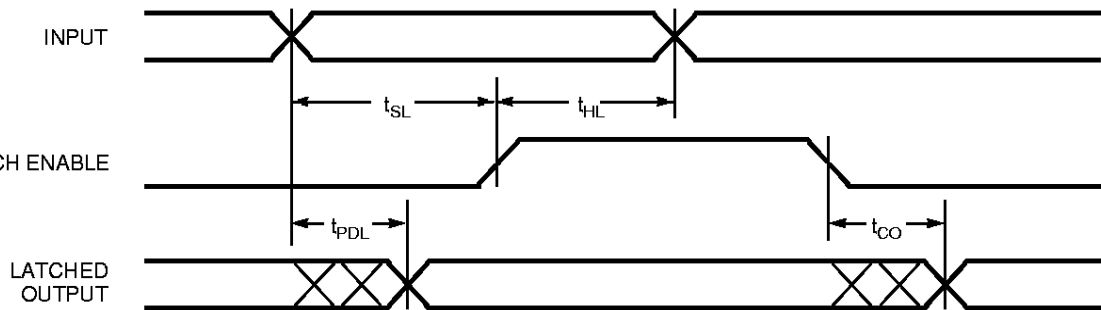
37384-14

**Registered Output with Product Term Clocking  
Input Going Through the Array**


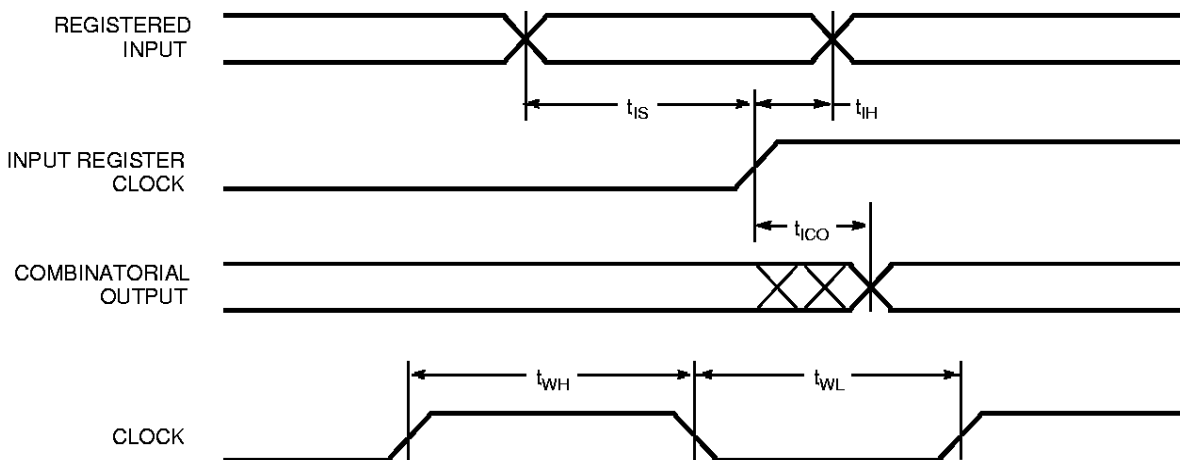
37384-15

**Switching Waveforms (continued)**
**Registered Output with Product Term Cloning  
Input Coming From Adjacent Buried Register**


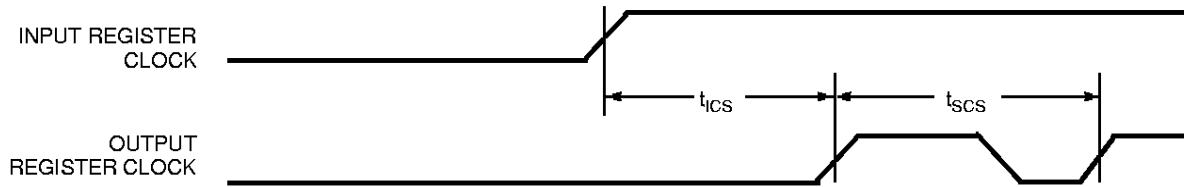
37384-16

**Latched Output**


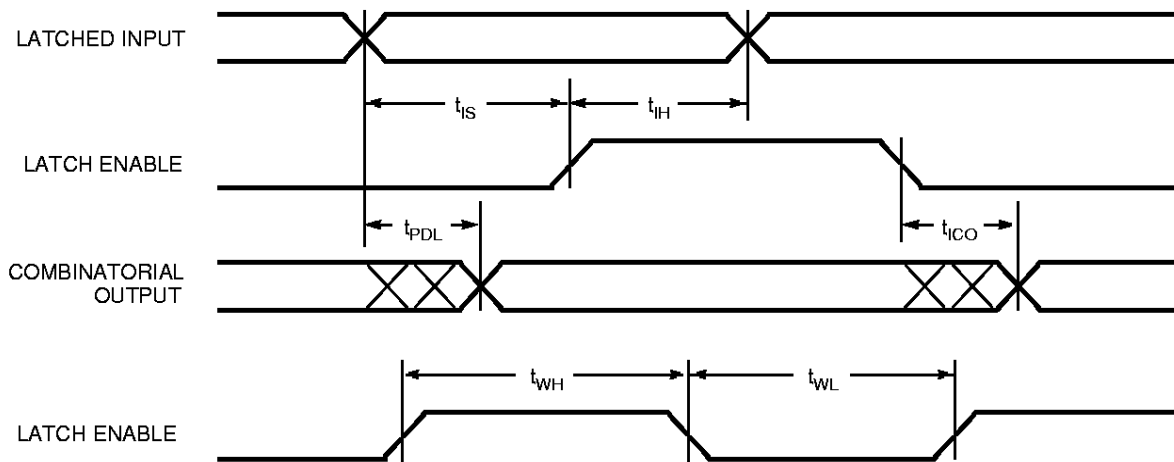
37384-17

**Registered Input**


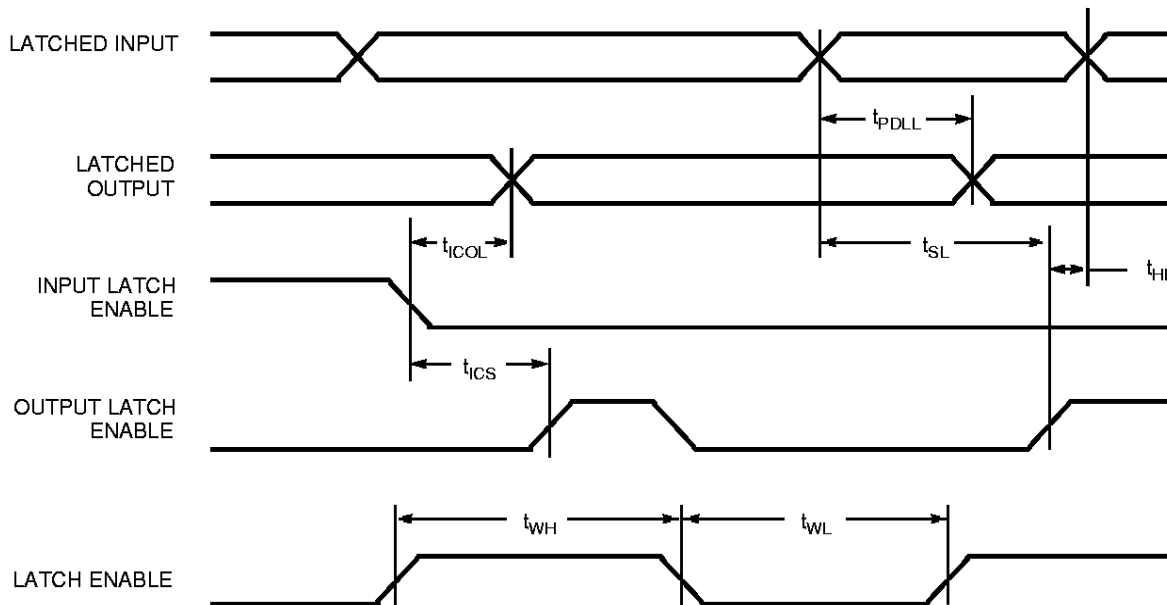
37384-18

**Switching Waveforms (continued)**
**Clock to Clock**


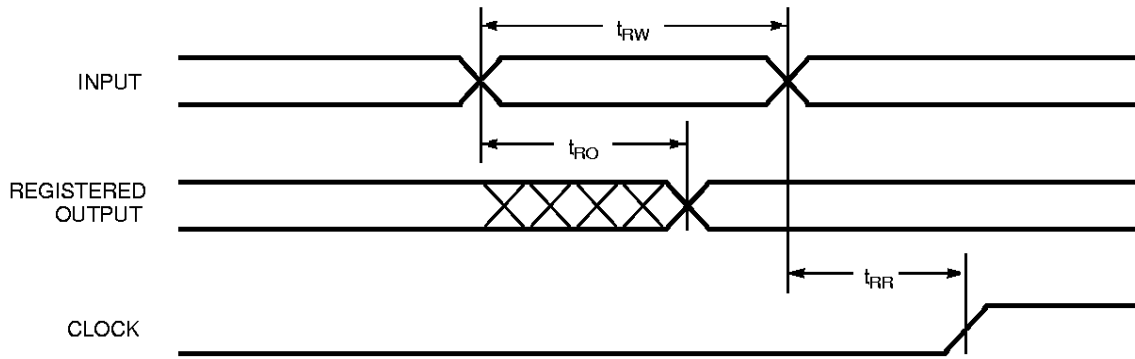
37384-19

**Latched Input**


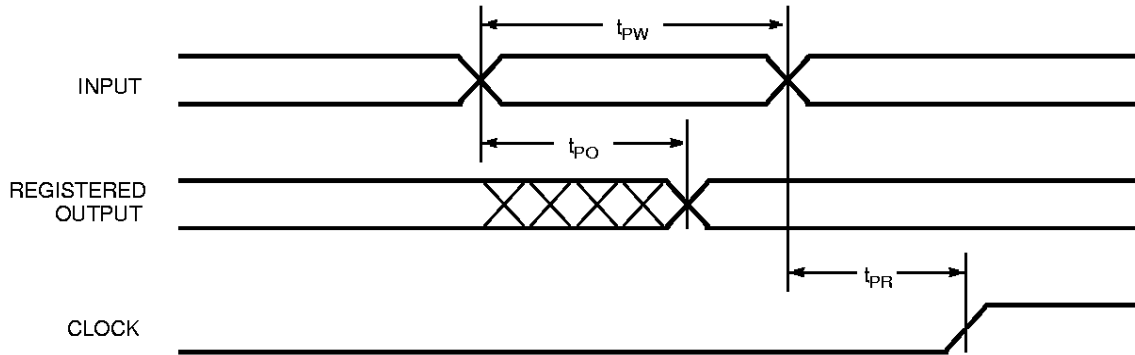
37384-20

**Latched Input and Output**


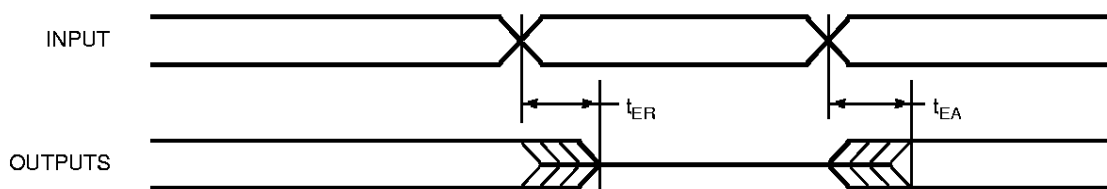
37384-21

**Switching Waveforms (continued)**
**Asynchronous Reset**


37384-22

**Asynchronous Preset**


37384-23

**Output Enable/Disable**


37384-24

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
154	CY37384P208-154NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37384P256-154BGC	BG256	256-Pin Ball Grid Array	
143	CY37384P208-143NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37384P256-143BGC	BG256	256-Pin Ball Grid Array	
125	CY37384P208-125NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37384P256-125BGC	BG256	256-Pin Ball Grid Array	
	CY37384P208-125NI	N208	208-Pin Plastic Quad Flatpack	Industrial
	CY37384P256-125BGI	BG256	256-Pin Ball Grid Array	
83	CY37384P208-83NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37384P256-83BGC	BG256	256-Pin Ball Grid Array	
	CY37384P208-83NI	N208	208-Pin Plastic Quad Flatpack	Industrial
	CY37384P256-83BGI	BG256	256-Pin Ball Grid Array	

Shaded areas contain advance information.

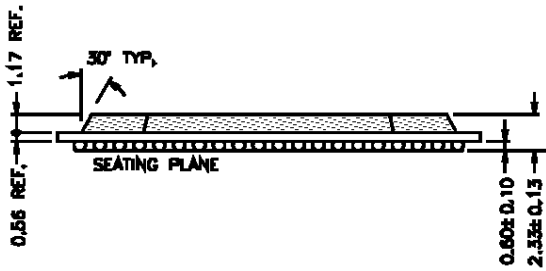
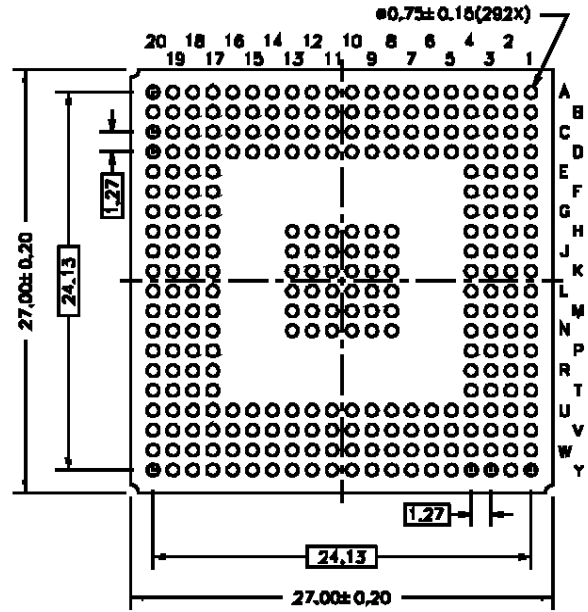
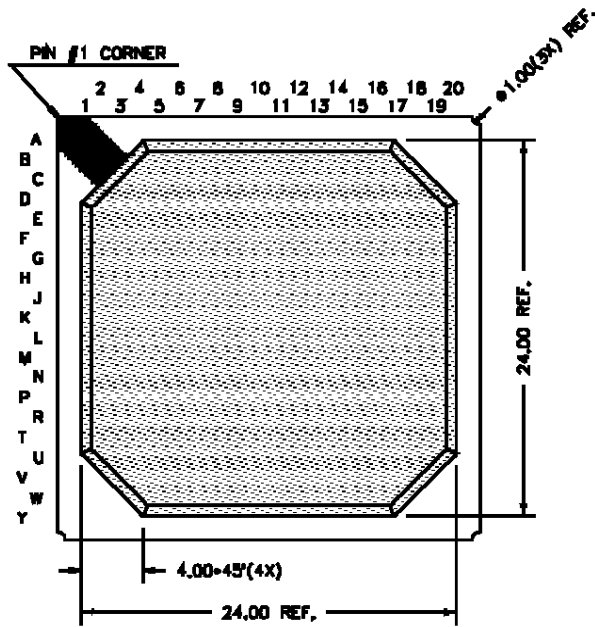
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Package Diagrams

256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256

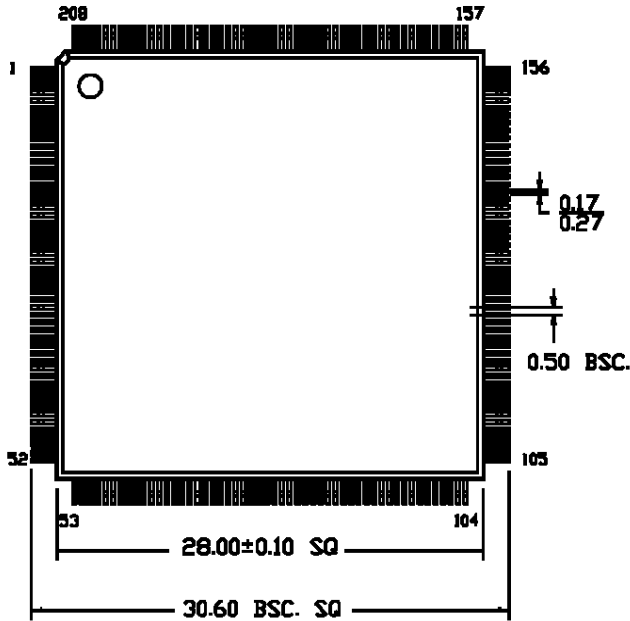


51-85097

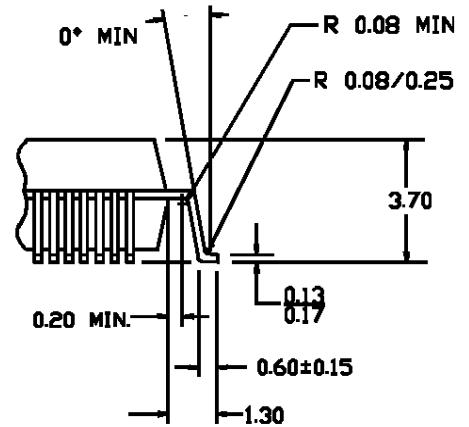


Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



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51-85069-B

