N-channel enhancement mode vertical D-MOS transistor

BSP89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptors in telephone sets and for application in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

PINNING

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

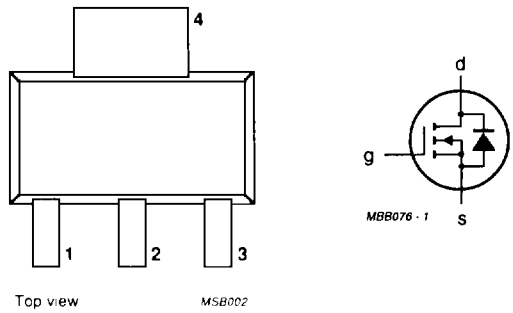

Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		-65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	240	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 340 mA; V_{GS} = 10 V	–	4	6	Ω
		I_D = 340 mA; V_{GS} = 4.5 V	–	–	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 340 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	65	140	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	9	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

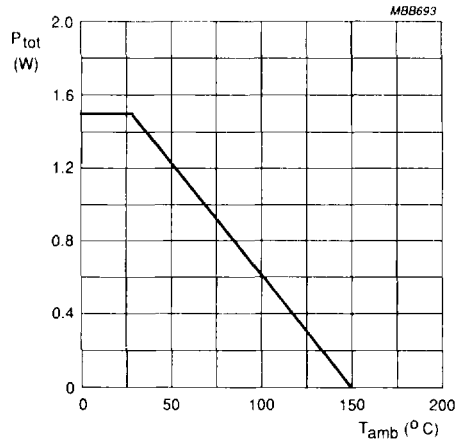
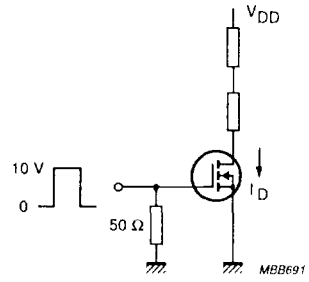


Fig.2 Power derating curve.



V_{DD} = 50 V.

Fig.3 Switching times test circuit.

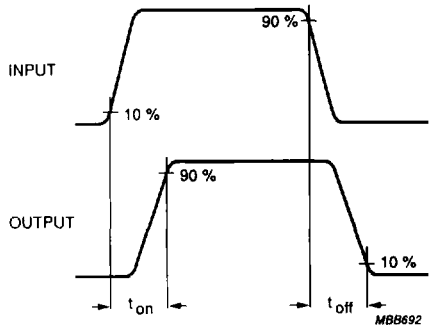


Fig.4 Input and output waveforms.