Marvell® PXA270 Processor

Electrical, Mechanical, Thermal Specification

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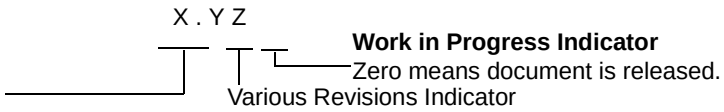

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1 Introduction

The Marvell® PXA270 processor (PXA270 processor) provides industry-leading multimedia performance, low-power capabilities, rich peripheral integration and second generation memory stacking. Designed from the ground up for wireless clients, it incorporates the latest Marvell advances in mobile technology over its predecessor, the Marvell® PXA255 processor. These same attributes and features also make the PXA270 processor ideal for embedded applications. The PXA270 processor redefines scalability by operating from 104 MHz up to 624 MHz, providing enough performance for the most demanding mobile applications.

The PXA270 processor is the first Marvell processor to include Intel® Wireless MMX™ technology, enabling high-performance, low-power multimedia acceleration with a general-purpose instruction set. The Marvell® Quick Capture Interface provides a flexible and powerful camera interface for capturing digital images and video. While performance is key in the PXA270 processor, power consumption is also a critical component. The new capabilities of Wireless Intel SpeedStep® technology set the standard for low-power consumption.

The PXA270 processor is offered in two packages: 13x13 mm VFBGA and 23x23 mm PBGA.

1.1 About This Document

This document constitutes the electrical, mechanical, and thermal specifications for the PXA270 processor. It contains a functional overview, mechanical data, package signal locations, targeted electrical specifications, and functional bus waveforms. For detailed functional descriptions other than parametric performance, refer to the *Marvell® PXA27x Processor Family Developers Manual*.

1.1.1 Number Representation

All numbers in this document are **base 10** unless designated otherwise. Hexadecimal numbers have a prefix of 0x, and binary numbers have a prefix of 0b. For example, 107 is represented as 0x6B in hexadecimal and 0b110_1011 in binary.

1.1.2 Typographical Conventions

All signal and register-bit names appear in uppercase. Active low items are prefixed with a lowercase “n”.

Bits within a signal name are enclosed in angle brackets:

EXTERNAL_ADDRESS<31:0>
nCS<1>

Bits within a register bit field are enclosed in square brackets:

REGISTER_BITFIELD[3:0]

REGISTER_BIT[0]

Single-bit items have either of two states:

- **clear** — the item contains the value 0b0. To clear a bit, write 0b0 to it.
- **set** — the item contains the value 0b1. To set a bit, write 0b1 to it.

1.1.3 Applicable Documents

Table 1 lists supplemental information sources for the PXA270 processor. Contact a Marvell representative for the latest document revisions and ordering instructions.

Table 1: Supplemental Documentation

Document Title
Marvell® PXA27x Processor Family Developers Manual
ARM® Architecture Version 5T Specification (Document number ARM DDI 0100D-10), and ARM® Architecture Reference Manual (Document number ARM* DDI 0100B)*
Intel XScale® Core Developer's Manual
Intel® Wireless MMX™ Technology Developer's Guide
Marvell® PXA27x Processor Design Guide
Marvell® PXA27x Processor Power Supply Requirements Application Note

2 Functional Overview

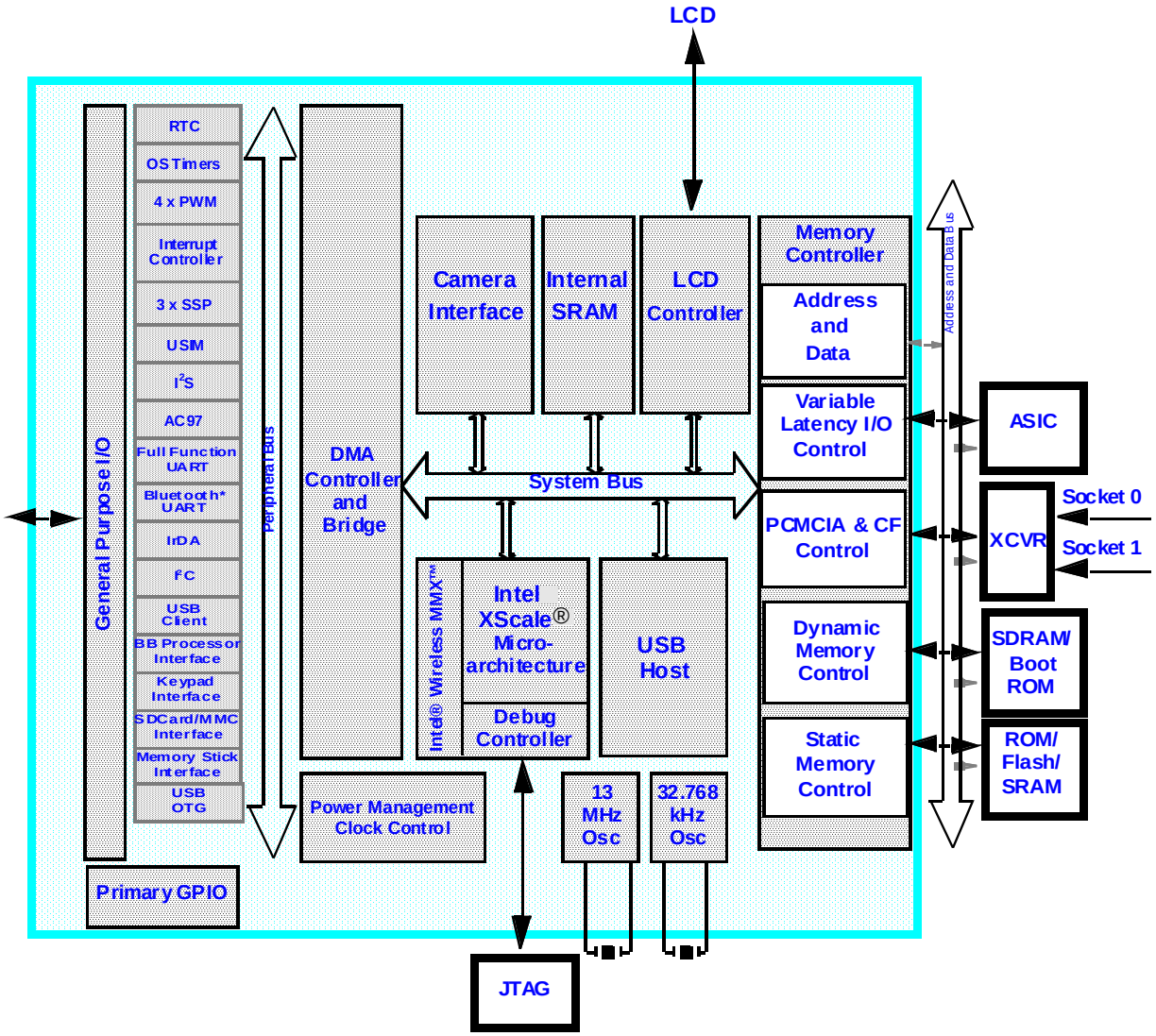
The Marvell® PXA270 processor is an integrated system-on-a-chip microprocessor for high performance, dynamic, low-power portable handheld and hand-set devices as well as embedded platforms. It incorporates the Intel XScale® technology which complies with the ARM* version 5TE instruction set (excluding floating-point instructions) and follows the ARM* programmer's model. The PXA270 processor also provides Intel® Wireless MMX™ media enhancement technology, which supports integer instructions to accelerate audio and video processing. In addition, it incorporates Wireless Intel Speedstep® Technology, which provides sophisticated power management capabilities enabling excellent MIPs/mW performance.

The PXA270 processor provides a scalable, bi-directional data interface to a cellular baseband processor, supporting seven logical channels and other features. The operating-system (OS) timer channels and synchronous serial ports (SSPs) also accept an external network clock input so that they can be synchronized to the cellular network. The processor also provides a Universal Subscriber Identity Module* (USIM) card interface.

The PXA270 processor memory interface gives designers flexibility as it supports a variety of external memory types. The processor also provides four 64 kilobyte banks of on-chip SRAM, which can be used for program code or multimedia data. Each bank can be configured independently to retain its contents when the processor enters a low-power mode. An integrated LCD panel controller supports displays up to 800 by 600 pixels, permitting 1-, 2-, 4-, and 8-bit gray scale and 1-, 2-, 4-, 8-, 16-, 18-, and 24-bit color pixels. A 256-byte palette RAM provides flexible color mapping.

A set of serial devices and general-system resources offers computational and connectivity capability for a variety of applications. Figure 1 shows the block diagram for a typical PXA270 processor system.

Figure 1: Marvell® PXA270 Processor Block Diagram, Typical System



Note

Memory Stick is not available on PXA270M (AP270M) SKUs.

3 Package Information

This chapter provides the mechanical specifications for the PXA270 processor.

The PXA270 processor is offered in two packages. Part numbers are shown in Figure 2. The 13- by 13-mm, 356-ball, 0.50-mm VF-BGA molded matrix array package is shown in Figure 3, Figure 4, Figure 5, and Figure 6. The 23- by 23-mm, 360-ball, 1.0-mm PBGA molded matrix array package is shown in Figure 7, Figure 8, Figure 9, and Figure 10.

Figure 2: Marvell® PXA270M Processor Part Numbers

AP270M (PXA270M) Part Numbers

Syntax:

88AP270M<revision>-<pkg code><env><temp><speed>

Where:

88AP270M: **Product Name**

<revision>: A2

<pkg code>: BGO – 13x13mm, 356L TFBGA, BHE – 23x23mm, 360L PBGA

<env>: 2 – Green, 1 – RoHS

<temp>: C – commercial temp, E – extended temp

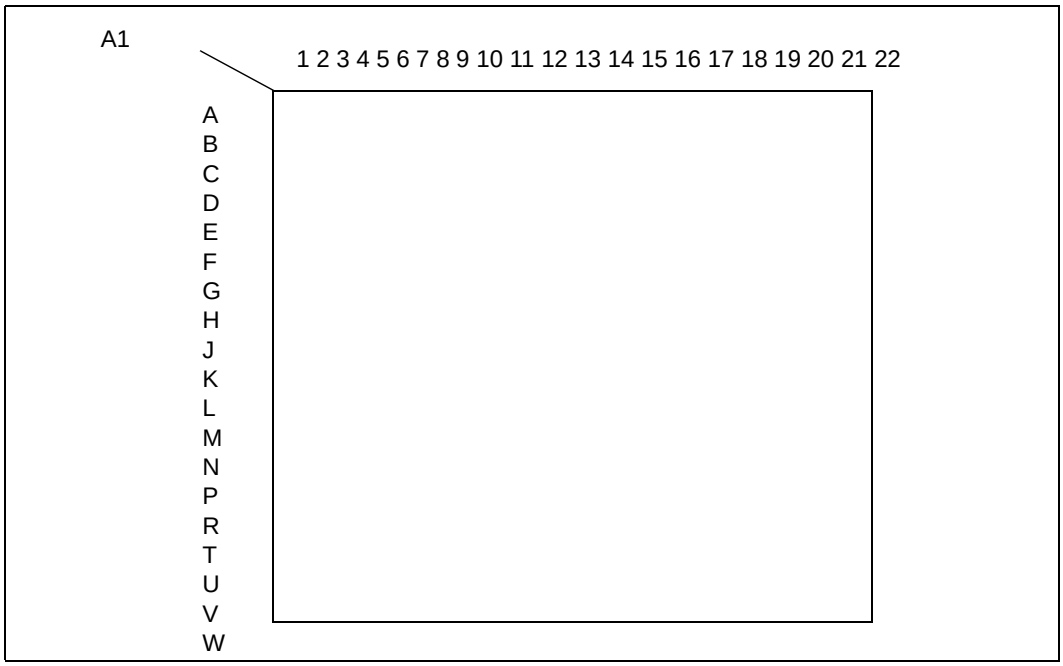
<speed>: 3-digit core speed, unit MHz

Examples:

Part Number	Description
88AP270MA2-BGO2C312	M180 (Bulverde TSMC) A2 13mm TFBGA Green Commercial Temp 312MHz in Tray
88AP270MA2-BGO2C416	M180 (Bulverde TSMC) A2 13mm TFBGA Green Commercial Temp 416MHz in Tray
88AP270MA2-BGO2C520	M180 (Bulverde TSMC) A2 13mm TFBGA Green Commercial Temp 520MHz in Tray
88AP270MA2-BGO2C624	M180 (Bulverde TSMC) A2 13mm TFBGA Green Commercial Temp 624MHz in Tray
88AP270MA2-BHE1C312	M180 (Bulverde TSMC) A2 23mm PBGA RoHS Commercial Temp 312MHz in Tray
88AP270MA2-BHE1C416	M180 (Bulverde TSMC) A2 23mm PBGA RoHS Commercial Temp 416MHz in Tray
88AP270MA2-BHE1C520	M180 (Bulverde TSMC) A2 23mm PBGA RoHS Commercial Temp 520MHz in Tray
88AP270MA2-BHE1C624	M180 (Bulverde TSMC) A2 23mm PBGA RoHS Commercial Temp 624MHz in Tray

3.1 Package Information

Figure 3: 13x13mm VF-BGA Marvell® PXA270 Processor Package, top view



Note

Figure 4 and Figure 5 show all dimensions in millimeters (mm).

Figure 4: 13x13mm VF-BGA Marvell® PXA270 Processor Package, bottom view

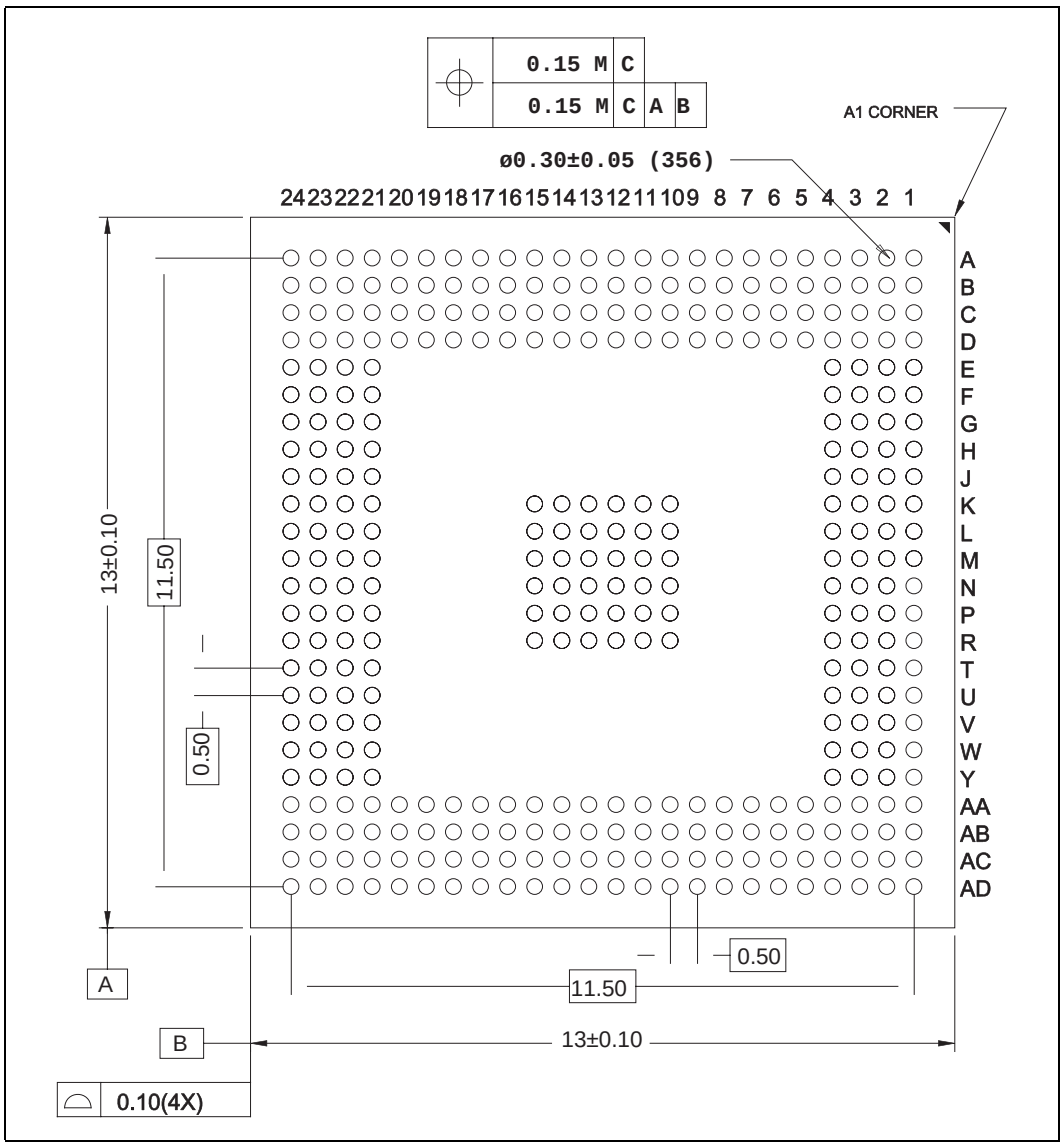


Figure 5: 13x13mm VF-BGA Marvell® PXA270 Processor Package, side view

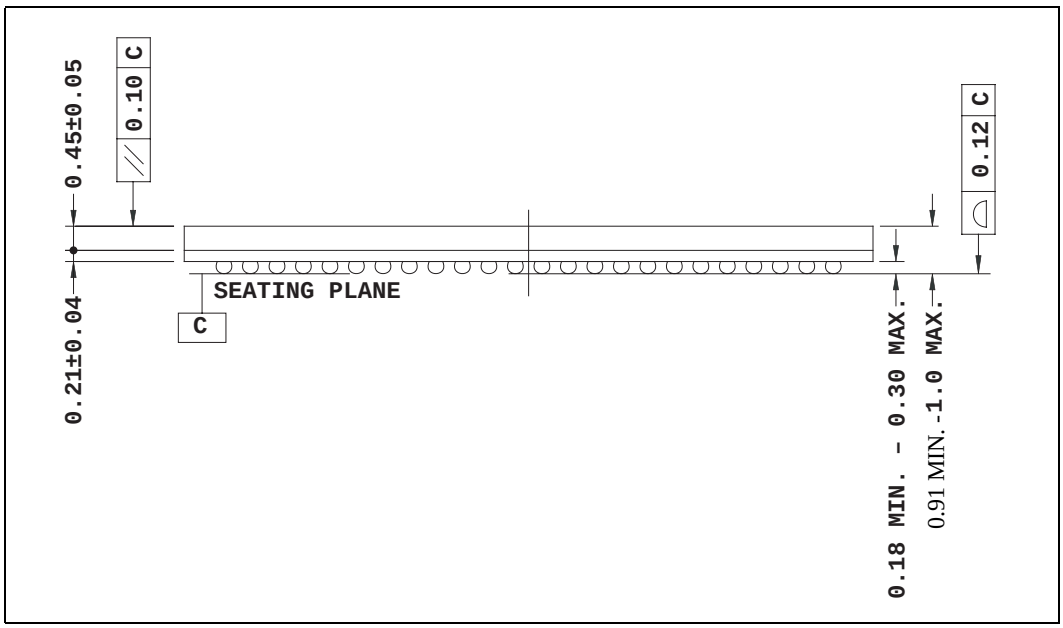


Figure 6: Marvell® PXA270M 13mm x 13mm Package Mark Diagram

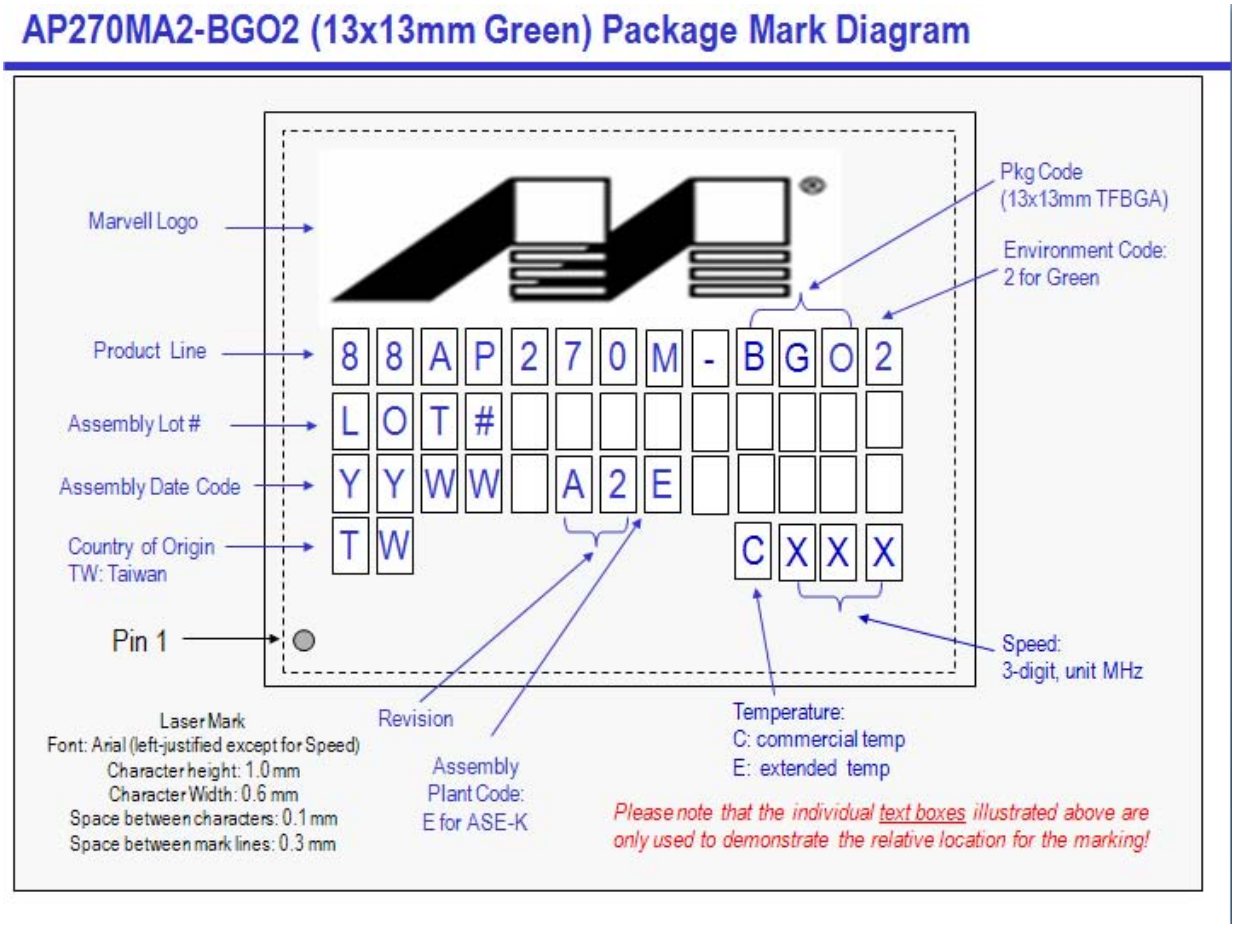
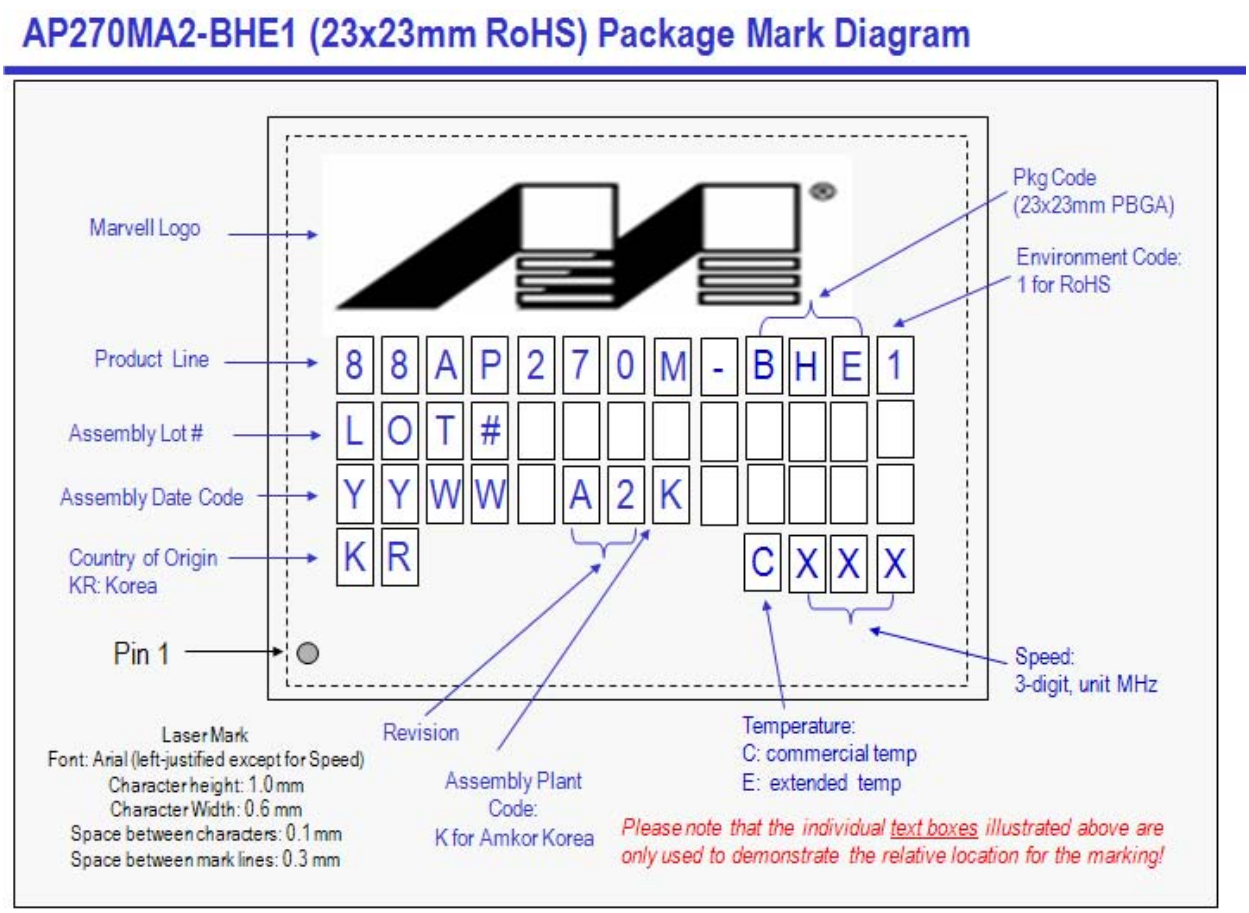


Figure 7: Marvell® PXA270M 23mm x 23mm Package Mark Diagram



Note

Figure 8, Figure 9 and Figure 10 show all dimensions in millimeters (mm).

Figure 8: 23x23 mm PBGA Marvell® PXA270 Processor Package (Top View)

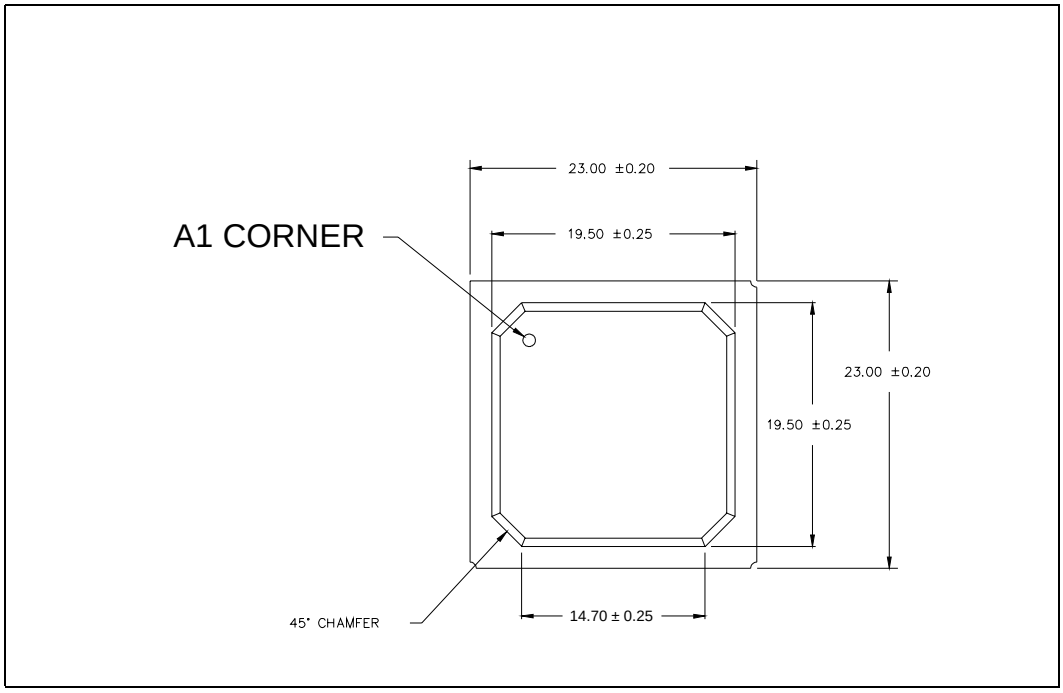


Figure 9: 23x23 mm PBGA Marvell® PXA270 Processor Package (Bottom View)

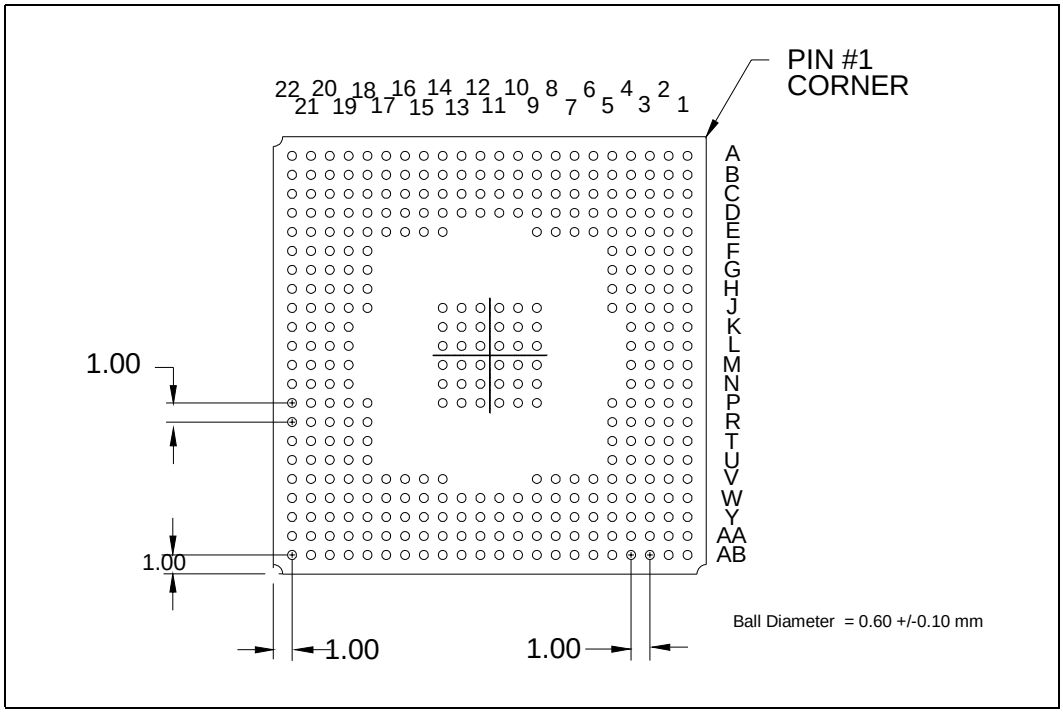


Figure 10: 23x23 mm PBGA Marvell® PXA270 Processor Package (Side View)

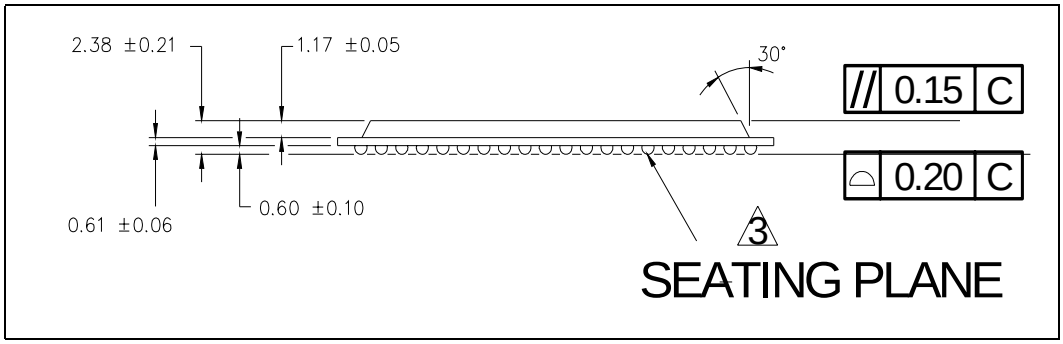
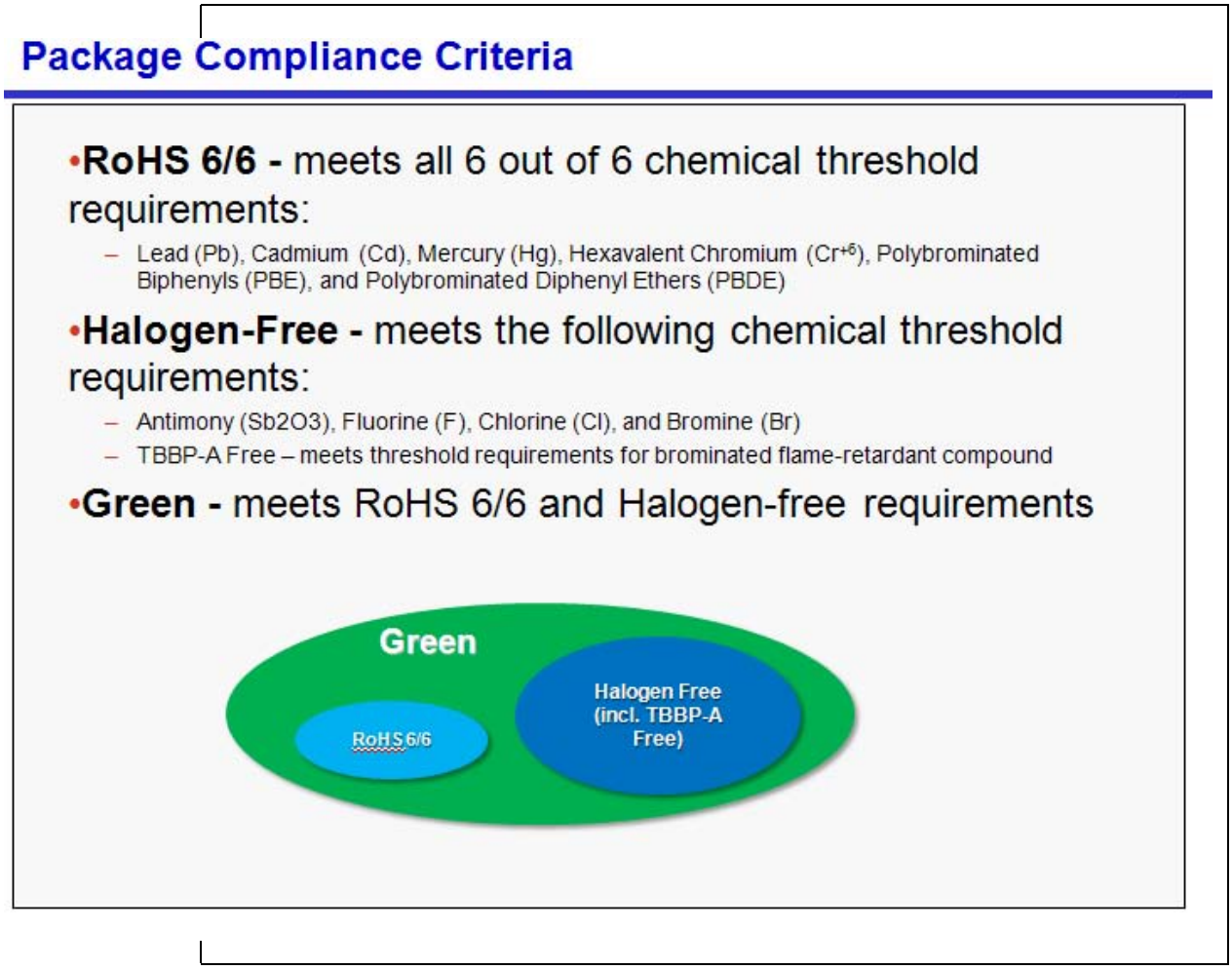


Figure 11: Package Compliance Criteria



3.2 Processor Materials

Figure 12: 13x13mm VF-BGA Marvell® PXA270 Processor Package, bottom view

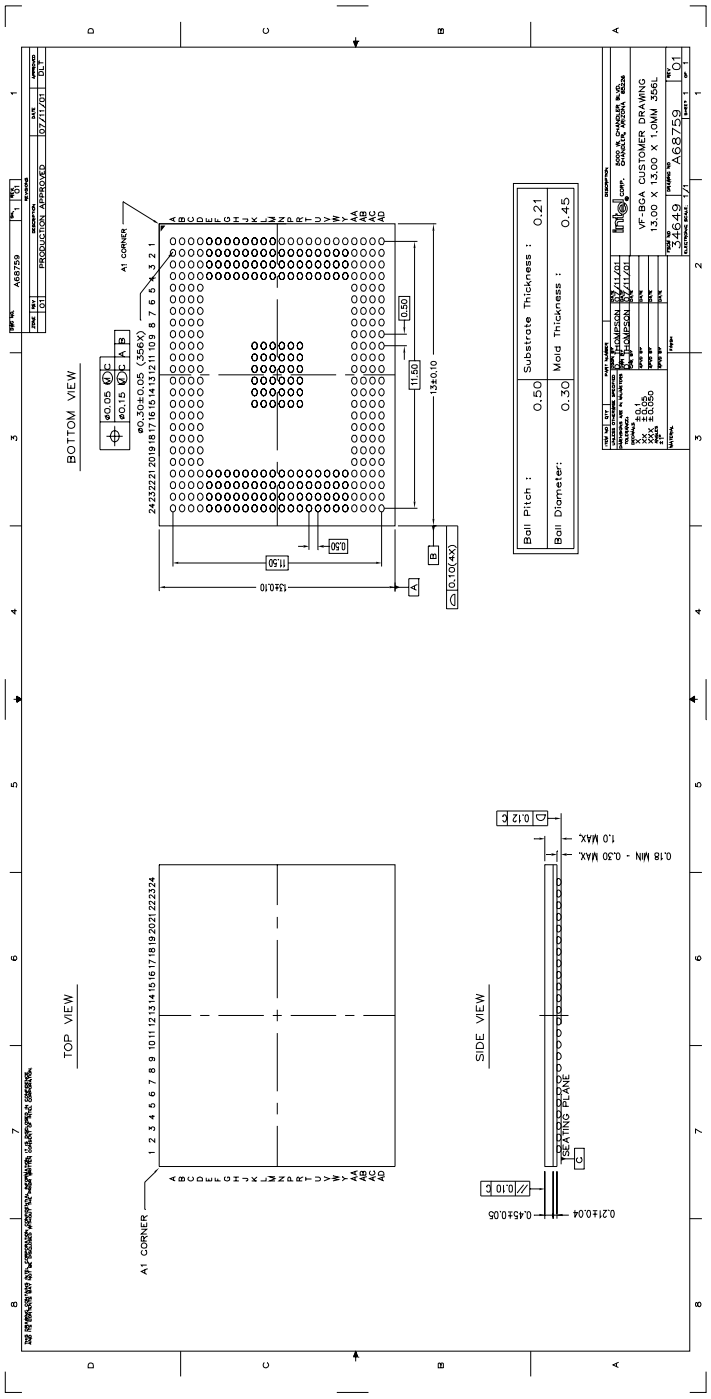


Table 2 describes the basic material properties of the processor components.

Table 2: Processor Material Properties

Component	VF-BGA Material	PBGA Material
Mold compound	ShinEtsu KMC 2500 VAT1	Sumitomo G770LE
Solder balls(Leaded)	63% Sn/37% Pb	63% Sn/37% Pb
Solder balls(Pb-free)	94.5% Sn / 5.0% Ag / 0.5% Cu	94.5% Sn / 5.0% Ag / 0.5% Cu

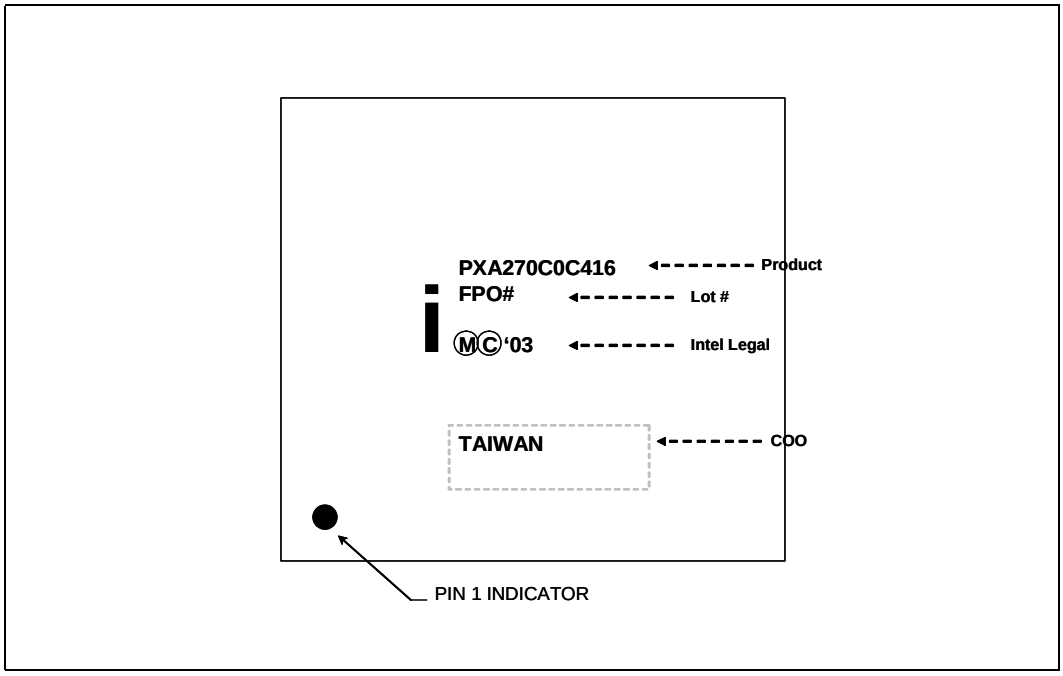
3.3 Junction To Case Temperature Thermal Resistance

Parameter	VF-BGA Value and Units	PBGA Value and Units
Theta Jc	2 degrees C / watt	1.4 degrees C / watt

3.4 Processor Markings

The diagram in this section details the processor's top markings, which identify the PXA270 processor in the 356-ball VF-BGA and 360-ball PBGA package. A Pb-Free (lead-free) package is indicated by the letter "E" on the 3rd line of information (Marvell legal line). The "E" appears after the date stamp.

Figure 13: Marvell® PXA270 Processor Production Markings, (Laser Mark on Top Side)



3.5 Tray Drawing

For tray drawing information, refer to the Intel Developer website for the *Intel® Wireless Communications and Computing Package Users Guide*.

§§

4 Pin Listing and Signal Definitions

This chapter describes the signals and pins for the Marvell® PXA270 processor.

For descriptions of all PXA270 processor signals, refer to the “System Architecture” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual*.

Table 4 lists the mapping of signals to specific package pins. Many of the package pins are multiplexed so that they can be configured for use as a general-purpose I/O signal or as one of two or three alternate functions using the GPIO alternate-function select registers. Some signals can be configured to appear on one of several different package pins.

4.1 Ball Map View

Note

In the following ball map figures the lowercase letter “n”, which normally indicates negation, appears as uppercase “N”.

4.1.1 13x13 mm VF-BGA Ball map

Figure 14 through Figure 17 shows the ball map for the VF-BGA PXA270 processor.

Figure 14: 13x13 mm VF-BGA Ball Map, Top View (upper left quarter)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_CORE	VSS_CORE	GPIO<15>	VCC_MEM	VCC_SRAM	MA<1>	VCC_CORE	VCC_SRAM	VCC_SRAM	GPIO<49>	GPIO<47>	VCC_IO
B	VSS_CORE	VSS_CORE	NCS<0>	VCC_SRAM	VSS_CORE	GPIO<33>	GPIO<78>	VCC_MEM	GPIO<18>	GPIO<12>	GPIO<46>	VCC_CORE
C	MA<18>	MA<22>	VCC_MEM	MA<24>	VSS_MEM	MA<0>	GPIO<80>	GPIO<79>	RDNWR	GPIO<13>	GPIO<11>	GPIO<31>
D	MA<17>	MA<21>	VCC_CORE	MA<23>	VSS_MEM	MA<25>	VSS_CORE	VSS_CORE	VSS_MEM	VSS_CORE	VSS_IO	VSS_CORE
E	MA<13>	VCC_MEM	MA<19>	MA<20>								
F	VCC_MEM	MA<14>	MA<16>	VSS_MEM								
G	MA<8>	MA<11>	MA<12>	MA<15>								
H	VCC_MEM	MA<9>	MA<10>	VSS_MEM								
J	MA<3>	MA<6>	MA<7>	VSS_MEM								
K	MD<15>	MA<4>	MA<5>	MA<2>						VSS_CORE	VSS_CORE	VSS_CORE
L	MD<14>	MD<31>	VCC_MEM	VSS_MEM						VSS_CORE	VSS_CORE	VSS_CORE
M	VCC_MEM	MD<30>	MD<29>	MD<13>						VSS_CORE	VSS_CORE	VSS_CORE

Figure 15: 13x13 mm VF-BGA Ball Map, Top View (upper right quarter)

13	14	15	16	17	18	19	20	21	22	23	24	
GPIO<113>	GPIO<28>	GPIO<37>	VCC_IO	GPIO<24>	GPIO<16>	GPIO<92>	GPIO<32>	GPIO<34>	GPIO<118>	VCC_USB	VCC_USB	**A**
GPIO<29>	GPIO<38>	GPIO<26>	GPIO<23>	GPIO<110>	GPIO<112>	GPIO<35>	GPIO<44>	VCC_CORE	USBC_P	VCC_USB	VCC_USB	**B**
GPIO<30>	GPIO<36>	GPIO<27>	GPIO<17>	GPIO<111>	GPIO<41>	GPIO<45>	USBC_N	GPIO<42>	GPIO<43>	GPIO<88>	GPIO<116>	**C**
GPIO<22>	GPIO<40>	VSS_IO	GPIO<25>	GPIO<109>	VSS_IO	GPIO<39>	GPIO<117>	VSS_CORE	GPIO<89>	USBH_N<1>	GPIO<114>	**D**
								GPIO<115>	USBH_P<1>	UIO	VCC_USIM	**E**
								VSS_IO	GPIO<90>	GPIO<91>	VCC_CORE	**F**
								VSS_CORE	GPIO<59>	GPIO<60>	GPIO<58>	**G**
								VSS_IO	GPIO<62>	GPIO<63>	GPIO<61>	**H**
								VSS_CORE	GPIO<64>	VCC_CORE	VCC_LCD	**J**
VSS_CORE	VSS_CORE	VSS_CORE						VSS_CORE	GPIO<66>	GPIO<67>	GPIO<65>	**K**
VSS_CORE	VSS_CORE	VSS_CORE						GPIO<68>	GPIO<71>	GPIO<69>	VCC_CORE	**L**
VSS_CORE	VSS_CORE	VSS_CORE						VSS_CORE	GPIO<73>	VCC_CORE	GPIO<70>	**M**

Figure 16: 13x13 mm VF-BGA Ball Map, Top View (bottom left quarter)

N	MD<27>	MD<28>	MD<12>	VSS_MEM						VSS_CORE	VSS_CORE	VSS_CORE
P	VCC_MEM	MD<11>	MD<26>	MD<10>						VSS_CORE	VSS_CORE	VSS_CORE
R	MD<24>	VSS_MEM	MD<25>	MD<9>						VSS_CORE	VSS_CORE	VSS_CORE
T	MD<23>	VCC_CORE	MD<8>	VSS_MEM								
U	MD<7>	VCC_MEM	VSS_CORE	MD<5>								
V	MD<21>	MD<22>	MD<6>	VSS_MEM								
W	MD<20>	VCC_MEM	VCC_CORE	VSS_CORE								
Y	MD<19>	MD<4>	MD<3>	VSS_MEM								
AA	MD<18>	VCC_MEM	MD<2>	MD<16>	VSS_MEM	NSDCAS	VSS_CORE	VSS_MEM	VSS_MEM	GPIO<55>	GPIO<84>	VSS_CORE
AB	MD<1>	VSS_MEM	MD<17>	MD<0>	NWE	GPIO<20>	NSDCS<0>	NSDCS<1>	DQM<0>	DQM<1>	GPIO<56>	GPIO<81>
AC	VCC_MEM	VCC_MEM	VSS_MEM	SDCLK<0>	NOE	VCC_MEM	NSDRAS	VCC_MEM	DQM<2>	DQM<3>	GPIO<57>	GPIO<85>
AD	VCC_MEM	VCC_MEM	SDCLK<2>	VCC_CORE	GPIO<21>	SDCKE	SDCLK<1>	VCC_MEM	GPIO<82>	GPIO<83>	VCC_CORE	VCC_BB
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**

Figure 17: 13x13 mm VF-BGA Ball Map, Top View (bottom right quarter)

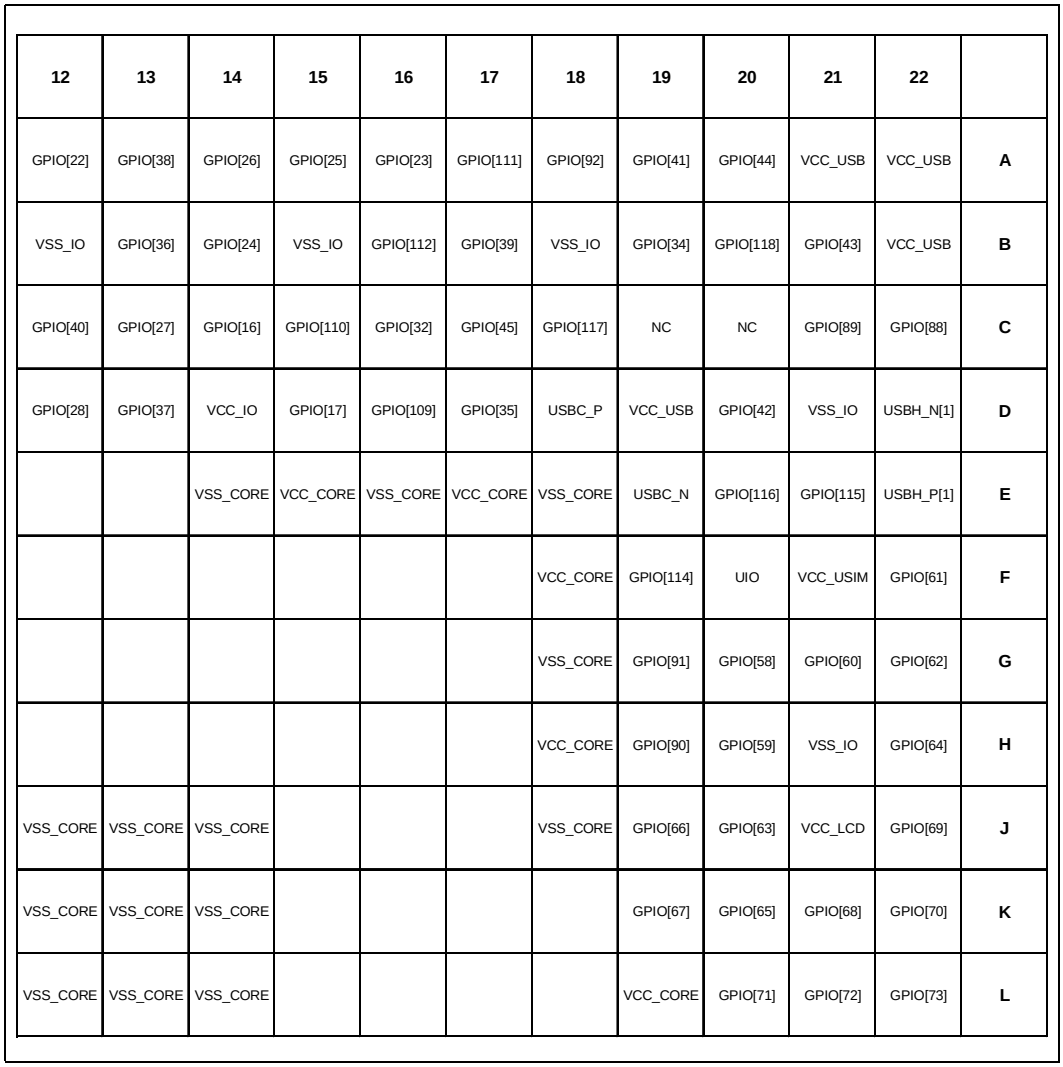
VSS_CORE	VSS_CORE	VSS_CORE						VSS_IO	GPIO<86>	GPIO<87>	GPIO<72>	**N**
VSS_CORE	VSS_CORE	VSS_CORE						VSS_CORE	GPIO<76>	GPIO<75>	VCC_LCD	**P**
VSS_CORE	VSS_CORE	VSS_CORE						GPIO<77>	GPIO<19>	GPIO<74>	VCC_CORE	**R**
								TMS	TCK	TESTCLK	GPIO<14>	**T**
								NTRST	GPIO<9>	TDI	VSS_IO	**U**
								VSS	GPIO<0>	GPIO<10>	TDO	**V**
								GPIO<3>	NVDD_FAULT	GPIO<4>	CLK_REQ	**W**
								NRESET_OUT	NRESET	PWR_EN	GPIO<1>	**Y**
VSS_BB	GPIO<54>	VSS_CORE	VSS_IO	GPIO<97>	GPIO<95>	VSS_IO	PWR_CAP<3>	VSS	TXTAL_IN	TXTAL_OUT	SYS_EN	**AA**
GPIO<50>	GPIO<53>	GPIO<106>	GPIO<105>	GPIO<102>	GPIO<99>	GPIO<93>	VCC_BATT	PWR_CAP<0>	PWR_OUT	BOOT_SEL	NBATT_FAULT	**AB**
GPIO<48>	GPIO<52>	GPIO<107>	GPIO<103>	GPIO<101>	GPIO<100>	GPIO<96>	VCC_PLL	PXTAL_IN	PWR_CAP<2>	VSS	VSS	**AC**
GPIO<51>	GPIO<108>	GPIO<104>	VCC_CORE	VCC_IO	GPIO<98>	GPIO<94>	VSS_PLL	PXTAL_OUT	PWR_CAP<1>	VSS	VSS	**AD**
13	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	

4.1.2 23x23 mm PBGA Ball map

Figure 18: 23x23 mm PBGA Ball Map, Top View (Upper Left Quarter)

	1	2	3	4	5	6	7	8	9	10	11
A	VSS_MEM	VSS_MEM	MA[25]	GPIO[15]	GPIO[79]	GPIO[13]	GPIO[12]	GPIO[11]	GPIO[46]	GPIO[113]	GPIO[29]
B	VSS_MEM	VCC_MEM	VSS_MEM	VCC_RAM	MA[1]	VSS_MEM	VCC_RAM	VCC_RAM	VSS_MEM	VCC_IO	GPIO[30]
C	MA[16]	MA[17]	VCC_MEM	MA[24]	VCC_RAM	VCC_MEM	GPIO[33]	RDNWR	VCC_MEM	GPIO[47]	GPIO[31]
D	MA[14]	MA[15]	MA[19]	MA[22]	MA[0]	NCS_0	GPIO[80]	GPIO[78]	GPIO[18]	GPIO[49]	VCC_CORE
E	MA[11]	MA[12]	MA[21]	MA[23]	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE		
F	MA[9]	VSS_MEM	VCC_MEM	MA[20]	VCC_CORE						
G	MA[7]	MA[8]	MA[13]	MA[18]	VSS_CORE						
H	MA[4]	VSS_MEM	VCC_MEM	MA[10]	VCC_CORE						
J	MA[3]	MA[2]	MA[6]	MA[5]	VSS_CORE				VSS_CORE	VSS_CORE	VSS_CORE
K	MD[15]	MD[30]	VCC_MEM	MD[31]					VSS_CORE	VSS_CORE	VSS_CORE
L	MD[14]	VSS_MEM	MD[29]	VCC_CORE					VSS_CORE	VSS_CORE	VSS_CORE

Figure 19: 23x23 mm PBGA Ball Map, Top View (Upper Right Quarter)



12	13	14	15	16	17	18	19	20	21	22	
GPIO[22]	GPIO[38]	GPIO[26]	GPIO[25]	GPIO[23]	GPIO[111]	GPIO[92]	GPIO[41]	GPIO[44]	VCC_USB	VCC_USB	**A**
VSS_IO	GPIO[36]	GPIO[24]	VSS_IO	GPIO[112]	GPIO[39]	VSS_IO	GPIO[34]	GPIO[118]	GPIO[43]	VCC_USB	**B**
GPIO[40]	GPIO[27]	GPIO[16]	GPIO[110]	GPIO[32]	GPIO[45]	GPIO[117]	NC	NC	GPIO[89]	GPIO[88]	**C**
GPIO[28]	GPIO[37]	VCC_IO	GPIO[17]	GPIO[109]	GPIO[35]	USBC_P	VCC_USB	GPIO[42]	VSS_IO	USBH_N[1]	**D**
		VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	USBC_N	GPIO[116]	GPIO[115]	USBH_P[1]	**E**
						VCC_CORE	GPIO[114]	UIO	VCC_USIM	GPIO[61]	**F**
						VSS_CORE	GPIO[91]	GPIO[58]	GPIO[60]	GPIO[62]	**G**
						VCC_CORE	GPIO[90]	GPIO[59]	VSS_IO	GPIO[64]	**H**
VSS_CORE	VSS_CORE	VSS_CORE				VSS_CORE	GPIO[66]	GPIO[63]	VCC_LCD	GPIO[69]	**J**
VSS_CORE	VSS_CORE	VSS_CORE					GPIO[67]	GPIO[65]	GPIO[68]	GPIO[70]	**K**
VSS_CORE	VSS_CORE	VSS_CORE					VCC_CORE	GPIO[71]	GPIO[72]	GPIO[73]	**L**

Figure 20: 23x23 mm PBGA Ball Map, Top View (Lower Left Quarter)

M	MD[13]	MD[11]	VCC_MEM	MD[12]					VSS_CORE	VSS_CORE	VSS_CORE
N	MD[28]	MD[26]	MD[24]	MD[25]					VSS_CORE	VSS_CORE	VSS_CORE
P	MD[27]	VSS_MEM	VCC_MEM	MD[8]	VSS_CORE				VSS_CORE	VSS_CORE	VSS_CORE
R	MD[10]	MD[23]	MD[21]	MD[7]	VCC_CORE						
T	MD[9]	VSS_MEM	VCC_MEM	MD[5]	VSS_CORE						
U	MD[22]	MD[6]	MD[4]	MD[2]	VCC_CORE						
V	MD[20]	VSS_MEM	VCC_MEM	MD[16]	VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE		
W	MD[19]	MD[18]	MD[1]	MD[0]	GPIO[20]	NSDRAS	SDCKE	DQM[0]	GPIO[55]	GPIO[81]	VCC_CORE
Y	MD[3]	MD[17]	VCC_MEM	NSDCAS	VCC_MEM	GPIO[21]	VCC_MEM	NSDCS[1]	VCC_MEM	GPIO[84]	GPIO[48]
AA	VSS_MEM	VCC_MEM	NWE	NOE	NSDCS[0]	VSS_MEM	DQM[1]	GPIO[82]	VSS_MEM	GPIO[85]	VCC_BB
AB	VSS_MEM	VSS_MEM	SDCLK[0]	SDCLK[2]	SDCLK[1]	DQM[2]	DQM[3]	GPIO[56]	GPIO[57]	GPIO[83]	VSS_BB
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**

Figure 21: 23x23 mm PBGA Ball Map, Top View (Lower Right Quarter)

VSS_CORE	VSS_CORE	VSS_CORE					VCC_LCD	GPIO[86]	VSS_IO	GPIO[87]	**M**
VSS_CORE	VSS_CORE	VSS_CORE					VSS_IO	GPIO[75]	GPIO[76]	GPIO[74]	**N**
VSS_CORE	VSS_CORE	VSS_CORE				VSS_CORE	GPIO[19]	GPIO[14]	GPIO[77]	TESTCLK	**P**
						VCC_CORE	TCK	TMS	TDO	TDI	**R**
						VSS_CORE	GPIO[4]	NTRST	CLK_REQ	GPIO[9]	**T**
						VCC_CORE	NBATT_FAULT	GPIO[0]	GPIO[1]	GPIO[10]	**U**
		VSS_CORE	VCC_CORE	VSS_CORE	VCC_CORE	VSS_CORE	BOOT_SEL	NVDD_FAULT	SYS_EN	GPIO[3]	**V**
GPIO[50]	GPIO[106]	GPIO[104]	VCC_IO	GPIO[96]	PWR_CAP[3]	VSS	PWR_OUT	NRESET	NRESET_OUT	PWR_EN	**W**
GPIO[52]	GPIO[105]	GPIO[102]	GPIO[97]	GPIO[93]	VCC_BATT	PWR_CAP[2]	PWR_CAP[0]	VSS	TXTAL_IN	TXTAL_OUT	**Y**
GPIO[53]	GPIO[108]	VSS_IO	GPIO[100]	GPIO[98]	GPIO[94]	VSS_IO	VSS_PLL	PXTAL_OUT	PWR_CAP[1]	VSS	**AA**
GPIO[51]	GPIO[54]	GPIO[107]	GPIO[103]	GPIO[101]	GPIO[99]	GPIO[95]	VCC_PLL	PXTAL_IN	VSS	VSS	**AB**
12	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	

4.2 Pin Use

The pin-use summary shown in Table 3 does not include the 36 center balls identified as K10 through R15 (VF-BGA) or J9 through P14 (PBGA), all of which function as VSS_CORE (see the recommendations for connecting the 36 center balls in the *Marvell® PXA27x Processor Family Design Guide*).

Each signal's alternate function inputs are shown in the upper section of each signal row and the outputs are shown in the lower section of each signal row. For example, GPIO<48> has a primary input function of CIF_DD<5> and a secondary output function of nPOE.

Table 3: Pin Use Summary (Sheet 1 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
VCC_MEM									
D6	A3	MA<25>	OCZ	MA<25>	MA<25>	—	—	Refer to Table 6	
C4	C4	MA<24>	OCZ	MA<24>	MA<24>	—	—	Refer to Table 6	
D4	E4	MA<23>	OCZ	MA<23>	MA<23>	—	—	Refer to Table 6	
C2	D4	MA<22>	OCZ	MA<22>	MA<22>	—	—	Refer to Table 6	
D2	E3	MA<21>	OCZ	MA<21>	MA<21>	—	—	Refer to Table 6	
E4	F4	MA<20>	OCZ	MA<20>	MA<20>	—	—	Refer to Table 6	
E3	D3	MA<19>	OCZ	MA<19>	MA<19>	—	—	Refer to Table 6	
C1	G4	MA<18>	OCZ	MA<18>	MA<18>	—	—	Refer to Table 6	
D1	C2	MA<17>	OCZ	MA<17>	MA<17>	—	—	Refer to Table 6	
F3	C1	MA<16>	OCZ	MA<16>	MA<16>	—	—	Refer to Table 6	
G4	D2	MA<15>	OCZ	MA<15>	MA<15>	—	—	Refer to Table 6	
F2	D1	MA<14>	OCZ	MA<14>	MA<14>	—	—	Refer to Table 6	
E1	G3	MA<13>	OCZ	MA<13>	MA<13>	—	—	Refer to Table 6	
G3	E2	MA<12>	OCZ	MA<12>	MA<12>	—	—	Refer to Table 6	
G2	E1	MA<11>	OCZ	MA<11>	MA<11>	—	—	Refer to Table 6	
H3	H4	MA<10>	OCZ	MA<10>	MA<10>	—	—	Refer to Table 6	
H2	F1	MA<9>	OCZ	MA<9>	MA<9>	—	—	Refer to Table 6	
G1	G2	MA<8>	OCZ	MA<8>	MA<8>	—	—	Refer to Table 6	
J3	G1	MA<7>	OCZ	MA<7>	MA<7>	—	—	Refer to Table 6	
J2	J3	MA<6>	OCZ	MA<6>	MA<6>	—	—	Refer to Table 6	
K3	J4	MA<5>	OCZ	MA<5>	MA<5>	—	—	Refer to Table 6	
K2	H1	MA<4>	OCZ	MA<4>	MA<4>	—	—	Refer to Table 6	
J1	J1	MA<3>	OCZ	MA<3>	MA<3>	—	—	Refer to Table 6	
K4	J2	MA<2>	OCZ	MA<2>	MA<2>	—	—	Refer to Table 6	
A6	B5	MA<1>	OCZ	MA<1>	MA<1>	—	—	Refer to Table 6	
C6	D5	MA<0>	OCZ	MA<0>	MA<0>	—	—	Refer to Table 6	

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 2 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
L2	K4	MD<31>	ICO CZ	MD<31>	MD<31>	—	—	Refer to Table 6	
M2	K2	MD<30>	ICO CZ	MD<30>	MD<30>	—	—	Refer to Table 6	
M3	L3	MD<29>	ICO CZ	MD<29>	MD<29>	—	—	Refer to Table 6	
N2	N1	MD<28>	ICO CZ	MD<28>	MD<28>	—	—	Refer to Table 6	
N1	P1	MD<27>	ICO CZ	MD<27>	MD<27>	—	—	Refer to Table 6	
P3	N2	MD<26>	ICO CZ	MD<26>	MD<26>	—	—	Refer to Table 6	
R3	N4	MD<25>	ICO CZ	MD<25>	MD<25>	—	—	Refer to Table 6	
R1	N3	MD<24>	ICO CZ	MD<24>	MD<24>	—	—	Refer to Table 6	
T1	R2	MD<23>	ICO CZ	MD<23>	MD<23>	—	—	Refer to Table 6	
V2	U1	MD<22>	ICO CZ	MD<22>	MD<22>	—	—	Refer to Table 6	
V1	R3	MD<21>	ICO CZ	MD<21>	MD<21>	—	—	Refer to Table 6	
W1	V1	MD<20>	ICO CZ	MD<20>	MD<20>	—	—	Refer to Table 6	
Y1	W1	MD<19>	ICO CZ	MD<19>	MD<19>	—	—	Refer to Table 6	
AA1	W2	MD<18>	ICO CZ	MD<18>	MD<18>	—	—	Refer to Table 6	
AB3	Y2	MD<17>	ICO CZ	MD<17>	MD<17>	—	—	Refer to Table 6	
AA4	V4	MD<16>	ICO CZ	MD<16>	MD<16>	—	—	Refer to Table 6	
K1	K1	MD<15>	ICO CZ	MD<15>	MD<15>	—	—	Refer to Table 6	

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 3 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
L1	L1	MD<14>	ICO CZ	MD<14>	MD<14>	—	—	Refer to Table 6	
M4	M1	MD<13>	ICO CZ	MD<13>	MD<13>	—	—	Refer to Table 6	
N3	M4	MD<12>	ICO CZ	MD<12>	MD<12>	—	—	Refer to Table 6	
P2	M2	MD<11>	ICO CZ	MD<11>	MD<11>	—	—	Refer to Table 6	
P4	R1	MD<10>	ICO CZ	MD<10>	MD<10>	—	—	Refer to Table 6	
R4	T1	MD<9>	ICO CZ	MD<9>	MD<9>	—	—	Refer to Table 6	
T3	P4	MD<8>	ICO CZ	MD<8>	MD<8>	—	—	Refer to Table 6	
U1	R4	MD<7>	ICO CZ	MD<7>	MD<7>	—	—	Refer to Table 6	
V3	U2	MD<6>	ICO CZ	MD<6>	MD<6>	—	—	Refer to Table 6	
U4	T4	MD<5>	ICO CZ	MD<5>	MD<5>	—	—	Refer to Table 6	
Y2	U3	MD<4>	ICO CZ	MD<4>	MD<4>	—	—	Refer to Table 6	
Y3	Y1	MD<3>	ICO CZ	MD<3>	MD<3>	—	—	Refer to Table 6	
AA3	U4	MD<2>	ICO CZ	MD<2>	MD<2>	—	—	Refer to Table 6	
AB1	W3	MD<1>	ICO CZ	MD<1>	MD<1>	—	—	Refer to Table 6	
AB4	W4	MD<0>	ICO CZ	MD<0>	MD<0>	—	—	Refer to Table 6	
AC5	AA4	NOE	OCZ	nOE	nOE	—	—	Refer to Table 6	
AB5	AA3	NWE	OCZ	nWE	nWE	—	—	Refer to Table 6	
AC7	W6	NSDRAS	OCZ	nSDRAS	nSDRAS	—	—	Refer to Table 6	

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 4 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AA6	Y4	NSDCAS	OCZ	nSDCAS	nSDCAS	—	—	Refer to Table 6	
AB9	W8	DQM<0>	OCZ	DQM<0>	DQM<0>	—	—	Refer to Table 6	
AB10	AA7	DQM<1>	OCZ	DQM<1>	DQM<1>	—	—	Refer to Table 6	
AC9	AB6	DQM<2>	OCZ	DQM<2>	DQM<2>	—	—	Refer to Table 6	
AC10	AB7	DQM<3>	OCZ	DQM<3>	DQM<3>	—	—	Refer to Table 6	
AB7	AA5	NSDCS<0>	OCZ	nSDCS<0>	nSDCS<0>	—	—	Refer to Table 6	
AB8	Y8	NSDCS<1>	OC	nSDCS<1>	nSDCS<1>	—	—	Refer to Table 6	
AD6	W7	SDCKE	OC	SDCKE	SDCKE	—	—	Refer to Table 6	
AC4	AB3	SDCLK<0>	OC	SDCLK<0>	SDCLK<0>	—	—	Refer to Table 6	
AD7	AB5	SDCLK<1>	OCZ	SDCLK<1>	SDCLK<1>	—	—	Refer to Table 6	
AD3	AB4	SDCLK<2>	OC	SDCLK<2>	SDCLK<2>	—	—	Refer to Table 6	
C9	C8	RDNWR	OCZ	RDnWR	RDnWR	—	—	Refer to Table 6	
B3	D6	NCS<0>	OCZ	nCS<0>	nCS<0>	—	—	Refer to Table 6	
A3	A4	GPIO<15>	ICOCZ	GPIO<15>	—	—	—	Pu-1 Note[1]	Note[4]
					nPCE<1>	nCS<1> Refer to Table 6	—		
B9	D9	GPIO<18>	ICOCZ	GPIO<18>	RDY	—	—	Pd-0 Note[1]	Note [3]
					—	—	—		
AB6	W5	GPIO<20>	ICOCZ	GPIO<20>	DREQ<0>	MBREQ	—	Pu-1 Note[1]	Note[3]
					nSDCS<2> Refer to Table 6	—	—		
AD5	Y6	GPIO<21>	ICOCZ	GPIO<21>	—	—	—	Pu-1 Note[1]	Note[3]
					nSDCS<3> Refer to Table 6	DVAL<0>	MBGNT		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 5 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
B6	C7	GPIO<33>	ICO CZ	GPIO<33>	FFRXD[19]	FFDSR[19]	—	Pu-1 Note[1]	Note [4]
					DVAL<1>	nCS<5> Refer to Table 6	MBGNT		
A10	D10	GPIO<49>	ICO CZ	GPIO<49>	—	—	—	Pu-1 Note[1]	Note [5]
					—	nPWE Refer to Table 6	—		
B7	D8	GPIO<78>	ICO CZ	GPIO<78>	—	—	—	Pu-1 Note[1]	Note[4]
					nPCE<2>	nCS<2> Refer to Table 6	—		
C8	A5	GPIO<79>	ICO CZ	GPIO<79>	—	—	—	Pu-1 Note[1]	Note[4]
					PSKTSEL	nCS<3> Refer to Table 6	PWM_OUT<2>		
C7	D7	GPIO<80>	ICO CZ	GPIO<80>	DREQ<1>	MBREQ	—	Pu-1 Note[1]	Note[4]
					—	nCS<4> Refer to Table 6	PWM_OUT<3>		
VCC_BB									
AC13	Y11	GPIO<48>	ICO CZ	GPIO<48>	CIF_DD<5>	—	—	Pu-1 Note[1]	Note [5]
					BB_OB_DAT<1>	nPOE Refer to Table 6	—		
AB13	W12	GPIO<50>	ICO CZ	GPIO<50>	CIF_DD<3>	—	SSPSCLK<2>	Pu-1 Note[1]	Note [5]
					BB_OB_DAT<2>	nPIOIR Refer to Table 6	SSPSCLK<2>		
AD13	AB12	GPIO<51>	ICO CZ	GPIO<51>	CIF_DD<2>	—	—	Pu-1 Note[1]	Note [5]
					BB_OB_DAT<3>	nPIOIW Refer to Table 6	—		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 6 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AC14	Y12	GPIO<52>	ICOCZ	GPIO<52>	CIF_DD<4>	SSPSCLK<3>	—	Pd-0 Note[1]	Note [3]
					BB_OB_CLK	SSPSCLK<3>	—		
AB14	AA12	GPIO<53>	ICOCZ	GPIO<53>	FFRXD	USB_P2_3	—	Pd-0 Note[1]	Note [3]
					BB_OB_STB	CIF_MCLK	SSPSYSCLK		
AA14	AB13	GPIO<54>	ICOCZ	GPIO<54>	—	BB_OB_WAIT	CIF_PCLK	Pd-0 Note[1]	Note [3]
						nPCE<2>	—		
AA10	W9	GPIO<55>	ICOCZ	GPIO<55>	CIF_DD<1>	BB_IB_DAT<1>	—	Pu-1 Note[1]	Note [5]
					—	nPREG	—		
AB11	AB8	GPIO<56>	ICOCZ	GPIO<56>	nPWAIT	BB_IB_DAT<2>	—	Pu-1 Note[1]	Note [5]
					USB_P3_4	—	—		
AC11	AB9	GPIO<57>	ICOCZ	GPIO<57>	nIOIS16	BB_IB_DAT<3>	—	Pu-1 Note[1]	Note [5]
					—	—	SSPTXD		
AB12	W10	GPIO<81>	ICOCZ	GPIO<81>	—	CIF_DD<0>	—	Pu-1 Note[1]	Note [3]
					SSPTXD3	BB_OB_DAT<0>	—		
AD9	AA8	GPIO<82>	ICOCZ	GPIO<82>	SSPRXD3	BB_IB_DAT<0>	CIF_DD<5>	Pu-1 Note[1]	Note [3]
					—	—	FFDTR		
AD10	AB10	GPIO<83>	ICOCZ	GPIO<83>	SSPSFRM3	BB_IB_CLK	CIF_DD<4>	Pd-0 Note[1]	Note [3]
					SSPSFRM3	FFTXD	FFRTS		
AA11	Y10	GPIO<84>	ICOCZ	GPIO<84>	SSPSCLK3	BB_IB_STB	CIF_FV	Pd-0 Note[1]	Note [3]
					SSPSCLK3	—	CIF_FV		
AC12	AA10	GPIO<85>	ICOCZ	GPIO<85>	FFRXD	DREQ<2>	CIF_LV	Pd-0 Note[1]	Note [3]
					nPCE<1>	BB_IB_WAIT	CIF_LV		
VCC_LCD									

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 7 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
T24	P20	GPIO<14>	ICO CZ	GPIO<14>	L_VSYNC	SSPSFRM2	—	Pd-0 Note[1]	Note [3]
					—	SSPSFRM2	UCLK		
R22	P19	GPIO<19>	ICO CZ	GPIO<19>	SSPSCLK2	—	FFRXD	Pd-0 Note[1]	Note [3]
					SSPSCLK2	L_CS	nURST		
G24	G20	GPIO<58>	ICO CZ	GPIO<58>	—	LDD<0>	—	Pd-0 Note[1]	Note [3]
					—	LDD<0>	—		
G22	H20	GPIO<59>	ICO CZ	GPIO<59>	—	LDD<1>	—	Pd-0 Note[1]	Note [3]
					—	LDD<1>	—		
G23	G21	GPIO<60>	ICO CZ	GPIO<60>	—	LDD<2>	—	Pd-0 Note[1]	Note [3]
					—	LDD<2>	—		
H24	F22	GPIO<61>	ICO CZ	GPIO<61>	—	LDD<3>	—	Pd-0 Note[1]	Note [3]
					—	LDD<3>	—		
H22	G22	GPIO<62>	ICO CZ	GPIO<62>	—	LDD<4>	—	Pd-0 Note[1]	Note [3]
					—	LDD<4>	—		
H23	J20	GPIO<63>	ICO CZ	GPIO<63>	—	LDD<5>	—	Pd-0 Note[1]	Note [3]
					—	LDD<5>	—		
J22	H22	GPIO<64>	ICO CZ	GPIO<64>	—	LDD<6>	—	Pd-0 Note[1]	Note [3]
					—	LDD<6>	—		
K24	K20	GPIO<65>	ICO CZ	GPIO<65>	—	LDD<7>	—	Pd-0 Note[1]	Note [3]
					—	LDD<7>	—		
K22	J19	GPIO<66>	ICO CZ	GPIO<66>	—	LDD<8>	—	Pd-0 Note[1]	Note [3]
					—	LDD<8>	—		
K23	K19	GPIO<67>	ICO CZ	GPIO<67>	—	LDD<9>	—	Pd-0 Note[1]	Note [3]
					—	LDD<9>	—		
L21	K21	GPIO<68>	ICO CZ	GPIO<68>	—	LDD<10>	—	Pd-0 Note[1]	Note [3]
					—	LDD<10>	—		
L23	J22	GPIO<69>	ICO CZ	GPIO<69>	—	LDD<11>	—	Pd-0 Note[1]	Note [3]
					—	LDD<11>	—		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 8 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
M24	K22	GPIO<70>	ICOCZ	GPIO<70>	—	LDD<12>	—	Pd-0 Note[1]	Note [3]
					—	LDD<12>	—		
L22	L20	GPIO<71>	ICOCZ	GPIO<71>	—	LDD<13>	—	Pd-0 Note[1]	Note [3]
					—	LDD<13>	—		
N24	L21	GPIO<72>	ICOCZ	GPIO<72>	—	LDD<14>	—	Pd-0 Note[1]	Note [3]
					—	LDD<14>	—		
M22	L22	GPIO<73>	ICOCZ	GPIO<73>	—	LDD<15>	—	Pd-0 Note[1]	Note [3]
					—	LDD<15>	—		
R23	N22	GPIO<74>	ICOCZ	GPIO<74>	—	—	—	Pd-0 Note[1]	Note [3]
					—	L_FCLK_RD	—		
P23	N20	GPIO<75>	ICOCZ	GPIO<75>	—	—	—	Pd-0 Note[1]	Note [3]
					—	L_LCLK _A0	—		
P22	N21	GPIO<76>	ICOCZ	GPIO<76>	—	—	—	Pd-0 Note[1]	Note [3]
					—	L_PCLK_WR	—		
R21	P21	GPIO<77>	ICOCZ	GPIO<77>	—	—	—	Pd-0 Note[1]	Note [3]
					—	L_BIAS	—		
N22	M20	GPIO<86>	ICOCZ	GPIO<86>	SSPRXD2	LDD<16>	USB_P3_5	Pd-0 Note[1]	Note [3]
					nPCE<1>	LDD<16>	—		
N23	M22	GPIO<87>	ICOCZ	GPIO<87>	nPCE<2>	LDD<17>	USB_P3_1	Pd-0 Note[1]	Note [3]
					SSPTXD2	LDD<17>	SSPSFRM2		
VCC_IO									
C11	A8	GPIO<11>	ICOCZ	GPIO<11>	EXT_SYNC<0>	SSPRXD2	USB_P3_1	Pd-0 Note[1]	Note [3], Note[11
					CHOUT<0>	PWM_OUT2	48_MHz		
B10	A7	GPIO<12>	ICOCZ	GPIO<12>	EXT_SYNC<1>	CIF_DD<7>	—	Pd-0 Note[1]	Note [3], Note[11
					CHOUT<1>	PWM_OUT3	48_MHz		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 9 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
C10	A6	GPIO<13>	ICOCZ	GPIO<13>	CLK_EXT	KP_DKIN<7>	KP_MKIN<7>	Pd-0 Note[1]	Note [3], Note[11]
					SSPTXD2	—	—		
A18	C14	GPIO<16>	ICOCZ	GPIO<16>	KP_MKIN<5>	—	—	Pd-0 Note[1]	Note [3]
					—	PWM_OUT<0>	FFTXD		
C16	D15	GPIO<17>	ICOCZ	GPIO<17>	KP_MKIN<6>	CIF_DD<6>	—	Pd-0 Note[1]	Note [3]
					—	PWM_OUT<1>	—		
D13	A12	GPIO<22>	ICOCZ	GPIO<22>	SSPEXTCLK2	SSPSCLKEN2	SSPSCLK2	Pd-0 Note[1]	Note [3]
					KP_MKOUT<7>	SSPSYSCLK2	SSPSCLK2		
B16	A16	GPIO<23>	ICOCZ	GPIO<23>	—	SSPSCLK	—	Pd-0 Note[1]	Note [3]
					CIF_MCLK	SSPSCLK	—		
A17	B14	GPIO<24>	ICOCZ	GPIO<24>	CIF_FV	SSPSFRM	—	Pd-0 Note[1]	Note [3]
					CIF_FV	SSPSFRM	—		
D16	A15	GPIO<25>	ICOCZ	GPIO<25>	CIF_LV	—	—	Pd-0 Note[1]	Note [3]
					CIF_LV	SSPTXD	—		
B15	A14	GPIO<26>	ICOCZ	GPIO<26>	SSPRXD	CIF_PCLK	FFCTS	Pd-0 Note[1]	Note [3]
					—	—	—		
C15	C13	GPIO<27>	ICOCZ	GPIO<27>	SSPEXTCLK	SSPSCLKEN	CIF_DD<0>	Pd-0 Note[1]	Note [3]
					SSPSYSCLK	—	FFRTS		
A14	D12	GPIO<28>	ICOCZ	GPIO<28>	AC97_BITCLK	I2S_BITCLK	SSPSFRM	Pd-0 Note[1]	Note [3]
					I2S_BITCLK	—	SSPSFRM		
B13	A11	GPIO<29>	ICOCZ	GPIO<29>	AC97_SDATA_IN_0	I2S_SDATA_IN	SSPSCLK	Pd-0 Note[1]	Note [3]
					SSPRXD2	—	SSPSCLK		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 10 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
C13	B11	GPIO<30>	ICOCZ	GPIO<30>	—	—	—	Pd-0 Note[1]	Note [3]
					I2S_SDATA_OUT	AC97_SDATA_OUT	USB_P3_2		
C12	C11	GPIO<31>	ICOCZ	GPIO<31>	—	—	—	Pd-0 Note[1]	Note [3]
					I2S_SYNC	AC97_SYNC	USB_P3_6		
A20	C16	GPIO<32>	ICOCZ	GPIO<32>	—	—	—	Pd-0 Note[1]	Note [3]
					MSSCLK	MMCLK	—		
A21	B19	GPIO<34>	ICOCZ	GPIO<34>	FFRXD	KP_MKIN<3>	SSPSCLK3	Pd-0 Note[1]	Note [3]
					USB_P2_2	—	SSPSCLK3		
B19	D17	GPIO<35>	ICOCZ	GPIO<35>	FFCTS	USB_P2_1	SSPSFRM3	Pd-0 Note[1]	Note [3]
					—	KP_MKOUT<6>	SSPTXD3		
C14	B13	GPIO<36>	ICOCZ	GPIO<36>	FFDCD	SSPSCLK2	KP_MKIN<7>	Pd-0 Note[1]	Note [3]
					USB_P2_4	SSPSCLK2	—		
A15	D13	GPIO<37>	ICOCZ	GPIO<37>	FFDSR	SSPSFRM2	KP_MKIN<3>	Pd-0 Note[1]	Note [3]
					USB_P2_8	SSPSFRM2	FFTXD		
B14	A13	GPIO<38>	ICOCZ	GPIO<38>	FFRI	KP_MKIN<4>	USB_P2_3	Pd-0 Note[1]	Note [3]
					SSPTXD3	SSPTXD2	PWM_OUT<1>		
D19	B17	GPIO<39>	ICOCZ	GPIO<39>	KP_MKIN<4>	—	SSPSFRM3	Pd-0 Note[1]	Note [3]
					USB_P2_6	FFTXD	SSPSFRM3		
D14	C12	GPIO<40>	ICOCZ	GPIO<40>	SSPRXD2	—	USB_P2_5	Pd-0 Note[1]	Note [3]
					KP_MKOUT<6>	FFDTR	SSPSCLK3		
C18	A19	GPIO<41>	ICOCZ	GPIO<41>	FFRXD	USB_P2_7	SSPRXD3	Pd-0 Note[1]	Note [3]
					KP_MKOUT<7>	FFRTS	—		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 11 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
C21	D20	GPIO<42>	ICOCZ	GPIO<42>	BTRXD	ICP_RXD	—	Pd-0 Note[1]	Note [3]
					—	—	CIF_MCLK		
C22	B21	GPIO<43>	ICOCZ	GPIO<43>	—	—	CIF_FV	Pd-0 Note[1]	Note [3]
					ICP_TXD	BTTXD	CIF_FV		
B20	A20	GPIO<44>	ICOCZ	GPIO<44>	BTCTS	—	CIF_LV	Pd-0 Note[1]	Note [3]
					—	—	CIF_LV		
C19	C17	GPIO<45>	ICOCZ	GPIO<45>	—	—	CIF_PCLK	Pd-0 Note[1]	Note [3]
					AC97_SYSCLK	BTRTS	SSPSYSCLK3		
B11	A9	GPIO<46>	ICOCZ	GPIO<46>	ICP_RXD	STD_RXD	—	Pd-0 Note[1]	Note [3]
					—	PWM_OUT<2>	—		
A11	C10	GPIO<47>	ICOCZ	GPIO<47>	CIF_DD<0>	—	—	Pd-0 Note[1]	Note [3]
					STD_TXD	ICP_TXD	PWM_OUT<3>		
C23	C22	GPIO<88>	ICOCZ	GPIO<88>	USBHPWR<1>	SSPRXD2	SSPSFRM2	Pd-0 Note[1]	Note [3]
					—	—	SSPSFRM2		
D22	C21	GPIO<89>	ICOCZ	GPIO<89>	SSPRXD3	—	FFRI	Pd-0 Note[1]	Note [3]
					AC97_SYSCLK	USBHPEN<1>	SSPTXD2		
A19	A18	GPIO<92>	ICOCZ	GPIO<92>	MMDAT<0>	—	—	Pd-0 Note[1]	Note [3]
					MMDAT<0>	MSBS	—		
AB19	Y16	GPIO<93>	ICOCZ	GPIO<93>	KP_DKIN<0>	CIF_DD<6>	—	Pd-0 Note[1]	Note [3]
					AC97_SDATA_OUT	—	—		
AD19	AA17	GPIO<94>	ICOCZ	GPIO<94>	KP_DKIN<1>	CIF_DD<5>	—	Pd-0 Note[1]	Note [3]
					AC97_SYNC	—	—		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 12 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AA18	AB18	GPIO<95>	ICOCZ	GPIO<95>	KP_DKIN<2>	CIF_DD<4>	KP_MKIN<6>	Pd-0 Note[1]	Note [3]
					AC97_RESET_n	—	—		
AC19	W16	GPIO<96>	ICOCZ	GPIO<96>	KP_DKIN<3>	MBREQ	FFRXD	Pd-0 Note[1]	Note [3]
						DVAL<1>	KP_MKOUT<6>		
AA17	Y15	GPIO<97>	ICOCZ	GPIO<97>	KP_DKIN<4>	DREQ<1>	KP_MKIN<3>	Pd-0 Note[1]	Note [3]
					—	MBGNT	—		
AD18	AA16	GPIO<98>	ICOCZ	GPIO<98>	KP_DKIN<5>	CIF_DD<0>	KP_MKIN<4>	Pd-0 Note [1]	Note [3]
					AC97_SYSCLK	—	FFRTS		
AB18	AB17	GPIO<99>	ICOCZ	GPIO<99>	KP_DKIN<6>	AC97_SDATA_IN_1	KP_MKIN<5>	Pd-0 Note [1]	Note [3]
					—	—	FFTXD		
AC18	AA15	GPIO<100>	ICOCZ	GPIO<100>	KP_MKIN<0>	DREQ<2>	FFCTS	Pd-0 Note[1]	Note [3]
					—	—	—		
AC17	AB16	GPIO<101>	ICOCZ	GPIO<101>	KP_MKIN<1>	—	—	Pd-0 Note[1]	Note [3]
					—	—	—		
AB17	Y14	GPIO<102>	ICOCZ	GPIO<102>	KP_MKIN<2>	—	FFRXD	Pd-0 Note[1]	Note [3]
					nPCE<1>	—	—		
AC16	AB15	GPIO<103>	ICOCZ	GPIO<103>	CIF_DD<3>	—	—	Pd-0 Note[1]	Note [3]
					—	KP_MKOUT<0>	—		
AD15	W14	GPIO<104>	ICOCZ	GPIO<104>	CIF_DD<2>	—	—	Pd-0 Note[1]	Note [3]
					PSKTSEL	KP_MKOUT<1>	—		
AB16	Y13	GPIO<105>	ICOCZ	GPIO<105>	CIF_DD<1>	—	—	Pd-0 Note[1]	Note [3]
					nPCE<2>	KP_MKOUT<2>	—		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 13 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AB15	W13	GPIO<106>	ICOCZ	GPIO<106>	CIF_DD<9>	—	—	Pd-0 Note[1]	Note [3]
					—	KP_MKOUT<3>	—		
AC15	AB14	GPIO<107>	ICOCZ	GPIO<107>	CIF_DD<8>	—	—	Pd-0 Note[1]	Note [3]
					—	KP_MKOUT<4>	—		
AD14	AA13	GPIO<108>	ICOCZ	GPIO<108>	CIF_DD<7>	—	—	Pd-0 Note[1]	Note [3]
					CHOUT<0>	KP_MKOUT<5>	—		
D17	D16	GPIO<109>	ICOCZ	GPIO<109>	MMDAT<1>	MSSDIO	—	Pd-0 Note[1]	Note [3]
					MMDAT<1>	MSSDIO	—		
B17	C15	GPIO<110>	ICOCZ	GPIO<110>	MMDAT<2>/MMCCS<0>	—	—	Pd-0 Note[1]	Note [3]
					MMDAT<2>/MMCCS<0>	—	—		
C17	A17	GPIO<111>	ICOCZ	GPIO<111>	MMDAT<3>/MMCCS<1>	—	—	Pd-0 Note[1]	Note [3]
					MMDAT<3>/MMCCS<1>	—	—		
B18	B16	GPIO<112>	ICOCZ	GPIO<112>	MMCMD	nMSINS	—	Pd-0 Note[1]	Note [3]
					MMCMD	—	—		
A13	A10	GPIO<113>	ICOCZ	GPIO<113>	—	—	USB_P3_3	Pd-0 Note[1]	Note [3]
					I2S_SYSCLK	AC97_RESET_n	—		
D24	F19	GPIO<114> Note [17]	ICOCZ	GPIO<114> Note [17]	CIFDD_<1>	—	—	Pd-0 Note[1]	Note [3]
						UVS0	—		
E21	E21	GPIO<115> Note [17]	ICOCZ	GPIO<115> Note [17]	DREQ<0>	CIF_DD<3>	MBREQ	Pu-1 Note[1]	Note [3]
					UEN	nUVS1	PWM_OUT<1>		

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 14 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
C24	E20	GPIO<116>	ICOCZ	GPIO<116>	CIF_DD<2>	AC97_SDATA_IN_0	UDET	Pu-1 Note[1]	Note [3]
					DVAL<0>	nUVS2	MBGNT		
D20	C18	GPIO<117>	ICOCZ	GPIO<117>	SCL	—	—	Pu-1 Note[1]	Note [3], Note[12]
					SCL	—	—		
A22	B20	GPIO<118>	ICOCZ	GPIO<118>	SDA	—	—	Pu-1 Note[1]	Note [3], Note[12]
					SDA	—	—		
VCC_USB									
B22	D18	USBC_P	IAOAZ	USBC_P	USBC_P	—	—	Hi-Z	Hi-Z
C20	E19	USBC_N	IAOAZ	USBC_N	USBC_N	—	—	Hi-Z	Hi-Z
E22	E22	USBH_P<1>	IAOAZ	USBH_P<1>	USBH_P<1>	—	—	Hi-Z	Hi-Z
D23	D22	USBH_N<1>	IAOAZ	USBH_N<1>	USBH_N<1>	—	—	Hi-Z	Hi-Z
VCC_USIM									
F22	H19	GPIO<90>	ICOCZ	GPIO<90>	KP_MKIN<5>	USB_P3_5	CIF_DD<4>	Pd-0 Note[1]	Note [3]
					—	nURST	—		
F23	G19	GPIO<91>	ICOCZ	GPIO<91>	KP_MKIN<6>	USB_P3_1	CIF_DD<5>	Pd-0 Note[1]	Note [3]
					—	UCLK	—		
E23	F20	UIO	ICOCZ	UIO	UIO	—	—	Driven Low	Hi-Z
VCC_REG									
V22	U20	GPIO<0>	ICOCZ	GPIO<0>	GPIO<0>	—	—	Pd-0 Note[1]	Note [3]
Y24	U21	GPIO<1>	ICOCZ	GPIO<1>	GPIO<1>	—	—	Pu-1 Note[1]	Note [7]

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 15 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
W21	V22	GPIO<3>	ICOCZ	GPIO<3>	PWR_SCL	—	—	Pu-1 Note[1]	Hi-Z
W23	T19	GPIO<4>	ICOCZ	GPIO<4>	PWR_SDA	—	—	Pu-1 Note[1]	Hi-Z
U22	T22	GPIO<9> Note [18]	ICOCZ	GPIO<9> Note [18]	—	—	FFCTS	Pd-0 Note[1]	Note [7]
					HZ_CLK	—	CHOUT<0>		
V23	U22	GPIO<10> Note [18]	ICOCZ	GPIO<10> Note [18]	FFDCD	—	USB_P3_5	Pd-0 Note[1]	Note [7]
					HZ_CLK	—	CHOUT<1>	Pd-0 Note[1]	Note [7]
W24	T21	CLK_REQ	ICOCZ	CLK_REQ	CLK_REQ	—	—	Pu-1	Note [8]
Y22	W20	NRESET	IC	nRESET	nRESET	—	—	Input - Note [9]	Input
Y21	W21	NRESET_OUT	OC	nRESET_OUT	nRESET_OUT	—	—	Low	Note [8]
AB23	V19	BOOT_SEL	IC	BOOT_SEL	BOOT_SEL	—	—	Input	Input
Y23	W22	PWR_EN	OC	PWR_EN	PWR_EN	—	—	Note[16]	Note [8]
AB24	U19	NBATT_FAULT	IC	nBATT_FAULT	nBATT_FAULT	—	—	Low	Input
W22	V20	NVDD_FAULT	IC	nVDD_FAULT	nVDD_FAULT	—	—	Low	Input
AA24	V21	SYS_EN	ICOCZ	SYS_EN	SYS_EN	—	—	—	Note [7]
AB21	Y19	PWR_CAP<0>	OA	—	PWR_CAP<0>	—	—	—	Note [7]
AD22	AA21	PWR_CAP<1>	OA	—	PWR_CAP<1>	—	—	—	Note [7]
AC22	Y18	PWR_CAP<2>	OA	—	PWR_CAP<2>	—	—	—	Note [7]

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 16 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AA20	W17	PWR_CAP<3>	OA	—	PWR_CAP<3>	—	—	—	Note [7]
U21	T20	NTRST	IC	nTRST	nTRST	—	—	Input - Note [9]	Input
U23	R22	TDI	IC	TDI	TDI	—	—	Input - Note [9]	Input
V24	R21	TDO	OCZ	TDO	TDO	—	—	Hi-Z	Hi-Z
T21	R20	TMS	IC	TMS	TMS	—	—	Input - Note [9]	Input
T22	R19	TCK	IC	TCK	TCK	—	—	Input	Input
T23	P22	TESTCLK	IC	TESTCLK	TESTCLK	—	—	Pd-0	Input
VCC_OSC									
AC21	AB20	PXTAL_IN	IA	PXTAL_IN	PXTAL_IN	—	—	Note[2]	Note [2]
AD21	AA20	PXTAL_OUT	OA	PXTAL_OUT	PXTAL_OUT	—	—	Note[2]	Note [2]
AA22	Y21	TXTAL_IN	IA	TXTAL_IN	TXTAL_IN	—	—	Note[2]	Note [2]
AA23	Y22	TXTAL_OUT	OA	TXTAL_OUT	TXTAL_OUT	—	—	Note[2]	Note [2]
AB22	W19	PWR_OUT	OA	PWR_OUT	PWR_OUT	—	—	Hi-Z	Hi-Z
SUPPLIES									
AB20	Y17	VCC_BATT	PS	VCC_BATT	VCC_BATT	—	—	Input	Input
A12	B10	VCC_IO	PS	VCC_IO	VCC_IO	—	—	Input	Input
AD17	W15	VCC_IO	PS	VCC_IO	VCC_IO	—	—	Input	Input
A16	D14	VCC_IO	PS	VCC_IO	VCC_IO	—	—	Input	Input
B24	A21	VCC_USB	PS	VCC_USB	VCC_USB	—	—	Input	Input
A24	A22	VCC_USB	PS	VCC_USB	VCC_USB	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 17 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
A23	B22	VCC_USB	PS	VCC_USB	VCC_USB	—	—	Input	Input
B23	D19	VCC_USB	PS	VCC_USB	VCC_USB	—	—	Input	Input
P24	M19	VCC_LCD	PS	VCC_LCD0	VCC_LCD	—	—	Input	Input
J24	J21	VCC_LCD	PS	VCC_LCD1	VCC_LCD	—	—	Input	Input
P1	B2	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
C3	C3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
E2	C6	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
L3	C9	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AD2	F3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AC2	H3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AC1	K3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AD1	M3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
M1	P3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
H1	T3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
F1	V3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AD8	Y3	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
U2	Y5	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 18 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AA2	Y7	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AC8	Y9	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
B8	AA2	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
A4	N/A	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AC6	N/A	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
W2	N/A	VCC_MEM	PS	VCC_MEM	VCC_MEM	—	—	Input	Input
AD12	AA11	VCC_BB	PS	VCC_BB	VCC_BB	—	—	Input	Input
AC20	AB19	VCC_PLL	PS	VCC_PLL	VCC_PLL	—	—	Input	Input
A9	B4	VCC_SRAM	PS	VCC_SRAM	VCC_SRAM	—	—	Input	Input
A8	B7	VCC_SRAM	PS	VCC_SRAM	VCC_SRAM	—	—	Input	Input
A5	B8	VCC_SRAM	PS	VCC_SRAM	VCC_SRAM	—	—	Input	Input
B4	C5	VCC_SRAM	PS	VCC_SRAM	VCC_SRAM	—	—	Input	Input
B12	D11	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
A7	E6	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
D3	E8	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
J23	F5	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
L24	H5	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 19 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
F24	L4	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
AD16	E15	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
R24	E17	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
M23	F18	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
B21	H18	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
W3	L19	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
AD4	R5	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
T2	U5	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
AD11	V6	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
N/A	V8	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
N/A	W11	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
N/A	R18	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
N/A	U18	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
N/A	V15	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
N/A	V17	VCC_CORE	PS	VCC_CORE	VCC_CORE	—	—	Input	Input
E24	F21	VCC_USIM	PS	VCC_USIM	VCC_USIM	—	—	Input	Input
AA21	W18	VSS	PS	VSS	VSS	—	—	Input	Input
AC24	Y20	VSS	PS	VSS	VSS	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 20 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AD24	AA22	VSS	PS	VSS	VSS	—	—	Input	Input
AC23	AB21	VSS	PS	VSS	VSS	—	—	Input	Input
AD23	AB22	VSS	PS	VSS	VSS	—	—	Input	Input
V21	N/A	VSS	PS	VSS	VSS	—	—	Input	Input
D11	B12	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
AA19	B15	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
D15	B18	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
N21	D21	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
AA16	H21	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
H21	M21	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
F21	N19	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
D18	AA14	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
U24	AA18	VSS_IO	PS	VSS_IO	VSS_IO	—	—	Input	Input
D5	A1	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
F4	A2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
H4	B1	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
J4	B3	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
AC3	B6	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
AB2	B9	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
L4	F2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
T4	H2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
V4	L2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 21 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
AA5	P2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
AA8	T2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
AA9	V2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
D9	AA1	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
N4	AA6	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
R2	AA9	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
C5	AB1	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
Y4	AB2	VSS_MEM	PS	VSS_MEM	VSS_MEM	—	—	Input	Input
AA13	AB11	VSS_BB	PS	VSS_BB	VSS_BB	—	—	Input	Input
AD20	AA19	VSS_PLL	PS	VSS_PLL	VSS_PLL	—	—	Input	Input
B2	E5	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
A2	E7	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
B1	E9	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
A1	G5	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
J21	J5	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
D10	E14	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
AA15	E16	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

Table 3: Pin Use Summary (Sheet 22 of 22)

VF-BGA Ball# (13x13)	PBGA Ball# (23x23)	Name	Type	Function After Reset	Primary Function	Secondary Alternate Function	Third Alternate Function	Reset State	Sleep State
M21	E18	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
U3	G18	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
AA7	J18	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
P21	P5	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
K21	T5	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
G21	V5	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
D21	V7	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
D12	V9	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
D8	P18	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
W4	T18	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
AA12	V14	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
B5	V16	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input
D7	V18	VSS_CORE	PS	VSS_CORE	VSS_CORE	—	—	Input	Input

NOTE: Refer to Table 4 for Numbered Notes on Reset and Sleep States.

4.3 Signal Types

Table 4: Pin Use and Mapping Notes (Sheet 1 of 2)

Note	Description
[1]	*GPIO reset/deep sleep operation:* After any reset is asserted or if the PXA270 processor is in deep sleep mode, these pins are configured as GPIO inputs by default. The input buffers for these pins are disabled to prevent current drain and must be enabled prior to use by clearing the *read disable hold* bit, PSSR[RDH]. Until RDH is cleared, each pin is pulled high (Pu-1), pulled low (Pd-0), or floated (Hi-Z).
[2]	*Crystal oscillator pins:* These pins connect the external crystals to the on-chip oscillators and are not affected by either reset or sleep. For more information, see the “Clocks and Power” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual*.
[3]	*GPIO sleep operation:* During the transition into sleep mode, the configuration of these pins is determined by the corresponding GPIO setting. This pin is not driven during sleep if the direction of the pin is selected to be an input. If the direction of the pin is selected as an output, the value contained in the Power Manager GPIO Sleep-State register (PGSR0/1/2/3) is driven out onto the pin and held while the PXA270 processor is in sleep mode. Upon exit from sleep mode, GPIOs that are configured as outputs continue to hold the standby, sleep, or deep-sleep state until software clears the peripheral control hold bit, PSSR[PH]. Software must clear this bit (by writing 0b1 to it) after the peripherals have been fully configured, as described in Note[1], but before the process actually uses them. GPIOs that are configured as inputs immediately after exiting sleep mode cannot be used until PSSR[RDH] is cleared.
[4]	*Static memory control pins:* During sleep mode, these pins can be programmed either to drive the value in the Power Manager GPIO Sleep-State register (PGSR0/1/2/3) or to be placed in a Hi-Z (undriven) state. To select the Hi-Z state, software must set PCFR[FS]. If FS is not set, these pins function as described in Note[3] during the transition to sleep mode.
[5]	*PCMCIA control pins:* During sleep mode, these pins can be programmed either to drive the value in the Power Manager GPIO Sleep-State register (PGSR0/1/2/3) or to be placed in a Hi-Z (undriven) state. To select the Hi-Z state, software must set PCFR[FP]. If FP is not set, these pins function as described in Note[3] during the transition to sleep mode.
[6]	(reserved)
[7]	When the power manager overrides the GPIO alternate function, the Power Manager GPIO Sleep-State registers (PGSR0/1/2/3) and the PSSR[RDH] bit are ignored. Pullup and pulldown are disabled immediately after the power manager overrides the GPIO function.
[8]	Output functions during sleep mode
[9]	Pull-up always enabled
[10]	(reserved)
[11]	Pins do not function during sleep mode if the OS timer is active
[12]	Pins must be floated by software during sleep mode (floating does not happen automatically)
[13]	(reserved)
[14]	(reserved)
[15]	The pin is three-stateable (Hi-Z) based on the value of PCFR[FS]. There is no PGSR0/1/2/3 setting associated with the pin because it is not a GPIO.
[16]	PWR_EN goes high during reset, between the assertion of the reset pin and the de-assertion of internal reset within the PXA270 processor, after SYS_EN is driven high.

Table 4: Pin Use and Mapping Notes (Sheet 2 of 2)

Note	Description
[17]	*GPIOs 114 and115:* The alternate function configuration of these pins is ignored when either PUCR[USIM114] or PUCR[USIM115] bits are set. Setting these bits forces the USIM enable signal onto these GPIOs.
[18]	When software sets the OSCC[PIO_EN] or OSCC[TOUT_EN] bits, then any GPIO alternate function setting applied to GPIO<9> or GPIO <10> is overridden with the CLK_PIO function on GPIO<9> and CLK_TOUT on GPIO<10>.
[19]	Refer to Table 6.

Table 5: Signal Types

Type	Description
IC	CMOS input
OC	CMOS output
OCZ	CMOS output, three-stateable
ICOCZ	CMOS bidirectional, three-stateable
IA	Analog input
OA	Analog output
IAOA	Analog bidirectional
IAOAZ	Analog bidirectional - three-stateable
PS	Power supply

4.4 Memory Controller Reset and Initialization

On reset, the SDRAM interface is disabled. Reset values for the boot ROM are determined by BOOT_SEL (see the *Marvell® PXA27x Processor Family Developers Manual*, Memory Controller chapter). Boot ROM is immediately available for reading upon exit from reset, and all memory interface control registers are available for writing.

On hardware reset, the memory pins and controller are in the state shown in Table 6.

Table 6: Memory Controller Pin Reset Values (Sheet 1 of 2)

Pin Name	Reset, Sleep, Standby, Deep-Sleep, Frequency Change, and Manual Self-Refresh Mode Values
SDCLK <3[1]:0>	0b000
SDCKE	0
DQM <3:0>	0b0000
nSDCS <3:2>	GPIO (memory controller drives 0b11)[†]
nSDCS <1:0>	0b11
nWE	1
nSDRAS	1
nSDCAS	1
nOE	1

Table 6: Memory Controller Pin Reset Values (Sheet 2 of 2)

Pin Name	Reset, Sleep, Standby, Deep-Sleep, Frequency Change, and Manual Self-Refresh Mode Values
MA <25:0>	0x0000_0000[1]
RDnWR	0
MD <31:0>	0x0000_0000[2]
nCS <0>	1
nCS <5:1>	GPIO (memory controller drives 0b11111)
nPIOIR	GPIO (memory controller drives high)
nPIOIW	GPIO (memory controller drives high)
nPOE	GPIO (memory controller drives high)
nPWE	GPIO (memory controller drives high)

NOTE:
† This indicates that the GPIO pin, if configured for the alternate function used by the memory controller during reset, drives the represented value.
NOTE: SCLK<3> is only available on PXA270 processor family packages
1. MA pins are driven
2. MD pins are pulled low

The address signals are driven low and data signals are pulled low during sleep, standby, deep-sleep, frequency-change modes, and manual self-refresh. All other memory control signals are in the same state that they are in after a hardware reset. If the SDRAMs are in self-refresh mode, they are kept there by driving SDCKE low.

4.5 Power-Supply Pins

Table 7 summarize the power-supply ball count.

Table 7: Discrete (13x13 VF-BGA) Power Supply Pin Summary (Sheet 1 of 2)

Name	Number of Package Balls 13x13 mm VF-BGA	Number of Pachage Balls 23x23 mm PBGA
VCC_BATT	1	1
VCC_IO	3	3
VCC_USB	4	4
VCC_LCD	2	2
VCC_MEM	19	16
VCC_BB	1	1
VCC_PLL	1	1
VCC_SRAM	4	4
VCC_CORE	14	20
VCC_USIM	1	1
VSS	6	5

Table 7: Discrete (13x13 VF-BGA) Power Supply Pin Summary (Sheet 2 of 2)

Name	Number of Package Balls 13x13 mm VF-BGA	Number of Pachage Balls 23x23 mm PBGA
VSS_IO	9	9
VSS_MEM	17	17
VSS_BB	1	1
VSS_PLL	1	1
VSS_CORE	56	56

5 Electrical Specifications

5.1 Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 8) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the Marvell® PXA270 processor.

Note

Absolute maximum ratings are not operating ranges.

Table 8: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
T_S	Storage temperature	–40	125	°C
V_{CC_OL1}	Offset voltage between any of the following pins: VCC_CORE	–0.3	0.3	V
V_{CC_OL2}	Offset voltage between any of the following pins: VCC_SRAM	–0.3	0.3	V
V_{CC_OH1}	Offset voltage between any of the following pins: VCC_MEM	–0.3	0.3	V
V_{CC_OH2}	Offset voltage between any of the following pins: VCC_IO	–0.3	0.3	V
V_{CC_OH3}	Offset voltage between VCC_LCD<0> and VCC_LCD<1>	–0.3	0.3	V
V_{CC_HV}	Voltage applied to high-voltage supply pins (VCC_BB, VCC_USB, VCC_USIM, VCC_MEM, VCC_IO<, VCC_LCD)	VSS–0.3	VSS+4.0	V
V_{CC_LV}	Voltage applied to low-voltage supply pins (VCC_CORE, VCC_PLL, VCC_SRAM)	VSS–0.3	VSS+1.45	V
V_{IP}	Voltage applied to non-supply pins except PXTAL_IN, PXTAL_OUT, TXTAL_IN, and TXTAL_OUT pins	VSS–0.3	VSS+4.0	V
V_{IP_X}	Voltage applied to XTAL pins (PXTAL_IN, PXTAL_OUT, TXTAL_IN, TXTAL_OUT)	VSS–0.3	VSS+1.45	V
V_{ESD}	Maximum ESD stress voltage, three stresses maximum: Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity	—	2000	V
I_{EOS}	Maximum DC input current (electrical overstress) for any non-supply pin	—	5	mA

5.2 Operating Conditions

This section shows operating voltage, frequency, and temperature specifications for the PXA270 processor.

Table 9 shows each power domains supported voltages (except for VCC_MEM and VCC_CORE). Table 10 shows all of the supported memory voltages and frequency operating ranges (VCC_MEM). Table shows all of the supported core voltage and frequency ranges (VCC_CORE).

The operating temperature specification is a function of voltage and frequency.

Table 9: Voltage, Temperature, and Frequency Electrical Specifications (Sheet 1 of 3)

Symbol	Description	Min	Typical	Max	Units
Operating Temperature					
Tcase	Package operating temperature† (Standard Temp)	-25	—	+85	°C
	Package operating temperature† (Extended Temp - PBGA ONLY)	-40	—	+85	
Theta Jc	Junction-to-case temperature gradient (VF-BGA)	—	2	—	°C / watt
	Junction-to-case temperature gradient (PBGA)	—	1.4	—	
VCC_BATT Voltage					
VVCC0	Voltage applied on VCC_BATT @3.0V	2.40	3.00	3.75	V
VVDF1	Voltage difference between VCC_BATT and VCC_IO during power-on reset or deep-sleep wake-up (from the assertion of SYS_EN to the de-assertion of nRESET_OUT)	0	—	0.30	V
VVDF2	Voltage difference between VCC_BATT and VCC_IO when VCC_IO is enabled	0	—	0.20	V
Tbramp	Ramp Rate	—	10	12	mV/µS
VCC_PLL Voltage					
VVCC1	Voltage applied on VCC_PLL @1.3V (+10 / -10%)	1.17	1.30	1.43	V
Tpwrramp	Ramp Rate	—	10	12	mV/µS
VCC_BB Voltages					
VVCC2a	Voltage applied on VCC_BB @1.8V (+20 / -5%)	1.71	1.80	2.16	V
VVCC2b	Voltage applied on VCC_BB @2.5V (+10 / -10%)	2.25	2.50	2.75	V
VVCC2c	Voltage applied on VCC_BB @3.0V (+10 / -10%)	2.70	3.0	3.30	V
VVCC2d	Voltage applied on VCC_BB @3.3V (+10 / -10%)	2.97	3.3	3.63	V
Tsysramp	Ramp Rate	—	10	12	mV/µS

Table 9: Voltage, Temperature, and Frequency Electrical Specifications (Sheet 2 of 3)

Symbol	Description	Min	Typical	Max	Units
VCC_BB may optionally be tied to the same PMIC regulator as VCC_IO if the system design allows both VCC_IO and VCC_BB to use the same voltage level. This allows the GPIO's on VCC_BB to be used at the same voltage level.					
VCC_LCD Voltages					
VVCC3a	Voltage applied on VCC_LCD @1.8V (+20 / -5%)	1.71	1.80	2.16	V
VVCC3b	Voltage applied on VCC_LCD @2.5V (+10 / -10%)	2.25	2.50	2.75	V
VVCC3c	Voltage applied on VCC_LCD @3.0V (+10 / -10%)	2.70	3.0	3.30	V
VVCC3d	Voltage applied on VCC_LCD @3.3V (+10 / -10%)	2.97	3.3	3.63	V
Tsysramp	Ramp Rate	—	10	12	mV/µS
VCC_IO Voltages					
VVCC4a	Voltage applied on VCC_IO @3.0V (+10 / -10.3%)	2.69175	3.0	3.30	V
VVCC4b	Voltage applied on VCC_IO @3.3V (+10 / -10%)	2.97	3.3	3.63	V
Tsysramp	Ramp Rate	—	10	12	mV/µS
VCC_IO must be maintained at a voltage as high as or higher than, all other supplies except for VCC_BATT and VCC_USB					
VCC_USIM Voltages					
VVCC5a	Voltage applied on VCC_USIM @1.8V (+20 / -5%)	1.71	1.80	2.16	V
VVCC5b	Voltage applied on VCC_USIM @3.0V (+10 / -10%)	2.70	3.0	3.30	V
Tsysramp	Ramp Rate	—	10	12	mV/µS
If the system does NOT use the USIM module, VCC_USIM can be tied to VCC_IO (at any supported VCC_IO voltage level). This allows the GPIO's on VCC_USIM to be used at the same voltage level as VCC_IO GPIO's. **NOTE:** Software must NOT configure USIM signals to be used if this is done.					
VCC_SRAM Voltage					
VVCC6	Voltage applied on VCC_SRAM @1.1V (+10 / -10%)	0.99	1.10	1.21	V
Tpwrramp	Ramp Rate	—	10	12	mV/µS
VCC_USB Voltage					
VVCC7a	Voltage applied on VCC_USB @3.0V (+10 / -10%)	2.70	3.00	3.30	V

Table 9: Voltage, Temperature, and Frequency Electrical Specifications (Sheet 3 of 3)

Symbol	Description	Min	Typical	Max	Units
VVCC7b	Voltage applied on VCC_USB @3.3V (+10 / -10%)	2.97	3.30	3.63	V
Tsysramp	Ramp Rate	—	10	12	mV/µS
† System design must ensure that the device case temperature is maintained within the specified limits. In some system applications it may be necessary to use external thermal management (for example, a package-mounted heat spreader) or configure the device to limit power consumption and maintain acceptable case temperatures.					

Table 10 shows the supported memory frequency and memory supply voltage operating ranges for the PXA270 processor.

Table 10: Memory Voltage and Frequency Electrical Specifications

Symbol	Description	Min	Typical	Max	Units
Memory Voltage and Frequency Range 1					
VMEM1	Voltage applied on VCC_MEM	1.71	1.80	2.16	V
fSM1A	External synchronous memory frequency, SDCLK1, SDCLK2	13	—	104	MHz
fSM1B	External synchronous memory frequency, SDCLK0	13	—	104	MHz
Tsysramp	Ramp Rate	—	10	12	mV/µS
Memory Voltage and Frequency Range 2					
VMEM2	Voltage applied on VCC_MEM	2.25	2.50	2.75	V
fSM2A	External synchronous memory frequency, SDCLK1, SDCLK2	13	—	104	MHz
fSM2B	External synchronous memory frequency, SDCLK0	13	—	104	MHz
Tsysramp	Ramp Rate	—	10	12	mV/µS
Memory Voltage and Frequency Range 3					
VMEM3	Voltage applied on VCC_MEM	2.70	3.0	3.3	V
fSM3A	External synchronous memory frequency, SDCLK1, SDCLK2	13	—	104	MHz
fSM3B	External synchronous memory frequency, SDCLK0	13	—	104	MHz
Tsysramp	Ramp Rate	—	10	12	mV/µS
Memory Voltage and Frequency Range 4					
VMEM4	Voltage applied on VCC_MEM	2.97	3.30	3.63	V
fSM4A	External synchronous memory frequency, SDCLK1, SDCLK2	13	—	104	MHz
fSM4B	External synchronous memory frequency, SDCLK0	13	—	104	MHz
Tsysramp	Ramp Rate	—	10	12	mV/µS

Table 11 shows the supported core frequency and core supply voltage operating ranges for the PXA270 processor. Each frequency range is specified in the following format:

(core frequency/internal system bus frequency/memory controller frequency/SDRAM frequency)

Note

Refer to the “Clocks and Power” section of the *Marvell® PXA27x Processor Family Developers Manual* for supported frequencies, clock register settings as listed in Table 11.

Table 11: Core Voltage and Frequency Electrical Specifications (Sheet 1 of 2)

Symbol	Description	Min	Typical	Max	Units
Core Voltage and Frequency Range 1 (13/13/13/13 CCCR[CPDIS]=1, CCCR[PPDIS]=1)					
VVCCC1	Voltage applied on VCC_CORE	0.95	1.0	1.705	V
fCORE1	Core operating frequency	13	—	13	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 2 (13/13/13/13 CCCR[CPDIS]=1, CCCR[PPDIS]=0), (91/45.5/91/45.5), and (104/104/104/104)					
VVCCC2	Voltage applied on VCC_CORE	0.95	1.0	1.705	V
fCORE2	Core operating frequency	91	—	104	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 3 (156/104/104/104)					
VVCCC3	Voltage applied on VCC_CORE	0.95	1.00	1.705	V
fCORE3	Core operating frequency	—	156	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 4 (208/208/208/104) and (208/208/104/104)					
VVCCC4	Voltage applied on VCC_CORE	1.12	1.18	1.705	V
fCORE4	Core operating frequency	—	208	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 4a (208/104/104/104)					
VVCCC4a	Voltage applied on VCC_CORE	0.9975	1.05	1.705	V
fCORE4a	Core operating frequency	—	208	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 5 (312/208/208/104) and (312/208/104/104)					
VVCCC5	Voltage applied on VCC_CORE	1.1875	1.25	1.705	V
fCORE5	Core operating frequency	—	312	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 5a (312/104/104/104)					
VVCCC5a	Voltage applied on VCC_CORE	0.99	1.1	1.705	V
fCORE5a	Core operating frequency	—	312	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS

Table 11: Core Voltage and Frequency Electrical Specifications (Sheet 2 of 2)

Core Voltage and Frequency Range 6 (416/208/208/104) amd (416/208/104/104)					
VVCCC6	Voltage applied on VCC_CORE	1.2825	1.35	1.705	V
fCORE6	Core operating frequency	—	416	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 7 (520/208/208/104) and (520/208/104/104)					
VVCCC7	Voltage applied on VCC_CORE	1.3775	1.45	1.705	V
fCORE7	Core operating frequency	—	520	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
Core Voltage and Frequency Range 8 (624/208/208/104) and (624/208/104/104)					
VVCCC8	Voltage applied on VCC_CORE	1.4725	1.55	1.705	V
fCORE8	Core operating frequency	—	624	—	MHz
Tpwrramp	Ramp Rate	—	10	12	mV/µS
†Core operating frequency not offered in PBGA package.					

5.2.1 Internal Power Domains

The external power supplies are used to generate several internal power domains, which are shown in Table 12. Refer to the Power Manager / Internal Power Domain Block Diagram in the “Clocks and Power” section of the *Marvell® PXA27x Processor Family Developers Manual* for more information on internal power domains.

Table 12: Internally Generated Power Domain Descriptions

Name	Units	Generation	Tolerance
VCC_REG	IO associated with deep-sleep-active units	Switched between VCC_BATT and VCC_IO	-
VCC_OSC	Oscillator power supplies	Generated from VCC_REG	+/- 30%
VCC_RTC	RTC and power manager supply	Switched between VCC_OSC and VCC_CORE	-
VCC_PI	Power manager I^2C supply	Switched between VCC_OSC and VCC_CORE	-
VCC_CPU	CPU core	Independent power-down from VCC_CORE	-
VCC_PER	Peripheral units	Independent power-down from VCC_CORE	-
VCC_Rx	Particular internal SRAM unit	Switched between VCC_OSC and VCC_SRAM	-

Table 13 shows the recommended core voltage specification for each of the lower power modes.

Table 13: Core Voltage Specifications For Lower Power Modes

Mode	Description	Min	Typical	Max	Units
Standby	Voltage applied on VCC_CORE	1.045	1.1	1.21	V
Deep-Idle	Voltage applied on VCC_CORE	0.95	1.0	1.705	V

5.3 Power-Consumption Specifications

Power consumption depends on the operating voltage and frequency, peripherals enabled, external switching activity, and external loading and other factors.

Use these specifications as a guideline for power consumption capacity. These typical guidelines vary across different platforms and software applications.

Table 14 contains three sets of power consumption information: *Active Power Consumption*, *Idle Power Consumption*, and *Low-Power Modes Power Consumption*.

The data set are projected numbers based off of measured data at room temperature. For Active Power Consumption data, no peripherals are enabled except for UART.

Table 15 contains idle and low power mode maximum power consumption information based on experimental and manufacturing test limits.

Table 14: Typical Power-Consumption Specifications (Sheet 1 of 4)

Parameter Description	Typical	Units	Conditions
Active Power Consumption			
624 MHz Active Power (208 MHz System bus)	925	mW	VCC_CORE = 1.55V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
520 MHz Active Power (208 MHz System bus)	747	mW	VCC_CORE = 1.45V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
416 MHz Active Power (208 MHz System bus)	570	mW	VCC_CORE = 1.35V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
312 MHz Active Power (208 MHz System bus)	390	mW	VCC_CORE = 1.25V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
312 MHz Active Power (104 MHz System bus)	375	mW	VCC_CORE = 1.1V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V

Table 14: Typical Power-Consumption Specifications (Sheet 2 of 4)

Parameter Description	Typical	Units	Conditions
208 MHz Active Power (208 MHz System bus)	279	mW	VCC_CORE = 1.15V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
104 MHz Active Power (104 MHz System bus)	116	mW	VCC_CORE = 0.9V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
13 MHz Active Power (CCCR[CPDIS=1)	44.2	mW	VCC_CORE = 0.85V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
Idle Power Consumption			
624 MHz Idle Power (208 MHz System bus)	260	mW	VCC_CORE = 1.55V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
520 MHz Idle Power (208 MHz System bus)	222	mW	VCC_CORE = 1.45V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
416 MHz Idle Power (208 MHz System bus)	186	mW	VCC_CORE = 1.35V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
312 MHz Idle Power (208 MHz System bus)	154	mW	VCC_CORE = 1.25V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V

Table 14: Typical Power-Consumption Specifications (Sheet 3 of 4)

Parameter Description	Typical	Units	Conditions
312 MHz Idle Power (104 MHz System bus)	109	mW	VCC_CORE = 1.1V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
208 MHz Idle Power (208 MHz System bus)	129	mW	VCC_CORE = 1.15V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
104 MHz Idle Power (104 MHz System bus)	64	mW	VCC_CORE = 0.9V VCC_SRAM = 1.1V VCC_PLL = 1.3V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
Low Power modes Power Consumption			
13 MHz Idle Mode[1] Power (LCD on)	15.4	mW	VCC_CORE, VCC_SRAM, VCC_PLL = 0.85V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
13 MHz Idle Mode[1] Power (LCD off)	8.5	mW	VCC_CORE, VCC_SRAM, VCC_PLL = 0.85V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
Deep-Sleep mode	0.1014	mW	VCC_CORE, VCC_SRAM, VCC_PLL = 0V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V

Table 14: Typical Power-Consumption Specifications (Sheet 4 of 4)

Parameter Description	Typical	Units	Conditions
Sleep mode	0.1630	mW	VCC_CORE, VCC_SRAM, VCC_PLL = 0V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
Standby mode	1.7224	mW	VCC_CORE, VCC_SRAM, VCC_PLL = 1.1V VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
NOTE: 1) 13 MHz Idle Mode (CCCR[CPDIS] =1 (CCCR[PPDIS] = 1)			

Table 15: Maximum Idle and Low Power Mode Power-Consumption Specifications

Parameter Description	Maximum	Units	Conditions
Idle Mode Power Consumption			
624MHz Idle Current on VCC_CORE (PX=208MHz)	770	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=1.705V, VCC_PERI[1]=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
520MHz Idle Current on VCC_CORE (PX=208MHz)	630	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=1.595V, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
416MHz Idle Current on VCC_CORE (PX=208MHz)	500	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=1.485V, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
312MHz Idle Current on VCC_CORE (PX=208MHz)	380	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=1.375V, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
208MHz Idle Current on VCC_CORE (PX=208MHz)	260	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=1.265V, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V

Parameter Description	Maximum	Units	Conditions
104MHz Idle Current on VCC_CORE, (PX=104MHz)	150	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=0.99V, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
Idle Current on VCC_PERI[1], All Core Speeds	200	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=any, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
Idle Current on VCC_IO, All Core Speeds	50	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=any, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
Idle Current on VCC_PLL, All Core Speeds	100	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=any, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
Deep-Idle Mode Power Consumption			
13MHz Deep Idle Current on VCC_CORE (LCD off)	105	mA	Temp=85C Tcase, VCC_CORE=VCC_SRAM=VCC_PLL=0.935V, VCC_PERI=3.63V, VCC_IO=3.63V, VCC_BATT=3.75V
Standby Mode Power Consumption			
Standby Current on VCC_CORE	5	mA	Temp=Room, VCC_CORE=VCC_SRAM=VCC_PLL=1.1V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V
Standby Current on VCC_PERI	1.6	mA	Temp=Room, VCC_CORE=VCC_SRAM=VCC_PLL=1.1V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V
Standby Current on VCC_IO	1	mA	Temp=Room, VCC_CORE=VCC_SRAM=VCC_PLL=1.1V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V
Sleep Mode Power Consumption			
Sleep Current on VCC_CORE	0.15	mA	Temp=Room, VCC_CORE=VCC_PLL=0V, VCC_SRAM=0.95V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V

Parameter Description	Maximum	Units	Conditions
Sleep Current on VCC_PERI	0.47	mA	Temp=Room, VCC_CORE=VCC_PLL=0V, VCC_SRAM=0.95V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V
Sleep Current on VCC_IO	0.70	mA	Temp=Room, VCC_CORE=VCC_PLL=0V, VCC_SRAM=0.95V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V
Sleep Current on VCC_PLL	0.043	mA	Temp=Room, VCC_CORE=VCC_PLL=0V, VCC_SRAM=0.95V, VCC_PERI=1.8V, VCC_IO=VCC_BATT=3.0V
NOTE: 1) VCC_PERI = VCC_MEM + VCC_BB + VCC_USIM + VCC_LCD			

5.4 DC Specification

The DC characteristics for each pin include input sense levels, output drive levels, and currents. These parameters can be used to determine maximum DC loading and to determine maximum transition times for a given load. Table 16 shows the DC operating conditions for the high- and low-strength input, output, and I/O pins.

Note

VCC_IO must be maintained at a voltage as high as or higher than all other supplies except VCC_BATT and VCC_USB.

Table 16: Standard Input, Output, and I/O Pin DC Operating Conditions (Sheet 1 of 2)

Symbol	Description	Min	Max	Units	Testing Conditions / Notes
Input DC Operating Conditions (VCC = 1.8V, 2.5, 3.0, 3.3 Typical)					
VIH[1]	Input high voltage, all standard input and I/O pins, relative to applicable VCC (VCC_IO, VCC_MEM, VCC_BB, VCC_LCD, or VCC_USIM)	0.8 * VCC	VCC + 0.1	V	—
VIH_USB	Input high voltage for the USB bus voltage domain (VCC_USB)	0.8 * VCC	3.6	V	—
VIL[1]	Input low voltage, all standard input and I/O pins, relative to applicable VSS (VSS_IO, VSS_MEM, or VSS_BB) and VCC (VCC_IO, VCC_MEM, VCC_BB, VCC_LCD, VCC_USB, or VCC_USIM)	VSS - 0.1	0.2 * VCC	V	—
OS	DC Overshoot voltage / duration	—	+1	V	Max duration of 4nS

Table 16: Standard Input, Output, and I/O Pin DC Operating Conditions (Sheet 2 of 2)

Symbol	Description	Min	Max	Units	Testing Conditions / Notes
US	DC Undershoot voltage / duration	—	-1	V	Max duration of 4nS
Output DC Operating Conditions (VCC = 1.8, 2.5, 3.0, 3.3 Typical)					
VOH[1]	Output high voltage, all standard output and I/O pins, relative to applicable VCC (VCC_IO, VCC_MEM, VCC_BB, VCC_LCD, VCC_USB, or VCC_USIM)	VCC - 0.3	VCC	V	IOH = -4 mA[2], -3 mA[3]
VOL[1]	Output low voltage, all standard output and I/O pins, relative to applicable VSS (VSS_IO, VSS_MEM, or VSS_BB)	VSS	VSS + 0.3	V	IOH = 4 mA[2], 3 mA[3]

NOTES:
1. Programmable drive strengths set to 0x5 for memory and LCD programmable signals.
2. The current for the high-strength pins are MA<25:0>, MD<31:0>, nOE, nWE, nSDRAS, nSDCAS, DQM<3:0>, nSDCS<3:0>, SDCKE<1>, SDCLK<3:0>, RDnWR, nCS<5:0>, and nPWE.
3. The current for all other output and I/O pins are low strength.

5.5 Oscillator Electrical Specifications

The PXA270 processor contains two oscillators: a 32.768-kHz oscillator and a 13.000-MHz oscillator. Each oscillator requires a specific crystal.

5.5.1 32.768-kHz Oscillator Specifications

The 32.768-kHz oscillator is connected between the TXTAL_IN (amplifier input) and TXTAL_OUT (amplified output). Table 17 and Table 18 list the appropriate 32.768-kHz specifications.

To drive the 32.768-kHz crystal pins from an external source:

1. Drive the TXTAL_IN pin with a digital signal that has low and high levels as listed in Table 18. Do not exceed VCC_PLL or go below VSS_PLL by more than 100 mV. The minimum slew rate is 1 volt per 1 µs. The maximum current drawn from the external clock source when the clock is at its maximum positive voltage is typically 1 mA.
2. Float the TXTAL_OUT pin or drive it in complement to the TXTAL_IN pin, with the same voltage level and slew rate.

Warning

The TXTAL_IN and TXTAL_OUT pins must not be driven from an external source if the PXA270 processor sleep / deep sleep DC-DC converter is enabled.

Table 17: Typical 32.768-kHz Crystal Requirements (Sheet 1 of 2)

Parameter	Minimum	Typical	Maximum	Units
Frequency range	—	32.768	—	kHz
Frequency tolerance	–30	—	+30	ppm
Frequency stability, parabolic coefficient	—	—	–0.04	ppm/(Δ°C)[2]

Table 17: Typical 32.768-kHz Crystal Requirements (Sheet 2 of 2)

Parameter	Minimum	Typical	Maximum	Units
Drive level	—	—	1.0	uW
Load capacitance (C_L)	6	7.5	12.5	pf
Shunt capacitance (C_O)	—	0.9	—	pf
Motional capacitance (C_l)	—	2.1	—	fF
Equivalent series resistance (R_S)	—	18	65	k Ω
Insulation resistance at 100 V_{DC}	100	—	—	M Ω
Aging, at operating temperature per year	—	—	±3.0	ppm

Table 18: Typical External 32.768-kHz Oscillator Requirements

Symbol	Description	Min	Typical	Max	Units
Amplifier Specifications					
VIH_X	Input high voltage, TXTAL_IN	0.99	1.10	1.21	V
VIL_X	Input low voltage, TXTAL_IN	–0.10	0.00	0.10	V
IIN_XT	Input leakage, TXTAL_IN	—	—	1	µA
CIN_XT	Input capacitance, TXTAL_IN/TXTAL_OUT	—	18	25	pf
tS_XT	Stabilization time	—	—	10	s
Board Specifications					
RP_XT	Parasitic resistance, TXTAL_IN/TXTAL_OUT to any node	20	—	—	MΩ
CP_XT	Parasitic capacitance, TXTAL_IN/TXTAL_OUT, total	—	—	5	pf
COP_XT	Parasitic shunt capacitance, TXTAL_IN to TXTAL_OUT	—	—	0.4	pf

5.5.2 13.000-MHz Oscillator Specifications

The 13.000-MHz oscillator is connected between the PXTAL_IN (amplifier input) and PXTAL_OUT (amplified output). Table 19 and Table 20 list the 13.000-MHz specifications.

To drive the 13.000-MHz crystal pins from an external source:

1. Drive the PXTAL_IN pin with a digital signal with low and high levels as listed in Table 20. Do not exceed VCC_PLL or go below VSS_PLL by more than 100 mV. The minimum slew rate is 1 volt / 1 ns. The maximum current drawn from the external clock source when the clock is at its maximum positive voltage typically is 1 mA.
2. Float the PXTAL_OUT pin or drive it in complement to the PXTAL_IN pin, with the same voltage level, slew rate, and input current restrictions.

Warning

The PXTAL_IN and PXTAL_OUT pins must not be driven from an external source if the PXA270 processor sleep / deep sleep DC-DC converter is enabled.

Table 19: Typical 13.000-MHz Crystal Requirements

Parameter	Minimum	Typical	Maximum	Units
Frequency range	12.997	13.000	13.002	MHz
Frequency tolerance at 25°C	–50	—	+50	ppm
Oscillation mode	—	Fnd	—	—
Maximum change over temperature range	–50	—	+50	ppm
Drive level	—	10	100	uW

Table 19: Typical 13.000-MHz Crystal Requirements (continued)

Parameter	Minimum	Typical	Maximum	Units
Load capacitance (C_L)	—	10	—	pf
Maximum series resistance (R_S)	—	50	—	Ω
Aging per year, at operating temperature	—	—	±5.0	ppm

Table 20: Typical External 13.000-MHz Oscillator Requirements

Symbol	Description	Min	Typical	Max	Units
Amplifier Specifications					
VIH_X	Input high voltage, PXTAL_IN	0.99	1.10	1.21	V
VIL_X	Input low voltage, PXTAL_IN	–0.10	0.00	0.10	V
IIN_XP	Input leakage, PXTAL_IN	—	—	10	µA
CIN_XP	Input capacitance, PXTAL_IN/PXTAL_OUT	—	40	50	pf
tS_XP	Stabilization time	—	—	67.8	ms
Board Specifications					
RP_XP	Parasitic resistance, PXTAL_IN/PXTAL_OUT to any node	20	—	—	MΩ
CP_XP	Parasitic capacitance, PXTAL_IN/PXTAL_OUT, total	—	—	5	pf
COP_XP	Parasitic shunt capacitance, PXTAL_IN to PXTAL_OUT	—	—	0.4	pf

5.6 CLK_PIO and CLK_TOUT Specifications

CLK_PIO can be used to drive a buffered version of the PXTAL_IN oscillator input or can be used as a clock input alternative to PXTAL_IN. Refer to Table 21 for CLK_PIO specifications.

A buffered and inverted version of the TXTAL_IN oscillator output is driven out on CLK_TOUT. Refer to Table 22 for CLK_TOUT specifications.

Note

CLK_TOUT and CLK_PIO are only available when software sets the OSCC[PIO_EN] and OSCC[TOUT_EN] bits.

Table 21: CLK_PIO Specifications

Parameter	Specifications
Frequency	13 MHz
Frequency Accuracy (derived from 13 MHz crystal)	+/-200ppm
Symmetry/Duty Cycle variation	30/70 to 70/30% at VCC

Table 21: CLK_PIO Specifications (continued)

Parameter	Specifications
Jitter	+/-20pS max
Load capacitance (C_L)	50pf max
Rise and Fall time (Tr & Tf)	15nS max with 50pF load

Table 22: CLK_TOUT Specifications

Parameter	Specifications
Frequency	32KHz
Frequency Accuracy (derived from 32 kHz crystal)	+/-200ppm
Symmetry/Duty Cycle variation	30/70 to 70/30% at VCC
Jitter	+/-20pS max
Load capacitance (C_L)	50pf max
Rise and Fall time (Tr & Tf)	15nS max with 50pF load

5.7 48 MHz Output Specifications

Software may configure GPIO<11> or GPIO<12> alternate functions to enable the 48-MHz clock output. The 48-MHz output clock is a divided-down output generated from the 312-MHz peripheral PLL. Refer to Table 23 for the 48-MHz output specifications. Refer to Section 3 of this document for GPIO alternate functions in the pin usage table.

Table 23: 48 MHz Output Specifications

Parameter	Specifications
Frequency (derived from 13 MHz crystal)	48 MHz
Frequency Accuracy (derived from 13 MHz crystal)	+/-200ppm (maximum)
Symmetry/Duty Cycle variation	30/70 to 70/30% at VCC
Jitter	+/-20pS max
Load capacitance (C_L)	50pf max
Rise and Fall time (Tr & Tf)	15nS max with 50pF load

6 AC Timing Specifications

A pin's alternating-current (AC) characteristics include input and output capacitance. These factors determine the loading for external drivers and other load analyses. The AC characteristics also include a derating factor, which indicates how much the AC timings might vary with different loads.

Note

The timing diagrams in this chapter show bursts that start at 0 and proceed to 3 or 7. However, the least significant address (0) is not always received first during a burst transfer, because the Marvell® PXA270 processor requests the critical word first during burst accesses.

Table 24 shows the AC operating conditions for the high- and low-strength input, output, and I/O pins. All AC specification values are valid for the device's entire temperature range.

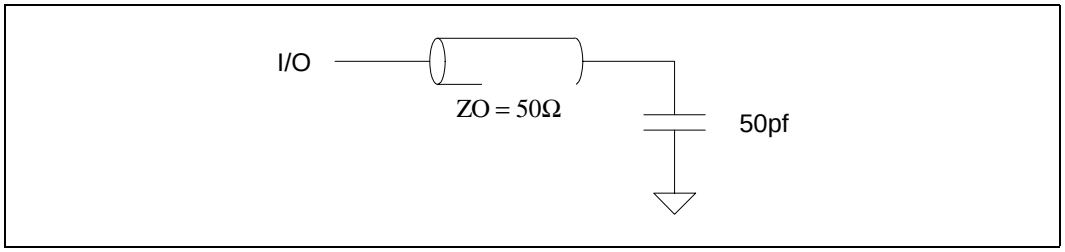
Table 24: Standard Input, Output, and I/O-Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
C_{IN}	Input capacitance, all standard input and I/O pins	—	—	10	pf
C_{OUT_H}	Output capacitance, all standard high-strength output and I/O pins	20	—	50	pf
C_{OUT_L}	Output capacitance, all standard low-strength output and I/O pins	20	—	50	pf

6.1 AC Test Load Specifications

Figure 22 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

Figure 22: AC Test Load



6.2 Reset and Power Manager Timing Specifications

The processor asserts the nRESET_OUT pin in one of several different modes:

- Power-on reset
- Hardware reset
- Watchdog reset
- GPIO reset
- Sleep mode
- Deep-sleep mode

The following sections give the timing and specifications for entry into and exit from these modes.

6.2.1 Power-On Timing Specifications

Power-on reset begins when a power supply is detected on the backup battery pin, VCC_BATT, after the processor has been powered off. A power-on reset is equivalent to a hardware reset, in that all units are reset to the same known state as with a hardware reset. A power-on reset is a complete and total reset that occurs only at initial power on.

The external power-supply system must enable the power supplies for the processor in a specific sequence to ensure proper operation. Figure 23 shows the timing diagram for a power-on reset sequence. Table 25 details the timing.

The sequence for power-on reset is as follows:

1. VCC_BATT is established, then nRESET should be de-asserted to initiate power-on reset.
2. PWR_OUT is asserted. The processor asserts nRESET_OUT.
3. The external power-control subsystem de-asserts nBATT_FAULT to signal that the main battery is connected and not discharged.
4. The processor asserts the SYS_EN signal to enable the power supplies VCC_IO, VCC_MEM, VCC_BB, VCC_USB, and VCC_LCD. VCC_USIM can be established at this time also but can be independently controlled through its own control signals. VCC_IO must be established first. The other supplies can turn on in any order, but they must all be established within 125 milliseconds of the assertion of SYS_EN.
5. The processor asserts the PWR_EN signal to enable the power supplies VCC_CORE, VCC_SRAM, and VCC_PLL. These supplies can turn on in any order but must all be established within 125 milliseconds of the assertion of PWR_EN.
6. The external power-control subsystem de-asserts nVDD_FAULT to signal that all system power supplies have been properly established.
7. The processor de-asserts nRESET_OUT and enters run mode, executing code from the reset vector.

Note

nVDD_FAULT is sampled only when the SYS_DEL and PWR_DEL timers have expired. Refer to the *Marvell® PXA27x Processor Family Developer's Manual*, "Initial Power On" and "Deep-Sleep Exit States" for a state diagram.

Figure 23: Power On Reset Timing

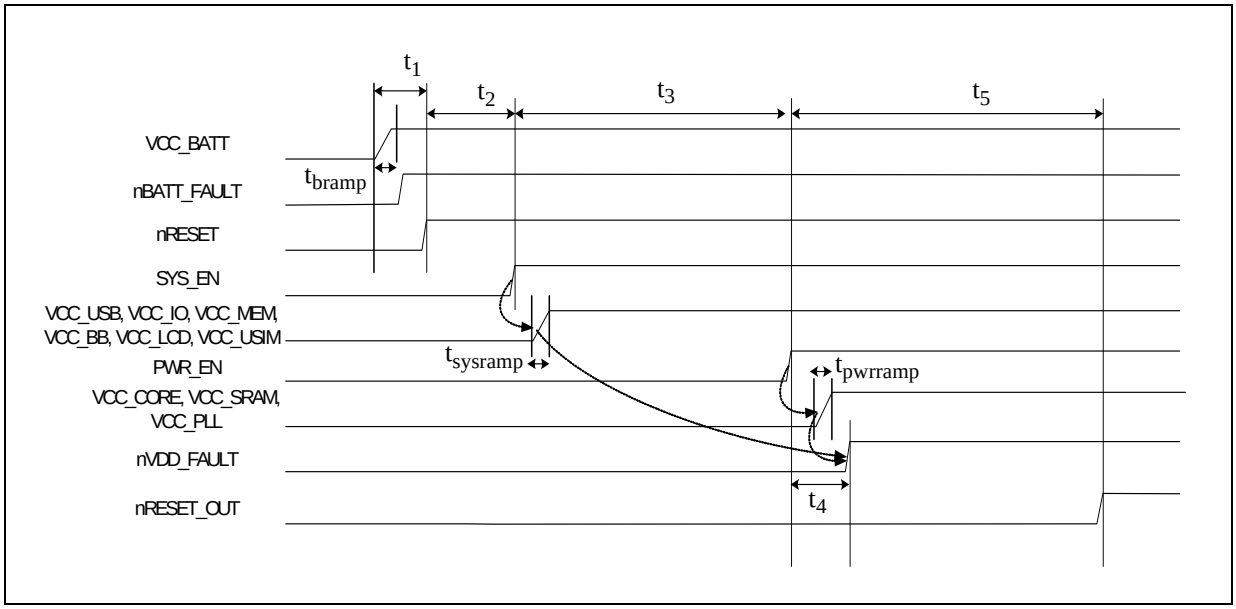


Table 25: Power-On Timing Specifications(OSCC[CRI] = 0)

Symbol	Description	Min	Typical	Max	Units
t_1	Delay from VCC_BATT assertion to nRESET de-assertion	10	—	—	ms
t_2	Delay from nRESET de-assertion to SYS_EN assertion	—	10[1]	—	ms
t_3	Delay from SYS_EN assertion to PWR_EN assertion	—	125	—	ms
t_4	Power supply stabilization time (time to the de-assertion of nVDD_FAULT after the assertion of PWR_EN)	—	—	120	ms
t_5	Delay from the assertion of PWR_EN to the de-assertion of nRESET_OUT	—	125	—	ms
t_{bramp}	VCC_BATT power-on Ramp Rate	—	10	12	mV/µS
$t_{sysramp}$	Power-on Ramp Rate for all external high -voltage power domains	—	10	12	mV/µS
$t_{pwrramp}$	Power-on Ramp Rate for all external low -voltage power domains (including dynamic voltage changes on VCC_CORE)	—	10	12	mV/µS

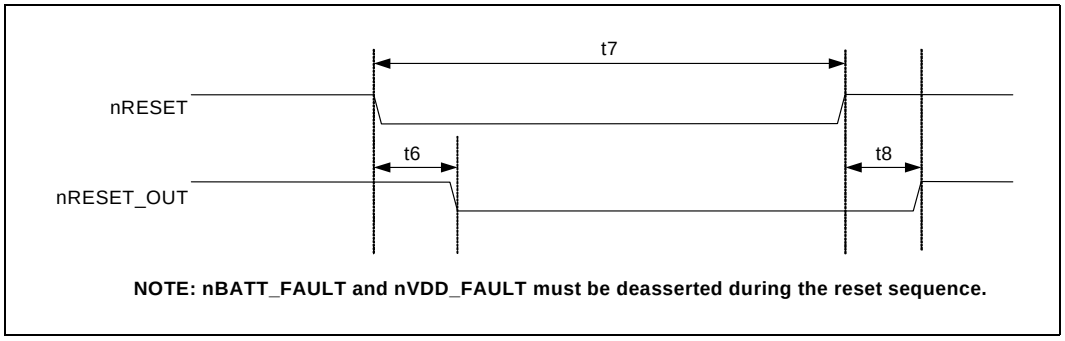
NOTES:
1. If the OSCC[CRI] =1 then the delay from nRESET de-assertion to SYS_EN assertion is 3000mS

NOTE: This long delay is attributed to the fact that when the CRI bit is read as 1, (which indicates that the CLK_REQ pin was floated during a hardware or power-on reset) the processor oscillator is supplied externally, which then forces the system to wait for the 32 kHz oscillator and the 13 MHz oscillator to stabilize.

6.2.2 Hardware Reset Timing

The timing sequences shown in Figure 24 for hardware reset and the specifications in Table 26 and Table 27 assume stable power supplies at the assertion of nRESET. Follow the timings indicated in Section 6.2.1 if the power supplies are unstable.

Figure 24: Hardware Reset Timing



NOTE: nBATT_FAULT and nVDD_FAULT must be deasserted during the reset sequence.

Table 26: Hardware Reset Timing Specifications (OSCC[CRI] = 0)

Symbol	Description	Min	Typical	Max	Units
t_6	Delay between nRESET asserted and nRESET_OUT asserted	—	< 100 ns	10	ms
t_7	Assertion time of nRESET	6	—	—	ms
t_8	Delay between nRESET de-asserted and nRESET_OUT de-asserted	256	—	265	ms

Table 27: Hardware Reset Timing Specifications (OSCC[CRI] = 1)

Symbol	Description	Min	Typical	Max	Units
t_6	Delay between nRESET asserted and nRESET_OUT asserted	—	< 100 ns	10	ms
t_7	Assertion time of nRESET	6	—	—	ms
t_8	Delay between nRESET de-asserted and nRESET_OUT de-asserted	2256	—	3265	ms

6.2.3 Watchdog Reset Timing

Watchdog reset is generated internally and therefore has no external pin dependencies. The SYS_EN and PWR_EN power signals de-assert and the nRESET_OUT pin asserts during watchdog reset. The timing is similar to that for power-on reset — see Figure 23 for details.

6.2.4 GPIO Reset Timing

GPIO reset is generated externally, and the reset GPIO source is reconfigured as a standard GPIO as soon as the reset propagates internally. The clocks module is not reset by GPIO reset, so the reset timing varies based on the selected clock frequency. Since GPIO assertions are ignored during a frequency change sequence, if GPIO<1> is asserted during a frequency change sequence, it must remain asserted low for 240 ns after the frequency change completes for the GPIO reset to be

recognized. Figure 25 shows the timing of GPIO reset, and Table 28 shows the GPIO reset timing specifications.

Note

When bit GPROD is set in the Power Manager General Configuration register, nRESET_OUT is not asserted during GPIO reset. For register details, see the “Clocks and Power Manager” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual*.

Figure 25: GPIO Reset Timing

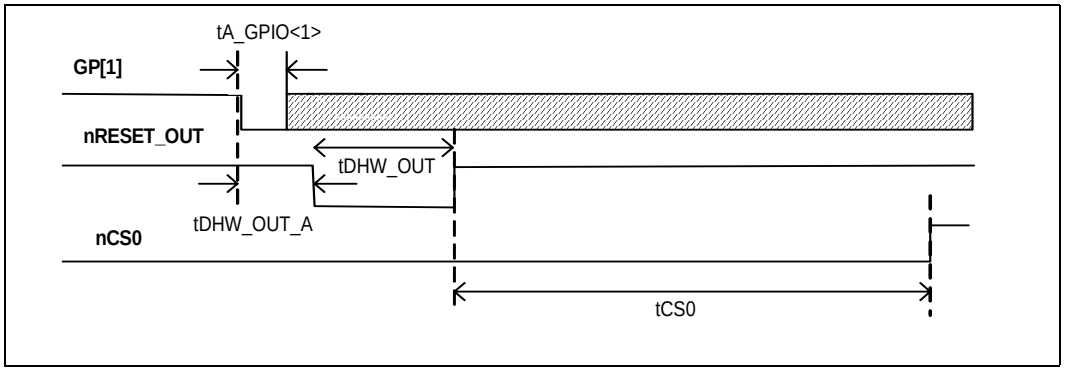


Table 28: GPIO Reset Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
tA_GPIO<1>	Minimum assert time of GPIO<1> in 13.000-MHz input clock cycles	4	—	—	cycles	1, 2, 4
tDHW_OUT_A	Delay between GPIO<1> asserted and nRESET_OUT asserted in 13.000-MHz input clock cycles	6	—	8	cycles	4
tDHW_OUT	Delay between nRESET_OUT asserted and nRESET_OUT de-asserted, run or turbo mode	230	—	—	nsec	

Symbol	Description	Min	Typical	Max	Units	Notes
tDHW_OUT_F	Delay between nRESET_OUT asserted and nRESET_OUT de-asserted, during frequency change sequence	5	—	380	µs	3
tCS0	Delay between nRESET_OUT de-assertion and nCS0 assertion	1000	—	—	ns	5

NOTES:
1. GPIO<1> is not recognized as a reset source again until configured to do so in software. Software must check the state of GPIO<1> before configuring as a reset to ensure that no spurious reset is generated. For details, see the “Clocks and Power Manager” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual*.
2. If GPIO<1> reset is asserted during a frequency change sequence, the minimum assert time of GPIO<1> needs to be 512*N processor clock cycles plus up to 4 cycles of the 13.000-MHz input clock cycles for the reset to be recognized.
3. Time during the frequency-change sequence depends on the state of the PLL lock detector at the assertion of GPIO reset. The lock detector has a maximum time of 350 µs plus synchronization.
4. In standby, sleep, and deep-sleep modes, this time is in addition to the wake-up time from the low-power mode.
5. The tCS0 specification is also applicable to Power-On reset, Hardware reset, Watchdog reset and Deep-Sleep/Sleep mode exit.

6.2.5 Sleep Mode Timing

Sleep mode is internally asserted, and it asserts the nRESET_OUT and PWR_EN signals. Figure 26 and Table 29 show the required timing parameters for sleep mode.

Note

Note

When bit SL_ROD is set in the Power Manager Sleep Configuration register, nRESET_OUT, is not asserted during sleep mode. See the “Clocks and Power Manager” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register details.

Figure 26: Sleep Mode Timing

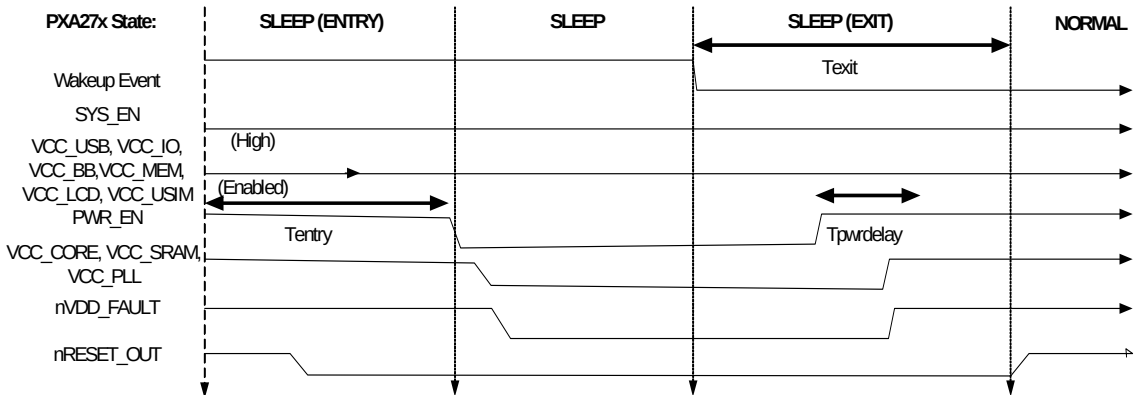


Table 29: Sleep-Mode Timing Specifications

Symbol	Description	Min	Typical	Max[3]	Units
t_{entry}[5]	Delay between MCR sleep command issue to de-assertion of PWR_EN	0.56	—	2.5[1]	msec
t_{exit}	Delay between wakeup event and run mode	0.50	—	136.65[2,4]	msec
$t_{pwrdelay}$	Delay between assertion of PWR_EN to PLL enable[2]	0	—	125	msec

NOTES:
1. -1mS if not using DC2DC and -0.94mS if any internal SRAM banks are not powered
2. 0.15ms less time if exiting from sleep mode to 13M mode
3. Add 0.1ms if the wake up event is external
4. Oscillator start/crystal stable times are programmable (300uS-11mS)

NOTE: 5ms is user programmable using the OSCC[OSD] bit. The remaining 6ms is an internal timer which counts until the oscillator is stable. (Typical stabilization is 500µs. Maximum can be upto 5ms)

5. nRESET_OUT and nVDD_FAULT are programmable during sleep mode

6.2.6 Deep-Sleep Mode Timing

Deep-sleep mode is internally asserted, and it asserts the nRESET_OUT and PWR_EN signals. Figure 27 and Table 30 show the required timing parameters for sleep mode. The timing specifications listed are for software-invoked (not battery or VDD fault) deep-sleep entry, unless specified.

Figure 27: Deep-Sleep-Mode Timing

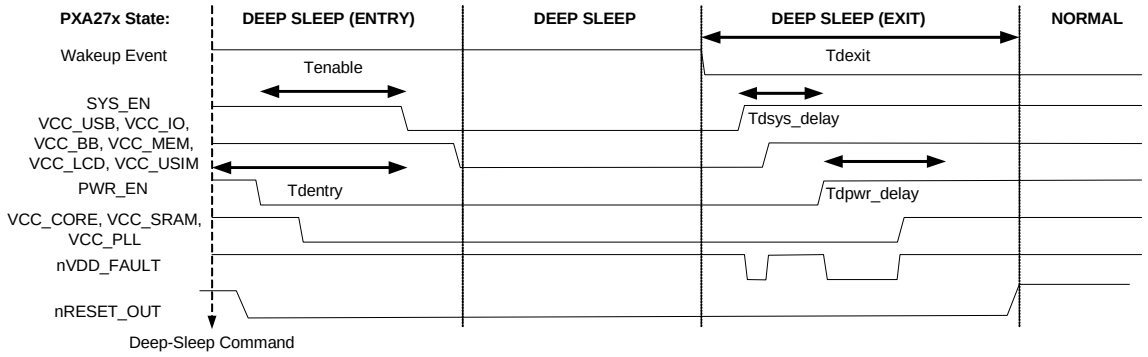


Table 30: Deep-Sleep Mode Timing Specifications (Sheet 1 of 2)

Symbol	Description	Min	Typical	Max[3]	Units
t_{dentry}[5]	Delay between deep-sleep command issue to de-assertion of SYS_EN	0.66	—	1.66[1]	msec
t_{enable}	Delay between de-assertion of PWR_EN and SYS_EN	—	30	—	usec
t_{dexit}	Delay between wakeup event and run mode	0.60	—	261.75[2,4]	msec

Table 30: Deep-Sleep Mode Timing Specifications (Sheet 2 of 2)

Symbol	Description	Min	Typical	Max[3]	Units
$t_{dsysdelay}$	Delay between assertion of SYS_EN to PWR_EN[2]	0	—	125	msec
$t_{dpwrdelay}$	Delay between assertion of PWR_EN to PLL enable[2]	0	—	125	msec
NOTE: Timing specifications for nBATT_FAULT and/or nVDD_FAULT asserted deep-sleep mode entry are below:					
Fault assert	Delay between nBATT_FAULT or nVDD_FAULT assertion (during all modes of operation including sleep mode) and deep-sleep mode entry[6](The de-assertion of SYS_EN defines when the processor is in deep-sleep mode)	0.33	—	1.56	msec

NOTES:
1. -1ms if not using DC2DC
2. 0.15ms less time if exiting from deep-sleep mode to 13M mode
3. Add 0.1ms if the wake up event is external
4. Oscillator start/crystal stable times are programmable (300uS-11mS)

NOTE: 6ms is user programmable using the OSCC[OSD] bit. The remaining 5ms is an internal timer which counts until the oscillator is stable. (Typical stabilization is 500µs. Maximum can be upto 5ms)

5. nRESET_OUT and nVDD_FAULT are programmable during sleep mode
6. Assumes PMCR[BIDAE or VIDAE] bits are set to zero (default state) - The PMCR[BIDAE or VIDAE] bits are only read by the processor if nBATT_FAULT or nVDD_FAULT signals are asserted

6.2.7 GPIO states in Deep-Sleep mode

If the external high voltage power domains (VCC_IO, VCC_MEM, VCC_BB, VCC_LCD, VCC_USB, VCC_USIM) remain powered on during deep-sleep, the PGSR values are driven onto all the GPIO pins (that are configured as outputs) for a finite time period, then the pins default to the reset state (Pu/Pd) as described in Chapter 2 of this manual. This sequence occurs for either software-initiated or fault-initiated deep-sleep entry.

Note

GPIOs<0,1,3,4,9,10> never float. They are powered from VCC_BATT so when the system and the core power domains are removed (controlled by SYS_EN and PWR_EN), the Pu/Pd resistors remain enabled due to VCC_BATT remaining on.

The delay between the initiation of deep-sleep mode and enabling the GPIO Pu/Pd states is system dependant because the processor is performing an unpredictable workload and requires an unknown amount of time to complete current processes. Refer to the deep-sleep mode, “Clocks and Power” section of the *Marvell® PXA27x Processor Family Developers Manual* for a description on deep-sleep mode entry sequence.

Table 31 shows the time period that the GPIO pullup/pulldowns are enabled. Listed below are the regulators and converter naming conventions:

L1 = Sleep/Deep-Sleep Linear Regulator

L2 = High-Current Linear Regulator

DC2DC = Sleep/Deep-Sleep DC-DC Converter

Table 31: GPIO Pu/Pd Timing Specifications for Deep-Sleep Mode

Description	L2	L1	DC2DC	Units
Duration of the GPIO Pu/Pd states being enabled and the de-assertion of PWR_EN	0.1	0.13	1.13	msec

Note

If the *external high voltage power domains* (VCC_IO, VCC_MEM, VCC_BB, VCC_LCD, VCC_USB, VCC_USIM) are powered off during deep-sleep mode, the GPIOs behave the same as described above; however, they float after the supplies are removed.

6.2.8 Standby-Mode Timing

Table 32: Standby-Mode Timing Specifications

Symbol	Description	Min	Typical	Max	Units
—	13M mode to standby mode entry	—	0.34	—	msec
—	Standby mode exit to 13M mode[1]	0.28	—	11.28[2]	msec
—	Run mode to standby mode entry	—	0.34	—	msec
—	Standby mode exit to run mode[1]	0.43	—	11.43[2]	msec

NOTES:
1. The 13M oscillator is programmable
2. Add 0.1ms if the wake up event is external

6.2.9 Idle-Mode Timing

Table 33: Idle-Mode Timing Specifications

Symbol	Description	Min	Typical	Max	Units
—	13M mode to deep idle mode entry	—	1	—	µs
—	Deep idle mode exit to 13M mode	—	1	—	µs
—	Run mode to idle run mode entry	—	1	—	µs
—	Idle run mode exit to run mode	—	1	—	µs

6.2.10 Frequency-Change Timing

Table 34: Frequency-Change Timing Specifications

Symbol	Description	Min	Typical	Max	Units
—	Delay between MCR command to frequency change sequence completion	—	150[1]	—	µs
—	Delay to change between turbo, half-turbo and run modes	—	1[2]	—	µs
—	Delay to enter 13M mode from any Run mode [3]	—	1	—	µs
—	Delay to exit 13M mode to any Run mode	—	2[4]	—	µs

NOTES:
1. Any change to the CCCR[2N or L] bits followed by a write to CLFCFG[F] to initiate a frequency change sequence, results in a PLL restart
2. Changing between turbo, half-turbo and run modes does not require a PLL restart
3. Software can only change into 13M mode from any run mode
4. Assuming software uses the PLL early enable feature (CCCR[PLL_EARLY_EN] prior to a frequency change sequence

6.2.11 Voltage-Change Timing

The PWR I^2C uses the regular I^2C protocol. The PWR I^2C is clocked at 40 kHz (160 kHz fast-mode operation is supported). Software controls the time required for initiating the voltage change sequence through completion. The voltage-change timing is a product of the number of commands

issued plus the number of software-programmed delays. Table 35 shows the timing of a 1 byte command issued to the power manager IC.

Set the I^2C programmable output ramp rate with a default/reset ramp rate of 10mV/µs (refer to VCC_CORE ramp rate specification in the *Electrical Section*) to support VCC_CORE dynamic voltage management.

Table 35: Voltage-Change Timing Specification for a 1-Byte Command

Symbol	Description	Min	Typical	Max	Units
—	Delay between voltage change sequence start[1] to command received by PMIC	—	18	—	cycles[2]

NOTES:
1. Write 1 to PWRMODE[VC]
2. 40 kHz cycles

6.3 GPIO Timing Specifications

Table 36 shows the general-purpose I/O (GPIO) AC timing specifications.

Table 36: GPIO Timing Specifications

Symbol	Parameter	Min	Max	Units	Notes
taGPIO[1]	Assertion time required to detect GPIO edge	154	—	ns	run, idle, or sense power modes
taGPIOLP[2]	Assertion time required to detect GPIO low-power edge	62.5	—	µs	standby, sleep, or deep-sleep power modes
tdGPIO[1]	De-assertion time required to detect GPIO edge	154	—	ns	run, idle, or sense power modes
tdGPIOLP[2]	De-assertion time required to detect GPIO low-power edge	62.5	—	µs	standby, sleep, or deep-sleep power modes
tdiGPIO[3]	Time required for a GPIO edge to be detected internally	231	—	ns	run, idle, or sense power modes
tdiGPIOLP[4]	Time required for a GPIO low-power edge to be detected internally	93.75	—	µs	standby, sleep, or deep-sleep power modes

NOTES:
1. Period equal to two 13-MHz cycles
2. Period equal to two 32-kHz cycles
3. Period equal to three 13-MHz cycles
4. Period equal to three 32-kHz cycles

Note 4 describes the complete timing for a standby, sleep, or deep-sleep wake up source to be asserted and detected internally (2 cycles for assertion (note 2) and 1 additional cycle for detection).

6.4 Memory and Expansion-Card Timing Specifications

Interfaces with the following memories must observe the AC timing requirements given in the following subsections:

- Section 6.4.1, “Internal SRAM Read/Write Timing Specifications”
- Section 6.4.2, “SDRAM Parameters and Timing Diagrams”
- Section 6.4.3, “ROM Parameters and Timing Diagrams”

- Section 6.4.4, “Flash Memory Parameters and Timing Diagrams”
- Section 6.4.5, “SRAM Parameters and Timing Diagrams”
- Section 6.4.6, “Variable-Latency I/O Parameters and Timing Diagrams”
- Section 6.4.7, “Expansion-Card Interface Parameters and Timing Diagrams”

Note

The diagrams in this section use the following conventions:

- Input signals to the processor are represented using dashed waveforms.
- Outputs and bidirectional signals are represented using solid waveforms.
- Fixed parameters are shown using double arrows in grey (black and white print) or green (color print).
- Programmable parameters are shown using bold single arrows.
- The processor register that is used to change a specific timing is given in the corresponding timing table.

6.4.1 Internal SRAM Read/Write Timing Specifications

Table 37: SRAM Read/Write AC Specification

Symbols	Parameters	MIN	TYP	MAX	Units
tsramRD	4-beat read transfer	—	9	—	system bus clocks
tsramWR	4-beat write transfer	—	7	—	system bus clocks

6.4.2 SDRAM Parameters and Timing Diagrams

Table 38 shows the timing parameters used in Figure 28. Also see Section 6.4.3 and Figure 32 for additional SDRAM bus tenure information. See Figure 31 for SDRAM fly-by bus tenures.

Table 38: SDRAM Interface AC Specifications (Sheet 1 of 3)

Symbols	Parameters	VCC_MEM = 1.8V +20% / –5%[3]			VCC_MEM = 2.5V +/- 10%[4]			VCC_MEM = 3.3V +/- 10%[5]			Units	Notes
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
tsdCLK	SDCLK1, SDCLK2 period	9.6	—	76.9	9.6	—	76.9	9.6	—	76.9	ns	1, 2
tsdCMD	nSDCAS, nSDRAS, nWE, nSDCS assert time	1	—	1	1	—	1	1	—	1	SDCLK	—
tsdCAS	nSDCAS to nSDCAS assert time	2	—	—	2	—	—	2	—	—	SDCLK	—
tsdRCD	nSDRAS to nSDCAS assert time	1	MDCNFG[DTCx]	3	1	MDCNFG[DTCx]	3	1	MDCNFG[DTCx]	3	SDCLK	6

Table 38: SDRAM Interface AC Specifications (Sheet 2 of 3)

Symbols	Parameters	VCC_MEM = 1.8V +20% / –5%[3]			VCC_MEM = 2.5V +/- 10%[4]			VCC_MEM = 3.3V +/- 10%[5]			Units	Notes
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
tsdRP	nSDRAS Pre charge	2	MDCNFG[DTCx]	3	2	MDCNFG[DTCx]	3	2	MDCNFG[DTCx]	3	SDCLK	6
tsdCL	CAS Latency	2	MDCNFG[DTCx]	3	2	MDCNFG[DTCx]	3	2	MDCNFG[DTCx]	3	SDCLK	6
tsdRAS	nSDRAS active time	3	MDCNFG[DTCx]	7	3	MDCNFG[DTCx]	7	3	MDCNFG[DTCx]	7	SDCLK	6
tsdRC	nSDRAS cycle time	4	MDCNFG[DTCx]	11	4	MDCNFG[DTCx]	11	4	MDCNFG[DTCx]	11	SDCLK	6
tsdWR	write recovery time (time from last data in the PRECHARGE)	2	—	2	2	—	2	2	—	2	SDCLK	—
tsdSDOS	MA<24:10>, MD<31:0>, DQM<3:0>, nSDCS<3:0>, nSDRAS, nSDCAS, nWE, nOE, SDCKE1, RDnWR output setup time to SDCLK<2:1> rise	2.5	—	—	2.5	—		2.5	—	—	ns	—
tsdSDOH	MA<24:10>, MD<31:0>, DQM<3:0>, nSDCS<3:0>, nSDRAS, nSDCAS, nWE, nOE, SDCKE1, RDnWR output hold time from SDCLK<2:1> rise	1.5	—	—	1.5	—		1.5	—	—	ns	—
		VCC_CORE = 0.85 V +/– 10%, with 1.71 V<= VCC_MEM <= 3.63 V			VCC_CORE = 1.1 V +/– 10%, with 1.71 V <= VCC_MEM <= 3.63 V			VCC_CORE = 1.3 V +/– 10%, with 1.71 V <= VCC_MEM <= 3.63 V				

Table 38: SDRAM Interface AC Specifications (Sheet 3 of 3)

Symbols	Parameters	VCC_MEM = 1.8V +20% / –5%[3]			VCC_MEM = 2.5V +/- 10%[4]			VCC_MEM = 3.3V +/- 10%[5]			Units	Notes
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
tsdSDIS	MD<31:0> read data input setup time from SDCLK<2:1> rise	3.0	—	—	3.0	—	—	0.5	—	—	ns	—
tsdSDIH	MD<31:0> read data input hold time from SDCLK<2:1> rise	2.0	—	—	2.0	—	—	1.8	—	—	ns	—

NOTES:
1. SDCLK for SDRAM slowest period is accomplished by divide-by-2 of the 26-MHz CLK_MEM. The fastest possible SDCLK is accomplished by configuring CLK_MEM at 104 MHz and not setting MDREFR[KxDB2].
2. SDCLK1 and SDCLK2 frequencies are configured to be CLK_MEM frequency divided by 1 or 2, depending on the bit fields MDREFR[K1DB2] and MDREFR[K2DB2] settings.
3. These numbers are for VCC_MEM = 1.8 V +20% / –5%, VOL = 0.4 V, and VOH = 1.4 V, with each applicable 4-bit field of the system memory buffer strength registers (BSCNTRP and BSCNTRN) set to TBD (msb:lsb) and each applicable SDCLK<2:1> divide-by-2 and divide-by-4 register bits MDREFR[KxDB2] clear.
4. These numbers are for VCC_MEM = 2.5 V +/– 10%, VOL = 0.4 V, and VOH = 2.1 V, with each applicable 4-bit field of the system memory buffer strength registers (BSCNTRP and BSCNTRN) set to 0b1010 (msb:lsb) and each applicable SDCLK<2:1> divide-by-2 and divide-by-4 register bit MDREFR[KxDB2] clear.
5. These numbers are for VCC_MEM = 3.3 V +/– 10%, VOL = 0.4 V, and VOH = 2.4 V, with each applicable 4-bit field of the system memory buffer strength registers (BSCNTRP and BSCNTRN) set to 0b1010 (msb:lsb) and each applicable SDCLK<2:1> divide-by-2 and divide-by-4 register bit MDREFR[KxDB2] clear.
6. Refer to the “Memory Controller” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register configuration.

Figure 28: SDRAM Timing

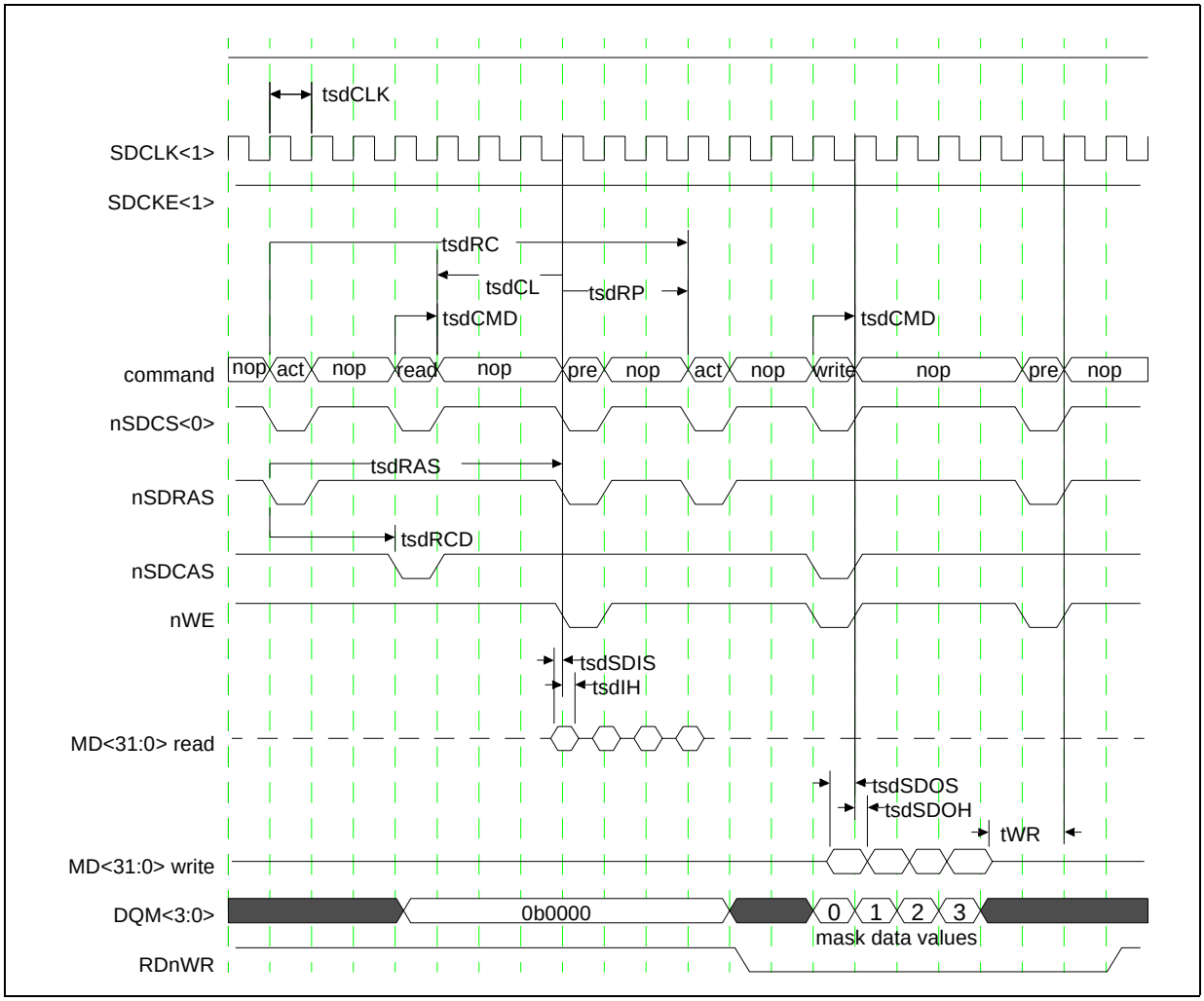
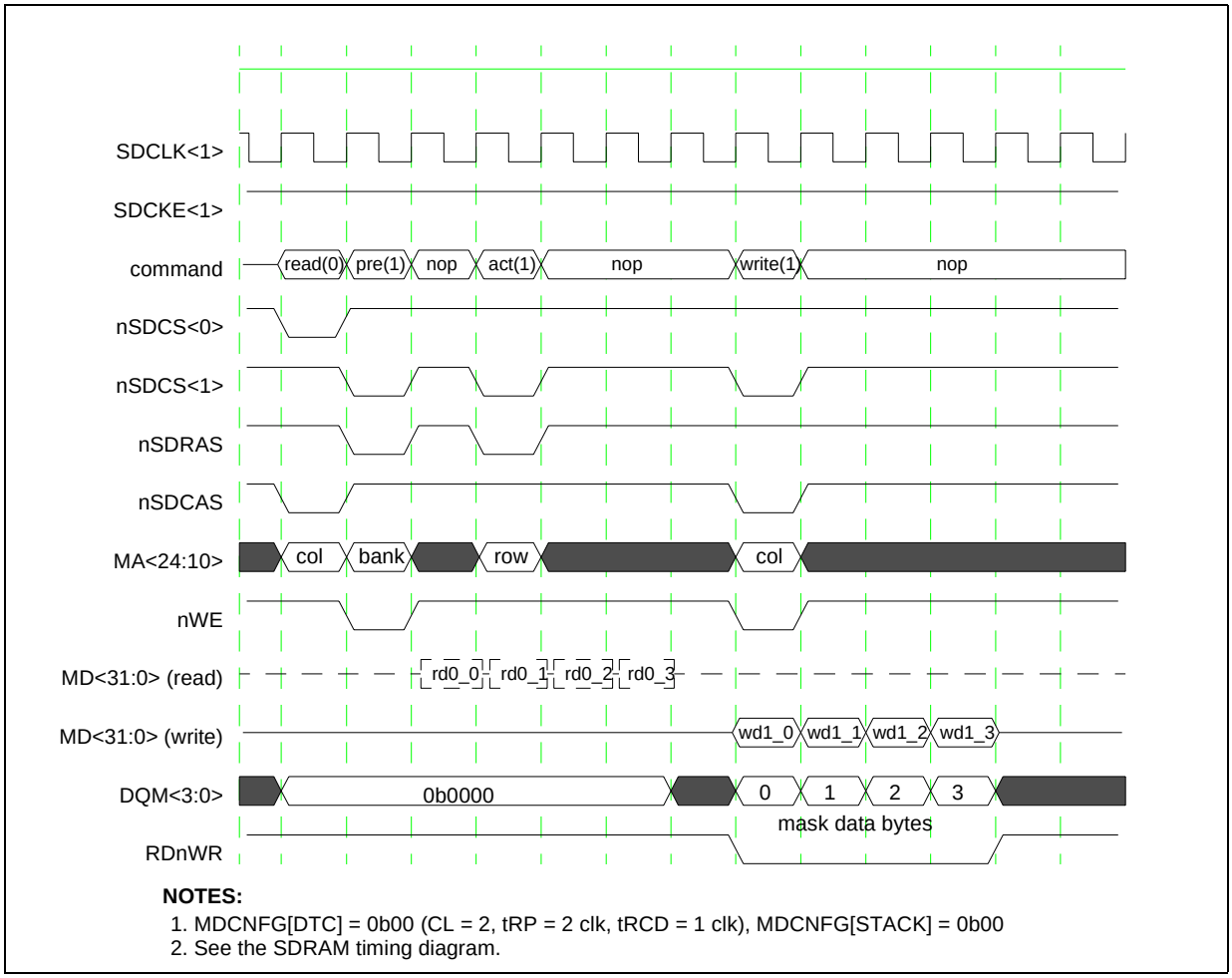


Figure 29: SDRAM 4-Beat Read/4-Beat Write, Different Banks Timing



NOTES:

1. MDCNFG[DTC] = 0b00 (CL = 2, tRP = 2 clk, tRCD = 1 clk), MDCNFG[STACK] = 0b00
2. See the SDRAM timing diagram.

Figure 30: SDRAM 4-Beat Write/4-Beat Write, Same Bank-Same Row Timing

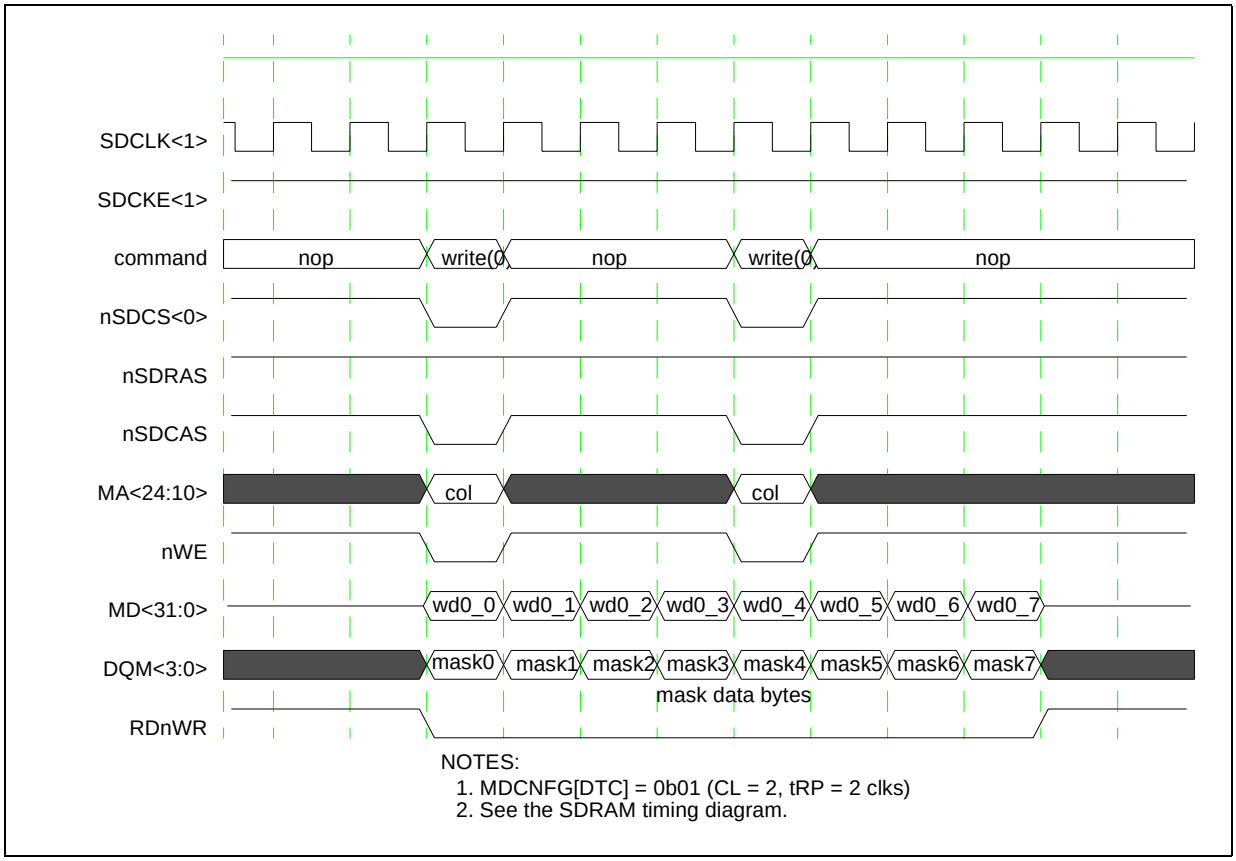
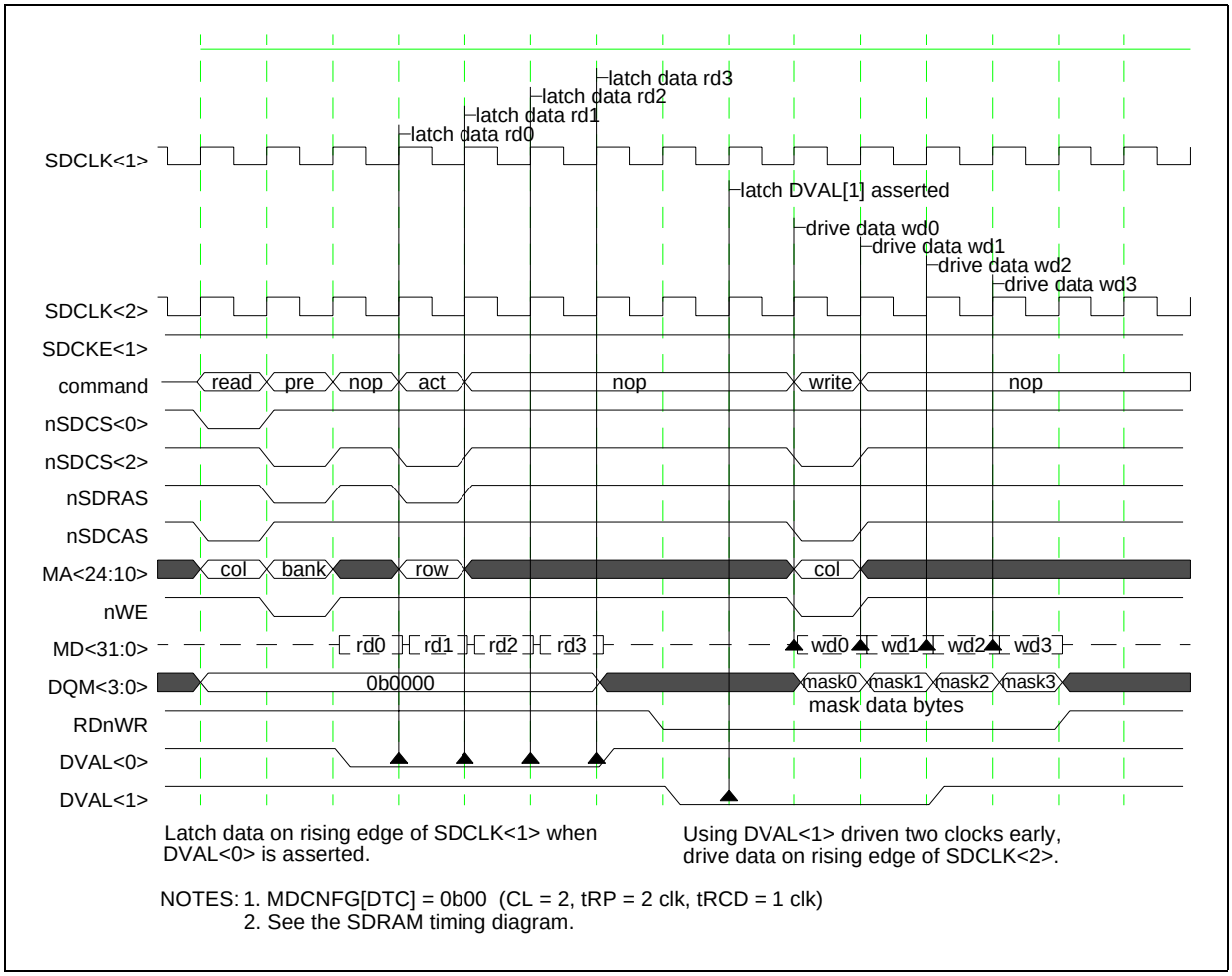


Figure 31: SDRAM Fly-by DMA Timing



6.4.3 ROM Parameters and Timing Diagrams

Table 39 lists the timings for ROM reads. See Figure 32, Figure 33, Figure 34, and Figure 35 for timings diagrams representing burst and non-burst ROM reads.

Note

Table 39 lists programmable register items. See the “Memory Controller” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register configurations for more information on these items.

Table 39: ROM AC Specification

Symbols	Parameters	MIN	TYP	MAX	Units†	Notes
tromAS	Address setup to nCS assert	1	—	1	clk_mem	—
tromCES	nCS setup to nOE asserted	—	—	0	clk_mem	—
tromCEH	nCS hold from nOE de-asserted	—	—	0	clk_mem	—
tromDSOH	MD setup to address valid	1.5	—	—	clk_mem	—
tromDOH	MD hold from address valid	0	—	—	clk_mem	—
tromAVDVF	Address valid to data latched for the first read access	2	MSCx[RDF]+2	32	clk_mem	—
tromAVDVS	Address valid to data latched for subsequent reads of non-burst devices	1	MSCx[RDF]+1	31	clk_mem	—
tflashAVDVS	Address valid to data valid for subsequent reads of burst devices	1	MSCx[RDN]+1	31	clk_mem	—
tromCD	nCS de-asserted after a read of next nCS or nSDCS asserted (minimum)	1	MSCx[RRR]*2+1	15	clk_mem	—

† Numbers shown as integer multiples of the clk_mem period are ideal. Actual numbers vary with pin-to-pin differences in loading and transition direction (rise or fall). For more information, refer to the “Memory Control” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual*.

Figure 32: 32-Bit Non-burst ROM, SRAM, or Flash Read Timing

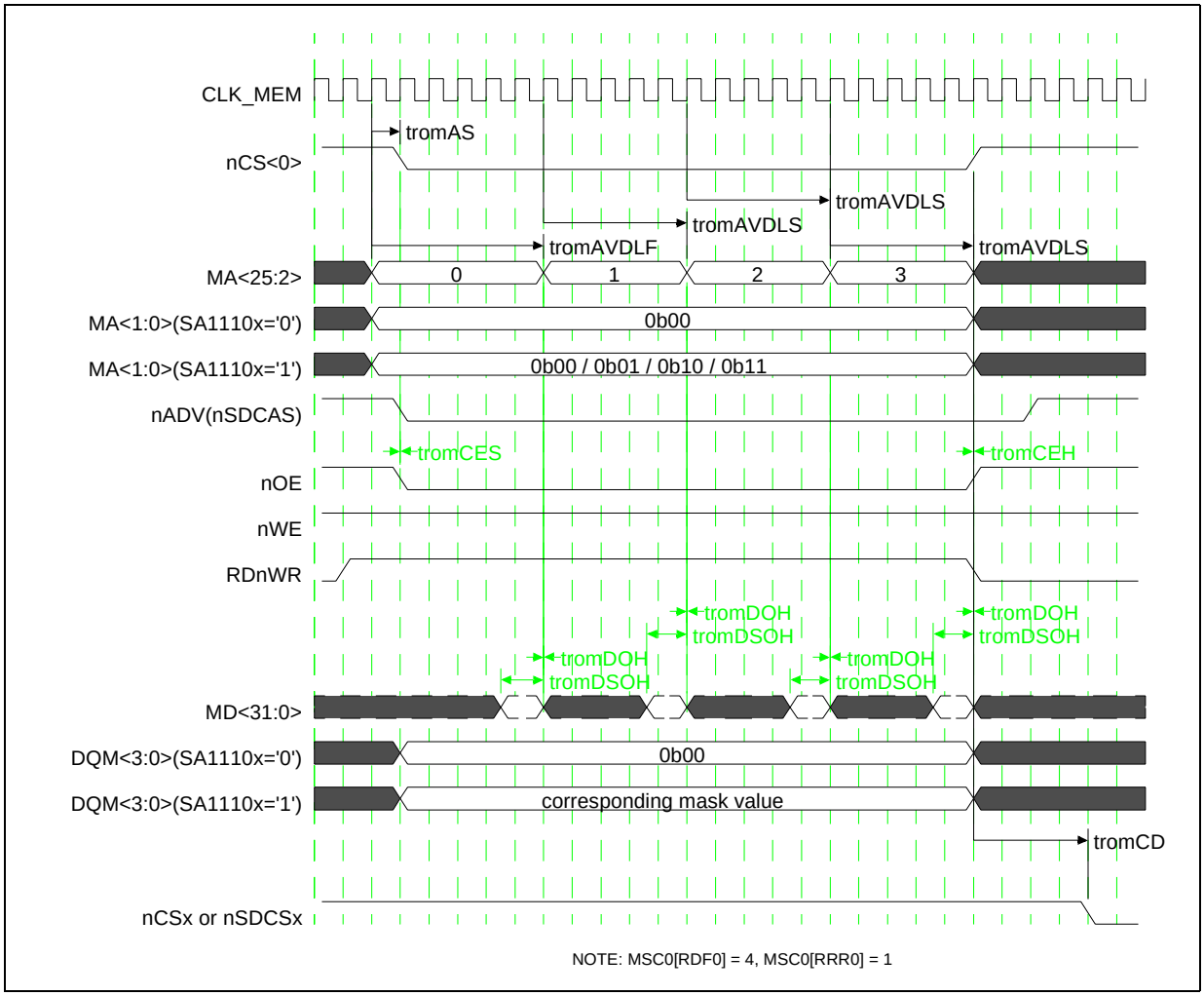


Figure 33: 32-Bit Burst-of-Eight ROM or Flash Read Timing

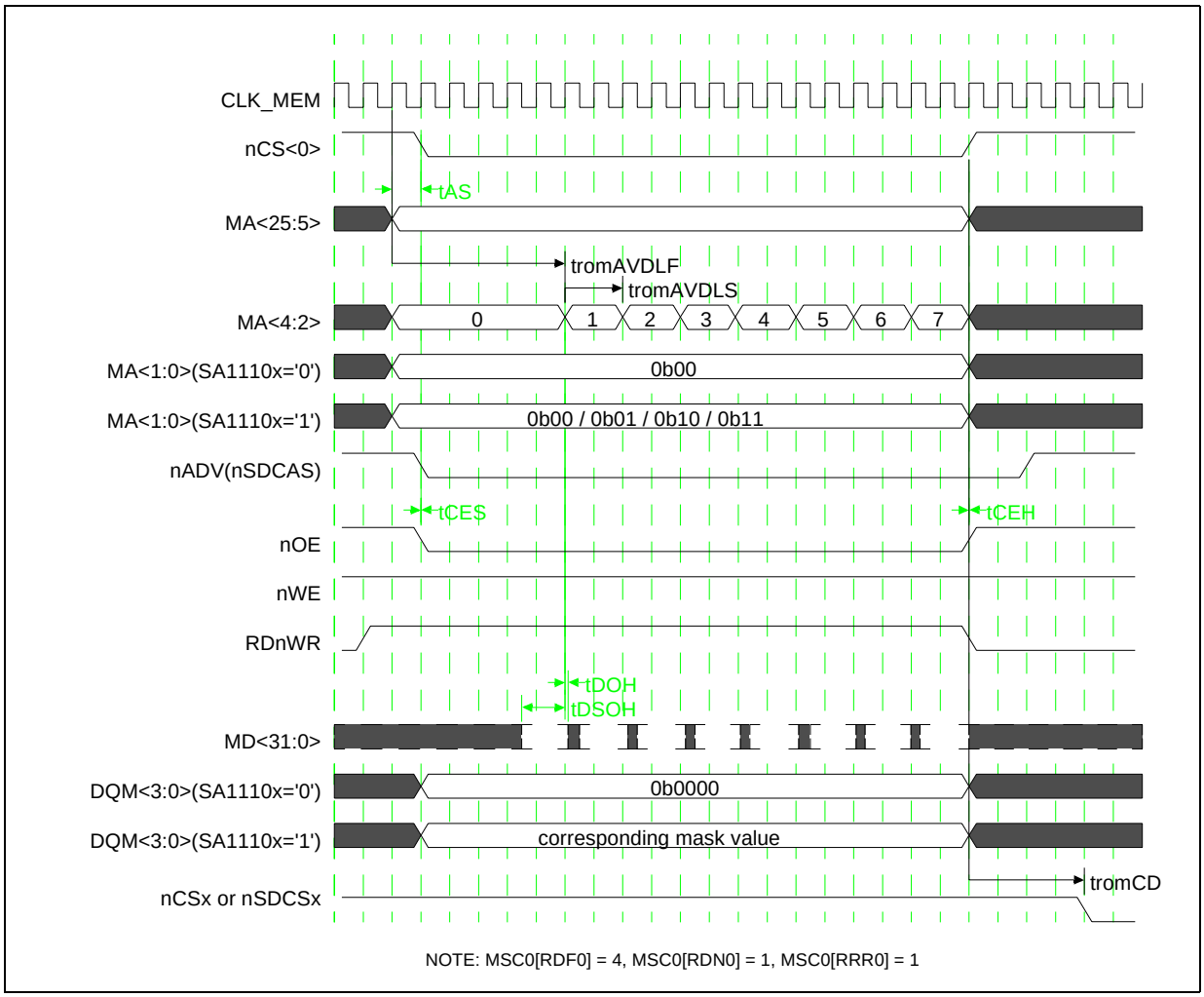


Figure 34: Eight-Beat Burst Read from 16-Bit Burst-of-Four ROM or Flash Timing

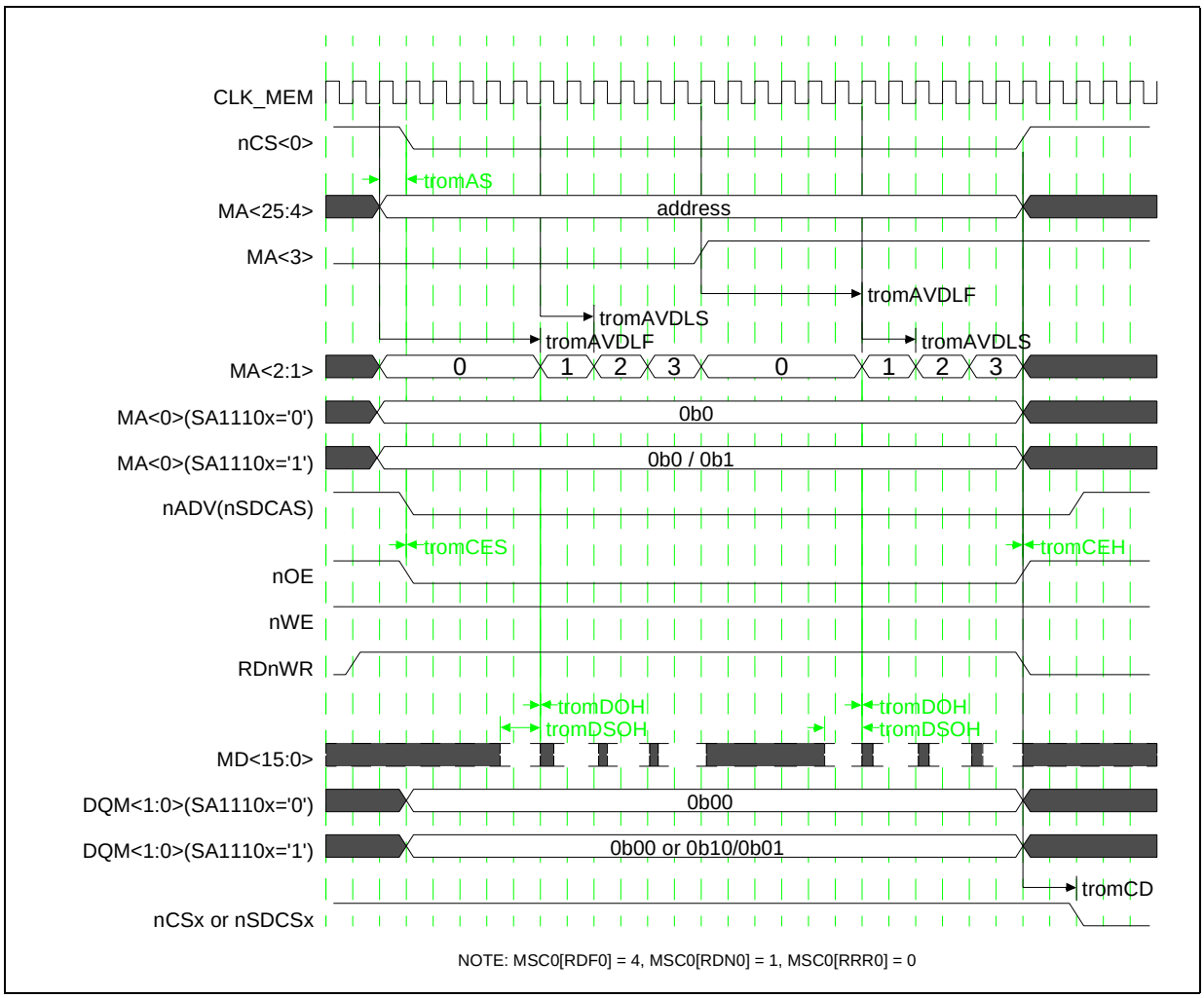
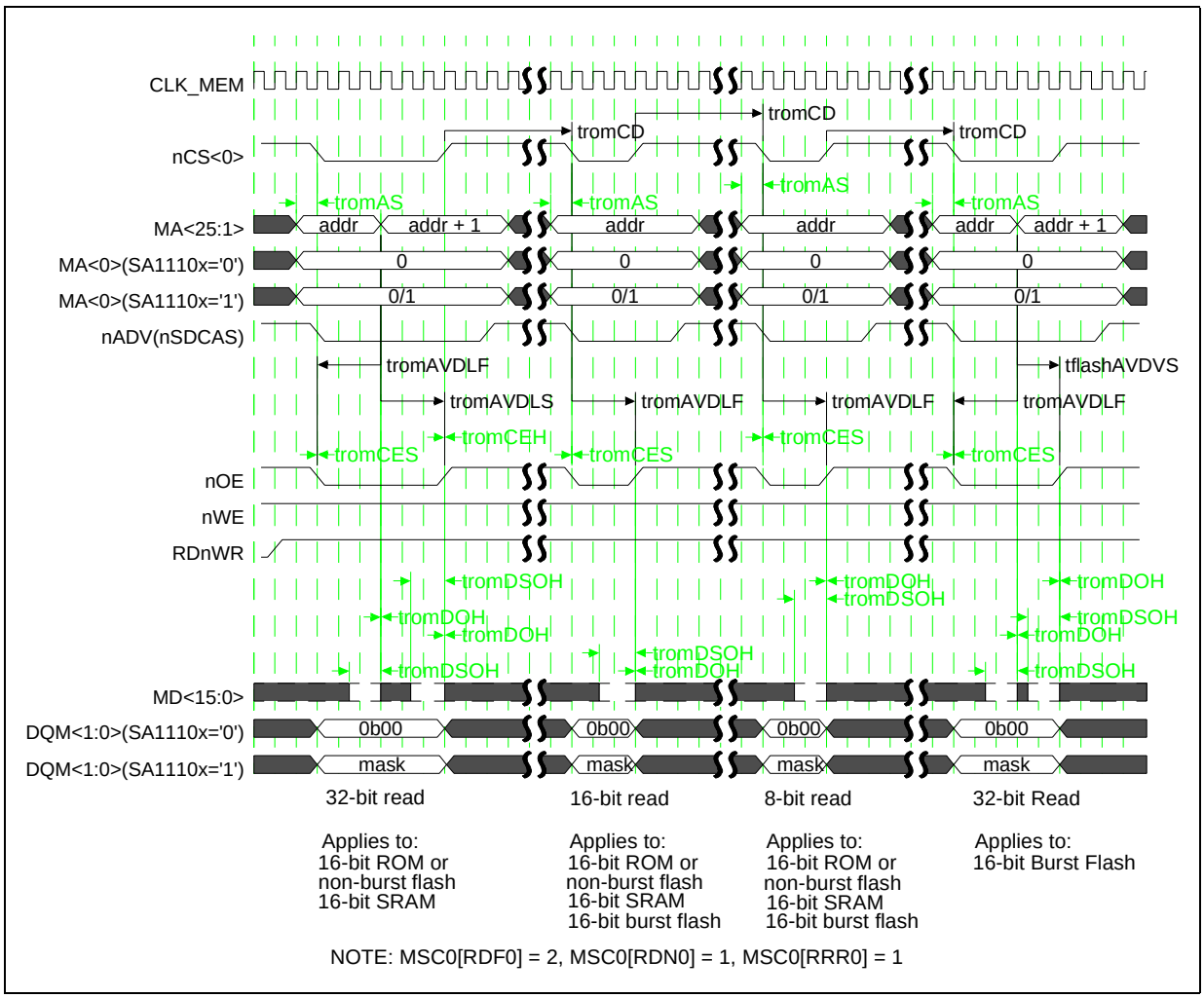


Figure 35: 16-bit ROM/Flash/SRAM Read for 4/2/1 Bytes Timing



6.4.4 Flash Memory Parameters and Timing Diagrams

The following sections describe the read/write parameters and timing diagrams for asynchronous and synchronous flash-memory interfaces with the memory controller.

6.4.4.1 Flash Memory Read Parameters and Timing Diagrams

Section 6.4.4.2 describes asynchronous flash reads. Section 6.4.4.3 describes synchronous flash reads.

6.4.4.2 Asynchronous Flash Read Parameters and Timing Diagrams

The timings listed in Table 39 for ROM reads also apply to asynchronous flash reads. See Figure 32, Figure 33, Figure 34, and Figure 35 for timings diagrams representative of an asynchronous flash read.

6.4.4.3 Synchronous Flash Read Parameters and Timing Diagrams

Table 40 lists the timing parameters used in Figure 36, and, for stacked flash packages, Figure 37.

Table 40: Synchronous Flash Read AC Specifications (Sheet 1 of 2)

Symbols	Parameters	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	Units	Notes
		Divide by 1[2]			Divide by 2[3]			Divide by 4[4]				
tffCLK	SDCLK0 period	9.6	—	38.5	19.2	—	76.9	38.5	—	154	ns	1
tffAS	MA<25:0> setup to nSDCAS (as nADV) asserted	1	—	1	1	—	2	1	—	4	CLK_MEM	—
tffCES	nCS setup to nSDCAS (as nADV) asserted	1	—	1	1	—	2	1	—	4	CLK_MEM	—
tffADV	nSDCAS (as nADV) pulse width	1	—	1	3	—	3	7	—	7	CLK_MEM	—
tffOS	nSDCAS (as nADV) de-assertion to nOE assertion	1	FCC – 1 (for FCC<5) FCC – 2 (for FCC>=5)	13	2	(FCC – 1) * 2 (for FCC<5) (FCC – 2) * 2 (for FCC>=5)	26	7	(FCC * 4) – 7 (for FCC<5) (FCC – 2) * 4 (for FCC>=5)	52	CLK_MEM	5
tffCEH	nOE de-assertion to nCS de-assertion	4	—	4	8	—	8	16	—	16	CLK_MEM	—
tffDS	CLK to data valid	2	FCC	15	2	FCC	15	2	FCC	15	CLK_MEM	5
		VCC_MEM = 1.8V +20% / -5%[6]			VCC_MEM = 2.5V +/- 10%[7]			VCC_MEM = 3.3V +/- 10%[8]				
tffSDOS	MA<25:0>, MD<31:0>, DQM<3:0>, nCS<3:0>, nSDCAS (nADV), nWE, nOE, RDnWR output setup time to SDCLK0 rise	8	—	—	8	—	—	8	—	—	ns	—
tffSDOH	MD<31:0>, DQM<3:0>, nCS<3:0>, nSDCAS (nADV), nWE, nOE, RDnWR output hold time from SDCLK0 rise	4.5	—	—	4.5	—	—	4.5	—	—	ns	—

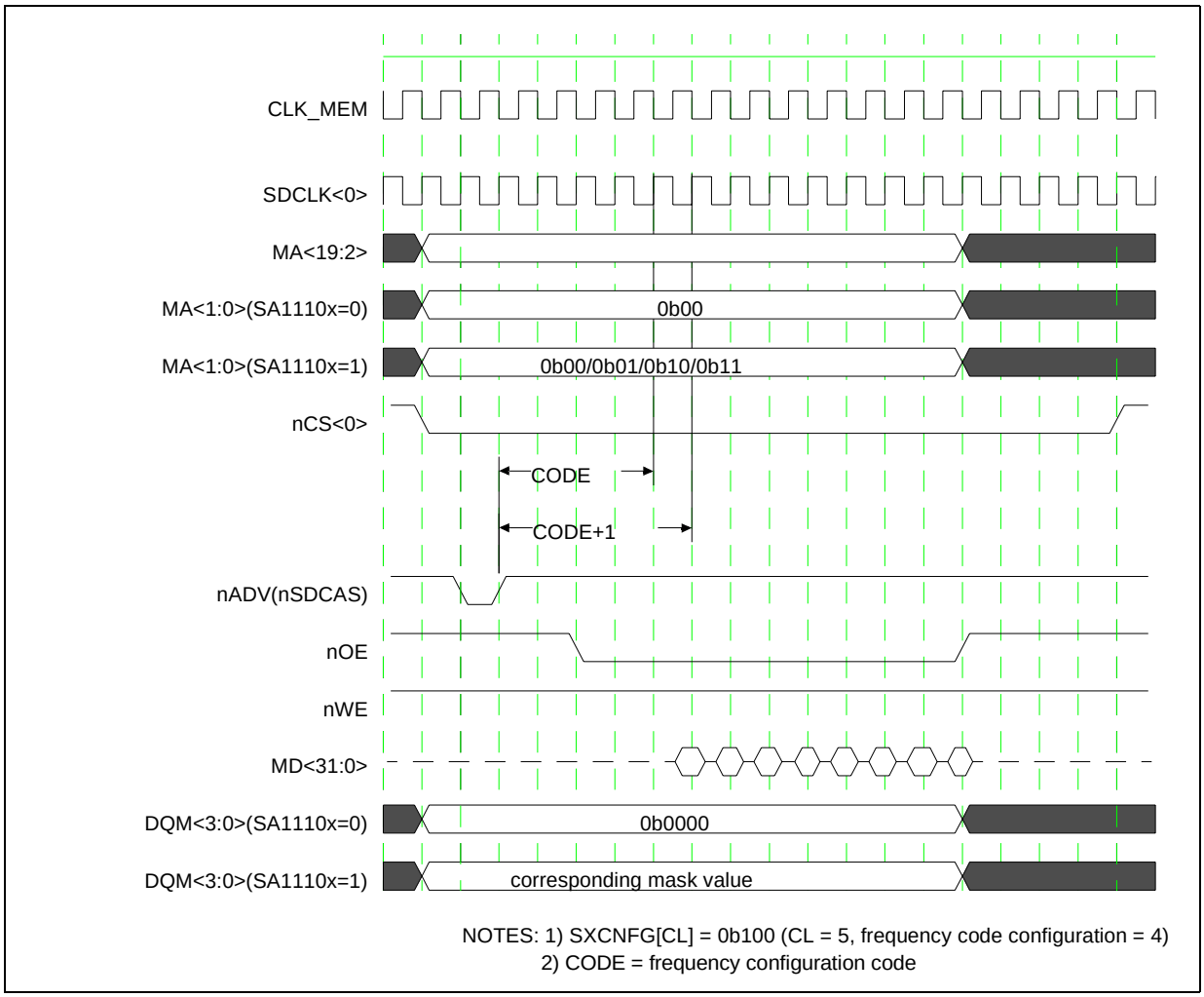
Table 40: Synchronous Flash Read AC Specifications (Sheet 2 of 2)

Symbols	Parameters	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	Units	Notes
		VCC_CORE = 0.85 V +/– 10%, with 1.71 V<= VCC_MEM <= 3.63 V			VCC_CORE = 1.1 V +/– 10%, with 1.71 V <= VCC_MEM <= 3.63 V			VCC_CORE = 1.3 V +/– 10%, with 1.71 V <= VCC_MEM <= 3.63 V				
tffSDIS	MD<31:0> read data input setup time from SDCLK0 rise	2.2	—	—	2.2	—	—	2.2	—	—	ns	—
tffSDIH	MD<31:0> read data input hold time from SDCLK0 rise	2.9	—	—	2.9	—	—	2.9	—	—	ns	—

NOTES:

1. SDCLK0 may be configured to be CLK_MEM divided by 1, 2 or 4. SDCLK0 for synchronous flash memory can be at the slowest, divide-by-4 of the 26-MHz CLK_MEM. The fastest possible SDCLK0 is accomplished by configuring CLK_MEM at 104 MHz and clearing the MDREFR[K0DB2] or MDREFR[K0DB4] bit fields.
2. SDCLK0 frequency equals CLK_MEM frequency (MDREFR[K0DB4] and MDREFR[K0DB2] bit fields are clear)
3. SDCLK0 frequency equals CLK_MEM/2 frequency (MDREFR[K0DB2] is set and MDREFR[K0DB4] is clear).
4. SDCLK0 frequency equals CLK_MEM/4 frequency (MDREFR[K0DB4] is set).
5. Use SXCNFG[SXCLx] to configure the value for the frequency configuration code (FCC).
6. These numbers are for VCC_MEM = 1.8 V +20% / -5%, VOL = 0.4 V, and VOH = 1.4 V, with each applicable 4-bit field of the system memory buffer strength registers (BSCN TRP and BSCNTRN) set to TBD (msb:lsb) and each applicable SDCLK0 divide-by-2 and divide-by-4 register bits (MDREFR[K0DB2] and MDREFR[K0DB4]) clear. If MDREFR[K0DB2 is set, the corresponding output setup and hold times are increased and decreased, respectively, by 0.25 times the SDCLK0 period.
7. These numbers are for VCC_MEM = 2.5 V +/– 10%, VOL = 0.4 V, and VOH = 2.1 V, with each applicable 4-bit field of the system memory buffer strength registers (BSCNTRP and BSCNTRN) set to 0b1010 (msb:lsb) and each applicable SDCLK0 divide-by-2 and divide-by-4 register bit (MDREFR[K0DB2] and MDREFR[K0DB4]) clear. If MDREFR[K0DB2 is set, the corresponding output setup and hold times are increased and decreased, respectively, by 0.25 times the SDCLK0 period.
8. These numbers are for VCC_MEM = 3.3 V +/– 10%, VOL = 0.4 V, and VOH = 2.4 V, with each applicable 4-bit field of the system memory buffer strength registers (BSCNTRP and BSCNTRN) set to 0b1010 (msb:lsb) and each applicable SDCLK0 divide-by-2 and divide-by-4 register bit (MDREFR[K0DB2] and MDREFR[K0DB4]) clear. If MDREFR[K0DB2 is set, the corresponding output setup and hold times are increased and decreased, respectively, by 0.25 times the SDCLK0 period.

Figure 36: Synchronous Flash Burst-of-Eight Read Timing



NOTES: 1) SXCNFG[CL] = 0b100 (CL = 5, frequency code configuration = 4)
2) CODE = frequency configuration code

Figure 37: Synchronous Flash Stacked Burst-of-Eight Read Timing

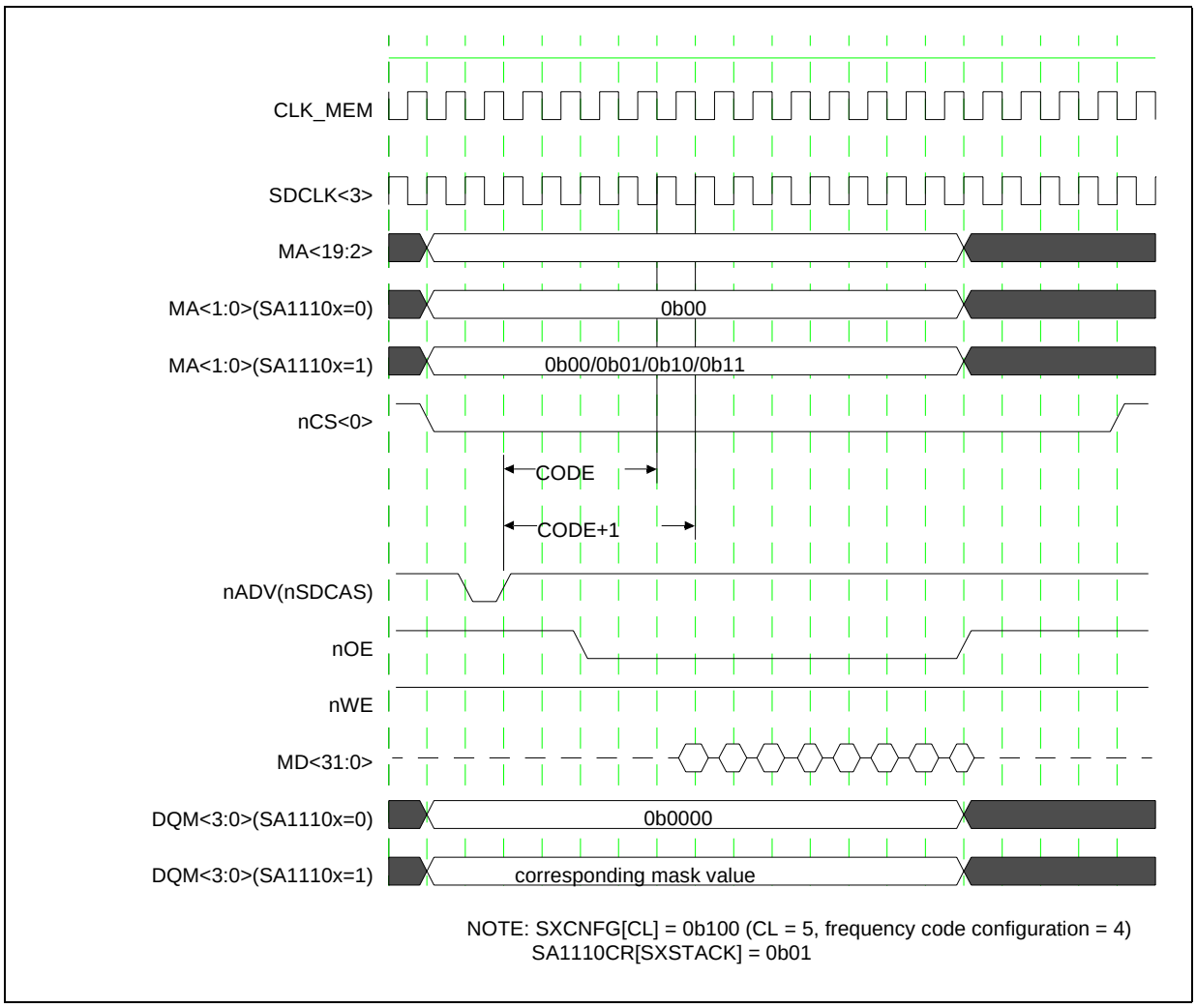
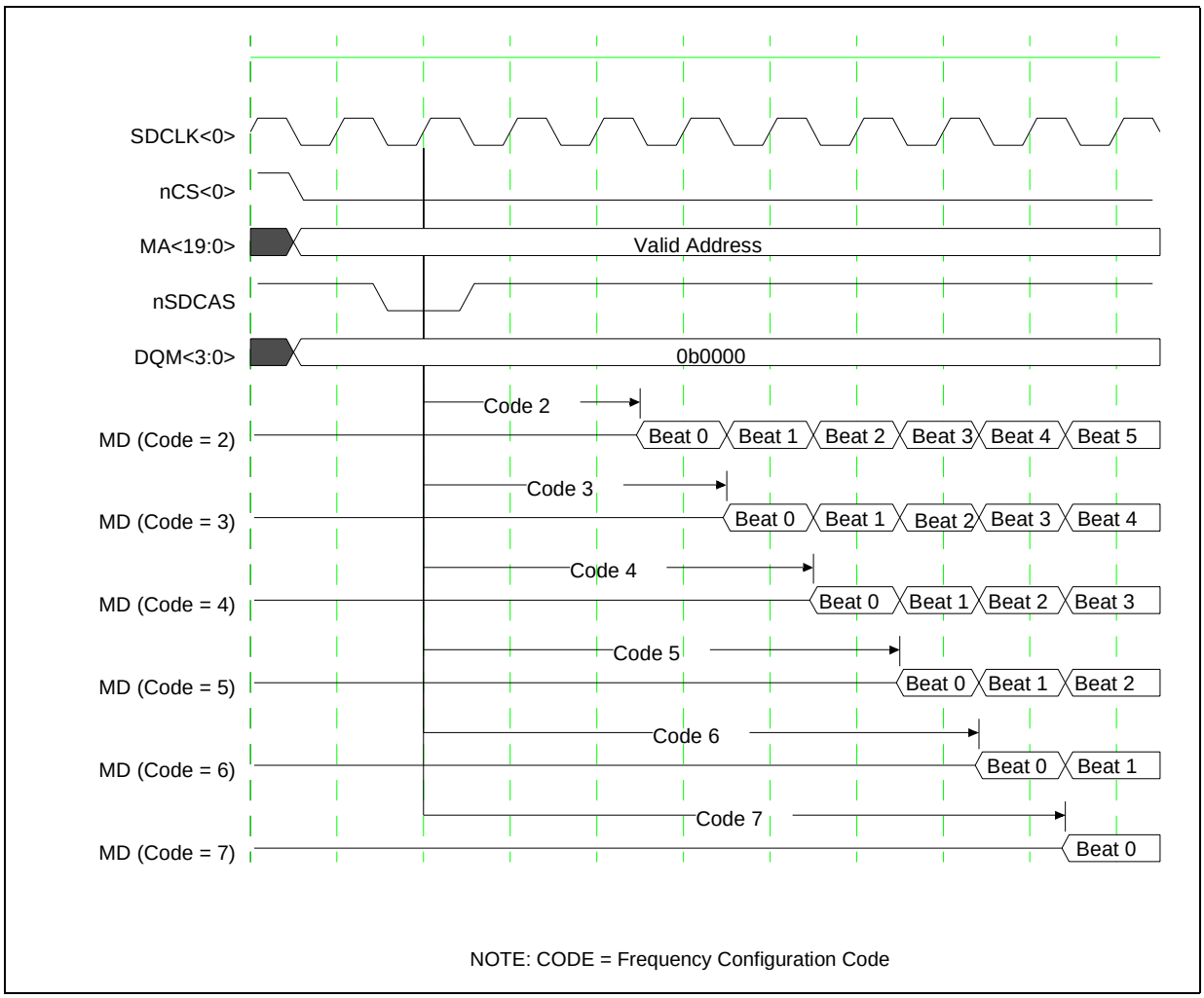


Figure 38 indicates which clock data would be latched following the assertion of nSDCAS(ADV), depending on the configuration of the SXCNFG[SXCLx] bit field. The period in the diagram indicated by different frequency configuration codes (Fcodes or FCCs) is equal to the number of SDCLK0 cycles between the READ command and the clock edge on which data is driven onto the bus.

Figure 38: First-Access Latency Configuration Timing



The burst read example shown in Figure 39 represents waveforms that result when SXCNFG[SXCLx] is configured as 0b0100, representing a frequency configuration code equal to 3. The following example can help determine the appropriate setting for SXCNFG[SXCLx].

Parameters defined by the processor:

- tffSDOH (max) = SDCLK<0> to CE# (nCE), ADV# (nADV), or address valid, whichever occurs last
- tffSDIS (min) = Data setup to SDCLK<0>

Parameters defined by flash memory:

- tVLQV (min) = ADV# low to output delay
- tVLCH (min) = ADV# low to clock
- tCHQV (max) = SDCLK<0> to output valid

Use the following equations when calculating the frequency configuration code:

(1) SDCLK period = (1 / frequency)

(2) n (SDCLK period) $\geq$ tVLQV - tVLCH - tCHQV

(3) n = (tVLQV - tVLCH - tCHQV) / SDCLK period, where

n = frequency configuration code rounded up to integer value

(4) SDCLK period ≥ tCHQV + tffSDIS

Example

The timing information below is only an example. See Table 40 for actual synchronous AC timings.

SDCLK<0> frequency = 50 MHz

tVLQV = 70 ns (typical timing from synchronous flash memory)

tVLCH = 10 ns (min)

tCHQV = 14 ns (min)

From Eq.(1):1 / 50 (MHz) = 20 ns

From Eq.(2):n(20 ns) ≥ 70 ns - 10 ns - 14 ns

n(20 ns) ≥ 46 ns

n = (46 / 20) ns = 2.3 ns

n = 3

Use Equation 4 to help verify the maximum possible frequency at which the synchronous flash memory can run with the memory controller. The following example uses Equation 4:

SDCLK<0> frequency = 66 MHz

tCHQV = 11 ns (max)

tffSDIS = 3 ns (min)

From Eq. (1):1 / 66 (MHz) = 15.15 ns

From Eq. (4):15.15 ns ≥ 11 ns + 3 ns

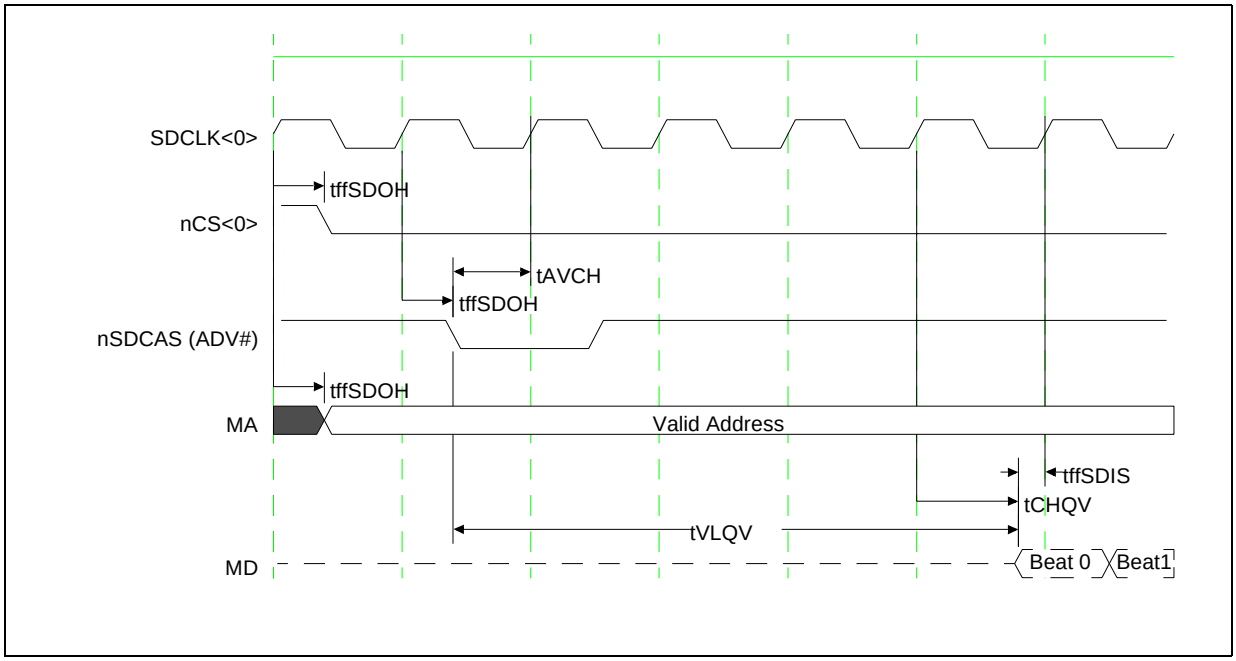
15.15 ns ≥ 14 ns

The results from this example indicate that the 66-MHz memory works without problems with the memory controller.

Note

All AC timings must be considered to avoid timing violations in the memory-to-memory-controller interface.

Figure 39: Synchronous Flash Burst Read Example



6.4.4.4 Flash Memory Write Parameters and Timing Diagrams

Table 41 lists the AC specification for both burst and non-burst flash writes shown in Figure 40 and, for stacked flash packages, Figure 41.

Table 41: Flash Memory AC Specification (Sheet 1 of 2)

Symbols	Parameters	MIN	TYP	MAX	Units[1]	Notes
tflashAS	Address setup to nCS assert	1	—	1	clk_mem	—
tflashAH	Address hold from nWE de-asserted	1	—	1	clk_mem	—
tflashASW	Address setup to nWE asserted	1	—	3	clk_mem	2
tflashCES	nCS setup to nWE asserted	2	—	2	clk_mem	—
tflashCEH	nCS hold from nWE de-asserted	1	—	1	clk_mem	—
tflashWL	nWE asserted time	1	MSCx[RDF]+1	31	clk_mem	—
tflashDSWH	MD/DQM setup to nWE de-asserted	2	MSCx[RDF]+2	32	clk_mem	—
tflashDH	MD/DQM hold from nWE de-asserted	1	—	1	clk_mem	—
tflashDSOH	MD setup to address valid	1.5	—	—	clk_mem	—

Table 41: Flash Memory AC Specification (Sheet 2 of 2)

Symbols	Parameters	MIN	TYP	MAX	Units[1]	Notes
tflashDOH	MD hold from address valid	0	—	—	clk_mem	—
tflashCD	nCS de-asserted after a read/write to next nCS or nSDCS asserted (minimum)	1	MSCx[RRR]*2 + 1	15	clk_mem	—

NOTES:
1. Numbers shown as integer multiples of the CLK_MEM period are ideal. Actual numbers vary with pin-to-pin differences in loading and transition direction (rise or fall).
2. On the first data beat of burst transfer, the tflashASW is 3 CLK_MEM periods. On subsequent data beats, the tflashASW is 1 CLK_MEM period.

Figure 40: 32-Bit Flash Write Timing

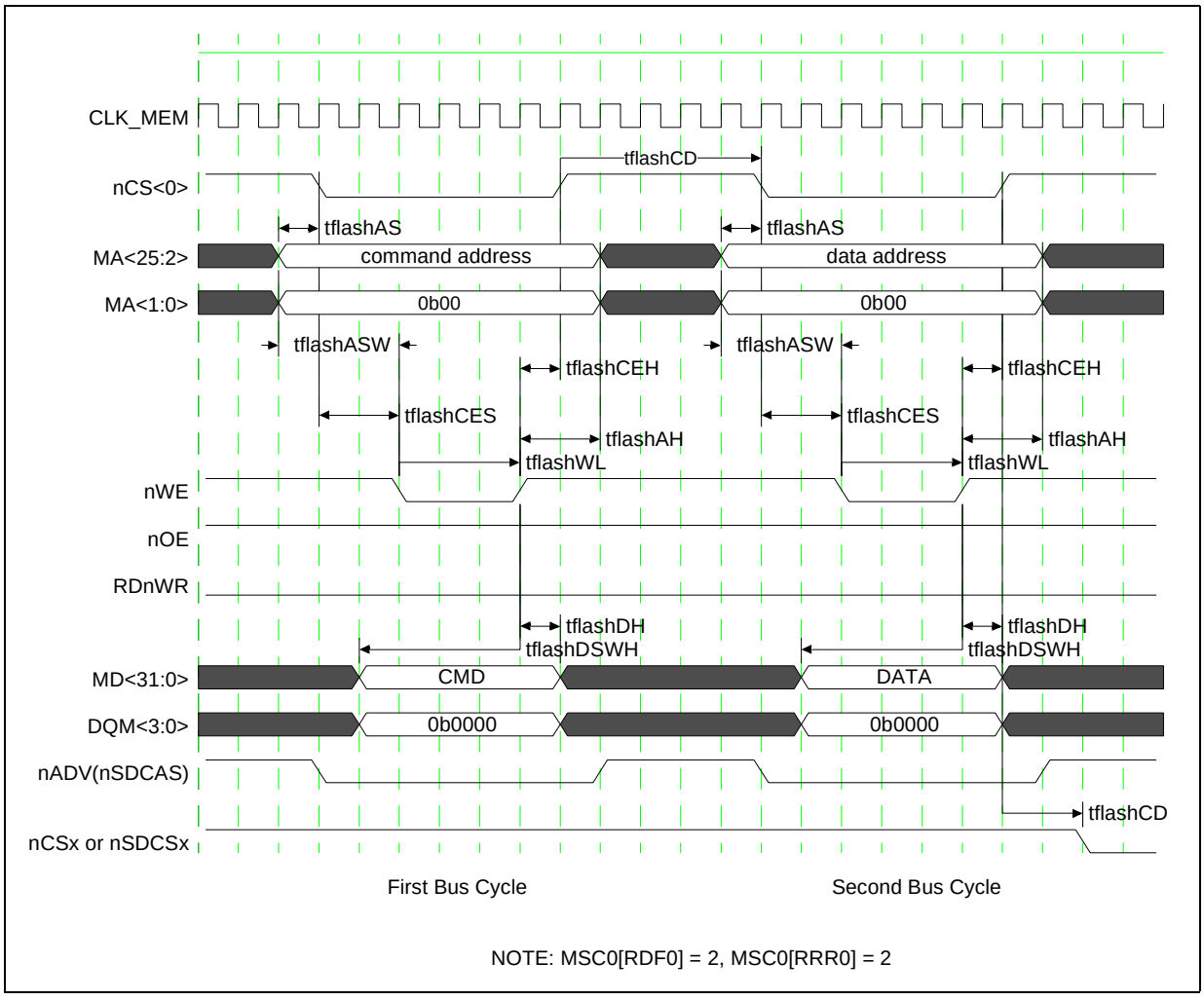


Figure 41: 32-Bit Stacked Flash Write Timing

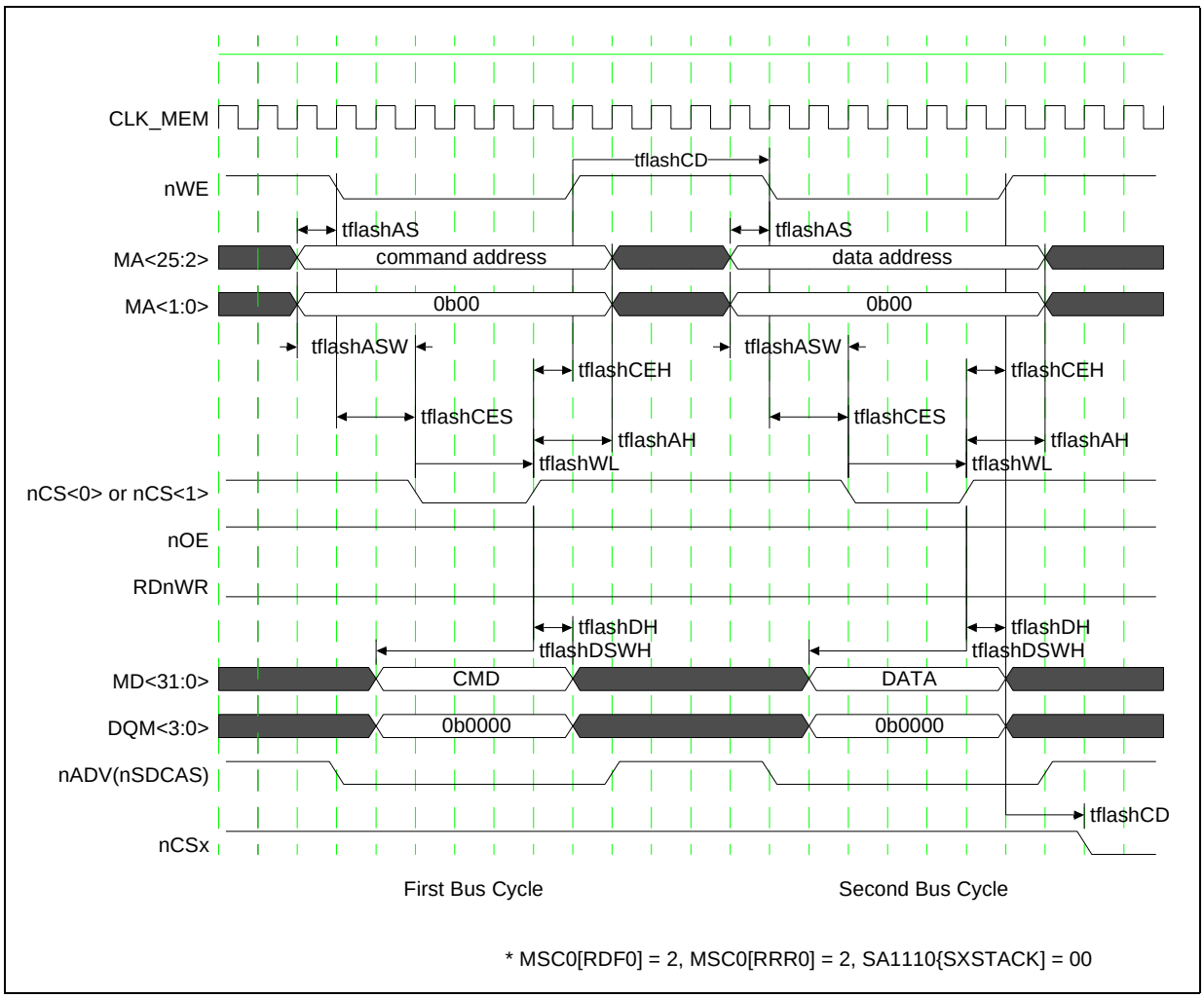
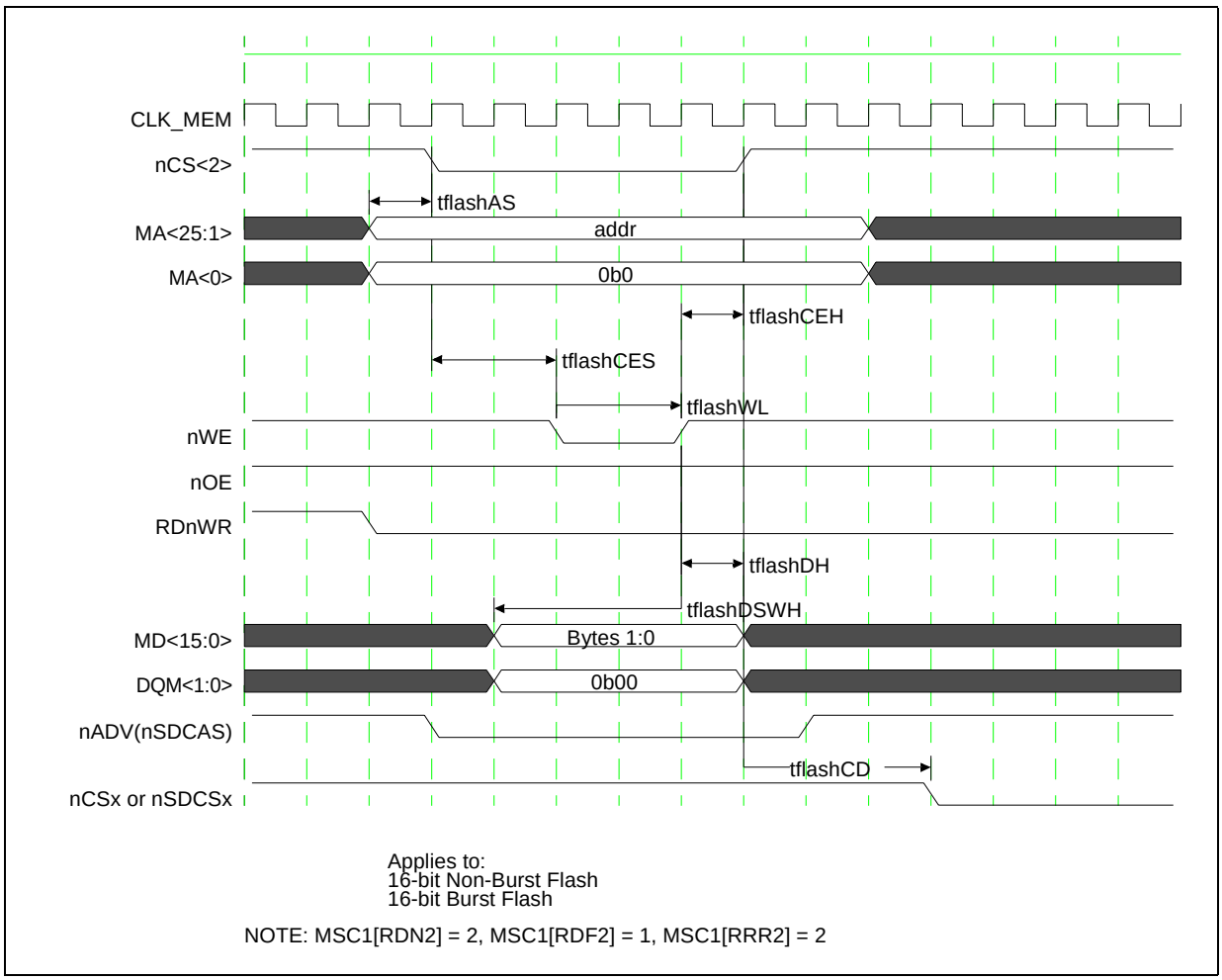


Figure 42: 16-Bit Flash Write Timing



6.4.5 SRAM Parameters and Timing Diagrams

The following sections describe the read/write parameters and timing diagrams for SRAM interfaces with the memory controller.

6.4.5.1 SRAM Read Parameters and Timing Diagrams

The timing for a read access is identical to that for a non-burst ROM read (see Figure 32). The timings listed in Table 39 for ROM reads are also used for SRAM reads. See Figure 32 and Figure 35 for timings diagrams representing 16-bit SRAM transferring four, two, and one byte(s) during read-bus tenures.

6.4.5.2 SRAM Write Parameters and Timing Diagrams

Figure 43 and Figure 44 show the timing for 32-bit and 16-bit SRAM writes. Table 42 lists the timings used in Figure 43 and Figure 44.

During writes, data pins are actively driven by the processor and are not three-stated, regardless of the states of the individual DQM signals. For SRAM writes, the DQM signals are used as byte enables.

Note

Table 42 lists programmable register items. See the “Memory Controller”chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register configurations for more information on these items.

Table 42: SRAM Write AC Specification

Symbols	Parameters	MIN	TYP	MAX	Units[1]	Notes
tsramAS	Address setup to nCS assert	1	—	1	clk_mem	—
tsramAH	Address hold from nWE de-asserted	1	—	1	clk_mem	—
tsramASW	Address setup to nWE asserted	1	—	3	clk_mem	2
tsramCES	nCS setup to nWE asserted	2	—	2	clk_mem	—
tsramCEH	nCS hold from nWE de-asserted	1	—	1	clk_mem	—
tsramWL	nWE asserted time	1	MSCx[RDN]+1	31	clk_mem	—
tsramDSWH	MD/DQM setup to nWE de-asserted	2	MSCx[RDN]+2	32	clk_mem	—
tsramDH	MD/DQM hold from nWE de-asserted	1	—	1	clk_mem	—
tramCD	nCS de-asserted after a read to next nCS or nSDCS asserted (minimum)	1	MSCx[RRR]*2+1	15	clk_mem	—

NOTES:
1. Numbers shown as integer multiples of the CLK_MEM period are ideal. Actual numbers vary with pin-to-pin differences in loading and transition direction (rise or fall).
2. On the first data beat of burst transfer, the tsramASW is 3 CLK_MEM periods. On subsequent data beats, the tsramASW is 1 CLK_MEM period.

Figure 43: 32-Bit SRAM Write Timing

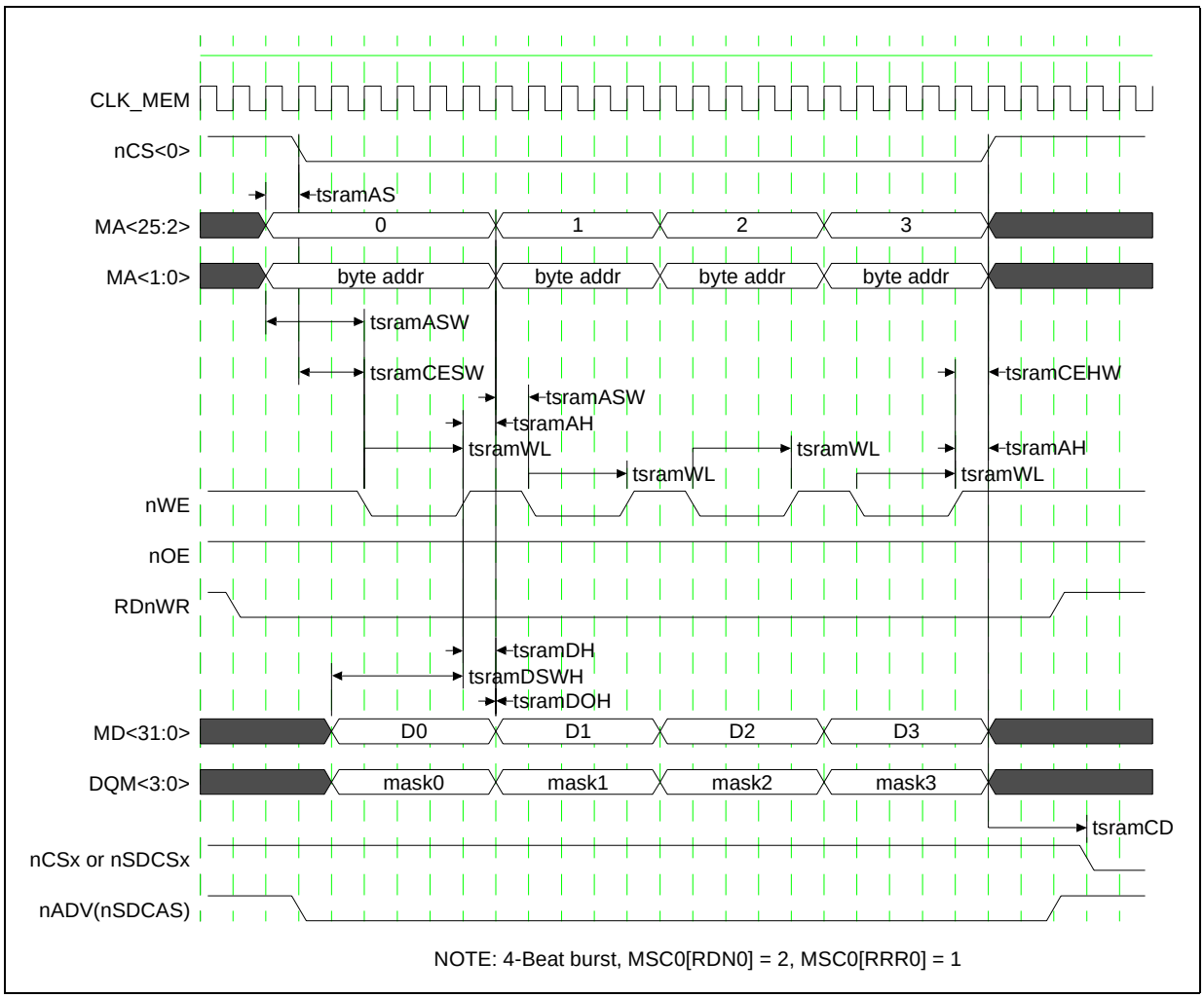
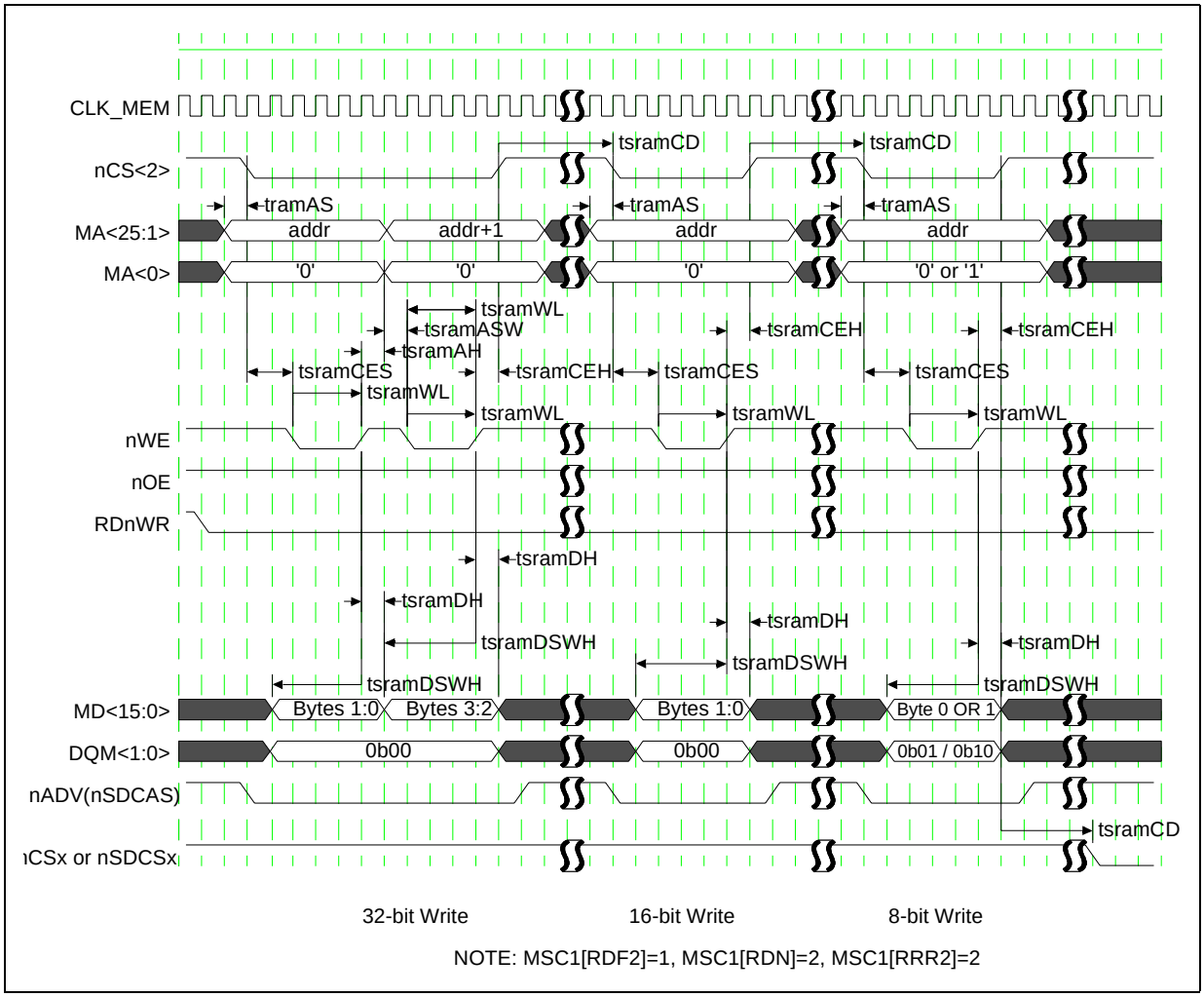


Figure 44: 16-bit SRAM Write for 4/2/1 Byte(s) Timing



6.4.6 Variable-Latency I/O Parameters and Timing Diagrams

The following sections describe the read/write parameters and timing diagrams for VLIO memory interfaces with the memory controller.

Table 43 lists the timing-information references for both the read and the write timing diagrams.

Note

Table 43 lists programmable register items. For more information on these items, see the “Memory Controller” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register configurations.

Table 43: VLIO Timing

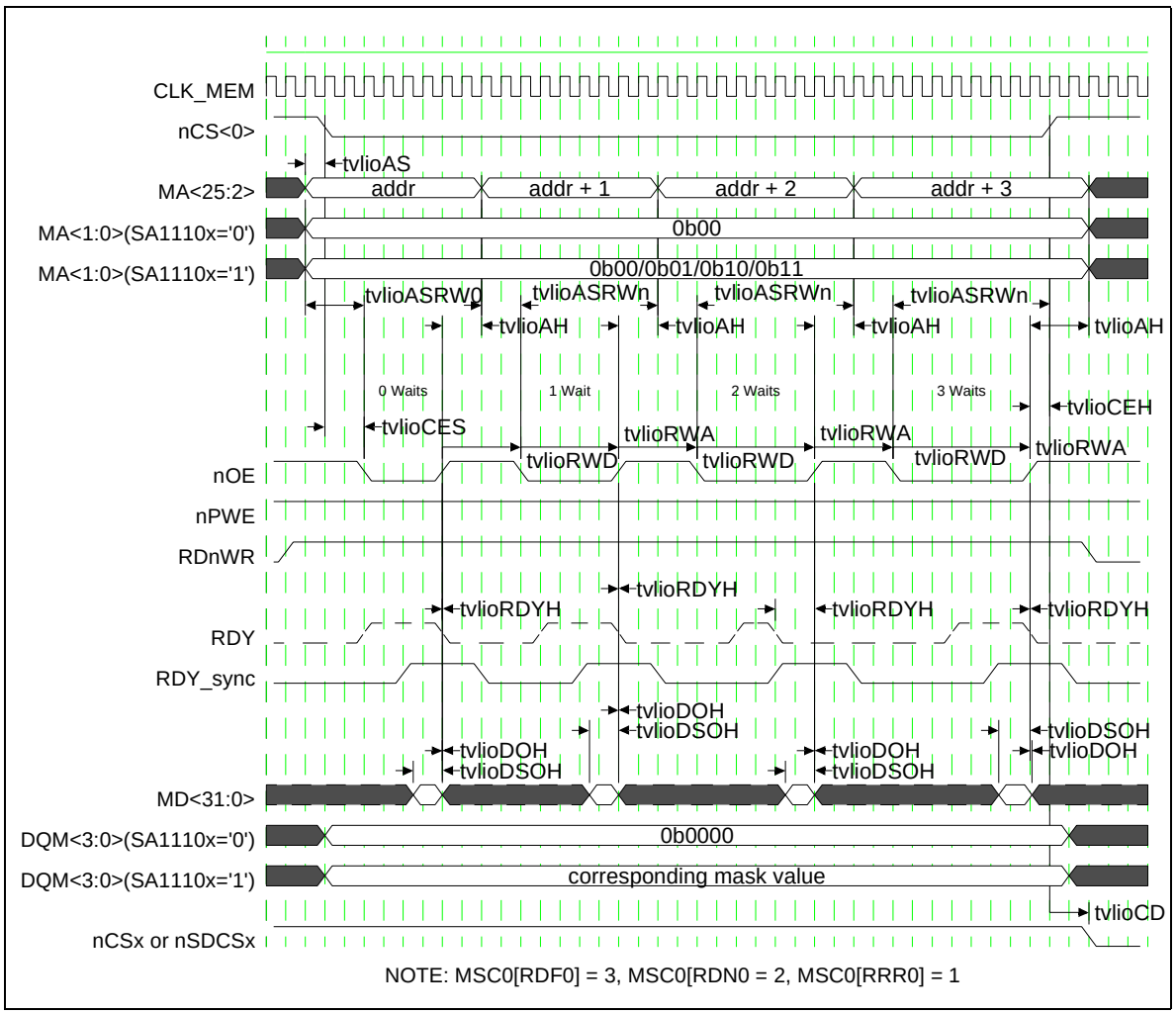
Symbols	Parameters	MIN	TYP	MAX[2]	Units[1]	Notes
tvlioAS	Address setup to nCS asserted	1	—	1	clk_mem	—
tvlioAH	Address hold from nPWE/nOE de-asserted	2	MSCx[RDN]	30	clk_mem	—
tvlioASRW0	Address setup to nPWE/nOE asserted (1st access)	3	—	3	clk_mem	—
tvlioASRWn	Address setup to nPWE/nOE asserted (next access(es))	2	MSCx[RDN]	30	clk_mem	—
tvlioCES	nCS setup to nPWE/nOE asserted	2	—	2	clk_mem	—
tvlioCEH	nCS hold from nPWE/nOE de-asserted	1	—	1	clk_mem	—
tvlioDSWH	MD/DQM setup (minimum) to nPWE de-asserted	5	MSCx[RDF]+2	32	clk_mem	—
tvlioDH	MD/DQM hold from nPWE de-asserted	2	MSCx[RDN]	30	clk_mem	—
tvlioDSOH	MD setup to address changing	1.5		—	clk_mem	—
tvlioDOH	MD hold from address changing	0		—	ns	—
tvlioRDYH	RDY hold from nPWE/nOE de-asserted	0	—	—	ns	—
tvlioRWA	nPWE/nOE assert period between writes	4	MSC[RDF]+1 + Waits	31 + Waits	clk_mem	—
tvlioRWD	nPWE/nOE de-asserted period between writes	4	MSCx[RDN*2]	60	clk_mem	3
tvlioCD	nCS de-asserted after a read/write to next nCS or nSDCS asserted (minimum)	1	MSCx[RRR]*2 + 1	15	clk_mem	—

NOTES:
1. Numbers shown as integer multiples of the CLK_MEM period are ideal. Actual numbers vary with pin-to-pin differences in loading and transition direction (rise or fall).
2. Maximum values reflect the register dynamic ranges.
3. Depending on the programmed value of MSC[RDN] and the clk_mem speed, this can be a significant amount of time. Processor does not drive the data bus during this time between transfers. If the VLIO does not drive the data bus during this time between transfers, the data bus is not driven for this period of time. If MSC[RDN] is programmed to 60 (which equals 60 CLK_MEM cycles), then the data bus could potentially not be driven for 30*2 = 60 CLK_MEM cycles.

6.4.6.1 Variable Latency I/O Read Timing

Figure 45 shows the timing for 32-bit variable-latency I/O (VLIO) memory reads. Table 43 lists the timing parameters used in these diagrams.

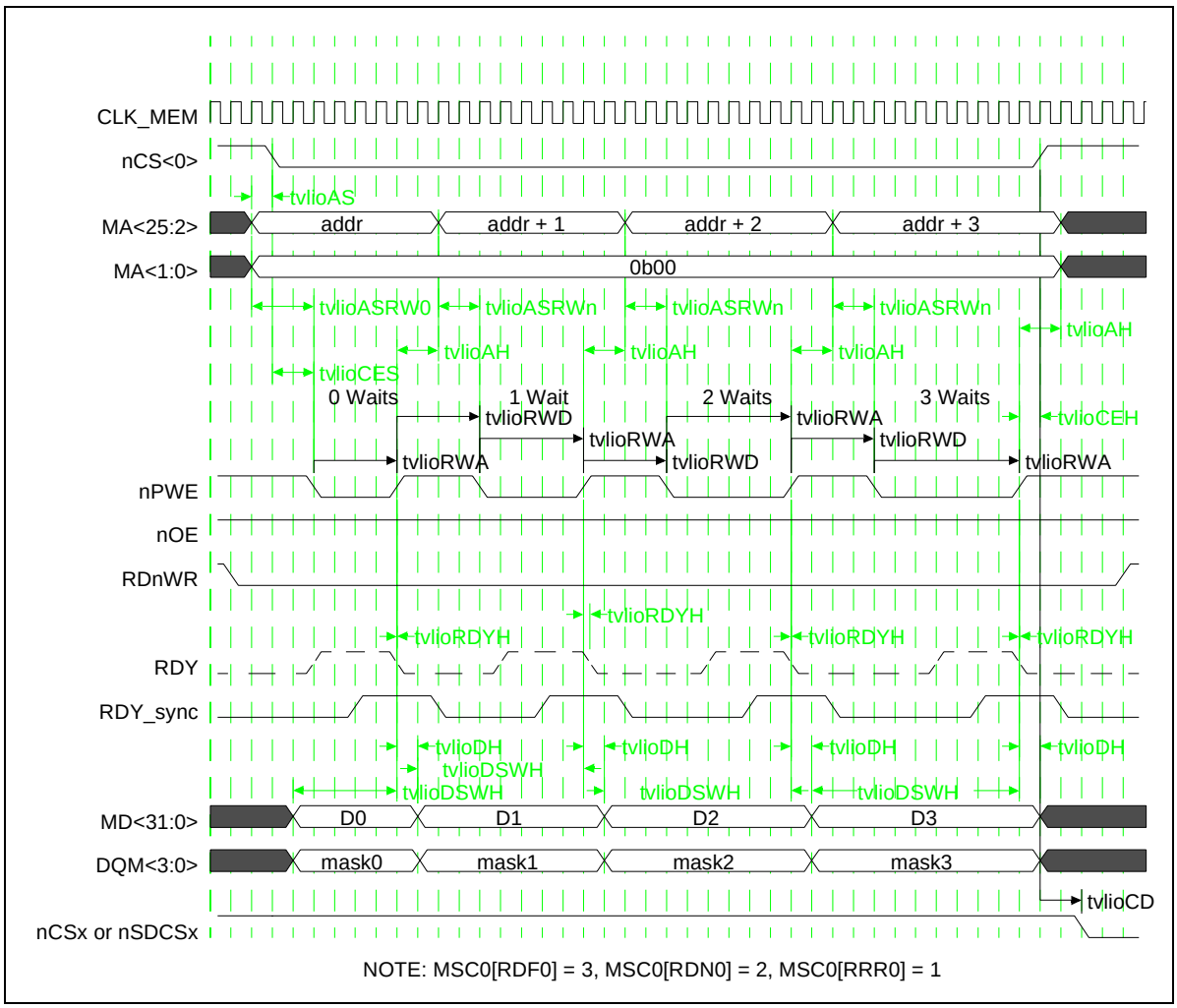
Figure 45: 32-Bit VLIO Read Timing



6.4.6.2 Variable-Latency I/O Write Timing

Figure 46 shows the timing for 32-bit VLIO memory writes. Table 43 list the timing parameters used in Figure 46.

Figure 46: 32-Bit VLIO Write Timing



NOTE: MSC0[RDF0] = 3, MSC0[RDN0] = 2, MSC0[RRR0] = 1

6.4.7 Expansion-Card Interface Parameters and Timing Diagrams

The following sections describe the read/write parameters and timing diagrams for CompactFlash* and PC Card* (expansion card) memory interfaces with the memory controller.

Table 44 shows the timing parameters used in the timing diagrams, Figure 47 and Figure 48.

Note

Table 44 lists programmable register items. See the “Memory Controller” chapter in the *Marvell® PXA27x Processor Family Developer’s Manual* for register configurations for more information on these items.

Table 44: Expansion-Card Interface AC Specifications

Symbols	Parameters	MIN	TYP	MAX	Units	Notes
tcdAVCL	Address Valid to CMD Low	2	MCx[SET]	127	CLK_MEM	1,2,3,4
tcdCHAI	CMD High to Address Invalid	0	MCx[HOLD]	63	CLK_MEM	1,2,3,5
tcdDVCL	Write Data Valid to CMD Low	—	1	—	CLK_MEM	1,3
tcdCHWDI	CMD High to Write Data Invalid	—	4	—	CLK_MEM	1,3
tcdDVCH	Read Data Valid to CMD High	2	—	—	CLK_MEM	1,3
tcdCHRDI	CMD High to Read Data Invalid	0	—	—	ns	3
tcdCMD	CMD Assert During Transfers	—	tcdCLPS + tcdPHCH + nPWAIT assertion	—	CLK_MEM	1,3
tcdILCL	nIOIS16 Low to CMD Low	4	—	—	CLK_MEM	1,3
tcdCHIH	CMD High to nIOIS16 High	2	—	—	CLK_MEM	1,3
tcdCLPS	CMD Low to nPWAIT Sample	—	x_ASST_WAIT	—	CLK_MEM	1,3,6,7
tcdPHCH	nPWAIT High to CMD High	—	x_ASST_HOLD	—	CLK_MEM	1,3,6,8

NOTES:
1. All numbers shown are ideal, integer multiples of the CLK_MEM period. Actual numbers vary with pin-to-pin differences in loading and transition direction (rise or fall).
2. Includes signals MA[25:0], nPREG, and nPSKTSEL.
3. CMD refers to signals nPWE, nPOE, nPIOW, and nPIOR
4. Refer to the *Marvell® PXA27x Processor Family Developer's Manual*, Expansion Memory Timing Configuration registers to change the assertion of CMD using the MCx[SET] bit fields.
5. Refer to the *Marvell® PXA27x Processor Family Developer's Manual*, Expansion Memory Timing Configuration registers to increase the assertion of CMD using the MCx[HOLD] bit fields.
6. Refer to the *Marvell® PXA27x Processor Family Developer's Manual*, Expansion Memory Timing Configuration registers to increase timings. The timings are changed by programming the MCx[ASST] respective bit fields. Refer to the PC Card Interface Command Assertion Code table to see the effect of MCx[ASST].
7. tcdCLPS equals CLK_MEM * x_ASST_WAIT. Refer to the PC Card Interface Command Assertion Code table in the *Marvell® PXA27x Processor Family Developer's Manual* for the correlation between x_ASST_WAIT and the MCx[ASST] bit field.
8. tcdPHCH equals CLK_MEM * x_ASST_HOLD. Refer to the PC Card Interface Command Assertion Code table in the *Marvell® PXA27x Processor Family Developer's Manual* for the correlation between x_ASST_HOLD and the MCx[ASST] bit field.

Figure 47: Expansion-Card Memory or I/O 16-Bit Access Timing

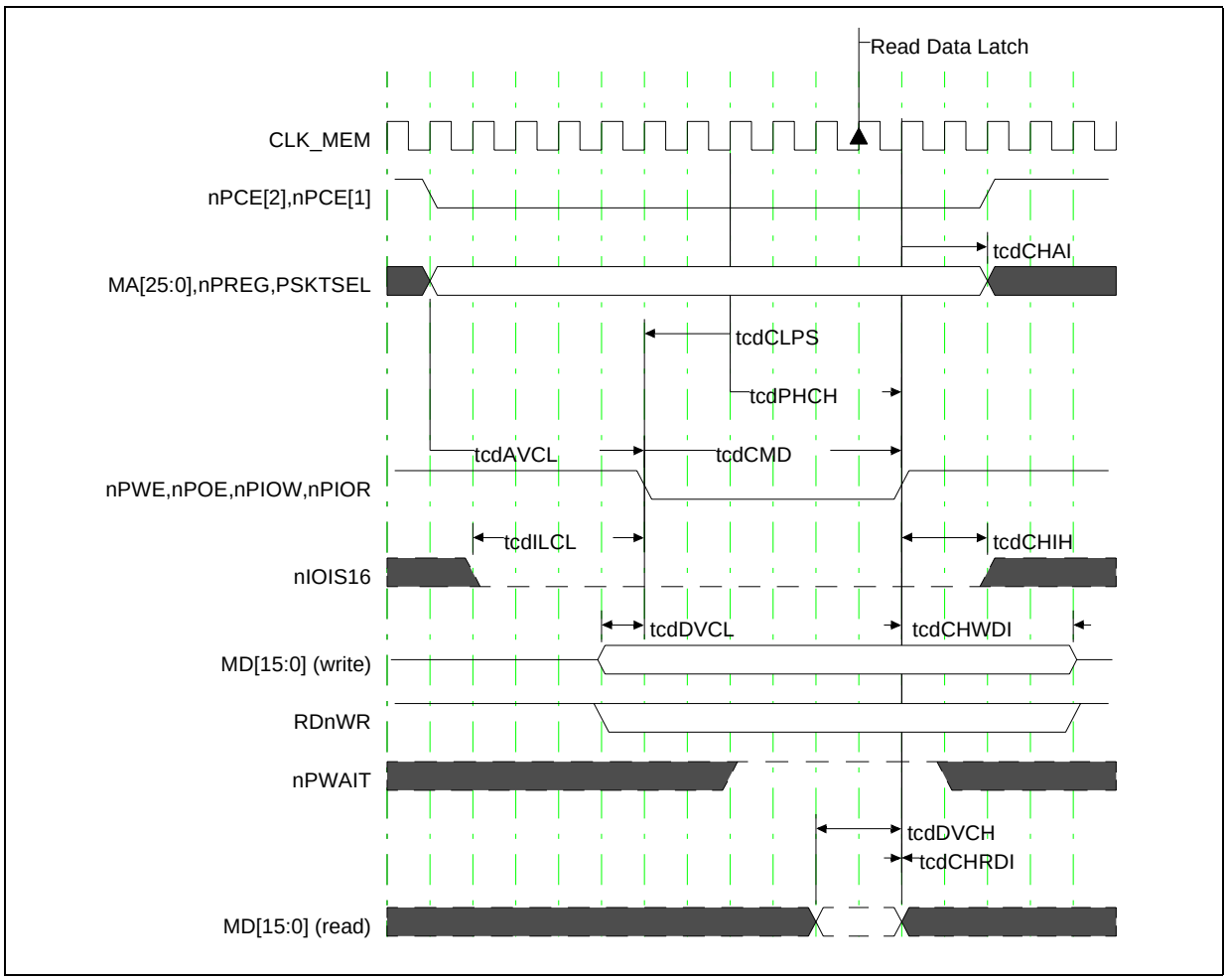
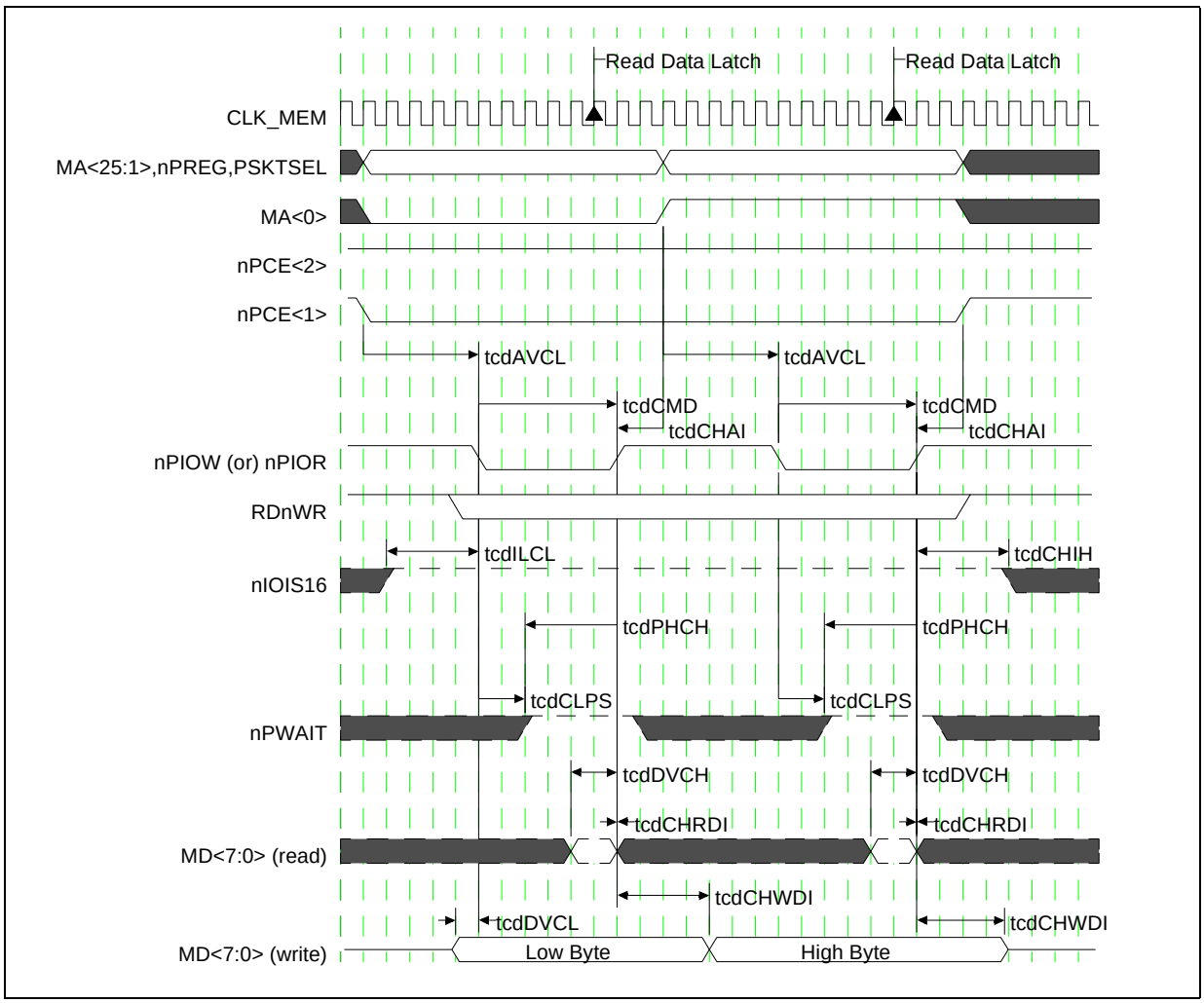


Figure 48: Expansion-Card Memory or I/O 16-Bit Access to 8-Bit Device Timing



6.5 LCD Timing Specifications

Figure 49 describes the LCD timing parameters. The LCD pin timing specifications are referenced to the pixel clock (L_PCLK_WR). Table 45 gives the values for the parameters.

Figure 49: LCD Timing Definitions

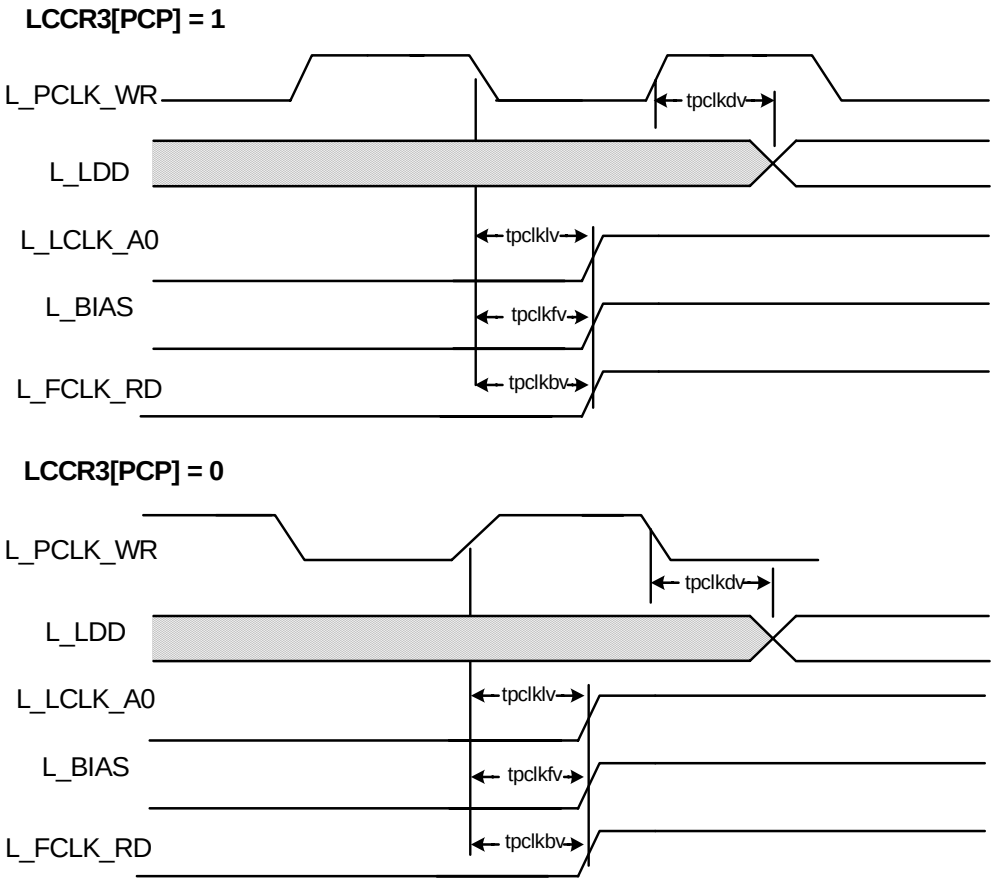


Table 45: LCD Timing Specifications

Symbol	Description	Min	Max	Units	Notes
Tpclkdv	L_PCLK_WR rise/fall to L_LDD<17:0> driven valid	—	7	ns	1
Tpclklv	L_PCLK_WR fall to L_LCLK_A0 driven valid	—	7	ns	2
Tpclkfv	L_PCLK_WR fall to L_FCLK_RD driven valid	—	7	ns	2
Tpclkbv	L_PCLK_WR rise to L_BIAS driven valid	—	14	ns	2

NOTES:
1. The LCD data pins can be programmed to be driven on either the rising or falling edge of the pixel clock (L_PCLK_WR).
2. These LCD signals can toggle when L_PCLK_WR is not clocking (between frames). At this time, they are clocked with the internal version of the pixel clock before it is driven out onto the L_PCLK_WR pin.

6.6 SSP Timing Specifications

Figure 50 describes the SSP timing parameters. The SSP pin timing specifications are referenced to SSPCLK. Table 46 gives the values for the parameters.

Note

In Figure 50, read the term “tSFMV” as “TSTXV.”

Figure 50: SSP Master Mode Timing Definitions

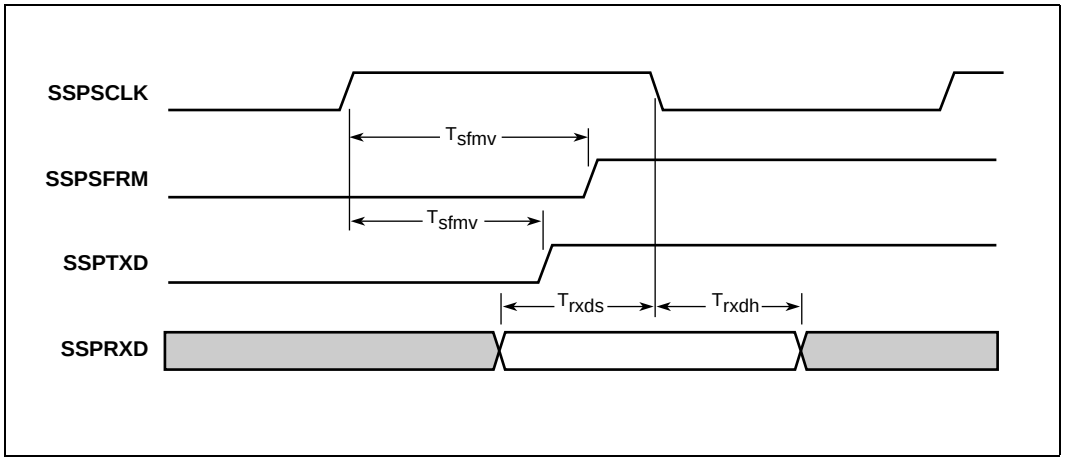


Table 46: SSP Master Mode Timing Specifications

Symbol	Description	Min	Max	Units	Notes
Tsfmv	SSPSCLK rise to SSPSFRM driven valid		21	ns	
Trxds	SSPRXD valid to SSPSCLK fall (input setup)	11		ns	
Trxdh	SSPSCLK fall to SSPRXD invalid (input hold)	0		ns	
Tsfmv	SSPSCLK rise to SSPTXD valid		22	ns	

Figure 51: Timing Diagram for SSP Slave Mode Transmitting Data to an External Peripheral

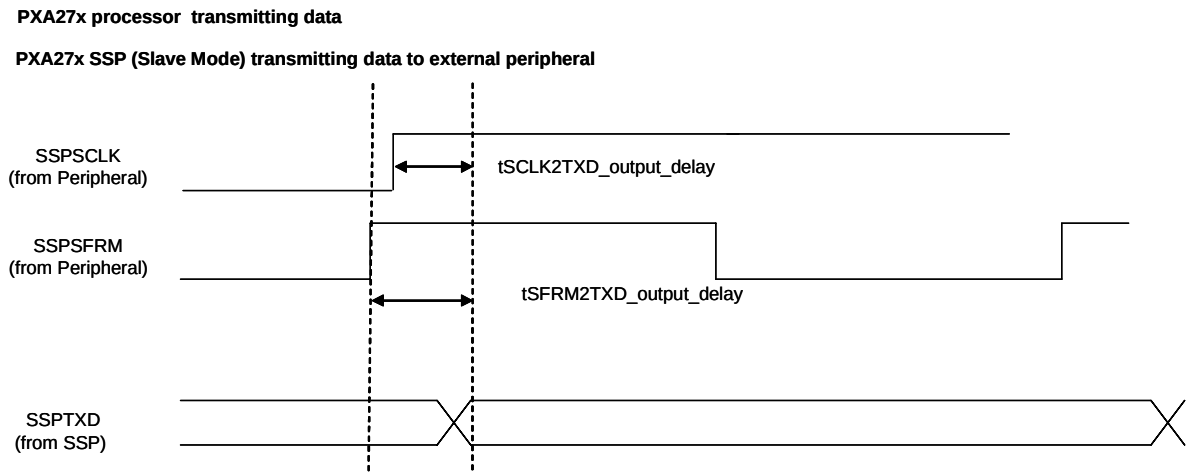


Table 47: Timing Specification SSP Slave Mode Transmitting Data to External Peripheral

Parameter	Description	Min	Typ	Max	Units
tSFRM2TXD_output_delay	Frame to TX Data Out		10.58		ns
tSCLK2TXD_output_delay	Clock to Tx Data Out		10.52		ns

Figure 52: Timing Diagram for SSP Slave Mode Receiving Data from External Peripheral

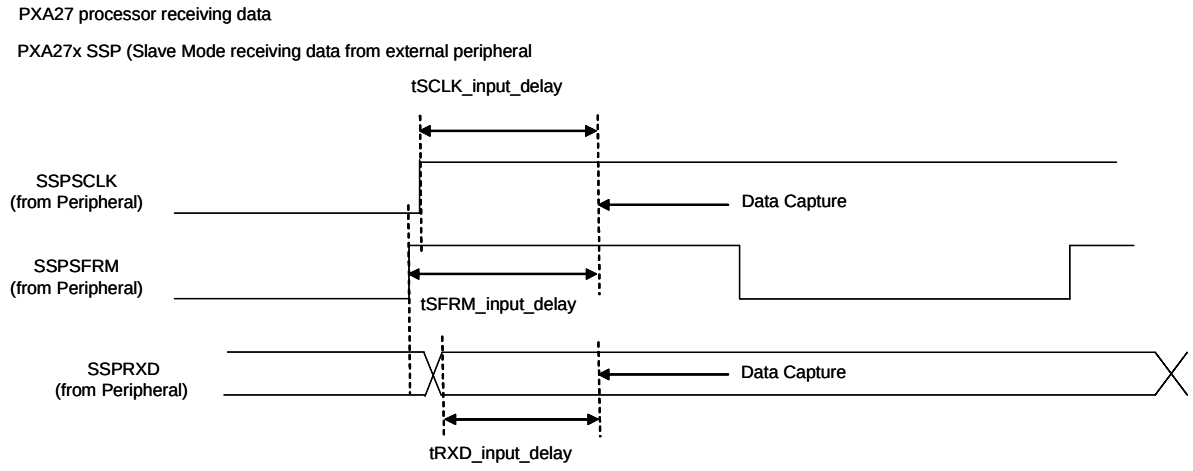


Table 48: Timing Specification for SSP Slave Mode Receiving Data from External Peripheral

Parameter	Description	Min	Typical	Max	Units
tSFRM_input_delay	Frame to Rx Data Capture		5.21		ns
tSCLK_input_delay	Clock to Rx Data Capture		5.04		ns
tRXD_input_delay	Rx Data Setup to Capture		4.81		ns

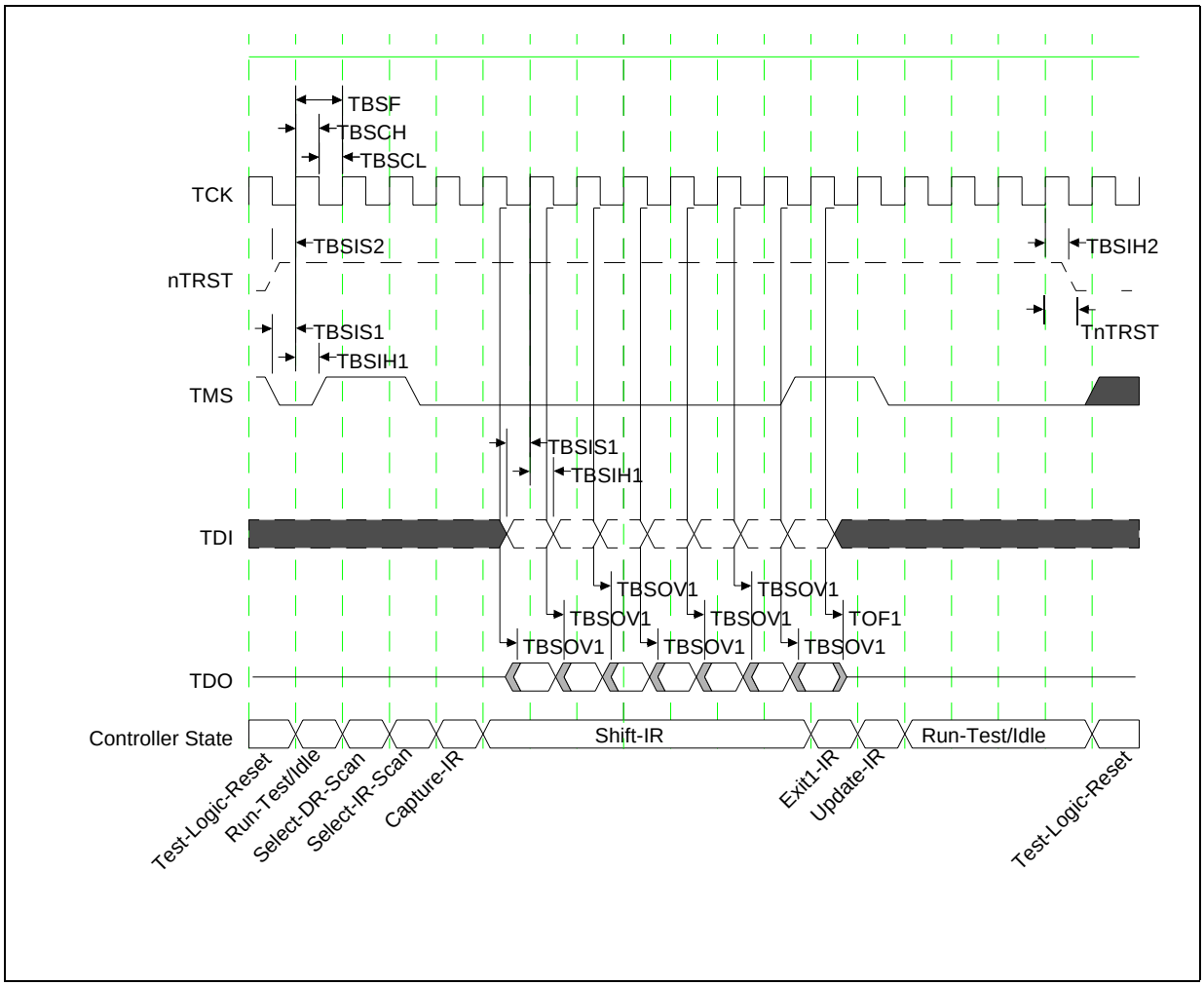
6.7 JTAG Boundary Scan Timing Specifications

Table 49 shows the AC specifications for the JTAG boundary-scan test signals. Figure 53 shows the timing diagram.

Table 49: Boundary Scan Timing Specifications

Symbol	Parameter	Min	Max	Units	Notes
TBSF	TCK Frequency	0.0	33.33	MHz	—
TBSCH	TCK High Time	15.0	—	ns	Measured at 1.5 V
TBSCL	TCK Low Time	15.0	—	ns	Measured at 1.5 V
TBSCR	TCK Rise Time	—	5.0	ns	0.8 V to 2.0 V
TBSCF	TCK Fall Time	—	5.0	ns	2.0 V to 0.8 V
TBSIS1	Input Setup to TCK TDI, TMS	4.0	—	ns	—
TBSIH1	Input Hold from TCK TDI, TMS	6.0	—	ns	—
TBSIS2	Input Setup to TCK nTRST	25.0	—	ns	—
TBSIH2	Input Hold from TCK nTRST	3.0	—	ns	—
TnTRST	Assertion time of nTRST	6	—	ms	—
TBSOV1	TDO Valid Delay	1.5	6.9	ns	Relative to falling edge of TCK
TOF1	TDO Float Delay	1.1	5.4	ns	Relative to falling edge of TCK

Figure 53: JTAG Boundary-Scan Timing



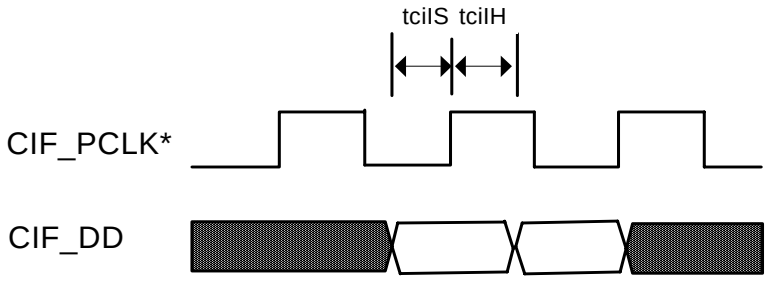
6.8 Marvell® Quick Capture Technology AC Timing

Table 50 lists the timing parameters used in Figure 54.

Table 50: Marvell® Quick Capture AC Timing Specification

Symbol	Description	Min	Typical	Max	Units
tciIS	Camera Interface Setup Time	5	—	—	ns
tciIH	Camera Interface Hold Time	5	—	—	ns

Figure 54: Marvell® Quick Capture Interface Timing



* CIF_PCLK Data Sampling edge determined by the CICR 4[PCP] setting

6.9 MultiMediaCard Timing Specifications

Figure 55: MultiMedia Card timing Diagrams

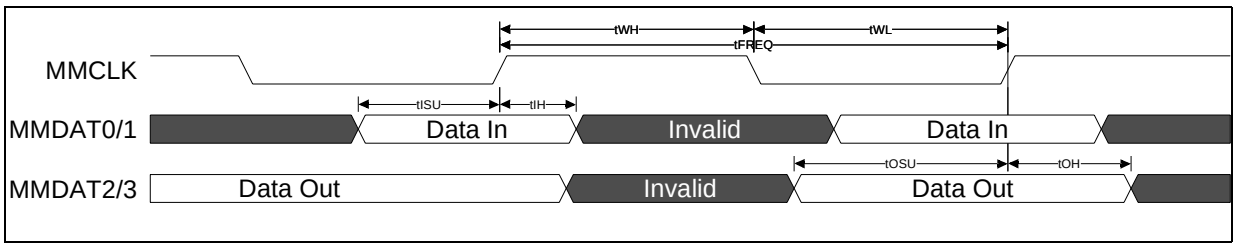


Table 51: MultiMedia Card timing specifications

Symbol	Parameter	Min	Max	Unit	Notes
t_{FREQ}	MMCLK Frequency Data Transfer Mode	0	19.5	MHz	
t_{FREQ}	MMCLK Frequency Identification Mode	0	400	KHz	
t_{WH}	Clock high time	10	—	ns	
t_{WL}	Clock low time	10	—	ns	
t_{rise}	Clock rise time	—	10	ns	1
t_{fall}	Clock fall time	—	10	ns	1
t_{ISU}	Data input setup time	3	—	ns	
t_{IH}	Data input hold time	3	—	ns	
t_{OSU}	Output data setup time	13.1	—	ns	
t_{OH}	Output data hold time	9.7	—	ns	
NOTE: 52. Rise and fall times measured from 10% - 90% of voltage level.					

t_{WH}	Clock high time	10	—	ns	
t_{WL}	Clock low time	10	—	ns	
t_{rise}	Clock rise time	—	10	ns	1
t_{fall}	Clock fall time	—	10	ns	1

6.10 Secure Digital (SD/SDIO) Timing

Figure 56 and Table 52 define the Secure Digital (SD/SDIO) controller AC timing specifications.

Figure 56: SD/SDIO timing diagrams

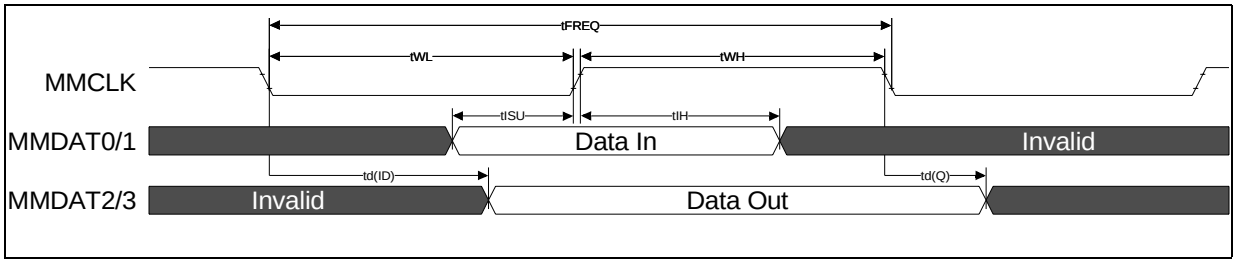


Table 52: SD/SDIO Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
t_{FREQ}	MMCLK Frequency Data Transfer Mode	0	19.5	MHz	
t_{FREQ}	MMCLK Frequency Identification Mode	0[1]/100	400	KHz	
t_{WH}	Clock high time	50	—	ns	
t_{WL}	Clock low time	50	—	ns	
t_{rise}	Clock rise time	—	10	ns	2
t_{fall}	Clock fall time	—	10	ns	2
t_{ISU}	Data input setup time	5	—	ns	
t_{IH}	Data input hold time	5	—	ns	
$t_{d(Q)}$	Output Delay time during Data Transfer Mode	0	14	ns	
$t_{d(ID)}$	Output Delay time during Identification Mode	0	50	ns	

NOTES:
1. 0 KHz is when the clock is stopped. The minimum 100 KHz frequency range is where continuous clock is required.
2. Rise and fall times measured from 10% - 90% of voltage level.

§§

Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.752.9028

www.marvell.com

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