128Kx32 5V FLASH MODULE *PRELIMINARY**

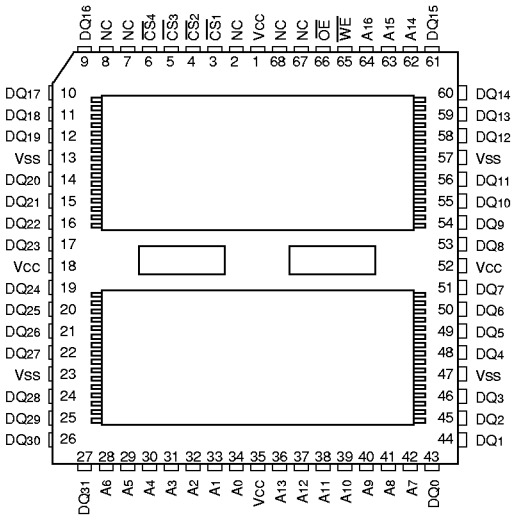
FEATURES

- Maximum Access Time of 55ns
- Packaging
  - 68 Lead, Plastic PLCC, 24.94 mm (0.982 inch) square
- Sector Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Minimum 100,000 Write/Erase Cycles
- Organized as 128Kx32
- Commercial and Industrial Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply
- Low Power CMOS, 500µA Standby Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time
- Built-in Decoupling Caps for Low Noise Operation

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION FOR WPF128K32-55PJX5

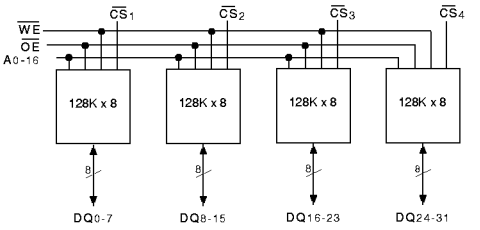
TOP VIEW



PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature (Com)	0 to +70	°C
Operating Temperature (Ind.)	-40 to +85	°C
Supply Voltage Range (V_{CC})	-2.0 to +7.0	V
Signal Voltage Range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-55 to +125	°C
Data Retention	10 years	
Endurance (write/erase cycles)	100,000 cycles min.	
A_9 Voltage for Sector Protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or DQ pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and DQ pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A_9 pin is -0.5V. During voltage transitions, A_9 may overshoot Vss to -2V for periods of up to 20ns. Maximum Dc input voltage on A_9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.
4. **Recommended soldering temperature not to exceed 215°C for 20 seconds.**

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Com)	T_A	0	+70	°C
Operating Temp. (Ind)	T_A	-40	+85	°C
A_9 Voltage for sector Protect	V_{ID}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	35	pF
$\overline{WE}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	12	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	12	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	35	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	-55		Unit
			Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = Vss to Vcc		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = Vss to Vcc		10	µA
Vcc Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		120	mA
Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		200	mA
Vcc Standby Current	I_{CC3}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}, f = 5MHz		500	µA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x Vcc		V
Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	Vcc -0.4		V
Low Vcc Lock Out Voltage	V_{LKO}		3.2		V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol		-55		Unit
			Min	Max	
Write Cycle Time (1)	t_{AVAV}	t_{WC}	55		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	30		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		ns
Data Setup Time	t_{DVWH}	t_{DS}	20		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		ns
Write Enable Pulse Width High (1)	t_{WHWL}	t_{WPH}	20		ns
Duration of Byte Programming Operation	t_{WHWH1}		14		µs
Sector Erase Time	t_{WHWH2}		2.2	30	sec
Read Recovery Time Before Write (1)	t_{GHWL}		0		µs
Vcc Setup Time (1)		t_{VCS}	50		µs
Chip Programming Time				12.5	sec
Output Enable Setup Time		t_{OES}	0		ns
Output Enable Hold Time (2)		t_{OEH}	10		ns
Chip Erase Time				120	sec

1. Guaranteed by design but not tested.
2. For Toggle and $\overline{Data}$ Polling.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol		-55		Unit
			Min	Max	
Write Cycle Time (1)	t_{AVAV}	t_{WC}	55		ns
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0		ns
$\overline{CS}$ Pulse Width	t_{ELEH}	t_{CP}	30		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		ns
Data Setup Time	t_{DVEH}	t_{DS}	20		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		ns
$\overline{WE}$ Hold from $\overline{WE}$ High	t_{EHWH}	t_{WH}	0		ns
$\overline{CS}$ Pulse Width High	t_{EHEL}	t_{CPH}	20		ns
Duration of Programming Operation	t_{WHWH1}		14		µs
Sector Erase Operation	t_{WHWH2}		2.2	30	sec
Read Recovery Before Write	t_{GHEL}		0		ns
Chip Programming Time				12.5	sec
Chip Erase Time				120	sec

1. Guaranteed by design but not tested.

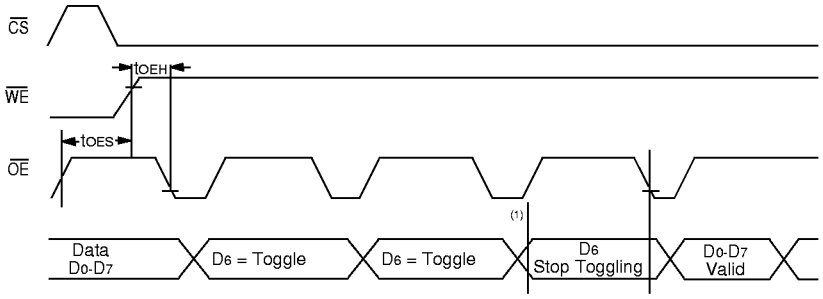
AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol		-55		Unit
			Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	55		ns
Address Access Time	t_{AVQV}	t_{ACC}		55	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		55	ns
$\overline{OE}$ to Output Valid	t_{GLQV}	t_{OE}		30	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		15	ns
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		15	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		ns

1. Guaranteed by design, not tested.

FIG. 2
AC WAVEFORMS FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS



NOTES:
1. D_6 stops toggling (the device has completed the Embedded operation).

FIG. 3
AC WAVEFORMS FOR READ OPERATIONS

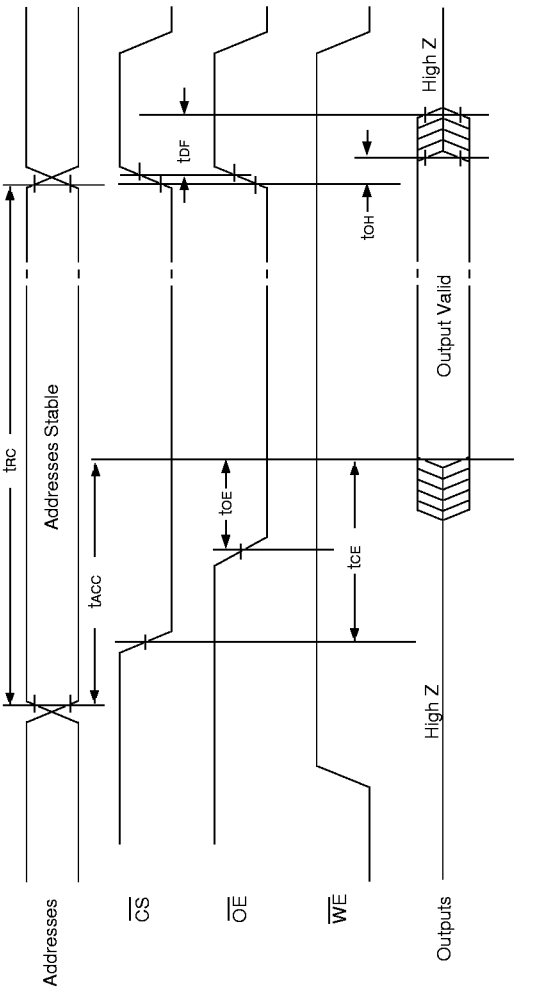
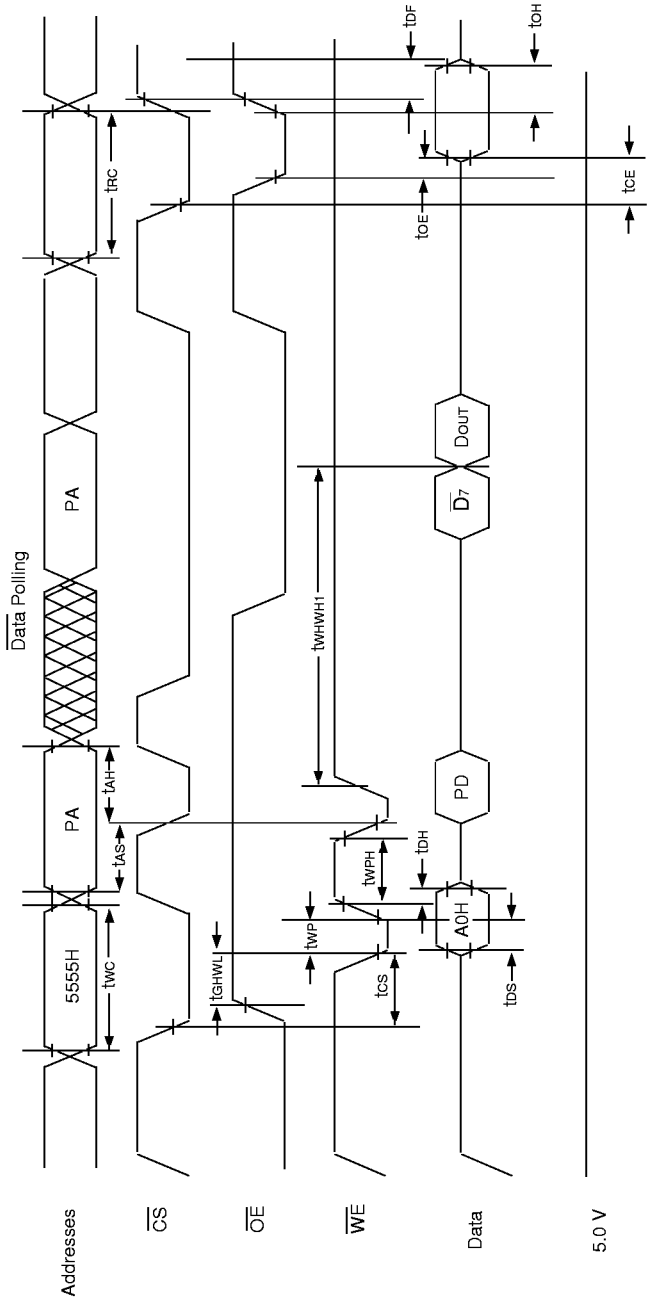
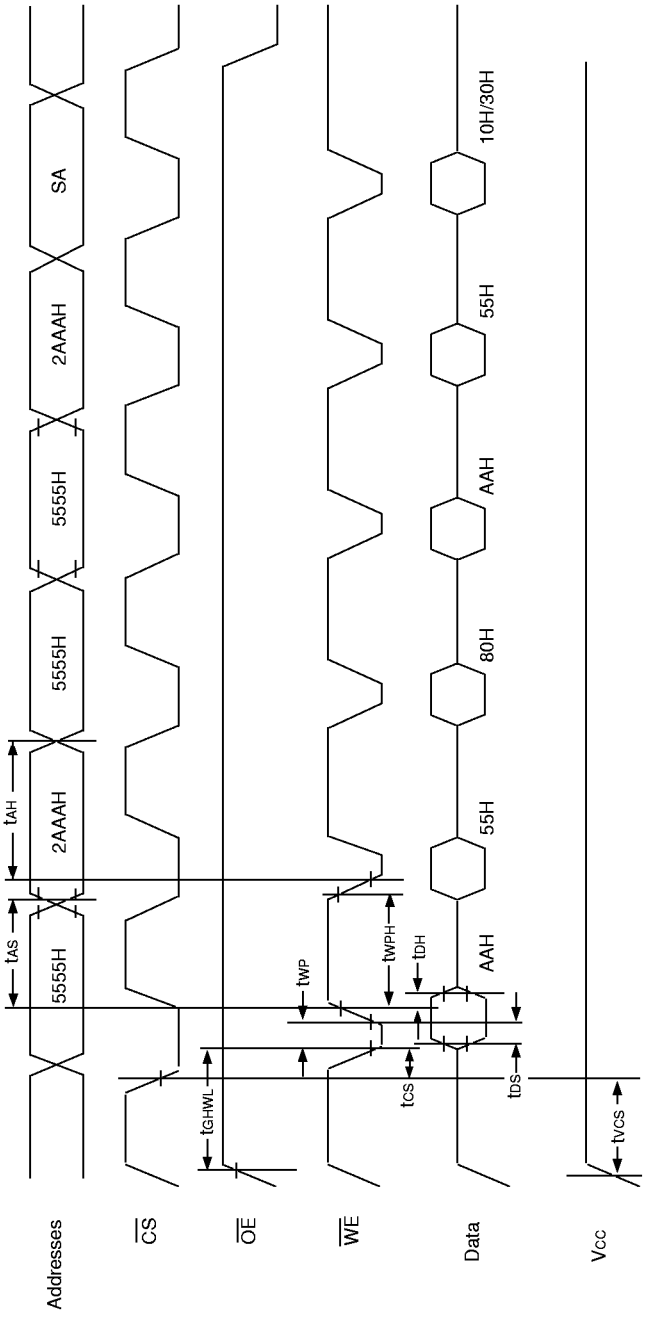


FIG. 4
WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIG. 5
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTES:
1. SA is the sector address for sector Erase.

FIG. 6
AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

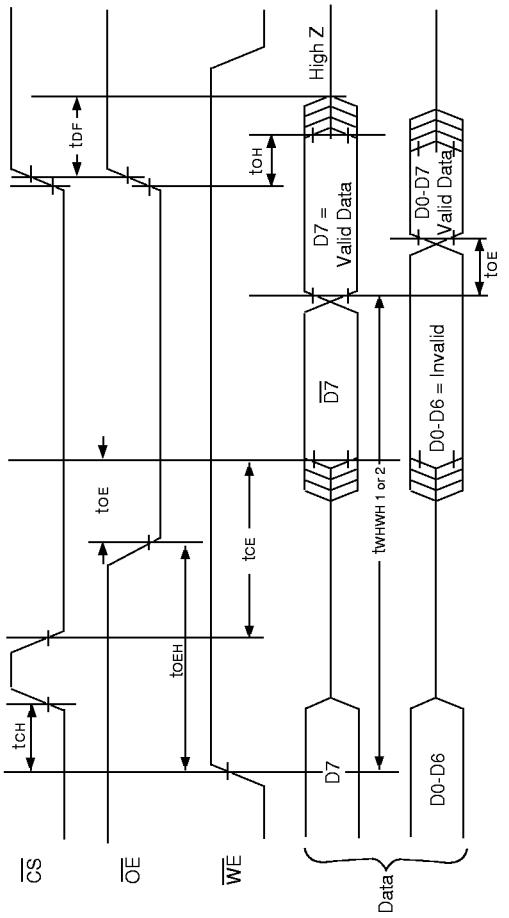


FIG. 7
WRITE/ERASE/PROGRAM OPERATION, $\overline{CS}$ CONTROLLED

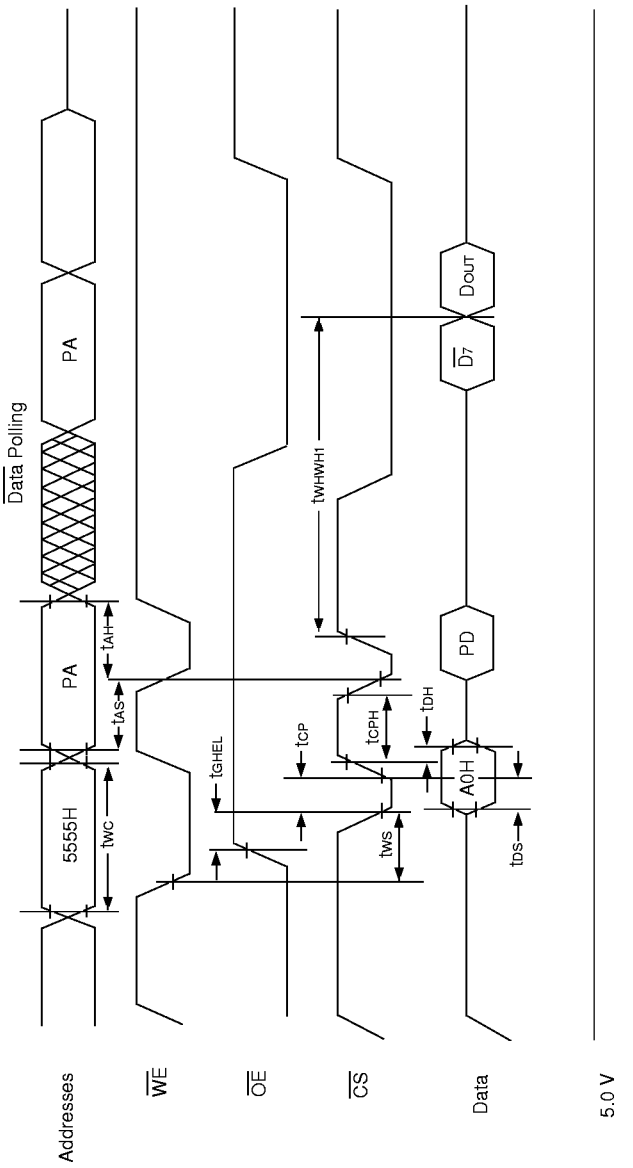


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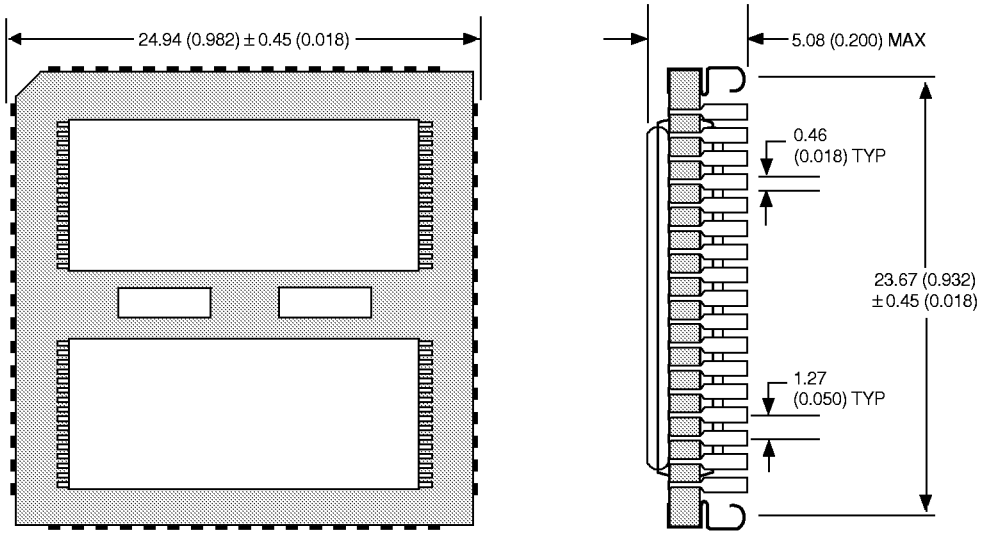
FIG. 8
PACKAGE DIMENSIONS



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P F 128K32 - 55 PJ X 5

V_{PP} PROGRAMMING VOLTAGE
5 = 5V

DEVICE GRADE:
C = Commercial 0 to +70°C
I = Industrial -40 to +85°C

PACKAGE TYPE:
PJ = 68 Lead Plastic PLCC

ACCESS TIME (ns)

ORGANIZATION, 128K x 32
User configurable as 256K x 16 or 512K x 8

Flash PROM

Plastic Multichip Module

WHITE MICROELECTRONICS