1-kBit Read/Write Contactless Identification Device

Features

- 1 kBit of EEPROM organized in 32 words of 32 bits
- 32 bit device serial number (read only laser ROM)
- 32 bit device identification (read only laser ROM)
- Power-on reset sequence
- Power-check for EEPROM write operation
- User defined read memory area at power-on
- User defined write inhibited memory area
- User defined read protected memory area
- Data transmission performed by amplitude modulation
- Two data rate options: 2 kBd (Opt64) or 4 kBd (Opt32) Bit period = 64 or 32 periods of field frequency
- 170 pF ± 3% on-chip resonant capacitor
- −40 to +85°C temperature range
- 100 to 150 kHz field frequency range
- On-chip rectifier and voltage limiter
- No external supply buffer capacitance needed due to low power consumption

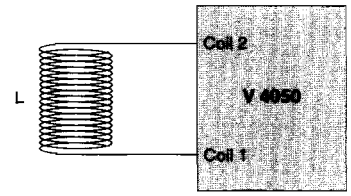
Description

The V 4050 is a CMOS integrated circuit for use in electronic read/write RF transponders. The chip contains 1 kBit of EEPROM which can be configured by the user, allowing a write inhibited area, a read protected area, and a read area output continuously at power-on. The memory can be secured by using the 32 bit password for all write and read protected operations. The password can be updated, but never read. The fixed code serial number and device identification are laser programmed making every chip unique. The V 4050 will transmit data to the transceiver by modulating the amplitude of the electromagnetic field, and receive data and commands in a similar way. Simple commands will enable write to EEPROM, to update the password, to read a specific memory area, and to reset the logic. The coil of the tuned circuit is the only external component required, all remaining functions are integrated in the chip.

Applications

- Ticketing
- Automotive immobilizer with rolling code
- High security hands-free access control
- Industrial automation with portable database
- Manufacturing automation
- Prepayment devices

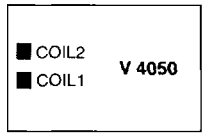
Typical Operating Configuration



Typical value of inductance at 125 kHz is 9.5 mH

Fig. 1

Pin Assignment



COIL 1 coil terminal / clock input
COIL 2 coil terminal

Fig. 2

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Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak current induced on COIL1 and COIL2	I_{COIL}	± 30 mA
Power supply	V_{DD}	−0.3 to 9.5 V
Max. voltage other pads	V_{max}	V_{DD} + 0.3 V
Min. voltage other pads	V_{min}	V_{SS} − 0.3 V
Storage temperature	T_{STORE}	−55 to +125° C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	1000 V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Maximum coil current	I_{COIL}			10	mA
AC voltage on coil	V_{COIL}		18*		V_{PP}
Supply frequency	f_{COIL}	100		150	kHz

* The AC voltage on coil is limited by the on-chip voltage limitation circuitry.

Table 2

System Principle

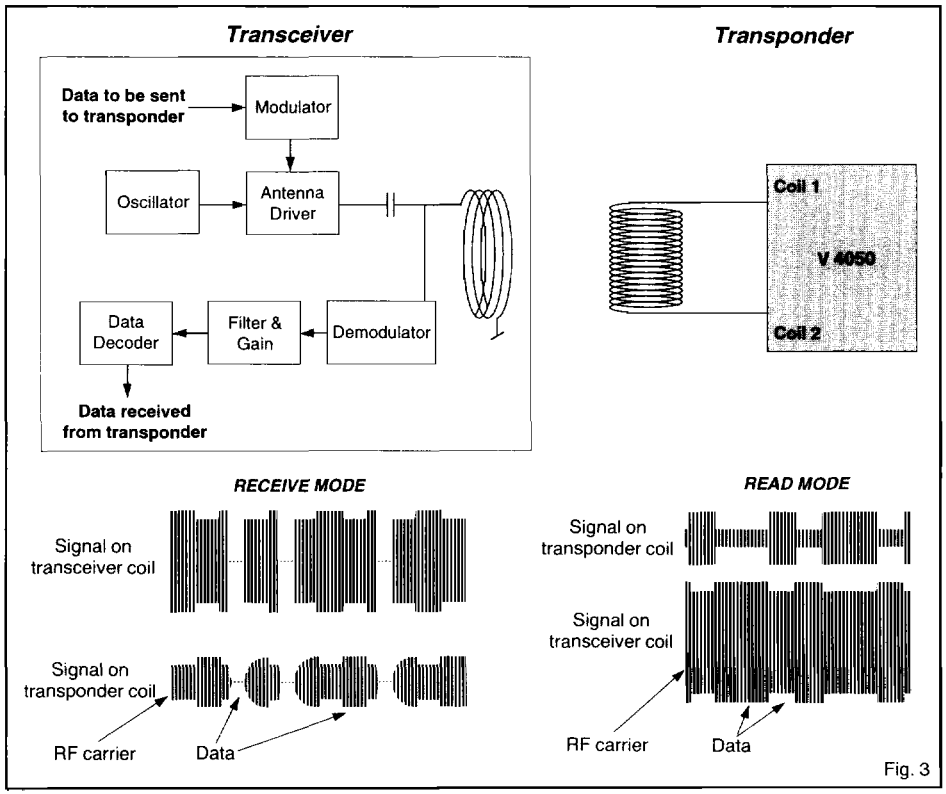

Fig. 3

Electrical Characteristics

V_{DD} = 2.5 V, V_{SS} = 0 V, f_{COIL} = 125 kHz sine wave, V_{COIL} = 1 V_{PP}, T_A = 25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}		2.0		[1]	V
Min. EEPROM write voltage	V_{DDee}		3.0			V
Power-check EEPROM write	$I_{PWcheck}$	$V_{(COIL1\ \ VSS)}$ = 5 V, V_{DD} = 5 V			80	µA
	$V_{PWcheck}$	$V_{(COIL1\ \ VSS)}$ applied for PWR check ok, V_{DD} = 5 V			6	V
Supply current / read	I_{RD}	Read mode		2.0	5.0	µA
Supply current / write	I_{WR}	Write mode (V_{DD} = 3 V)		40	70	µA
Modulator on voltage drop	V_{ON}	$V_{(COIL1\ \ VSS)}$ and $V_{(COIL2\ \ VSS)}$, I_{COIL} = 100 µA			0.50	V
		$V_{(COIL1\ \ VSS)}$ and $V_{COIL2\ \ VSS)}$, I_{COIL} = 5 mA			2.50	V
Resonance capacitor	C_R		165	170	175	pF
Power-on reset level high	V_{PRH}	Rising supply		2.2	2.8	V
Clock extractor input min.	V_{CLKmin}	Minimum voltage for clock extraction	1.0			V_{PP}
Clock extractor input max.	V_{CLKmax}	Maximum voltage to detect modulation stop			50	mV_{PP}
EEPROM data endurance	N_{CY}	Erase all / write all at V_{DD} = 7 V	100'000			cycles
EEPROM retention	T_{RET}	T_A = 55°C after 100'000 cycles [2]	10			years

[1] Maximum voltage is defined by forcing 10 mA on Coil 1 - Coil 2
[2] Based on 1'000 hours at 150°C

Table 3

Timing Characteristics

V_{DD} = 2.5 V, V_{SS} = 0 V, f_{COIL} = 125 kHz sine wave, V_{COIL} = 1 V_{PP}, T_A = 25°C, unless otherwise specified
All timings are derived from the field frequency and are specified as a number of RF periods

Parameter	Symbol	Test Conditions	Value	Units
Option: 64 clocks per bit	**OPT64**			
Read bit period	t_{RDB}		64	RF periods
LIW/ACK/NACK pattern duration	t_{PATT}		320	RF periods
Read 1 word duration	t_{RDW}	Including LIW	3200	RF periods
Processing pause time	t_{PP}		64	RF periods
Write access time	t_{WA}		64	RF periods
Initialization time	t_{INIT}		2112	RF periods
EEPROM write time	t_{Wee}	V_{DD} = 3 V	3200	RF periods
Option: 32 clocks per bit	**OPT32**			
Read bit period	t_{RDB}		32	RF periods
LIW/ACK/NACK pattern duration	t_{PATT}		160	RF periods
Read 1 word duration	t_{RDW}	Including LIW	1600	RF periods
Processing pause time	t_{PP}		32	RF periods
Write access time	t_{WA}		32	RF periods
Initialization time	t_{INIT}		1056	RF periods
EEPROM write time	t_{Wee}	V_{DD} = 3 V	2624	RF periods

Table 4

RF periods represent periods of the carrier frequency emitted by the transceiver unit. For example, if 125 kHz is used:
The read bit period (Opt64) would be: 1/125'000*64 = 512 µs, and the time to read 1 word: 1/125'000*3200 = 25.6 ms
The read bit period (Opt32) would be: 1/125'000*32 = 256 µs, and the time to read 1 word: 1/125'000*1600 = 12.8 ms

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Block Diagram

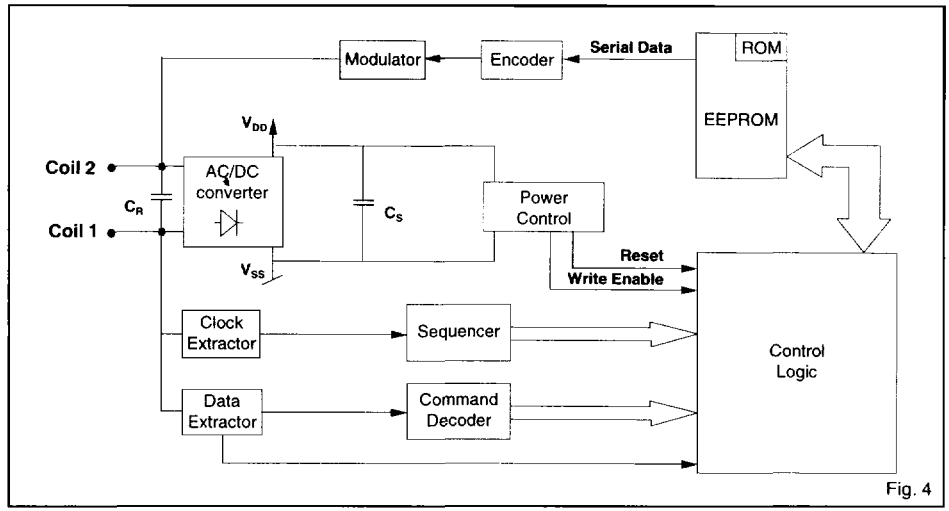

Fig. 4

Pad Description

Pad	Name	Function
1	COIL1	Coil terminal 1
2	TEST_IN	Test input with pull-down
3	V_{DD}	Positive internal supply voltage
4	V_{SS}	Negative internal supply voltage
5	TEST	Test mode input with pull-down
6	TEST_OUT	Test output
7	TEST_CLK	Test clock input with pull-down
8	CAP_TRIM1	Capacitor trimming 1
9	CAP_TRIM2	Capacitor trimming 2
10	CAP_TRIM3	Capacitor trimming 3
11	COIL2	Coil terminal 2

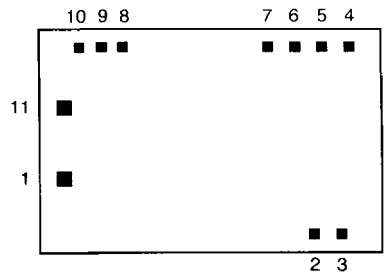

Table 5

Functional Description

General

The V 4050 is supplied by means of an electromagnetic field induced on the attached coil. The AC voltage is rectified in order to provide a DC internal supply voltage. When the DC voltage crosses the power-on level, the chip enters the standard read mode and sends data continuously. The data to be sent in this mode is user defined by storing the first and last addresses to be output. When the last address is sent, the chip will continue with the first address until the transceiver sends a request. In the read mode, a listen window (LIW) is generated before each word. During this time, the V 4050 will turn to the receive mode (RM) if it receives a valid RM pattern. The chip then expects a valid command.

Mode of Operation

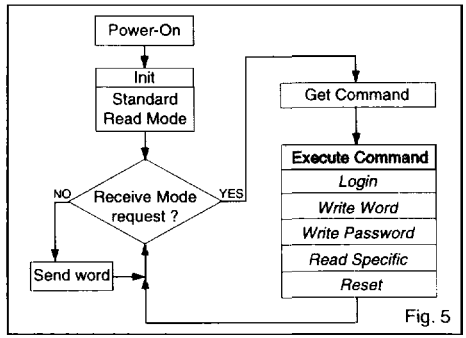

Fig. 5

Memory Organization

The 1024 bit EEPROM is organized in 32 words of 32 bits. The first three words are assigned to the password, the protection word, and the control word. In order to write one of these three words, it is necessary to send the valid password. At fabrication, the V 4050 comes with all bits of the password programmed to a logic "0". The password cannot be read out. The memory contains two extra words of laser ROM. These words are laser programmed during fabrication for every chip, are unique and cannot be altered.

Memory Map

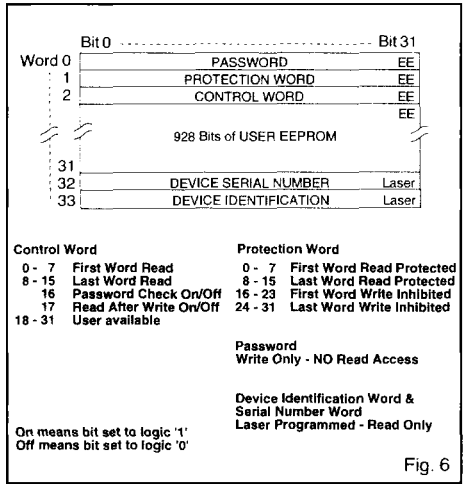

Fig. 6

Standard Read Mode

After a power-on reset and upon completion of a command, the chip will execute the standard read mode, in which it will send data continuously, word by word from the memory section defined between the first word read (FWR) and last word read (LWR). When the last word is output, the chip will continue with the first word until the transceiver sends a request. If FWR and LWR are the same, the same word will be sent repetitively. The listen window (LIW) is generated before each word to check if the transceiver is sending data. The LIW has a duration of 320 periods (Opt64) / 160 periods (Opt32) of the RF field. FWR and LWR have to be programmed as valid addresses (FWR ≤ LWR ≤ 33). The words sent by the V 4050 comprise 32 data bits and parity bits. The parity bits are not stored in the EEPROM, but generated while the message is sent as described below. The parity is even for rows and columns, meaning that the total number of "ones" is even (including the parity bit).

Word Organization (Words 0 to 32)

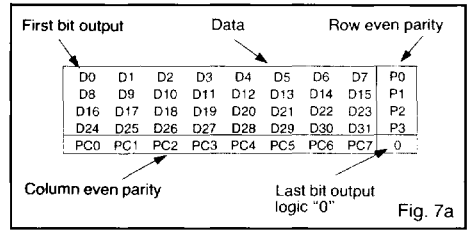

Fig. 7a

When a word is read protected, the output will consist of 45 bits set to logic "0". The password has to be used to output correctly a read protected memory area.

Word Organization (Word 33)

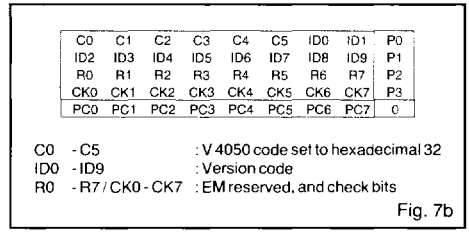

Fig. 7b

Read Sequence

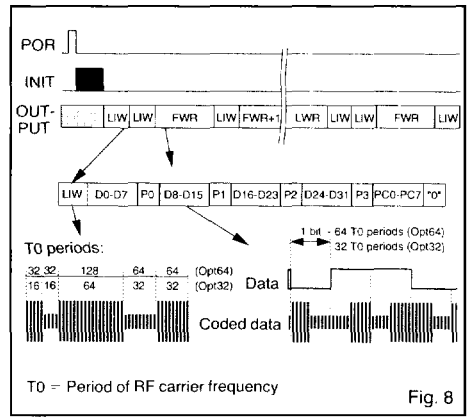

Fig. 8

Receive Mode

To activate the receive mode, the transceiver sends to the chip the RM pattern (while in the modulated phase of a listen window LIW). The V 4050 will stop sending data upon reception of a valid RM. The chip then expects a command. The RM pattern consists of 2 bits "0" sent by the transceiver. The first bit "0" transmitted is to be detected during the 64 periods / 32 periods (Opt64 / Opt32) where the modulation is "ON" in LIW.

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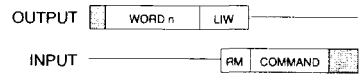


RM : Two consecutive bits set to logic "0"

Fig. 9

Commands

The commands are composed of nine bits: eight data bits and one even parity bit (total amount of "ones" is even including the parity bit).

COMMAND BITS	*FUNCTION*
0 0 0 0 0 0 0 1 1	LOGIN
0 0 0 1 0 0 0 1 0	WRITE PASSWORD
0 0 0 1 0 0 1 0 0	WRITE WORD
0 0 0 0 1 0 1 0 0	SELECTIVE READ MODE
1 0 0 0 0 0 0 0 1	RESET

First bit received

Parity bit

Fig. 10

Selective Read Mode

The selective read mode is used to read other data than that defined between FWR and LWR. To enter selective read mode, the transceiver has to send during LIW a receive mode pattern (RM) to convert the V 4050 into receive mode. Then the selective read mode command is sent by the transceiver followed by the first and last addresses to be read. The FWR and LWR are then replaced by the new addresses and the chip is operating in the same way as the standard read mode. The control word is not modified by this command, and the next standard read mode operation will work with the original FWR and LWR (selected area is read once and then the chip returns to standard read mode). To read words which are read protected, a login command has to be sent by the transceiver prior to the selective read command. The login command is to be used only once for all subsequent commands requiring a password. The selective read mode command is followed by a single 32-bit word containing the new first and last addresses. Bits 0 to 7 correspond to the first word read and bits 8 to 15 correspond to the last word read. Bits 16 to 31 have to be sent but are not used in the chip. The parities must be sent according to the word organization as described in Fig. 7. Note that bit 31 is transmitted first. To read the device identification or the serial number, the selective read command allows direct access to the laser programmed words. These words can also be addressed in the standard read mode by selecting the addresses accordingly.

Selective Read Command

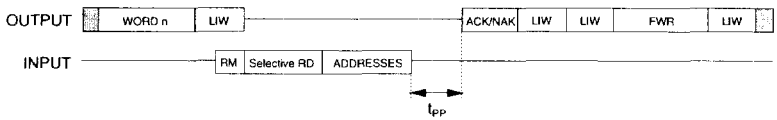


Fig. 11

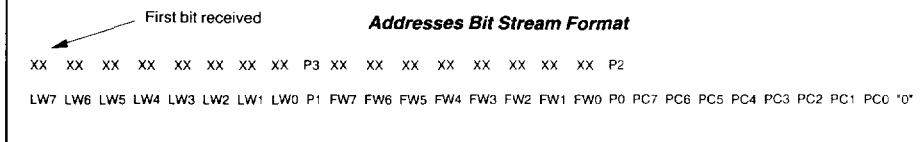


Fig. 12

Reset Command
The reset command will return from any mode to the standard read mode. The next word out is the FWR.

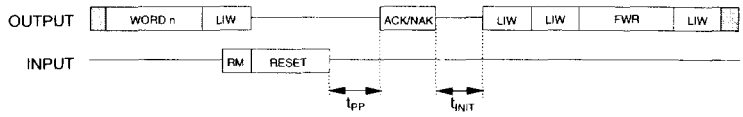


Fig. 13

Login
The login command is used to access protected memory areas. This command has to be used only once to perform several password protected commands. The power-on sequence and the reset command will reset the password entry, and a new login command has to be received to perform further password protected operations. Upon reception of a correct password, the V 4050 will respond with an acknowledge pattern (ACK) and then continue in standard read mode. If the login is correct then the password protected operations are allowed. If the password is incorrect, a NAK pattern is issued and password protected operations will not be possible (refer to write word for password data structure).

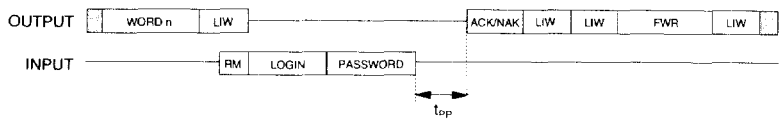


Fig. 14

If bit 16 of the control word is disabled (password check ON/OFF), the login is still mandatory to modify the protection word, the control word, and the password, but not to write in the EEPROM which is not write inhibited. In order to modify a write inhibited word, the protection word has to be modified first. The read protected area always requires the login to be read. If the write protection word is write protected, the write protection configuration is locked.

Write Password
When a write password command is received, the chip next expects information on the actual valid password. The chip sends back an ACK pattern if the password is correct. Then the chip expects the new password consisting of 32 bits + parity bit to be stored in the EEPROM. The chip will respond with an ACK pattern for a correct reception of data upon reception of the new password, and then will send another acknowledge pattern (ACK) to announce that the data is stored in the EEPROM. The read after write function has no effect on this command. If the password is wrong or the transmission is faulty, the chip will: send a NAK pattern; return to the standard read mode; and, the password will remain the same (refer to write word for password data structure).

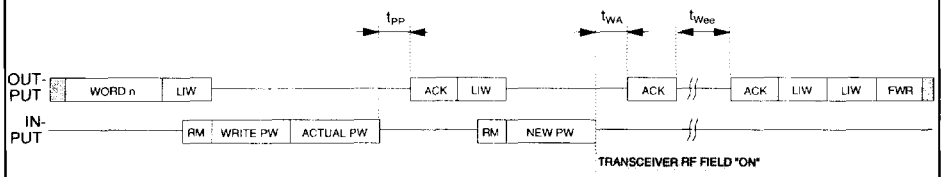


Fig. 15

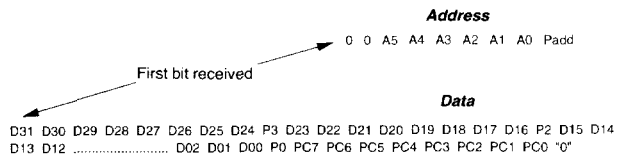
Write Word

The write mode allows modification of the EEPROM contents word by word. To modify address 1 (protection word) and address 2 (control word), it is mandatory to first send a login command in order to log in (like in a computer). The new written values will take effect only after performing a reset command. It is strongly recommended to check the result of modifying the contents of these addresses effecting the function of the chip. Address 0 (password) cannot be modified with this command but can be changed with the write password command. Addresses 3 to 31 are programmable according to the defined protections. If the password check bit is off (bit 16 of control word) and the word is not write inhibited, the selected word can be freely modified without password. If the password check bit is on and the word is not write inhibited, the selected word can be modified with a previous login. In any case, if the word is write inhibited, the protection word has to be changed before programming can occur.

Write to Address	Check Password Bit (bit 16/ Control Word	Write Inhibit (Protection Word)	Write Operation
0	X	X	Only with write password command
1 - 2	X	OFF	Login always required
1 - 2	X	ON	Write configuration LOCKED
3 - 31	OFF	OFF	Freely programmable
3 - 31	ON	OFF	Login required
3 - 31	X	ON	Change protection word first

Table 6

The write word command is followed by the address and data. The address consists of a 9 bit block containing 8 data bits and 1 even parity bit. Only 6 bits from the data section are used for the word addressing, and the first three bits sent must be "0". The data consists of 4 times 9 bit blocks, each block consisting of 8 data bits and 1 associated even parity bit and one additional block consisting of 8 column parity bits and "0" as stop bit (refer to Fig. 7).



Note: A5 in write mode always "0" (addresses laser ROM)

Fig. 16

After reception he command, the address, and the data, the V 4050 will check the parity, the write protection status, the login status, and also if the available power from the RF field is sufficient. If all the conditions are satisfied, an acknowledge pattern (ACK) will be issued afterwards and the EEPROM writing process will start. At the end of programming, the chip will send an acknowledge pattern (ACK). If at least one of the checks fails, the chip will issue a no acknowledge pattern (NAK) instead of ACK and return to the standard read mode. The transceiver will keep the RF field permanently "ON" during the whole writing process time.
The read after write function (bit 17 of control word) controls the mode of operation following a write operation. When "ON", the latest written word will be read out and output next to the ACK pattern and two listen windows (LIW-LIW) even if the word is read protected. When "OFF", the ACK is followed immediately by a LIW-LIW and FWR. The last written word is not output. If a request from the transceiver to return in receive mode (RM) is generated during the LIW, another word can be written in. Otherwise, the V 4050 will return in the standard read mode.

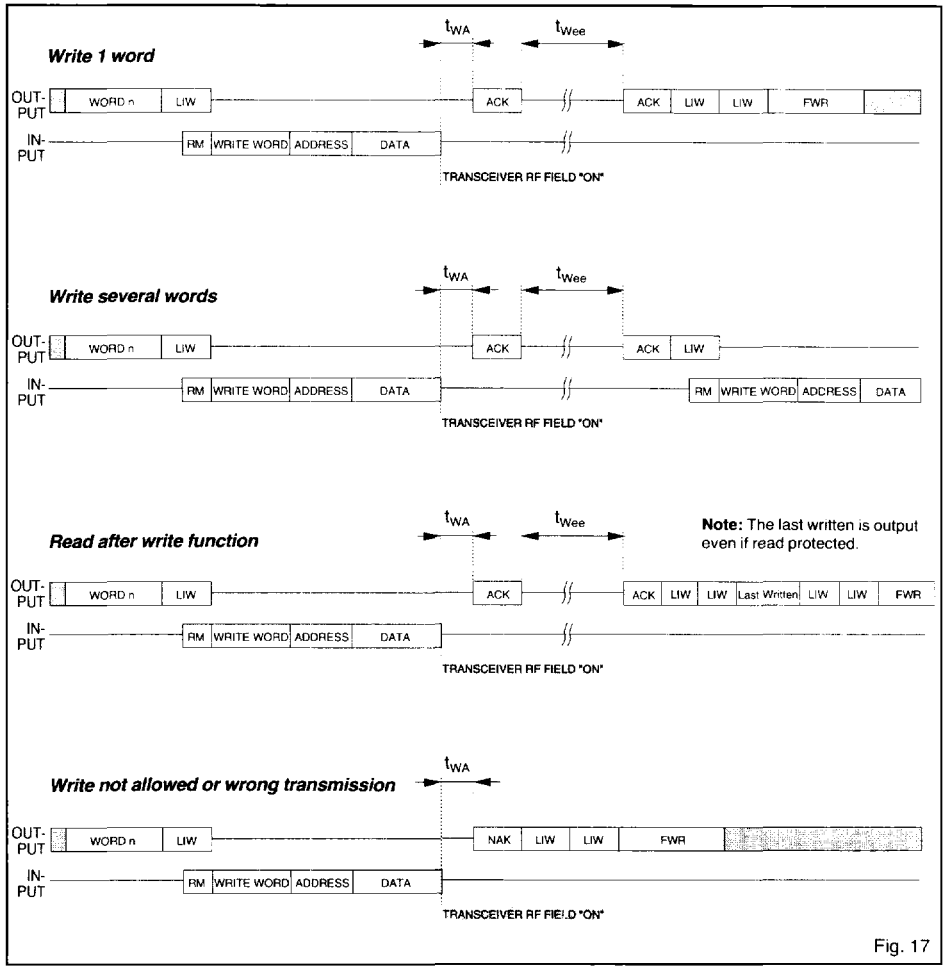


Fig. 17

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Power-on Reset (POR)

When the V 4050 with its attached coil enters an electromagnetic field, the built-in AC/DC converter will supply the chip. The DC voltage is monitored and a reset signal is generated to initialize the logic. The contents of the control word and protection word will be down-loaded to enable the functions (INIT). The power-on reset is also provided in order to make sure that the chip will start issuing correct data. Hysteresis is provided to avoid improper operation at the limit level.

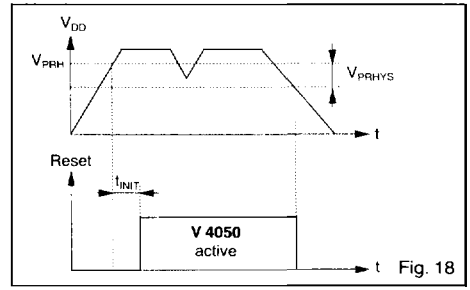


Fig. 18

Lock All / Lock Memory Area
The V 4050 can be converted to a read-only chip or be configured to read/write and read-only areas by programming the protection word. This configuration can be locked by write inhibiting the write protection word. Great care should be taken in doing this operation as there is no further possibility to change the write protection word. The control word can also be protected in the same way, thus freezing the operation mode.

Clock Extractor
The clock extractor will generate a system clock with a frequency corresponding to the frequency of the RF field. The system clock is used by a sequencer to generate all internal timings.

Data Extractor
The transceiver generated field will be amplitude modulated to transmit data to the V 4050. The data extractor demodulates the incoming signal to generate logic levels, and decodes the incoming data.

Modulator
The data modulator is driven by the serial data output from the memory which is Manchester encoded. The modulator will draw a large current from both coil terminals, thus amplitude modulating the RF field according to the memory data.

AC/DC Converter and Voltage Limiter
The AC/DC converter is fully integrated on-chip and will extract the power from the incident RF field. The internal DC voltage will be clamped to avoid high internal DC voltage in strong RF fields.

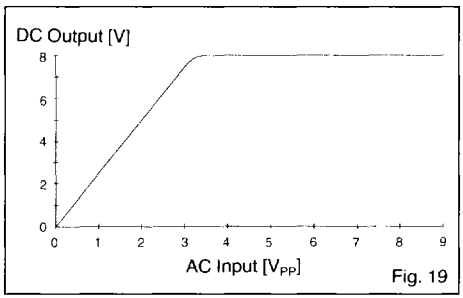


Fig. 19

Resonance Capacitor
The resonance capacitor is integrated, and its tolerance is adjusted to ± 3% over the whole production.

Typical Capacitor Variation Value versus Temperature

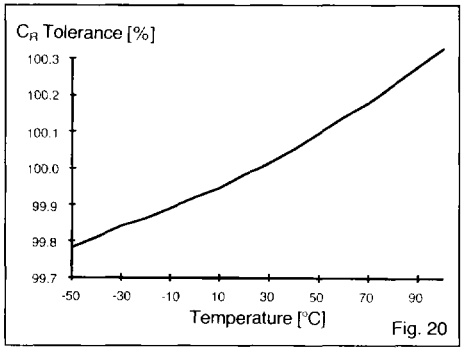


Fig. 20

Special Timings
The processing pause time (t_{PP}), write access time (t_{WA}) and EEPROM write time (t_{Wee}) are timings where the V 4050 is executing internal operations. During these pauses, the RF field will be influenced.

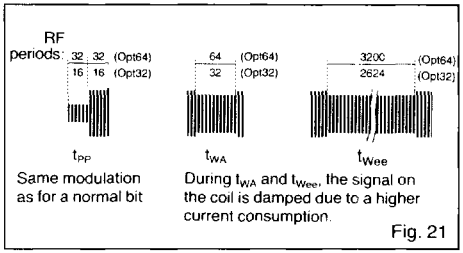


Fig. 21

Communication from the Transponder to the Transceiver (Read Mode)
The V 4050 modulates the amplitude of the RF field to transmit data to the transceiver. Data are output serially from the EEPROM and Manchester encoded.

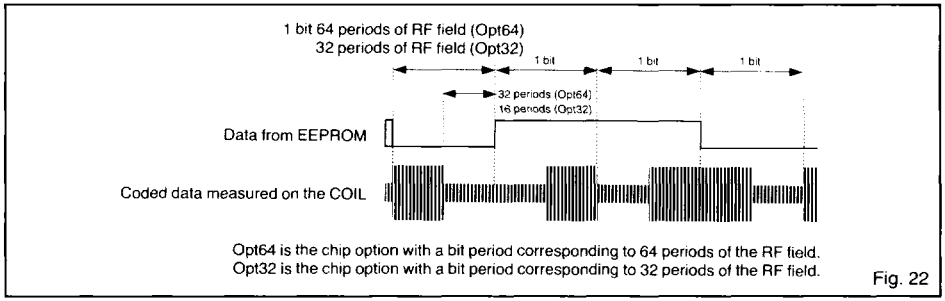
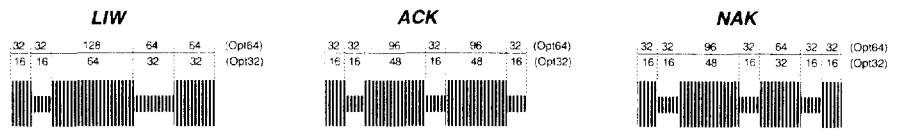


Fig. 22

The V 4050 uses different patterns to send status information to the transceiver. Their structure cannot be confused with a bit pattern sequence. These patterns are the listen window (LIW) to inform the transceiver that data can be accepted, the acknowledge (ACK) indicating proper communication and end of EEPROM write, and the no acknowledge (NAK) when something is wrong.
The LIW, due to its special structure, can be used to synchronize the transceiver during a read operation. The LIW is sent before each word, and is sent twice before FWR.



All numbers represent number of periods of RF field.
Opt64 is the chip option with a bit period corresponding to 64 periods of the RF field.
Opt32 is the chip option with a bit period corresponding to 32 periods of the RF field.

Fig. 23

Communication from the Transceiver to the Transponder (Receive Mode)
The V 4050 can be switched to the receive mode **only during a listen window**. The transceiver is synchronized with the incoming data from the transponder and expects a LIW before each word. During the phase where the chip has its modulator "ON" (64/32 periods of RF [Opt64/Opt32]), the transceiver has to send a bit "0". A certain phase shift in the read path of the transceiver can be accepted due to the fact that, when entering receive mode, the transceiver becomes the master.
At reception of the first "0", the chip immediately stops the LIW sequence and then expects another bit "0" to activate the receive mode. Once the V 4050 has received the first bit "0", the transceiver is imposing the timing for synchronization. The V 4050 turns "ON" its modulator at the beginning of each frame of a bit period. To send a logic "1", the transceiver continues to send clocks without modulation. Half a bit period later, the modulation device of the V 4050 is turned "OFF" allowing recharge of the internal supply capacitor. To send a logic "0", the transceiver stops sending clocks (100% modulation) during the first half of a bit period. The transceiver must not turn "OFF" the field earlier than clock 1 of the bit period. It is recommended to turn "OFF" the field after 7/4 clocks of the bit period (Opt64/Opt32). The field is stopped for the remaining first half of the bit period, and then turned "ON" again for the second half of the bit period. The 32nd/16th clock (Opt64/Opt32) defines the end of the bit.
To ensure synchronization between the transceiver and the transponder, a logic bit set to "0" has to be transmitted at regular intervals. The RM pattern consists of two bits set to "0", thus allowing initial synchronization. In addition, the chosen data structure contains even parity bits which will not allow more than eight consecutive bits set to logic "1" where no modulation occurs.
While the transceiver is sending data to the transponder, two different modulations will be observed on both coils. During the first half of the bit period, the V 4050 is switching "ON" its modulation device causing a modulation of the RF field. This modulation can also be observed on the transceiver's coil. The transceiver sending a bit "0" will switch "OFF" the field, causing a 100% modulation being observed on the transponder coil.

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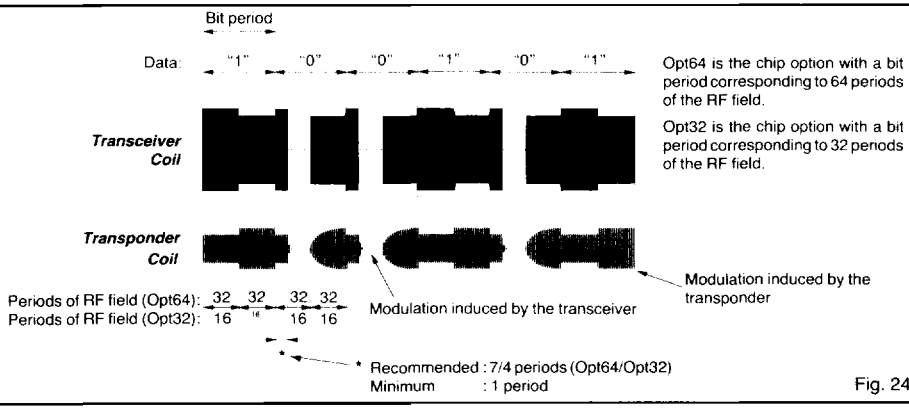
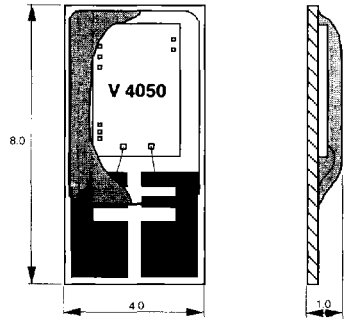


Fig. 24

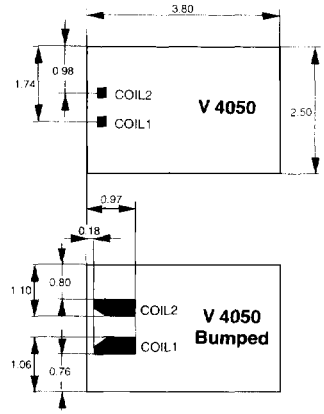
Package and Ordering Information

Dimensions of PCB Version



Dimensions in mm — Fig. 25

Chip Dimensions



IC thickness: 280 μm $\pm$ 25 μm
Bump height: 25 μm $\leq$ 5 μm

Dimensions in mm — Fig. 26

Ordering Information

The V 4050 is available in chip form:
without bumps V 4050 IC
or with bumps V 4050 bumped IC

Specify data rate option as:
Opt64 - 64 clocks bit period
Opt32 - 32 clocks bit period

For sampling the following versions are available:
PCB V 4050 COB 8040/2 EM 2286