TFEC0410G 2.5/10 Gbits/s Optical Networking Interface with Strong/Weak FEC and Digital Wrapper

1 Document Organization

This document is primarily intended for designers who require design implementation information and block interface specifications. This is a companion document to the TFEC0410G document group, which consists of the following documents:

- TFEC0410G Product Description
- TFEC0410G Operational Description
- TFEC0410G Hardware Register Memory Map
- TFEC0410G Hardware Design Guide
- TFEC0410G System Design Guide

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2 Device Overview

The following diagrams show simplified pictures of the major blocks and I/O information of the TFEC0410G device. The device has a flexible setup to allow for operation in terminal and regenerator applications. Figure 1 shows the device in 2.5 Gbits/s mode, and Figure 2 on page 7 shows the device in 10 Gbits/s mode. For convenience, two symbol sets are provided for the transmit and receive line and system interface pins, based on the mode of the device.

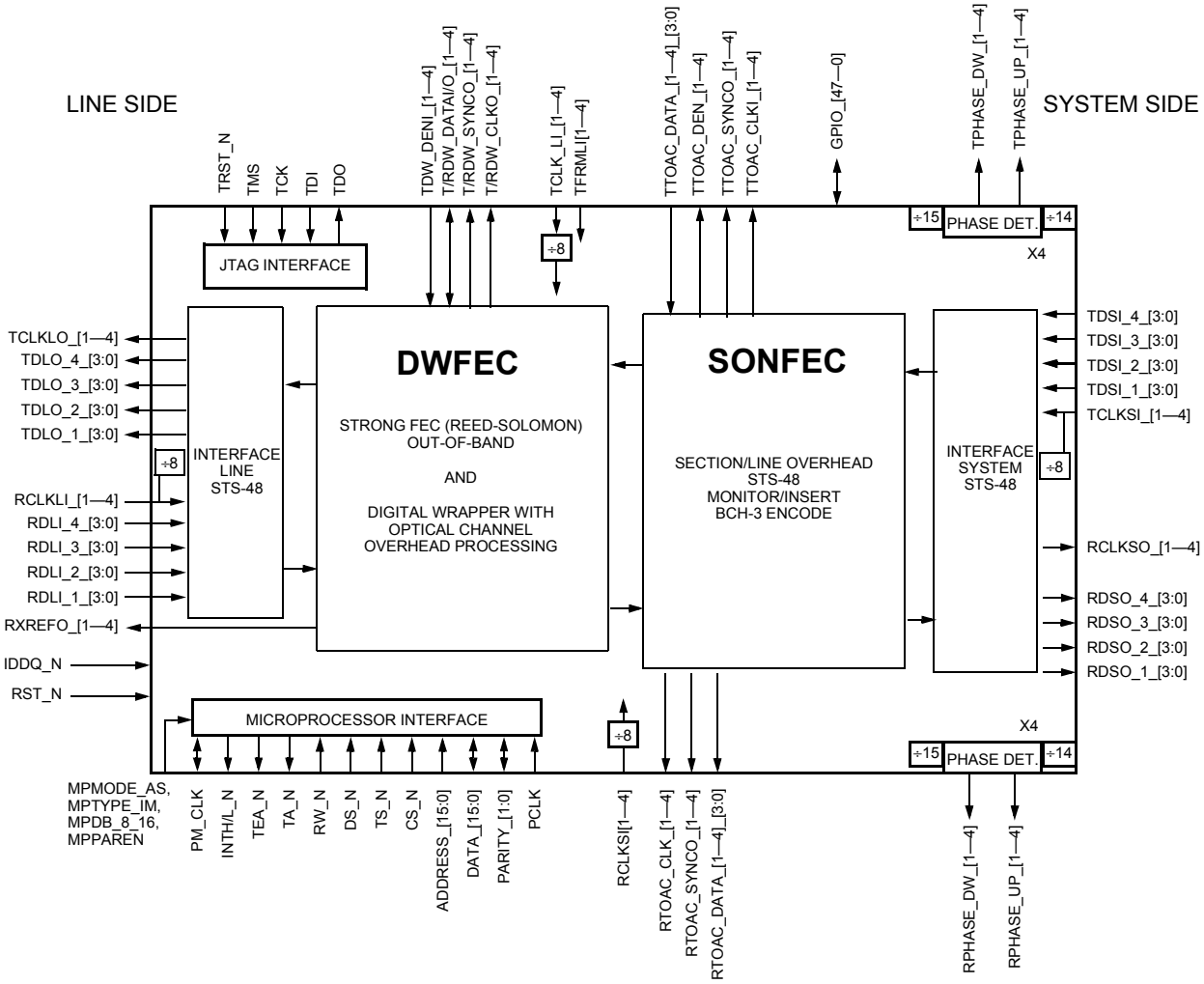


Figure 1. TFEC I/O Block Diagram—2.5 Gbits/s Mode

2 Device Overview (continued)

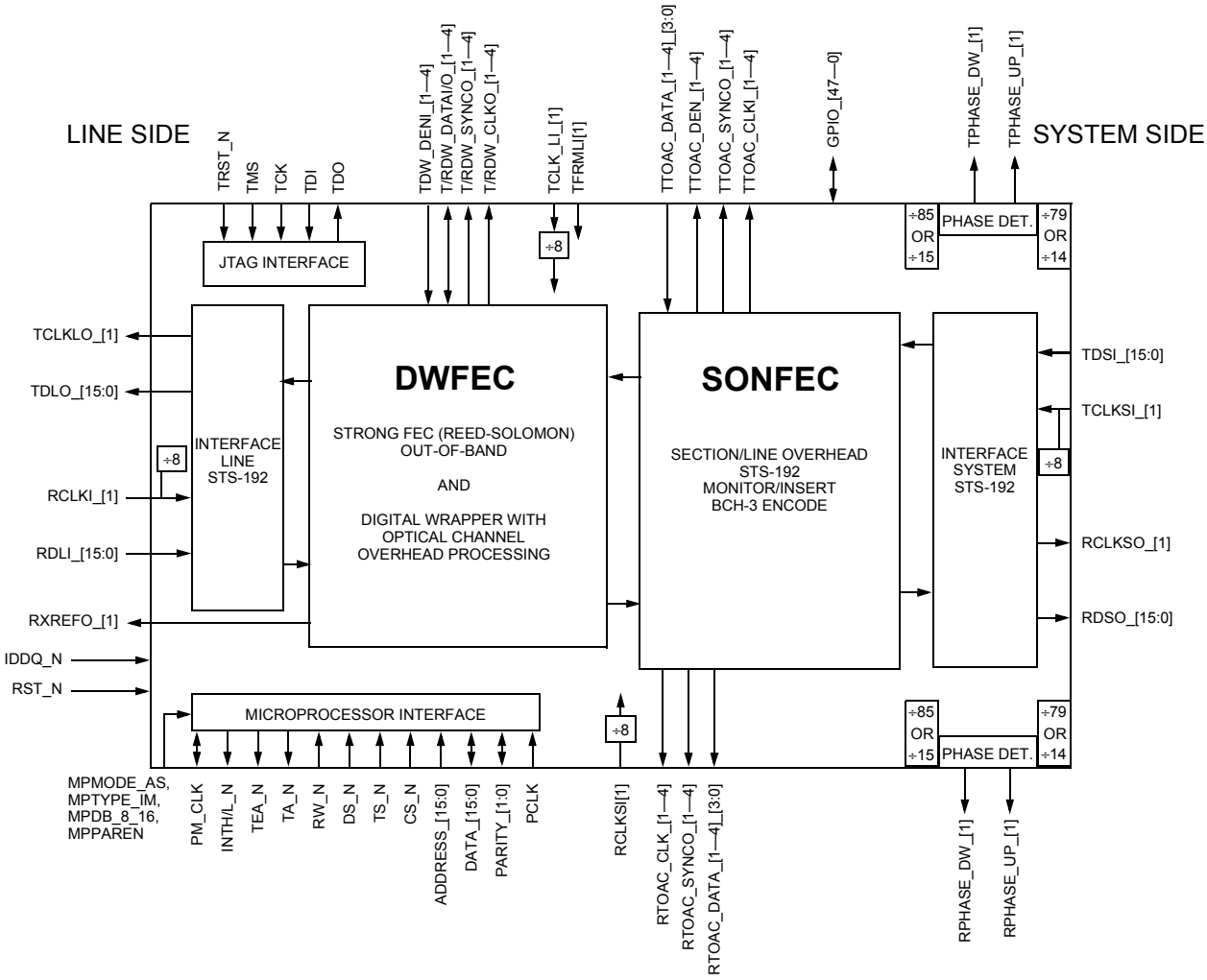


Figure 2. TFEC I/O Block Diagram—10 Gbits/s Mode

2 Device Overview (continued)

2.1 Device Modes Overview

The TFEC0410G has several functional modes to allow for operation in terminal and regenerator applications. Table 1, TFEC0410G Operating Modes, on page 8 outlines the system and line interface rate requirements in different applications. Other combinations which may be acceptable operating modes of the device can be programmed, but are not guaranteed to function error-free.

Table 1. TFEC0410G Operating Modes

Mode		Receive Interface		Transmit Interface	
		Rx—Line (Gbits/s)	Rx—System (Gbits/s)	Tx—System (Gbits/s)	Tx—Line (Gbits/s)
Strong FEC/Digital Wrapper—Terminal	10G	10.7 (10.66)	9.953	9.953	10.7 (10.66)
	Quad 2.5G	2.66	2.48	2.48	2.66
	GbE	11.05	10.312	10.312	11.05
Strong FEC/Digital Wrapper—Regenerator	10G	10.7 (10.66)	Internal Loopback		10.7 (10.66)
	Quad 2.5G	2.66	Internal Loopback		2.66
	GbE	11.05	Internal Loopback		11.05
Strong FEC or Digital Wrapper with Strong FEC—Bidirectional Mode	10G	10.7 (10.66)	10.7 (10.66)	10.7 (10.66)	10.7 (10.66)
	Quad 2.5G	2.66	2.66	2.66	2.66
Weak FEC—Terminal	10G	9.953	9.953	9.953	9.953
	Quad 2.5G	2.488	2.488	2.488	2.488
Weak FEC—Regenerator	10G	9.953	Internal Loopback		9.953
	Quad 2.5G	2.488	Internal Loopback		2.488
Strong/Weak—Terminal	10G	10.7 (10.66)	9.953	9.953	10.7 (10.66)
	Quad 2.5G	2.66	2.488	2.488	2.66
Strong/Weak —Regenerator	10G	10.7 (10.66)	Internal Loopback		10.7 (10.66)
	Quad 2.5G	2.66	Internal Loopback		2.66
Digital Wrapper/Weak —Terminal	10G	10.7 (10.66)	9.953	9.953	10.7 (10.66)
	Quad 2.5G	2.66	2.488	2.488	2.66
Asymmetric Multiplex Mode	10G ↔ Quad 2.5G	10.7 (10.66)/9.953	2.488	2.488	10.7 (10.66)/9.953
Single 2.5 Gbits/s Mode (16-Bit Line/System Interface)	2.5G ↔ 2.5G	2.66/2.488	2.66/2.488	2.66/2.488	2.66/2.488
Asymmetric: Strong/Digital Wrapper with/without Weak	10G → Quad 2.5G	10.7 (10.66)	Quad—2.488	9.953	Quad—2.66
Asymmetric—Weak	10G → Quad 2.5G	9.953	Quad—2.488	9.953	Quad—2.488
Asymmetric—Tx/Rx Directions	e.g., Rx = 10G Weak, Tx = Quad 2.5G Strong	9.953	9.953	2.488	2.66

Note: The number in parenthesis, when present, is the effectual rate due to no stuffing.

2 Device Overview (continued)

2.2 System Interface Overview

- The system interface block has the three following modes of operation:
  - One group of 16 bits at 622.08/666.51/669.32 Mbits/s for a 9.953 Gbits/s data rate.
  - Four groups of 4 bits at 622.08/666.51 Mbits/s for quad 2.488 Gbits/s.
  - One group of 16 bits at 155.52/166.63 Mbits/s.

This interface allows transmit-to-receive loopback.

Note: The system interface can run at other rates in strong FEC or digital wrapper mode. This rate is dependent on the system-side data rate, where this rate is 238/255 (14/15) or 237/255 (79/85) (10 Gbits/s mode with one fixed stuff column) of the line rate.

2.3 Section/Line Overhead Insert/Drop Overview (Figure 3)

The section/line overhead blocks accept four clocks and four 32-bit data streams in quad 2.5 Gbits/s mode, one clock and one 32-bit data stream in single 2.5 Gbits/s mode, or one clock and one 128-bit data bus in single STS-192/STM-64 mode. Serial TOAC channels for insert (4)/drop (4) of the transport overhead bytes are provided.

The section/line overhead block (Figure 3, SONET/SDH Line/Section Overhead Processing with BCH-3 Capability, on page 10) performs framing—normal/enhanced (OOF, LOF), loss-of-signal detection (LOS), scrambling/descrambling, time-slot interchange (TSI) (if necessary) (STS-192/STM-64 only), alignment FIFO (asymmetric multiplex mode only), internal monitoring/insertion of select section and line overhead bytes (J0, B1, F1, B2, K1/K2 (AIS-L, RDI-L), B2, S1, M1), and FEC status correction (FSI) (BCH-3 processing). Along with these monitoring/insert capabilities, the generation of AIS-L under hardware or software control is provided. Four BER algorithms are provided per stream (STS-48/STM-16 or STS-192/STM-64) to calculate signal fail (SF) and signal degrade (SD) conditions before and after BCH-3 error correction. The B1/B2 calculation (insert) monitor, scramble/descramble, transpose, alignment FIFO, BCH-3 encoder/decoder, and section/line overhead can all be bypassed independently per function and per STS-48/STS-192 stream.

A PRBS generator and monitor are provided per STS-48 signal for continuity checking. This signal is placed into the STS-48 or within each STS-48 signal within a STS-192 payload with a pointer value of 522. This fixed value allows monitoring at the receiver end without the need for a pointer interpreter.

Note: The pointer is set by the incoming signal. Only when PRBS data is injected into the SONET frame is the pointer set, by the device, to 522.

2 Device Overview (continued)

2.3 Section/Line Overhead Insert/Drop Overview (Figure 3) (continued)

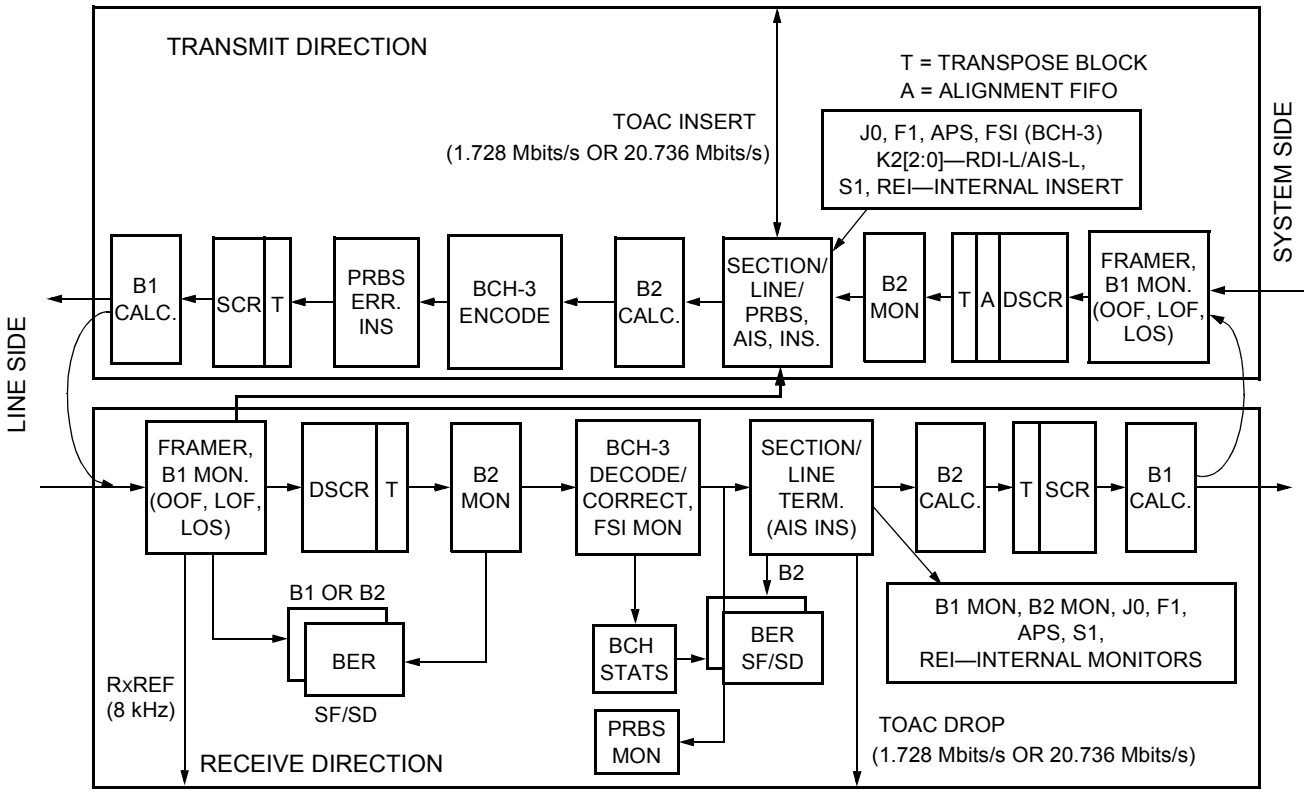


Figure 3. SONET/SDH Line/Section Overhead Processing with BCH-3 Capability

2.4 TOAC Insert/Drop Channel Overview

Four TOAC insert/drop functions are provided in quad STS-48/STM-16 mode and one function is provided in STS-192/STM-64 mode. These interfaces can operate in full TOAC drop/insert mode (Section 2.4.1) and in partial insert/drop mode (Section 2.4.2 on page 12).

2.4.1 Mode 1—Full TOAC Drop/Insert Mode

- The following signals are provided per channel:
  - — One output clock at 20.736 MHz.
  - — One output sync at 8 kHz coincident with the MSN (most significant nibble) of the first A1 byte.
  - — One input enable signal (Tx only) active during the MSN (most significant nibble) and/or the LSN (least significant nibble) of each byte that may be inserted into the output stream. There is only one control signal per stream. This is an encoded signal programmed as follows:
    - — 11 = Insert TOAC data.
    - — 00 = Default.
    - — 01 = Pass data from incoming data stream.
    - — 10 = Software controlled data.
  - — One set per STS-48/STM-16 frame input/output data bus (insert/drop—Tx/Rx direction, respectively)—4 bits/stream at 20.736 Mbits/s that transition at the rising edge of the clock (10,368 bits per STS-48/STM-16 SONET/SDH frame). Each STS-48/STM-16 within the STS-192/STM-64 stream is output independently.

2 Device Overview (continued)

2.4 TOAC Insert/Drop Channel Overview (continued)

Table 2 shows the byte ordering for a STS-192/STM-64 signal in SONET/SDH byte ordering, and Table 3 on page 11 shows a STS-192/STM-64 in STS-48/STM-16 byte ordering. The TOAC channels output/accept the nibble data in STS-48/STM-16 byte order independent of the full drop/insert mode. Therefore, in STS-192/STM-64 mode, four TOAC channels are needed to drop/insert the entire transport overhead bytes. A byte is inserted into the transmit data stream through an external input that is sampled per clock cycle.

Table 2. TOAC—STS-192 SONET/SDH Byte Ordering

Time (Top to Bottom, then Left to Right) ⇓ ⇒												STS-192 Number
1	49	97	145	2	50	98	146	3	51	99	147	1
4	52	100	148	5	53	101	149	6	54	102	150	
7	55	103	151	8	56	104	152	9	57	105	153	
10	58	106	154	11	59	107	155	12	60	108	156	
13	61	109	157	14	62	110	158	15	63	111	159	
16	64	112	160	17	65	113	161	18	66	114	162	
19	67	115	163	20	68	116	164	21	69	117	165	
22	70	118	166	23	71	119	167	24	72	120	168	
25	73	121	169	26	74	122	170	27	75	123	171	
28	76	124	172	29	77	125	173	30	78	126	174	
31	79	127	175	32	80	128	176	33	81	129	177	
34	82	130	178	35	83	131	179	36	84	132	180	
37	85	133	181	38	86	134	182	39	87	135	183	
40	88	136	184	41	89	137	185	42	90	138	186	
43	91	139	187	44	92	140	188	45	93	141	189	
46	94	142	190	47	95	143	191	48	96	144	192	

Table 3. TOAC—STS-192 or STS-48 (Use STS-192 Numbers) in STS-48 Byte Ordering

Time (Top to Bottom, then Left to Right for Each STS-48 Channel) ⇒												TOAC Pins
1	13	25	37	2	14	26	38	3	15	27	39	RTOAC_DATAO_4_[3:0]
4	16	28	40	5	17	29	41	6	18	30	42	
7	19	31	43	8	20	32	44	9	21	33	45	
10	22	34	46	11	23	35	47	12	24	36	48	
49	61	73	85	50	62	74	86	51	63	75	87	RTOAC_DATAO_3_[3:0]
52	64	76	88	53	65	77	89	54	66	78	90	
55	67	79	91	56	68	80	92	57	69	81	93	
58	70	82	94	59	71	83	95	60	72	84	96	
97	109	121	133	98	110	122	134	99	111	123	135	RTOAC_DATAO_2_[3:0]
100	112	124	136	101	113	125	137	102	114	126	138	
103	115	127	139	104	116	128	140	105	117	129	141	
106	118	130	142	107	119	131	143	108	120	132	144	
145	157	169	181	146	158	170	182	147	159	171	183	RTOAC_DATAO_1_[3:0]
148	160	172	184	149	161	173	185	150	162	174	186	
151	163	175	187	152	164	176	188	153	165	177	189	
154	166	178	190	155	167	179	191	156	168	180	192	

2 Device Overview (continued)

2.4 TOAC Insert/Drop Channel Overview (continued)

2.4.2 Mode 2—Partial Insert/Drop Mode

- The first STS-1/STM-0 (J0, E1, D1—D3, D4—D12, S1, E2, etc.), including the M1 byte, are accessible:
  - One output clock at 1.728 MHz.
  - One output sync at 8 kHz coincident with the MSB (most significant bit) of the first A1 bit.
  - One input enable signal (Tx only) active during bit 7 (MSB) and/or bit 6 of each byte that may be inserted into the output stream. There is only one control signal per stream. This is an encoded signal which behaves as follows:
    - 11 = Insert TOAC data.
    - 00 = Default.
    - 01 = Pass data from incoming data stream.
    - 10 = Software controlled data.
  - One input/output data bit (insert/drop—Tx/Rx direction, respectively)—1 bit at 1.728 Mbits/s that transitions at the rising edge of the clock (216 bits per STS-192/STM-64 or STS-48/STM-16 frame).

Table 4 summarizes the frame format in the STS-1/STM-0 mode. Data is transmitted from left to right, then top to bottom, with A1 bit 7 being the first bit to be transmitted/received.

Table 4. TOAC Insert/Drop Frame Format—STS-1/STM-0 Mode

Row		Column Numbers		
		1	2	3
Section/RS	1	A1	A2	J0
	2	B1	E1	F1
	3	D1	D2	D3
Line/MS	4	H1	H2	H3
	5	B2	K1	K2
	6	D4	D5	D6
	7	D7	D8	D9
	8	D10	D11	D12
	9	S1	M1[1]	E2

1. The Z2 byte is overwritten by the M1 value.

2 Device Overview (continued)

2.5 In-Band (Weak) FEC Overview (Bose-Chaudhuri-Hocquenghem (BCH-3))

The weak FEC operates on a quad STS-48/STM-16 and a single STS-192/STM-64 signal as per T1X1.5/99-218R2 and G.707 standards. The bit-interleaved (x8) BCH-3 (4359, 4320) allows for triple error correction per block. In quad STS-48/STM-16 mode, 24 consecutive bit errors can be corrected. In STS-192/STM-64 mode, 96 consecutive bit errors can be corrected because the signal is encoded on a per-STS-48/STM-16 basis.

The check bit locations, per row, are fixed per the standards. The decoder allows a hardware control of the decoder/error correction logic per stream or software control of the decoder/encoder correction logic. Either mode is provisionable through software. The modes are as follows:

1. Hardware mode: transition between the two submodes is hitless and controlled by the FSI status bits:
   —Correct with data delay.
   —Do not correct with data delay.
2. Software control (independent of FSI status):
   —FEC correction enabled.
   —FEC correction off with decoder delay.
   —FEC correction off without decoder delay.
   —FEC monitor mode without decoder delay.

The raw bit error count/block count is provided to the software along with the number of uncorrectable blocks. These values are accumulated in individual saturating counters per STS-48/STM-16/STS-192/STM-64 stream.

The encoder allows three modes of operation per stream entirely under software control. Transition between hardware mode and software control is hitless.

1. FEC encoder on with delay.
2. FEC encoder off with delay.
3. FEC encoder off without delay.

The total delay through the encoder or decoder is less than 15 μs each.

2 Device Overview (continued)

2.6 Strong FEC (G.975) and Digital Wrapper (OTN) Processing Overview

The strong FEC performs out-of-band forward error correction in quad STS-48/STM-16 mode or in single STS-192/STM-64 mode. For example, in quad STS-48/STM-16 mode, the payload rate (system interface) is 2.488 Gbits/s while the line rate is 2.66 Gbits/s. In single STS-192/STM-64 mode, the payload rate is 9.953 Gbits/s while the line rate is 10.66 (10.7) Gbits/s (stuff). Any line/system rates that satisfy the 15/14 (255/238) ratio or 85/79 (255/237) are acceptable inputs for the TFEC0410G device. The macro (Figure 4) consists of eight elastic stores (four Tx, four Rx), an FEC/DW frame create/monitor, an FEC/DW—DWAC (digital wrapper access channel) drop/insert block, an RS encoder/decoder, a scrambler/descrambler, an FEC/DW framer block, a byte interleaver, and a byte deinterleaver.

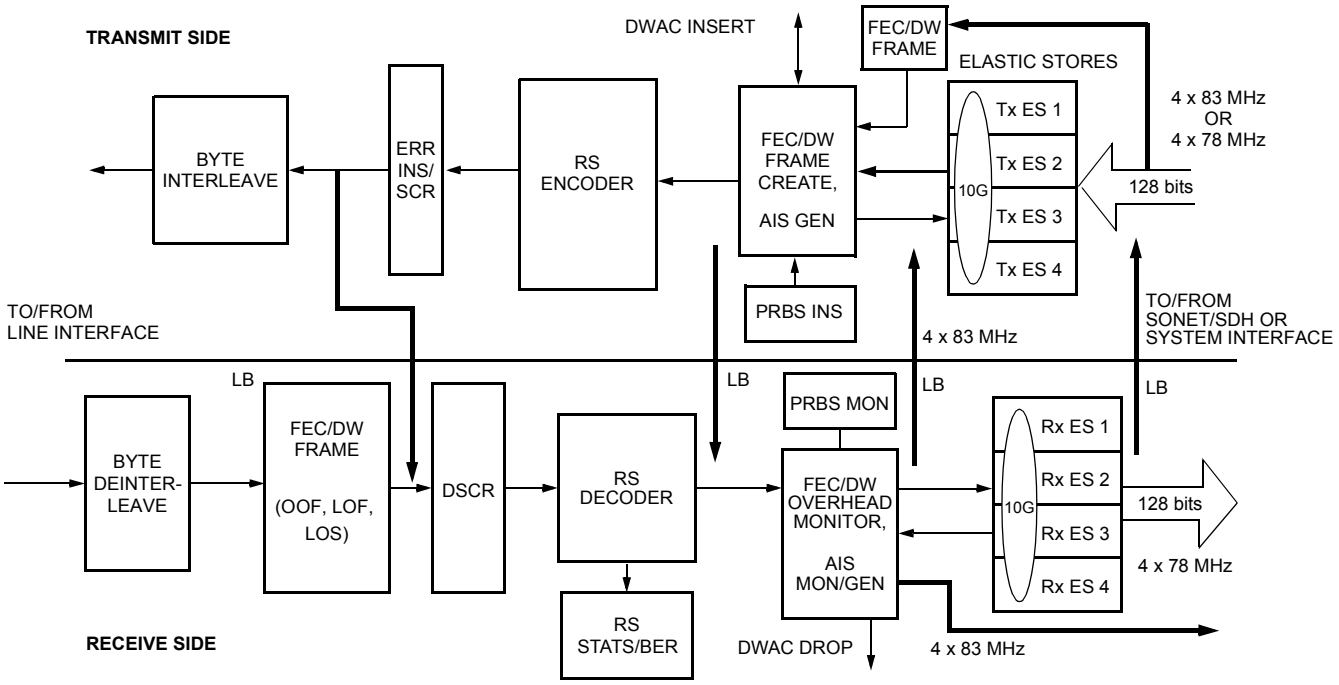


Figure 4. Digital Wrapper and Strong FEC Block Diagram

2.6.1 Elastic Stores (ES)

Four elastic stores per direction are provided to map/demap data to/from the FEC/DW frame format. Each elastic store functions independently in quad mode, while in single mode all four work together. They have no stuffing mechanism to accommodate sustained differences between the incoming and outgoing clocks. This requires the read and write clocks to be locked together using the on-board phase detector outputs (or equivalent circuitry) as inputs to external PLL logic.

2 Device Overview (continued)

2.6 Strong FEC (G.975) and Digital Wrapper (OTN) Processing Overview (continued)

2.6.2 RS Encoder/Decoder and Digital Wrapper Basis Frame Format

The strong FEC code used to protect the payload/overhead information against transmission errors is a Reed-Solomon code specified in ITU-T/G.975 and G.709. The RS (255, 239) code block, shown in Figure 5, is a nonbinary code and belongs to the family of systematic linear cyclic block codes.

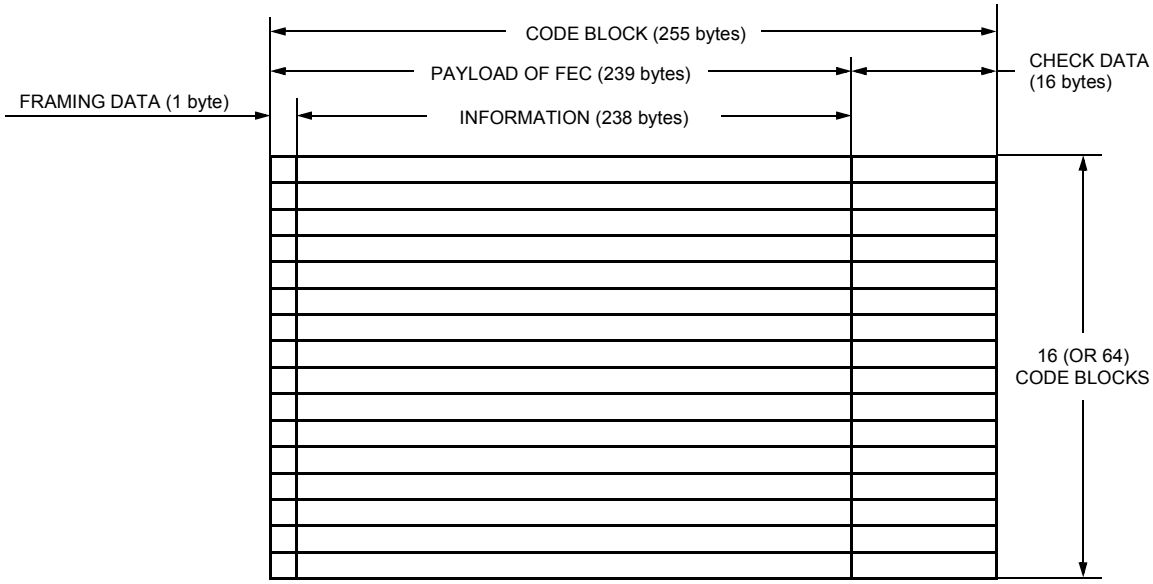


Figure 5. 16-Way (or 64-Way) Interleaved RS (255, 239) Frame (FEC Frame)

As can be seen, there is 1 overhead byte, 238 information bytes, and 16 check bytes per RS (255, 239) code block. In order to enhance the immunity of transmission system to the burst errors, 16 (or 64) RS (255, 239) code blocks are interleaved to form a FEC frame. Transmission order is column-by-column, i.e., after 16 (or 64) overhead bytes are transmitted, the first information byte of the second column will be transmitted.

There are five different modes of operation, as shown in Table 5.

Table 5. Modes of Operation

FEC Payload Type	Interleaving Depth	Overhead Processing
Quad 2488 Mbits/s	16	FEC Frame
		Digital Wrapper (DW) Frame
Single 9952 Mbits/s	16	FEC Frame
		Digital Wrapper (DW) Frame
	64	Digital Wrapper (DW) Frame

2 Device Overview (continued)

2.6 Strong FEC (G.975) and Digital Wrapper (OTN) Processing Overview (continued)

In quad 2.5 Gbits/s mode, the strong FEC macro processes four different 32-bit wide data streams at four different 83 MHz clocks. In 10 Gbits/s mode, the strong FEC macro processes a single 128-bit wide data stream at a single 83 MHz clock. 16-way or 64-way interleaving is programmable in 10 Gbits/s mode, while there is only 16-way interleaving in quad 2.5 Gbits/s mode.

The TFEC0410G supports the following synchronous G.709 mappings:

- (System Interface) CBR2G5 ↔ OPU1 ↔ ODU1 ↔ OTU1 (Line Interface) (STS-48/STM-16, ATM, IP, Ethernet, etc.)
- (System Interface) CBR10G ↔ OPU2 ↔ ODU2 ↔ OTU2 (Line Interface) (STS-192/STM-64, ATM, IP, Ethernet, etc.)

The DW frame consists of four FEC frames, and each FEC frame consists of 16-way interleaving RS (255, 239) code blocks, as shown in Figure 6. In 16-way interleaving (dashed arrow), the overhead columns are spaced by 4064 bytes (254 × 16 rows/FEC frame), while in 64-way interleaving (solid arrow), all 64 overhead bytes are consecutively transmitted and repeated after 16256 bytes (4 × [254 × 16]). Each RS block can correct up to eight symbol errors. Therefore, with 16-way interleaving, 1024 (16 interleaving × 8 symbols × 8 bits/symbol) consecutive bit errors can be corrected; while in 64-way interleaving, 1024 × 4 = 4096 consecutive bit errors can be corrected. The number of bit or block errors and uncorrected blocks are accumulated in saturating counters per stream. This information is used as the raw input to a BER algorithm.

When the strong FEC is in digital wrapper mode, overhead definition and processing are different from those in FEC mode.

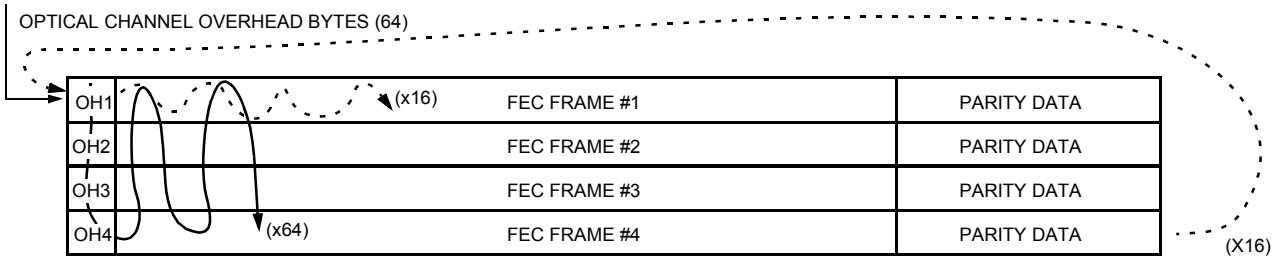


Figure 6. Digital Wrapper—Optical Channel Overhead (16-Way/64-Way Interleaving)

2 Device Overview (continued)

2.6 Strong FEC (G.975) and Digital Wrapper (OTN) Processing Overview (continued)

2.6.3 FEC Overhead and Digital Wrapper Overhead Definition

The entire overhead for both FEC and DW frames is programmable through the digital wrapper access channel (DWAC). This allows flexibility in its definition for future changes in the standards. Internally, 4 bytes can be monitored with continuous N-times detect (CNTD) monitors. These monitors can be combined in four different configurations. They can be grouped as four 1-byte monitors, two 2-byte monitors, one 3-byte and one 1-byte monitor, or one 4-byte monitor. The multiple bytes do not need to be continuous. 4 bytes can be inserted from an internal register per stream.

Table 6 summarizes the overhead sources for each byte in the FEC or DW frame. The FEC overhead repeats every FEC frame. The position and location of the framing bytes are provisionable from a minimum of 2 bytes to a maximum of 16 bytes in steps of 2 bytes. All other bytes that have not been assigned as framing bytes can come from the four internal registers for each 2.5 Gbits/s signal or from the DWAC. Backward error indications (BEI) and status indications (BDI) are provided on-chip.

Table 6. FEC/Digital Wrapper Overhead Source

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	Programmable Framing Bytes (Location/Value—Internal), and Others from DWAC or Internal Registers (4 Max)															
2	Programmable Framing Bytes (Location/Value—Internal), and Others from DWAC or Internal Registers (4 Max)															
3	Programmable Framing Bytes (Location/Value—Internal), and Others from DWAC or Internal Registers (4 Max)															
4	Programmable Framing Bytes (Location/Value—Internal), and Others from DWAC or Internal Registers (4 Max)															

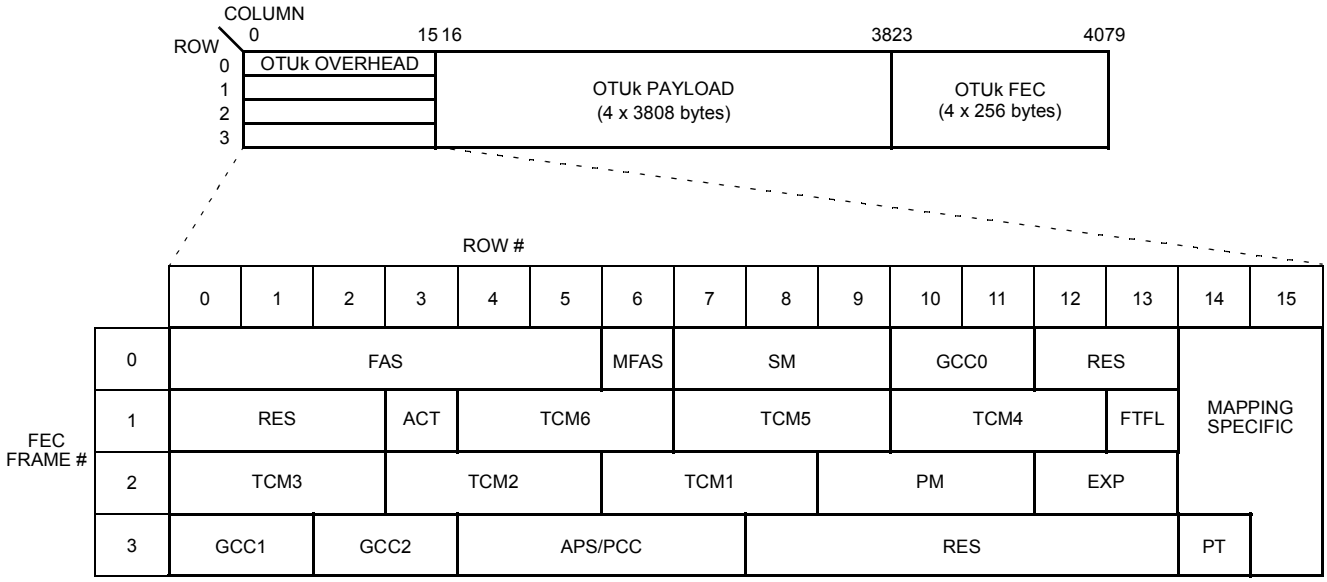
Notes: Any value not from an internal register or the DWAC channel is set to zero.

Two (three) BIP-8 calculations are provided over the OPUk and payload bytes only; overhead and check bits are excluded from the calculation. The calculated values can be compared against a selected overhead byte. Errors are accumulated in saturating counters.

A possible DW/OTM-0 signal overhead format is defined in Figure 7 on page 18. This format and many others are allowed and created from the internal and DWAC capabilities.

2 Device Overview (continued)

2.6 Strong FEC (G.975) and Digital Wrapper (OTN) Processing Overview (continued)



Note: Column and row are defined as row and frame, respectively, for register definitions.

Figure 7. Possible Overhead Definition for OTUk Signals

2.6.4 FEC/DW—DWAC (Digital Wrapper Access Channel) Drop/Insert Block

Four insert digital wrapper access channels (DWACs) are provided on-chip along with four drop DWACs. These channels provide most of the monitoring and insert capability for the FEC/DW overhead bytes.

- The insert DWAC consists of the four following signals per channel (for a total of four DW access channels):
  - — One output clock at ~10.455 MHz (10 Gbits/s mode and quad 2.5 Gbits/s mode).
  - — One output superframe sync (~326.7 kHz/~81.68 kHz—10 Gbits/s (FEC/DW), ~81.68 kHz/~20.42 kHz—quad 2.5 Gbits/s (FEC/DW)) coincident with the MSB (most significant bit) of the first byte in frame 0, output on the rising edge of the clock. A double-wide pulse coincident with bit 6 (2.5 Gbits/s mode) or LSN (10 Gbits/s mode) indicates the corresponding frame contains an MFAS value of zero.
  - — Input data: 4 bits in 10 Gbits/s mode and 1 bit per stream in quad 2.5 Gbits/s mode, sampled on the rising edge of the clock.
  - — Input insert enable signal: active-high signal coincident with the MSB[7]—bit[6] of the byte to insert in quad 2.5 Gbits/s mode or coincident with the MSN and LSN in 10 Gbits/s mode. This is an encoded signal set as follows:
    - — 11 = insert DWAC data
    - — 00 = default
    - — 10 or 01 = pass data from incoming data stream.
- The drop DWAC consists of the following three signals per channel (total of four DW access channels):
  - — One output clock at ~10.455 MHz (10 Gbits/s mode and quad 2.5 Gbits/s mode).
  - — One output superframe sync (~326.7 kHz/~81.68 kHz—10 Gbits/s (FEC/DW), ~81.68 kHz/~20.42 kHz—quad 2.5 Gbits/s (FEC/DW)) coincident with the MSB (most significant bit) of the first byte in frame 0, output on the rising edge of the DWAC clock.
  - — Output data: 4 bits in 10 Gbits/s mode and 1 bit per stream in quad 2.5 Gbits/s mode, samples on the rising edge of the DWAC clock.

2 Device Overview (continued)

2.6 Strong FEC (G.975) and Digital Wrapper (OTN) Processing Overview (continued)

The data stream format to/from the device is shown in Figure 8.

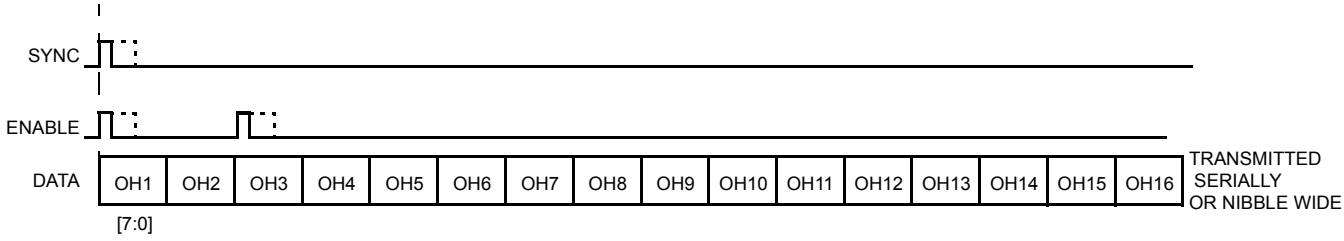


Figure 8. DWAC Frame Definition

2.6.5 Receive/Transmit FEC/DW Framer

- An alpha/delta framer is provided to find the FEC/DW overhead framing pattern. The following parameters of the framer are programmable through software:
  - — Number of framing pairs.
  - — Framing values (OA1/OA2).
  - — Number of bytes examined to go in-frame.
  - — Number of bytes examined to go out-of-frame.
  - — Number of consecutive error-free framing patterns to declare in-frame.
  - — Number of consecutive errored framing patterns to declare out-of-frame.

The framer will detect a loss-of-frame (LOF) state and LOF parameters are programmable (number of frames to declare and number of frames to clear). Under software or hardware control, an AIS signal will be generated (all-ones pattern in all overhead except the framing bytes). Data is optionally descrambled (Rx side only) using one of the two possible polynomials ($x^7 + x + 1$ or $x^{16} + x^{12} + x^3 + x + 1$) under user control.

2.7 Line Interface—MUX/DeMUX Overview

- The line MUX/deMUX allows the three following modes of operation:
  - — One group of 16 bits at 622.08/666.51/669.32 Mbits/s—10 Gbits/s mode
  - — One group of 16 bits at 155/166 Mbits/s—single 2.5 Gbits/s mode
  - — Four groups of 4 bits at 622.08/666.51—quad 2.5 Gbits/s mode.

All modes support forward clocking only. These blocks perform parallel-to-parallel conversions from 128 bits ↔ 16 bits, 32 bits ↔ 16 bits, or 32 bits ↔ 4 bits, respectively. Facility loopback and terminal loopback capabilities are provided at this interface for diagnostic purposes. This interface can run at other clock rates as long as the 15/14 (255/237) ratio between the system clock and line clock is maintained.

2 Device Overview (continued)

2.8 Alarm Status Output Signals Overview

The status of the internal LOC, OOF, LOF, and LOS monitors per 2.5 Gbits/s slice are accessible on eight external transmit and eight external receive pins (16 total—GPIO[15:0]). The specified alarm output on each pin is programmable under software control. These outputs allow automatic actions to occur during certain failure conditions. (See the *TFEC0410G 2.5/10 Gbits/s Optical Networking Interface with Strong/Weak FEC and Digital Wrapper Hardware Register Map* document for more information.)

2.9 Microprocessor Interface Overview

The TFEC0410G microprocessor interface architecture is configured for glueless interface to the *Motorola*® MPC860 and MC68360 microprocessors. The *Intel* ® microcontrollers 8XC251 and 80C196 and the i960 microprocessor may also be utilized to interface to the TFEC0410G. However, provisions on the board need to be made to (de)multiplex the address and data bus. The state of the MPTYPE_IM input signal indicates to the device whether it interfaces to a *Motorola* microprocessor or an *Intel* microcontroller. Other microprocessors may be used if their timing requirements fit to one of the modes described.

The TFEC0410G has separate 16-bit wide address and data busses. The MPDB_8_16 input distinguishes between an 8-bit or 16-bit wide microprocessor data bus being used. In case of an 8-bit wide microprocessor data bus interface, the eight upper bits of the device data bus ports are not being used and are held 3-state. The microprocessor interface operates at the frequency of the microprocessor clock (PCLK) input which should be in the range of 10 MHz to 100 MHz.

All internal counters are latched using an external or internal PM latch pulse that must occur once per second (programmable) to ensure all internal counters do not saturate.

2.9.1 Transfer Error Acknowledge (TEA_N) (with MPC860 and MC68360 Only)

The TFEC0410G contains a bus time-out counter. When this counter saturates, a bus error is generated to the external processor through the transfer error acknowledge (TEA_N) signal. This feature must be considered with respect to the external ability of the processor to generate its own internal bus time-out. TEA_N will be asserted if an internal data acknowledgment is not received within 32 PCLK periods. This interval is used since all valid internal accesses to the device will be completed in significantly less than 32 PCLK periods.

TEA_N is also asserted if the calculated parity value does not match the parity generated by the external microprocessor on a data transfer.

2.9.2 Interrupt Structure

The interrupt structure of the TFEC0410G minimizes the effort for software/firmware to isolate the interrupt source. The interrupt structure is comprised of different registers depending on the consolidation level. At the lowest level (source level), there are two registers. The first is an alarm register (AR). An alarm register is typically of the write 1 clear (W1C) type. The second is an interrupt mask (IM) register of the read/write (R/W) type.

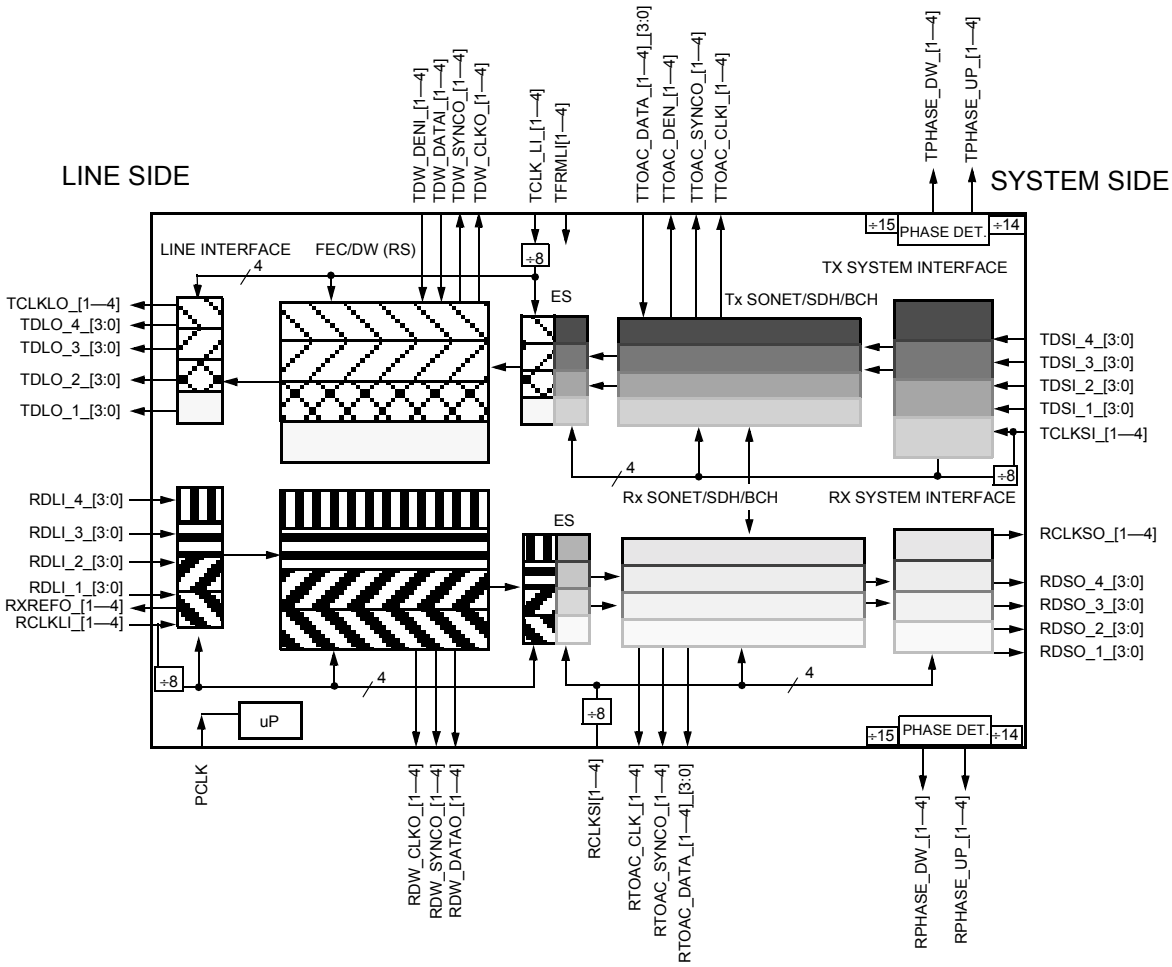
An alarm register latches a raw status alarm. This latched alarm may contribute to an interrupt if its corresponding interrupt mask bit is disabled. Individual latched alarms are consolidated into an interrupt status register (ISR). If any of the latched alarms that are consolidated into a bit of an ISR are set and unmasked, the ISR bit is set. The ISR bit may contribute to an interrupt if its corresponding interrupt mask bit is disabled. ISRs may be consolidated into a higher-level ISR in a similar fashion until all alarms are consolidated into the chip-level ISR. The alarm register that causes an interrupt can be determined by traversing the tree of ISRs, starting at the chip-level ISR, until the source alarm is found.

Note: Interrupts are disabled when the corresponding bit in the mask register is 0. If the mask register bit is 1, the interrupt is enabled. Two levels of alarms are provided: a high-interrupt output and a low-interrupt output from the device.

2 Device Overview (continued)

2.10 Clocking Overview

The following diagrams show simplified pictures of the major clock domains within the TFEC0410G in quad 2.5 Gbits/s and 10 Gbits/s strong/digital wrapper/weak SONET/SDH mode. In 10 Gbits/s mode, each block has one clock domain for a total of four transmission clocks along with one microprocessor clock.

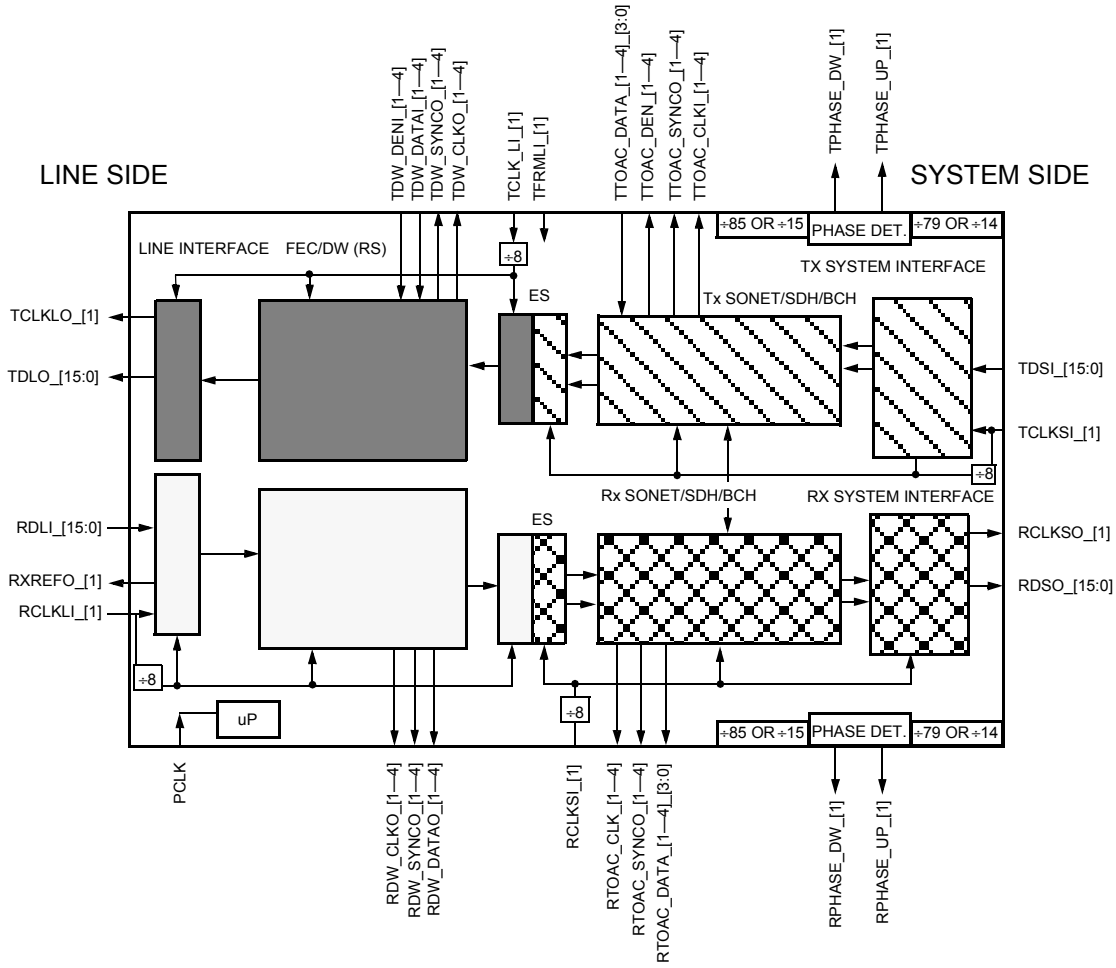


Note: There are a total of 16 different transmission clocks and 1 microprocessor clock.

Figure 9. Quad 2.5 Gbits/s Clocking Overview—Terminal Mode

2 Device Overview (continued)

2.10 Clocking Overview (continued)



Note: There are a total of 4 different transmission clocks and 1 microprocessor clock.

Figure 10. 10 Gbits/s Clocking Overview—Terminal Mode

3 Block Diagrams

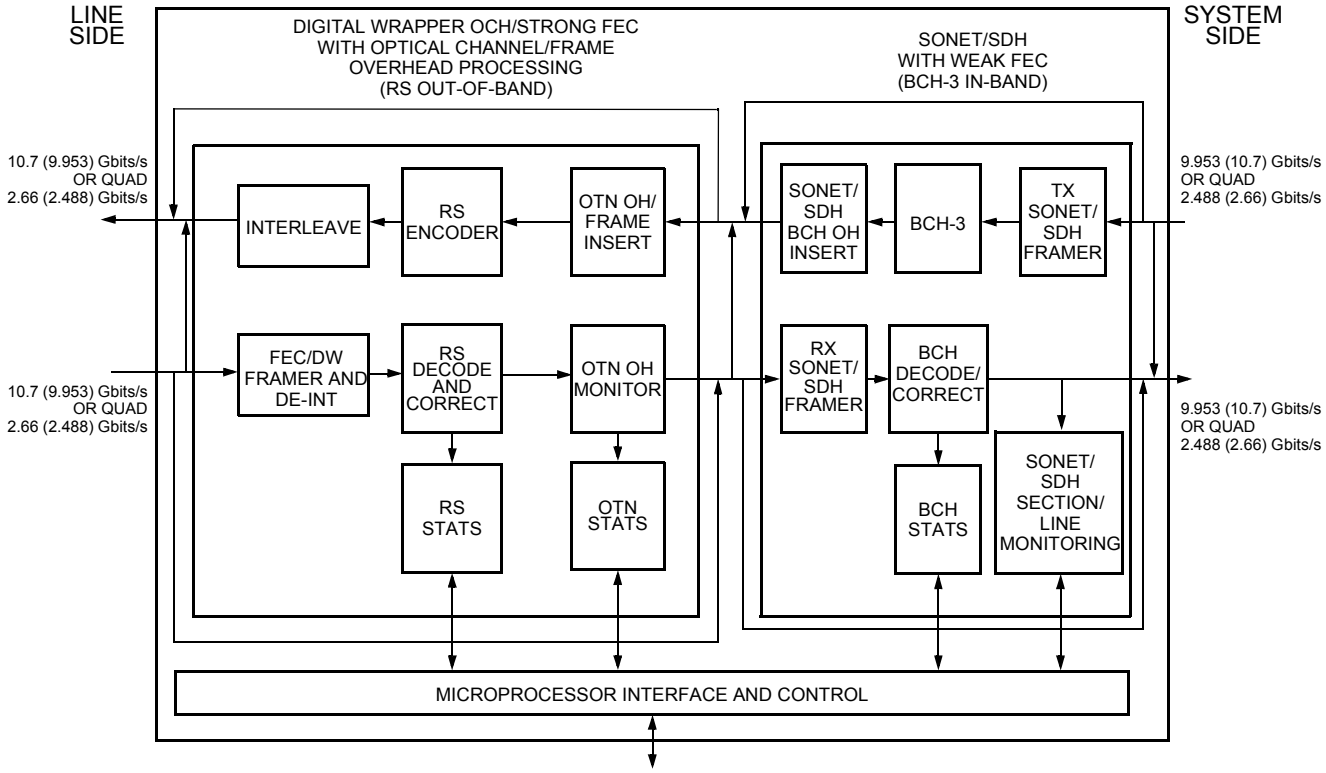


Figure 11. TFEC0410G Block Diagram

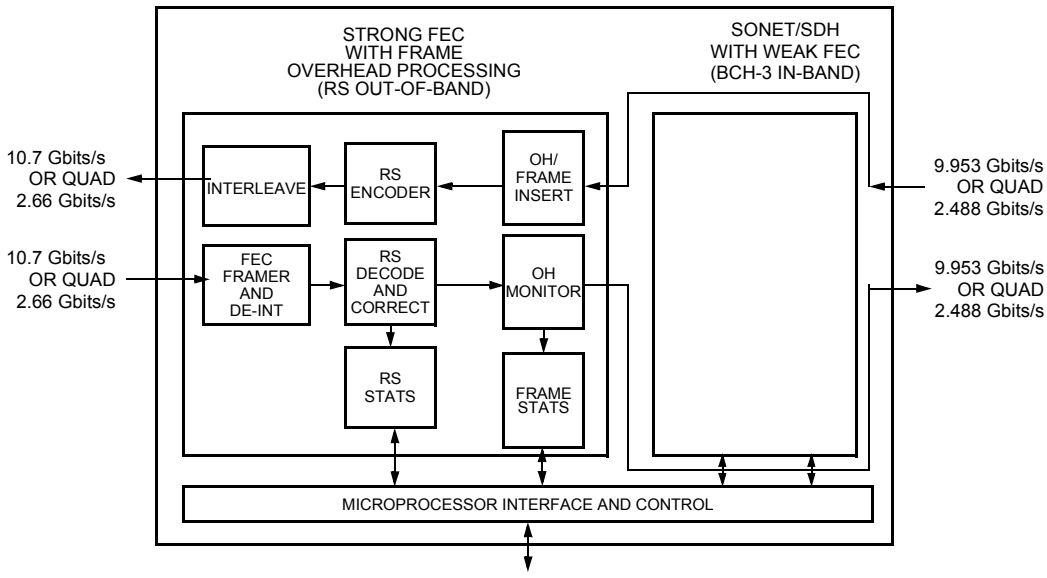


Figure 12. Strong FEC Application: Terminal

3 Block Diagrams (continued)

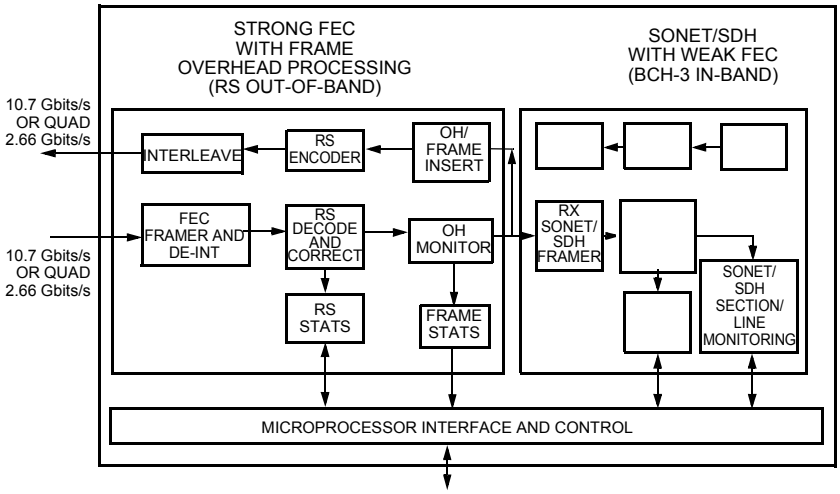


Figure 13. Strong FEC Application: Regenerator (SONET/SDH Section Monitoring Possible)

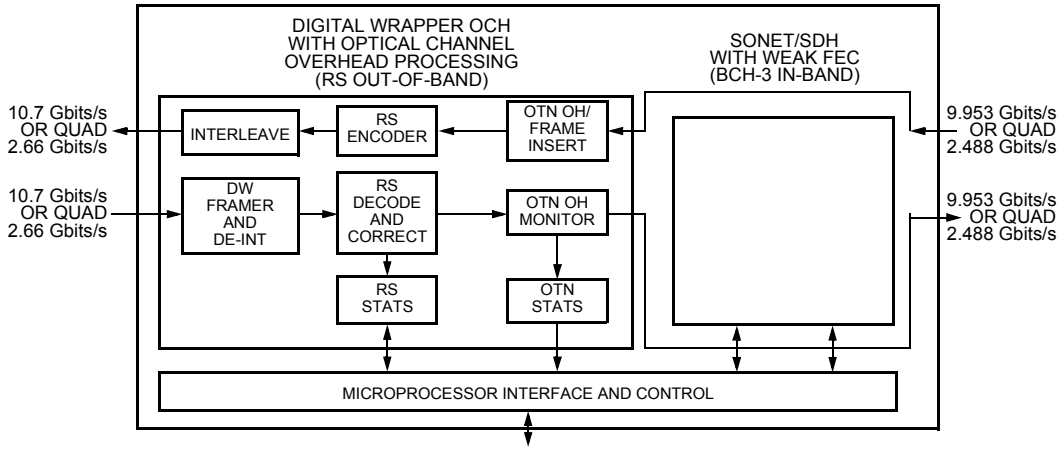


Figure 14. Digital Wrapper (OCh) Application: OTN Adapter

3 Block Diagrams (continued)

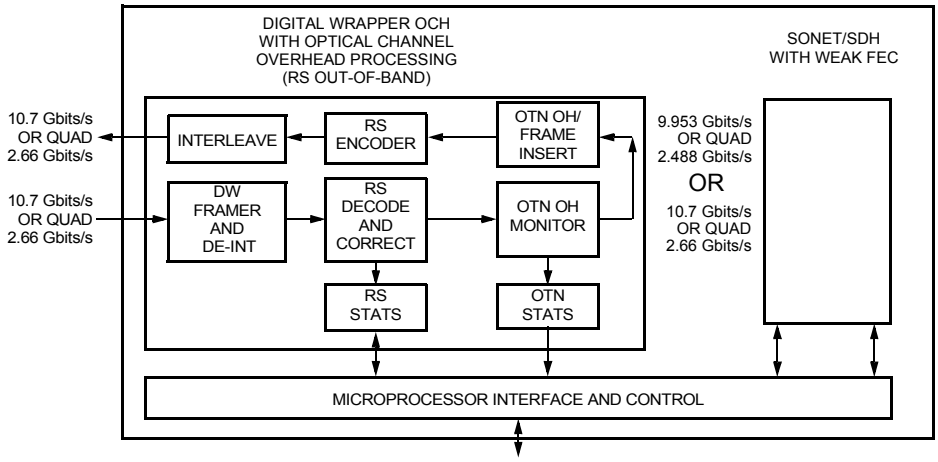


Figure 15. Digital Wrapper (OCh) Application: OTN Regenerator

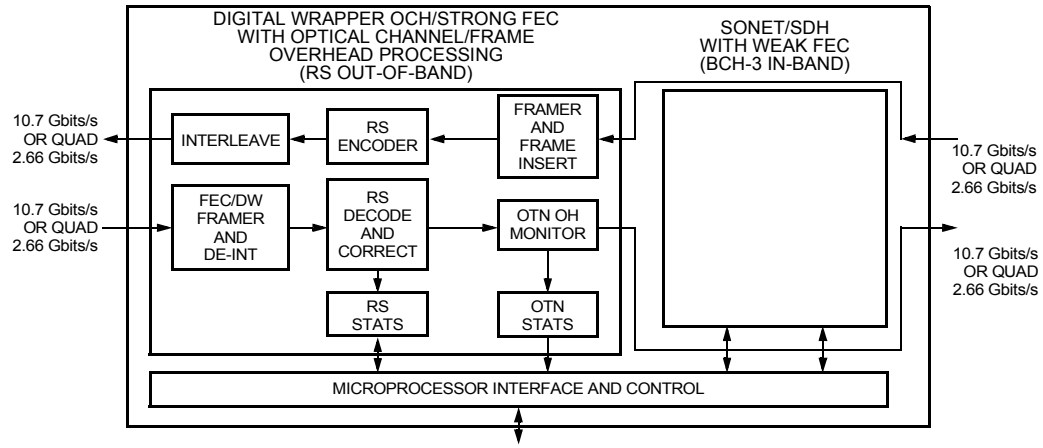


Figure 16. Strong FEC or Digital Wrapper (OCh) with Strong FEC: Bidirectional Mode

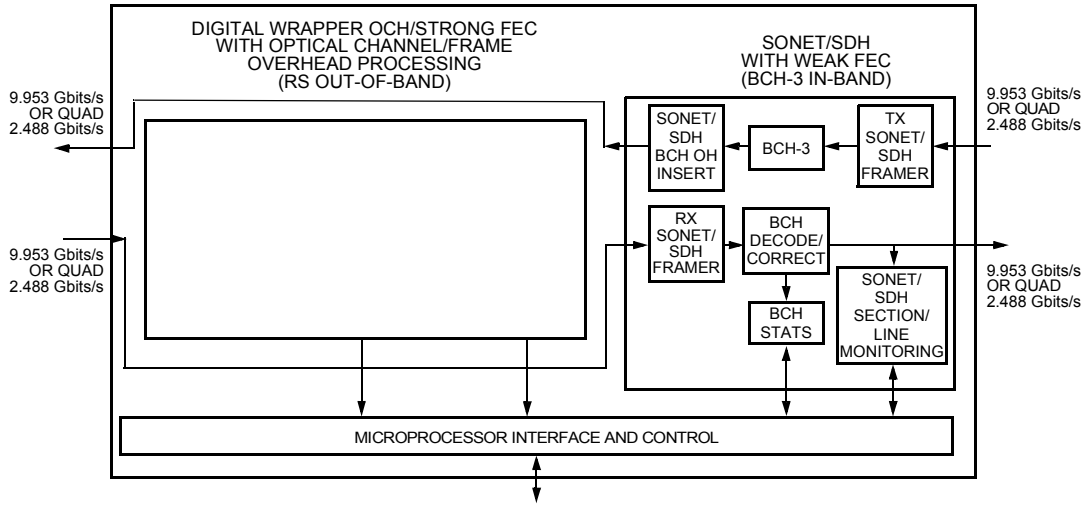


Figure 17. Weak FEC Application: SONET/SDH Terminal

3 Block Diagrams (continued)

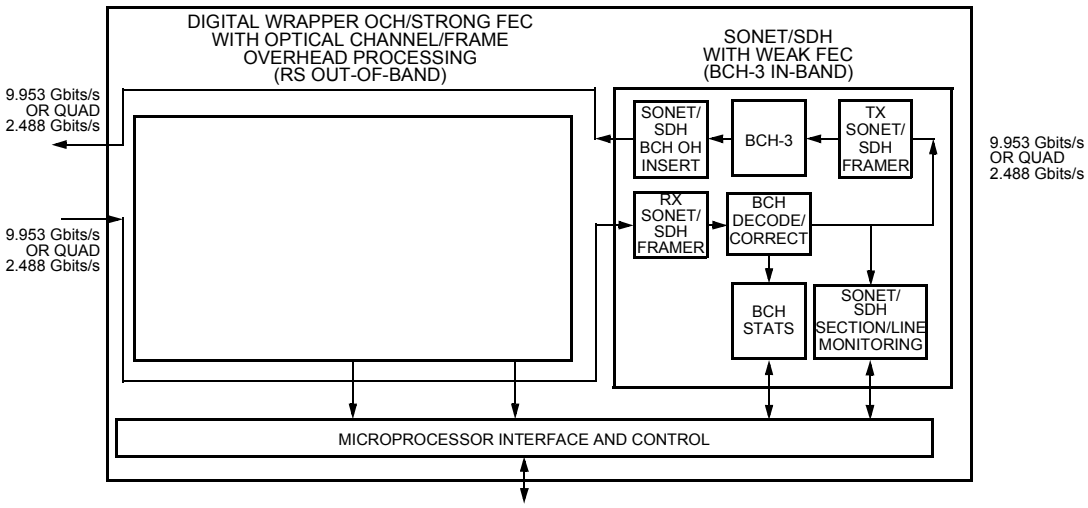


Figure 18. Weak FEC Application: SONET/SDH Regenerator

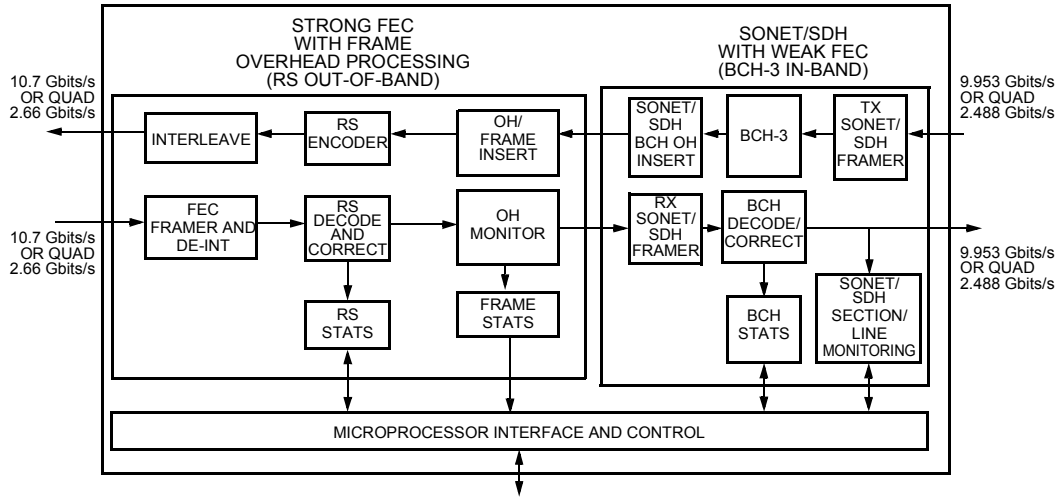


Figure 19. Strong/Weak FEC Application: SONET/SDH Terminal

3 Block Diagrams (continued)

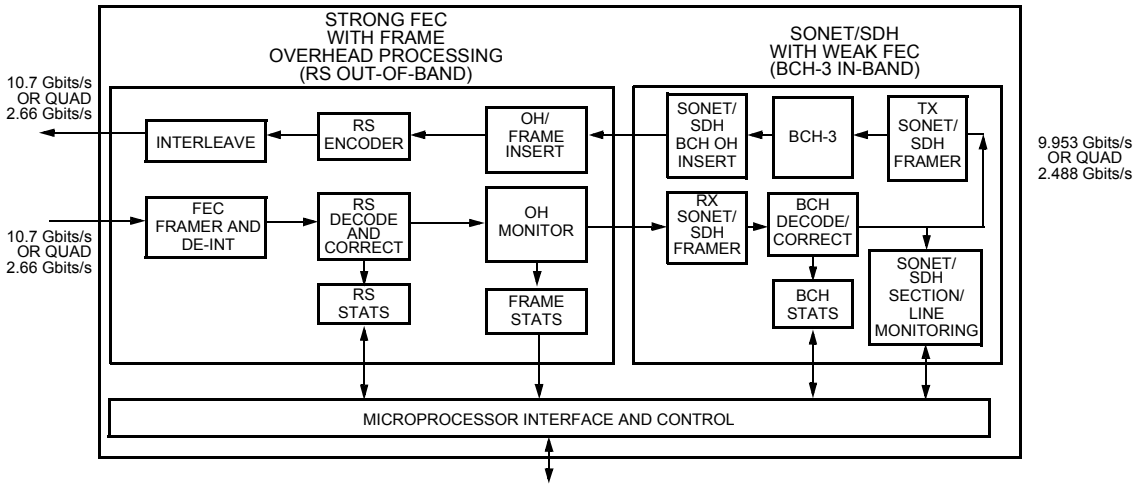


Figure 20. Strong/Weak FEC Application: SONET/SDH Regenerator

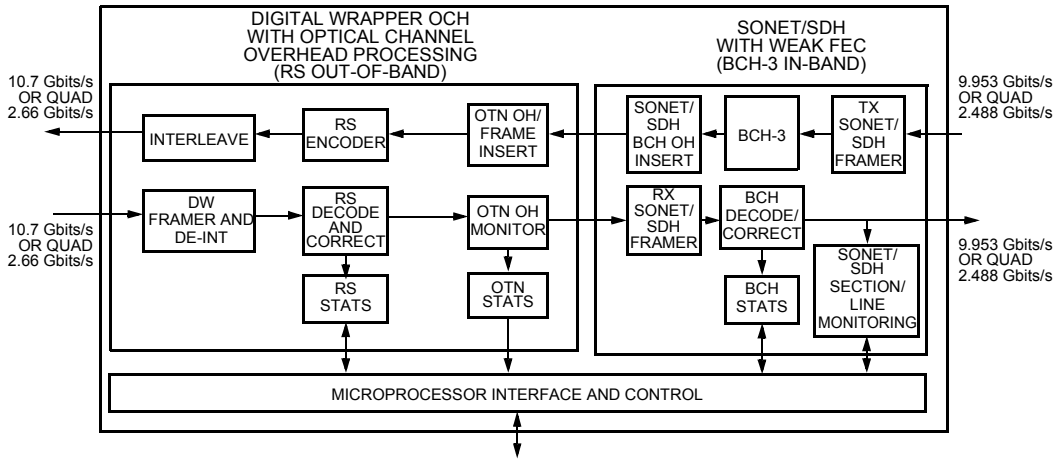


Figure 21. Digital Wrapper (OCh)/Weak FEC: OTN with SONET/SDH Termination

3 Block Diagrams (continued)

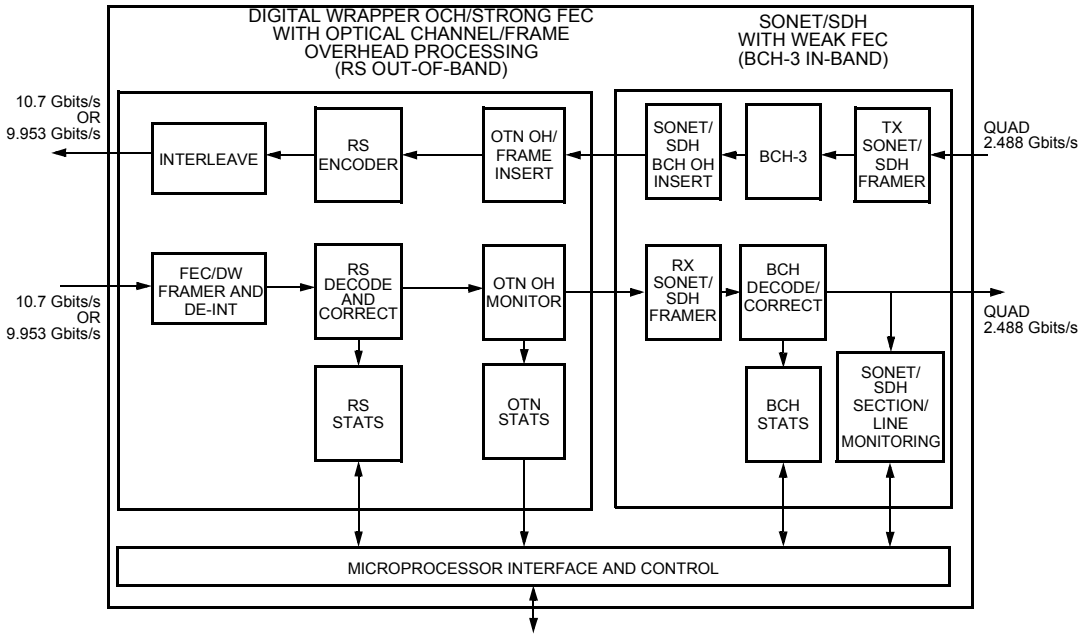


Figure 22. Asymmetric Multiplex Mode: SONET/SDH Terminal with/without Strong/Weak FEC

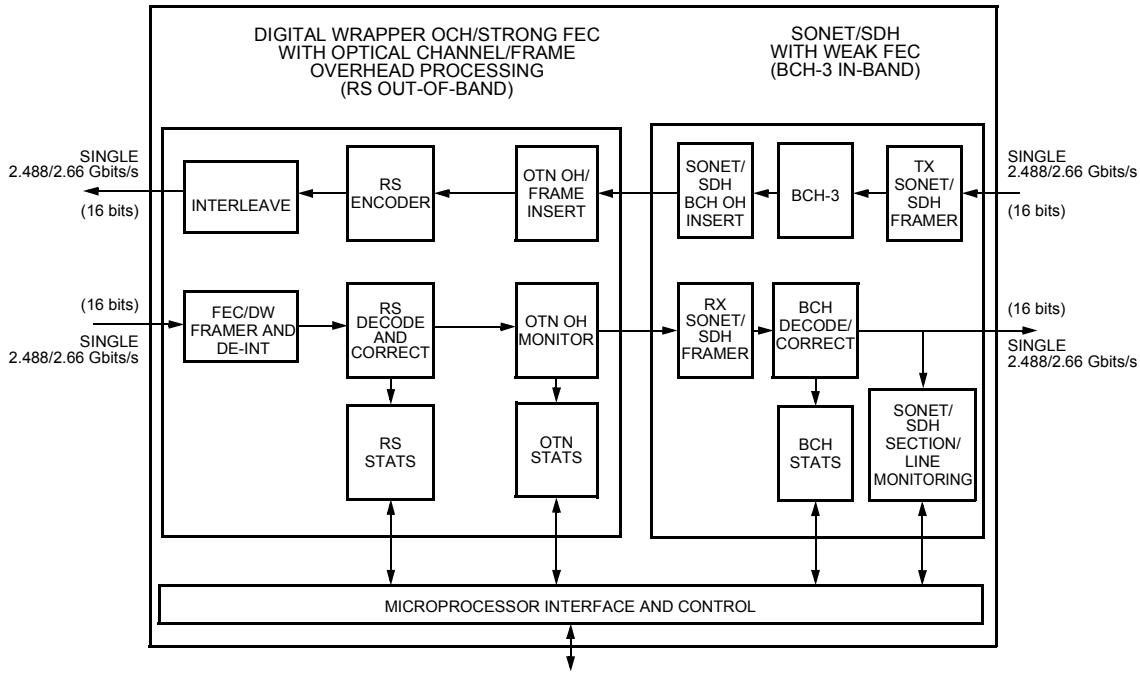


Figure 23. Single 2.5 Gbits/s Mode: SONET/SDH, Terminal/Regenerator, with Strong or Weak FEC

4 Top-Level Overview

4.1 Top-Level Functionality

The top-level block outlines the following functionality in detail:

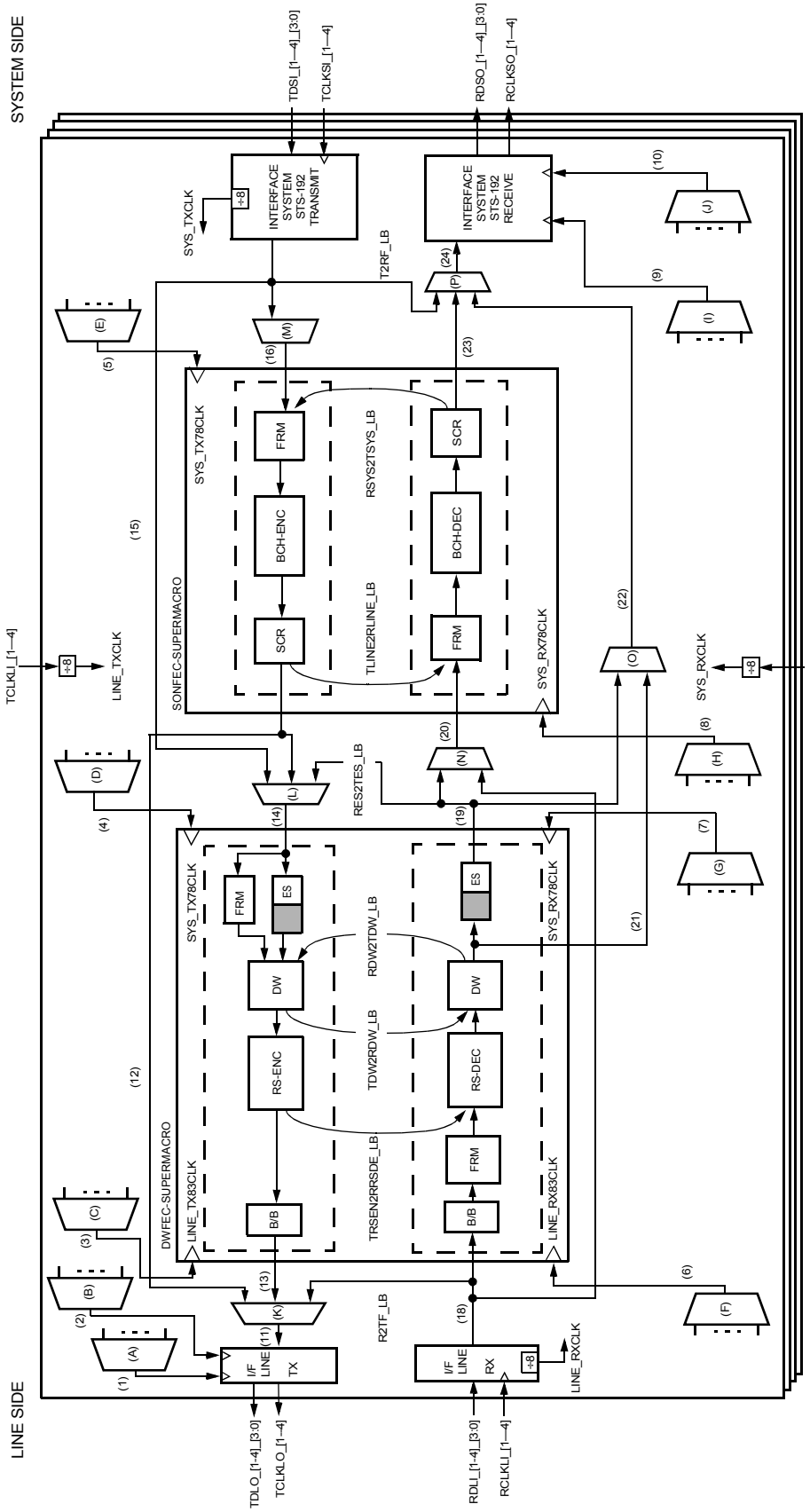
- Top-level clock and data MUXes (Section 4.2).
- Loss-of-clock detectors (LOC) (Section 4.3 on page 31).
- Reset architecture (hardware/software) (Section 4.4 on page 32).
- Loopback controls (Section 4.5 on page 33).
- Powerdown control functionality (Section 4.6 on page 33).
- Phase detectors (Section 4.7 on page 34).
- Line timing reference signal generation (Section 4.8 on page 35).
- Alarm status output signals through GPIO pins (Section 4.9 on page 36).

4.2 Top-Level Clocking

Figure 24, Top-Level Clock and Datapath Overview (1 of 4 Slices), on page 30 shows a detailed picture of the major clock domains and datapaths within the TFEC0410G in quad 2.5 Gbits/s strong/digital wrapper/weak SONET/SDH mode. In 10 Gbits/s mode, each block only has one clock domain for a total of four transmission clocks in addition to one microprocessor clock.

4 Top-Level Overview (continued)

4.2 Top-Level Clocking (continued)



CLOCK MULTIPLEXERS:
(A) LINE_TX_HS_CLKMUX
(B) LINE_TX_LS_CLKMUX
(C) LINE_TX_DWFEC_CLKMUX
(D) SYS_TX_DWFEC_CLKMUX
(E) SYS_TX_SONFEC_CLKMUX
(F) LINE_RX_DWFEC_CLKMUX
(G) SYS_RX_DWFEC_CLKMUX
(H) SYS_RX_SONFEC_CLKMUX
(I) SYS_RX_LS_CLKMUX
(J) SYS_RX_HS_CLKMUX

DATA MULTIPLEXERS:
(K) LINE_TX_DMUX
(L) DWFEC_TX_DMUX
(M) SONFEC_TX_DMUX
(N) SONFEC_RX_DMUX
(O) SONFEC_RX_BYP_DMUX
(P) SYS_RX_DMUX

CLOCK SIGNALS:
(1) LINE_TX_HSCLK
(2) LINE_TX_LSCLK
(3) LINE_TX83CLK
(4) DWFEC_TX78CLK
(5) SONFEC_TX78CLK
(6) LINE_RX83CLK
(7) DWFEC_RX78CLK
(8) SYS_RX78CLK
(9) SYS_RX_LSCLK
(10) SYS_RX_HSCLK

DATA SIGNALS:
(11) LINE_TXDATAO[127:0]
(12) SONFEC_TXDATAO[127:0]
(13) DWFEC_TXDATAO[127:0]
(14) DWFEC_TXDATAI[127:0]
(15) SYS_TXDATAI[127:0]
(16) SONFEC_TXDATAI[127:0]
(18) LINE_RXDATAI[127:0]
(19) DWFEC_RXDATAO[127:0]
(20) SONFEC_RXDATAI[127:0]
(21) DWFEC_RX83DATA[127:0]
(22) SONFEC_RXBYPDATA[127:0]
(23) SONFEC_RXDATAO[127:0]
(24) SYS_RXDATAO[127:0]

Figure 24. Top-Level Clock and Datapath Overview (1 of 4 Slices)

4 Top-Level Overview (continued)

4.3 Top-Level Loss-of-Clock Detectors

All high-speed input clocks have loss-of-clock (LOC) detectors. These detectors use the microprocessor clock as a reference and will not declare LOC if the MPU clock is lost. These detectors check for activity on the monitored signal. If the MPU clock is lost, the detectors will clear their LOC state and will not activate the respective LOC indicator until the MPU clock recovers.

Table 7. Loss of Clock Registers

Function	Register Name (First Occurrence)	Register Bits	Qty.[1]	1st Addr[2] (hex)
LOC Interrupt Alarm	DEV_LOC_ALARM_S0 (W1C)	DEV_LOC_LINE_TXCLK_A	4	0×14
		DEV_LOC_LINE_RXCLK_A	4	0×14
		DEV_LOC_SYS_TXCLK_A	4	0×14
		DEV_LOC_SYS_RXCLK_A	4	0×14
LOC Alarm Mask	DEV_LOC_MASK_S0 (R/W)	DEV_LOC_LINE_TXCLK_M	4	0×43
		DEV_LOC_LINE_RXCLK_M	4	0×43
		DEV_LOC_SYS_TXCLK_M	4	0×43
		DEV_LOC_SYS_RXCLK_M	4	0×43
LOC Persistency	DEV_LOC_PERSIST_S0 (RO)	DEV_LOC_LINE_TXCLK_P	4	0×70
		DEV_LOC_LINE_RXCLK_P	4	0×70
		DEV_LOC_SYS_TXCLK_P	4	0×70
		DEV_LOC_SYS_RXCLK_P	4	0×70
LOC State	DEV_LOC_STATE_S0 (RO)	DEV_LOC_LINE_TXCLK	4	0×90
		DEV_LOC_LINE_RXCLK	4	0×90
		DEV_LOC_SYS_TXCLK	4	0×90
		DEV_LOC_SYS_RXCLK	4	0×90

1. Qty. refers to the number of registers that are similar to the one shown in the table. There may be more registers to control different channels, or several registers of similar type used for a particular function.
2. 1st Addr (hex) refers to the address (in hex) of the first occurrence of this type of register.

4 Top-Level Overview (continued)

4.4 Top-Level Reset Architecture (Hardware/Software)

All slices are reset when the external reset signal is asserted. The device will not exit the reset state until a clock is provided to the MACRO block. The reset monitor registers indicate the reset status of each block. The datapath of each slice can be individually reset through a software register. In 10 Gbits/s mode, all slice resets must be written. The MPU blocks within the SONFEC supermacro and the DWFEC supermacro can be reset independently through software control.

Table 8. Software Reset Registers

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
MPU Reset	DEV_MPUREG_SWRST (R/W)	DEV_DWFEC_MPU_SWRST	1	0×300
		DEV_SONFEC_MPU_SWRST	1	0×300
		DEV_MPU_REG_SWRST	1	0×300
Datapath Reset	DEV_DP_SWRST_S0 (R/W)	DEV_DWFEC_DAT_SWRST	4	0×301
		DEV_SONFEC_DAT_SWRST	4	0×301
DWFEC Reset Monitor	DWFEC_RST_MON (RO)	DWFEC_RX_RST_MON_S3	1	0×2001
		DWFEC_RX_RST_MON_S2	1	0×2001
		DWFEC_RX_RST_MON_S1	1	0×2001
		DWFEC_RX_RST_MON_S0	1	0×2001
		DWFEC_TX_RST_MON_S3	1	0×2001
		DWFEC_TX_RST_MON_S2	1	0×2001
		DWFEC_TX_RST_MON_S1	1	0×2001
		DWFEC_TX_RST_MON_S0	1	0×2001
SONFEC Reset Monitor	SONFEC_RST_MON (RO)	RX_RST_MON_S3	1	0×1001
		RX_RST_MON_S2	1	0×1001
		RX_RST_MON_S1	1	0×1001
		RX_RST_MON_S0	1	0×1001
		TX_RST_MON_S3	1	0×1001
		TX_RST_MON_S2	1	0×1001
		TX_RST_MON_S1	1	0×1001
		TX_RST_MON_S0	1	0×1001

4 Top-Level Overview (continued)

4.5 Top-Level Loopback Control Signals

All loopback control signals are generated from the top MPU block (see Section 38, Microprocessor Interface, on page 167 for more details). Some loopback configurations are controlled by the internal data MUXes.

Table 9. Loopback Control Signals

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Loopback Control	DEV_CTL_LPBK_S0 (R/W)	DEV_RSYS2TSYS_LB	4	0×B0
		DEV_TLINE2RLINE_LB	4	0×B0
		DEV_RDW2TDW_LB	4	0×B0
		DEV_TDW2RDW_LB	4	0×B0
		DEV_TRSEN2RRSDE_LB	4	0×B0

4.6 Top-Level Powerup Control Registers

The device allows the powerup of all LVDS and 3-statable input/output buffers on a per 2.5 Gbits/s basis through software control registers. The MPU clock to the SONFEC and DWFEC blocks can be inhibited. All I/O and transmission paths are in the powerdown state upon hardware and MPU software resets.

Table 10. Powerup Control Registers

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Clock Inputs	DEV_PDN_CLKIN_S0 (R/W)	DEV_RCLKSI_PDN	4	0×160
		DEV_RCLKLI_PDN	4	0×160
		DEV_TCLKLI_PDN	4	0×160
		DEV_TCLKSI_PDN	4	0×160
Data and Frame Inputs	DEV_PDN_IN_S0 (R/W)	DEV_TFRMLI_PDN	4	0×164
		DEV_TDSI_PDN	4	0×164
		DEV_RDLI_PDN	4	0×164
Output Data	DEV_PDN_OUT_S0 (R/W)	DEV_TCLKLO_PDN	4	0×168
		DEV_TDLO_PDN	4	0×168
		DEV_RCLKSO_PDN	4	0×168
		DEV_RDSO_PDN	4	0×168
TOAC Clock/Sync/Data	DEV_PDN_TOACO_S0 (R/W)	DEV_TTOAC_PDN	4	0×16D
		DEV_RTOAC_CS_PDN	4	0×16D
		DEV_RTOAC_DAT_PDN	4	0×16D
DWAC Clock/Sync/Data	DEV_PDN_DWACO_S0 (R/W)	DEV_RDW_CS_PDN	4	0×171
		DEV_RDW_DATO_PDN	4	0×171
		DEV_TDW_CS_PDN	4	0×171
SONFEC/DWFEC MPU Powerup	DEV_PDN_ICLK (R/W)	DEV_DWFEC_PCLK_PDN	1	0×16C
		DEV_SONFEC_PCLK_PDN	1	0×16C

4 Top-Level Overview (continued)

4.7 Top-Level Phase Detectors

The internal phase detector generates PUMP_UP and PUMP_DN signals for locking the Tx 666/669 MHz line clock to the Tx 622 MHz system clock with external elements such as VCO and LPF (locking the Rx 622 MHz system clock to the Rx 666/669 MHz line clock).

For various applications, reference clock (REF_CLK) and variable clock (VAR_CLK) can be selected out of any four clocks: TCLKLI, TCLKSI, RCLKLI, and RCLKSI. Output polarity (PUMP_UP, PUMP_DN) can be controlled by software.

4.7.1 PD Engine

The flip-flop based phase detector (PD) of the TFEC is used to detect the phase difference. The PD's detecting range is –2pi ~ +2pi. In its initial state, both flip-flops are cleared by RESETN, which is active-low. If REF_PHS is leading VAR_PHS, then the up pulse is output until VAR_PHS's rising edge is received. This will result in making VAR_CLK faster. If REF_PHS is lagging VAR_PHS, then the down pulse is output until VAR_PHS's rising edge is received. This will result in making VAR_CLK slower. A timing diagram is shown in Figure 25.

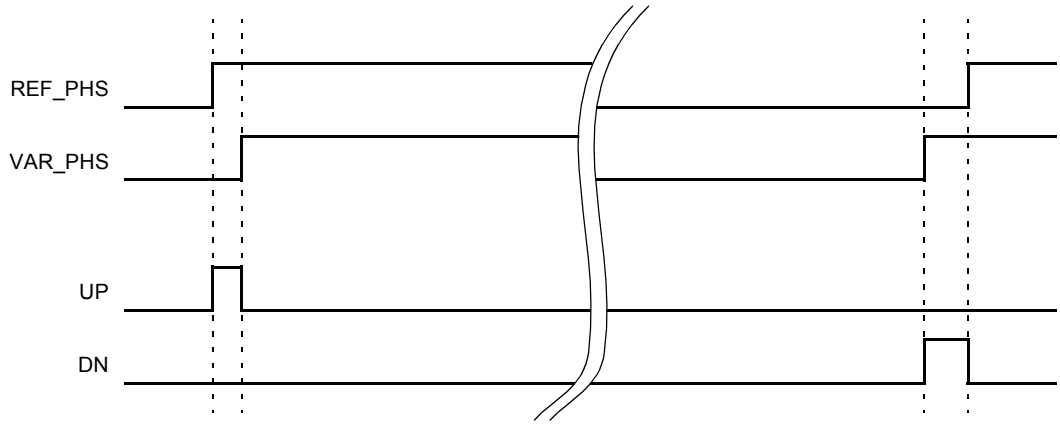


Figure 25. Timing Diagram of Phase Detector

Table 11. Phase Detector Control Registers

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Phase Detector Receive Direction Control Registers	DEV_CTL_RX_PHDET_S0 (R/W)	DEV_PHDET_RX_POL	4	0×CC
		DEV_PHDET_RX_VARDIV	4	0×CC
		DEV_PHDET_RX_REFDIV	4	0×CC
		DEV_PHDET_RX_VARSEL	4	0×CC
		DEV_PHDET_RX_REFSEL	4	0×CC
Phase Detector Transmit Direction Control Registers	DEV_CTL_TX_PHDET_S0 (R/W)	DEV_PHDET_TX_POL	4	0×D0
		DEV_PHDET_TX_VARDIV	4	0×D0
		DEV_PHDET_TX_REFDIV	4	0×D0
		DEV_PHDET_TX_VARSEL	4	0×D0
		DEV_PHDET_TX_REFSEL	4	0×D0

4 Top-Level Overview (continued)

4.8 Top-Level Line Timing Signal Reference

One external pin per 2.5 Gbits/s interface is provided for line timing reference purposes (RXREFO[4—1]). The source of these outputs is user controllable. The choices are summarized as follows:

- Free-running 50% duty cycle at 8 kHz sync (toggle output after 4860 clock cycles) derived from the RCLKLI[4—1] input clocks.
- Free-running 50% duty cycle at 8 kHz sync (toggle output after 5207 clock cycles) derived from the RCLKSI[4—1] input clocks.

The reference signals are 8 kHz only with 622/666/669 MHz input clocks.

Table 12. Line Timing Reference Select Register

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Line Timing Reference	DEV_LTIM_REF_SEL_S0 (R/W)	DEV_LTIM_REF_SEL	4	0×DC

4 Top-Level Overview (continued)

4.9 Top-Level Alarm Status Output Signals (Through GPIO)

Sixteen signals are provided, one per 2.5 Gbits/s interface per transmit and receive direction accessible through the GPIO[15:0] signals. The output of these signals is the ORing of the following alarms with their associated inhibit bits. The equations are summarized as follow:

- RX_DW_ALM[4—1] = DEV_LOC_LINE_RXCLK and NOT DEV_DWFEC_RX_LOC_INH or
  FRM_RXLOS and NOT DEV_DWFEC_RX_LOS_INH or
  FRM_RXOOF and NOT DEV_DWFEC_RX_OOF_INH or
  FRM_RXLOF and NOT DEV_DWFEC_RX_LOF_INH
- RX_SON_ALM[4—1] = DEV_LOC_SYS_RXCLK and NOT DEV_SONFEC_RX_LOC_INH or
  RX_LOS and NOT DEV_SONFEC_RX_LOS_INH or
  RX_SEF and NOT DEV_SONFEC_RX_OOF_INH or
  RX_LOF and NOT DEV_SONFEC_RX_LOF_INH
- TX_DW_ALM[4—1] = DEV_LOC_LINE_TXCLK and NOT DEV_DWFEC_TX_LOC_INH or
  FRM_TXLOS and NOT DEV_DWFEC_TX_LOS_INH or
  FRM_TXOOF and NOT DEV_DWFEC_TX_OOF_INH or
  FRM_TXLOF and NOT DEV_DWFEC_TX_LOF_INH
- TX_SON_ALM[4—1] = DEV_LOC_SYS_TXCLK and NOT DEV_SONFEC_TX_LOC_INH or
  TX_LOS and NOT DEV_SONFEC_TX_LOS_INH or
  TX_SEF and NOT DEV_SONFEC_TX_OOF_INH or
  TX_LOF and NOT DEV_SONFEC_TX_LOF_INH

Table 13. Receive/Transmit Alarm Inhibit Registers

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Receive Direction Alarm Inhibit Registers	DEV_RX_ALRMSTAT_INH_S0 (R/W)	DEV_DWFEC_RX_LOS_INH	4	0×D4
		DEV_DWFEC_RX_LOF_INH	4	0×D4
		DEV_DWFEC_RX_OOF_INH	4	0×D4
		DEV_DWFEC_RX_LOC_INH	4	0×D4
		DEV_SONFEC_RX_LOS_INH	4	0×D4
		DEV_SONFEC_RX_LOF_INH	4	0×D4
		DEV_SONFEC_RX_OOF_INH	4	0×D4
		DEV_SONFEC_RX_LOC_INH	4	0×D4
Transmit Direction Alarm Inhibit Registers	DEV_TX_ALRMSTAT_INH_S0 (R/W)	DEV_DWFEC_TX_LOS_INH	4	0×D8
		DEV_DWFEC_TX_LOF_INH	4	0×D8
		DEV_DWFEC_TX_OOF_INH	4	0×D8
		DEV_DWFEC_TX_LOC_INH	4	0×D8
		DEV_SONFEC_TX_LOS_INH	4	0×D8
		DEV_SONFEC_TX_LOF_INH	4	0×D8
		DEV_SONFEC_TX_OOF_INH	4	0×D8
		DEV_SONFEC_TX_LOC_INH	4	0×D8

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro

5.1 Strong FEC Introduction

This section provides the functional description of the strong FEC supermacro core: out-of-band. The functional description includes requirements that must be met, as derived from various specifications. The strong FEC supermacro core consists of the following:

- Elastic store (78 MHz ↔ 83 MHz) [ES] macro.
- Digital wrapper with optical channel overhead processing [DW] macro.
- Reed-Solomon (RS) macro.
- FEC/DW framer (FRM) macro.
- PRBS insert and monitor (PRBS) macro.
- Byte interleave and deinterleave (INTLV) macro.

This section contains the specifications and requirements for strong forward error correction (FEC).

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.2 Functional Description of Strong FEC

The structure of strong FEC supermacro is shown in Figure 26.

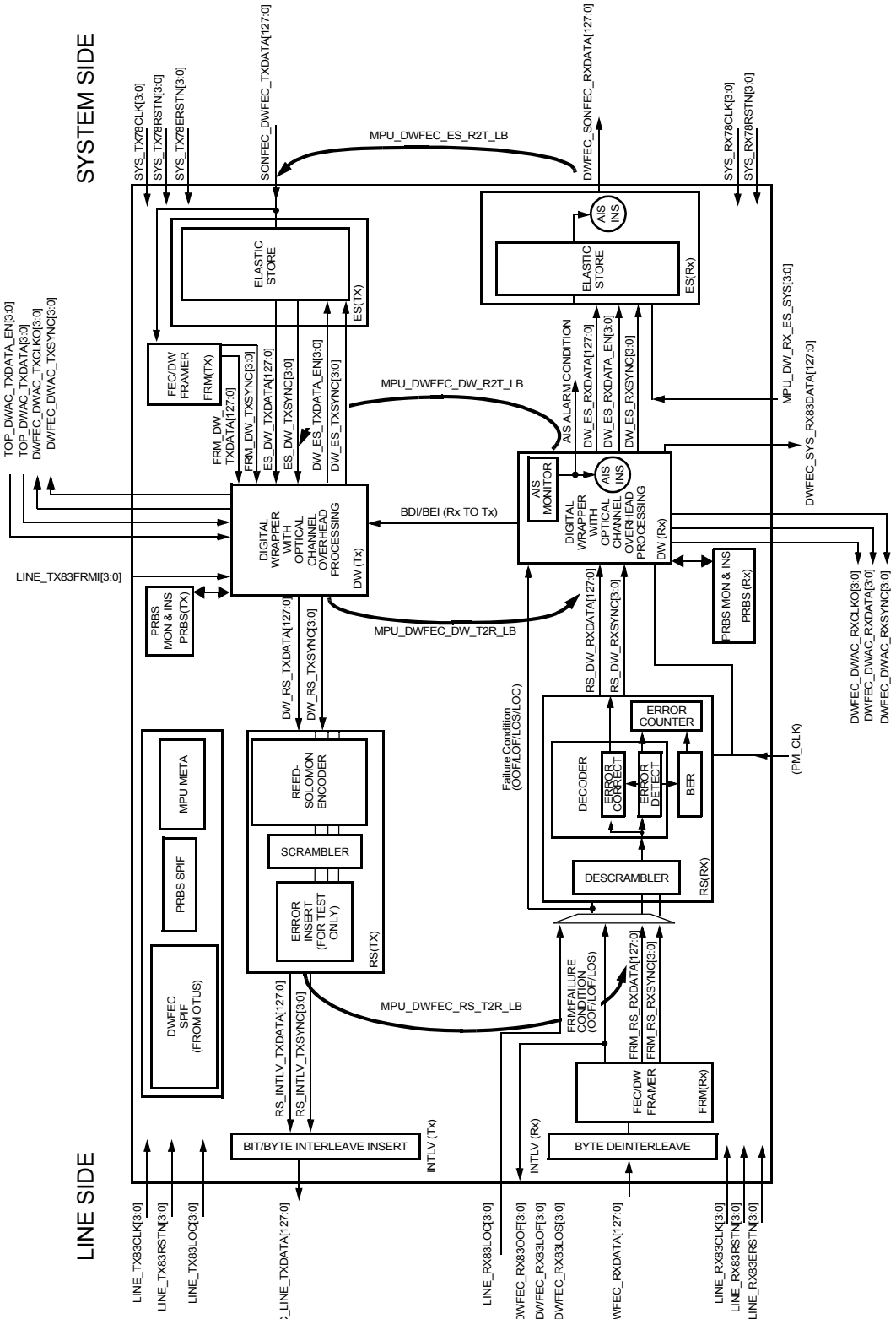


Figure 26. Strong FEC Supermacro

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.2 Functional Description of Strong FEC (continued)

5.2.1 Strong FEC Mode Description

All the strong forward error correction (FEC) code out-of-band features are supported in digital wrapper mode equipped with overhead byte insertion and monitor.

The strong FEC code, used to protect the payload/overhead information against transmission errors, is a Reed-Solomon code specified in ITU-T/G.975: RS (255, 239). There is 1 overhead byte, 238 infomation bytes (payload and fix stuff), and 16 check bytes per RS (255, 239) code block. The 16 (or 64) RS (255, 239) code blocks are interleaved to form an FEC frame. Transmission order is column-by-column, i.e., after 16 (or 64) overhead bytes are transmitted, then the first information byte of the second column will be transmitted.

The Reed-Solomon (RS) macro performs out-of-band forward error correction. The encoder generates check bytes of the quad 2488 Mbits/s signals or single 9952 Mbits/s signal. Error correction is performed in the decoder.

The RS (255, 239) code shown in Figure 27 is a nonbinary code and belongs to the family of systematic linear cyclic block codes.

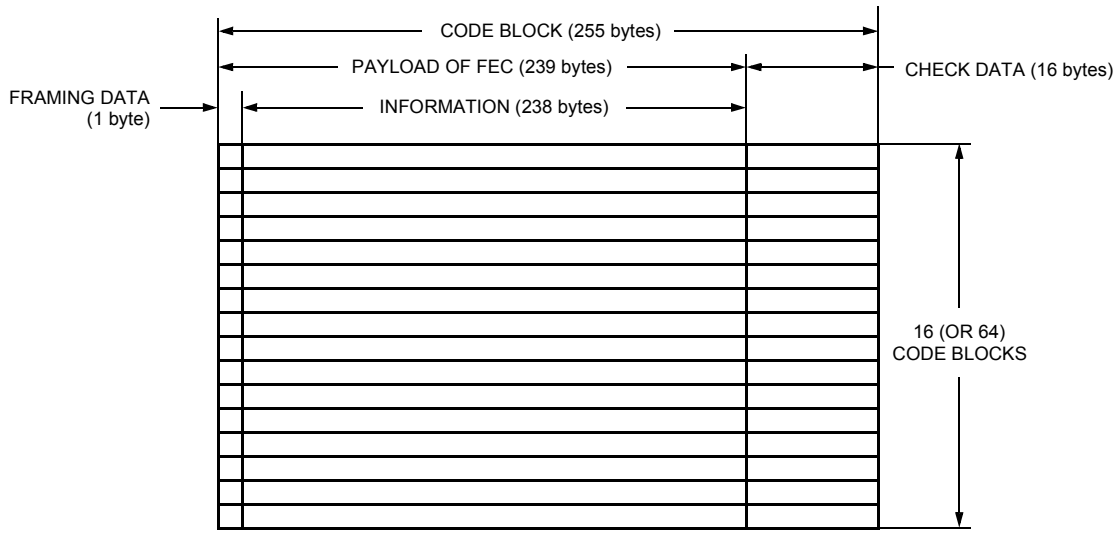


Figure 27. 16-Way (or 64-Way) Interleaved RS (255, 239) Frame

There is 1 framing byte, 238 information bytes (payload and fix stuff), and 16 check bytes per RS (255, 239) code block. In order to enhance the immunity of transmission system to burst errors, 16 (or 64) RS (255, 239) code blocks are interleaved.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.2 Functional Description of Strong FEC (continued)

There are five different modes of operation, as shown in Table 14.

Table 14. Modes of Operation

FEC Payload Type (DWFEC_TX_10G_2G5/ DWFEC_RX_10G_2G5)	Interleaving Depth (DWFEC_TX_16_64/ DWFEC_RX_16_64)	OH Processing (DWFEC_TX_FEC_DW/ DWFEC_RX_FEC_DW)
Quad 2488 Mbits/s	16	FEC Frame
		Digital Wrapper (DW) Frame
Single 9952 Mbits/s	16	FEC Frame
		Digital Wrapper (DW) Frame
	64	Digital Wrapper (DW) Frame

Note: Digital wrapper (DW) frame mode is equivalent to four multiframe FEC frames.

In quad 2.5 Gbits/s mode, the strong FEC macro processes four different 32-bit wide data streams at four different 83 MHz clocks. In 10 Gbits/s mode, the strong FEC macro processes a single 128-bit wide data stream at a single 83 MHz clock. 16-way or 64-way interleaving is programmable in 10 Gbits/s mode, while there is only 16-way interleaving in quad 2.5 Gbits/s mode.

The FEC function can be provided as a part of the digital wrapper (DW) frame. The DW frame consists of four FEC frames and each FEC frame consists of 16-way interleaving RS (255, 239) code blocks, as shown in Figure 28. In 16-way interleaving (solid arrow), the overhead columns are spaced by 4064 bytes (254 $\times$ 16 rows/FEC frame), while in 64-way interleaving (dashed arrow), all 64 overhead bytes are consecutively transmitted and repeat after 16256 bytes (4 $\times$ [254 $\times$ 16]).

When the strong FEC is in DW mode, overhead definition and processing are different from those in FEC mode. (See Table 7, Loss of Clock Registers, on page 31.)

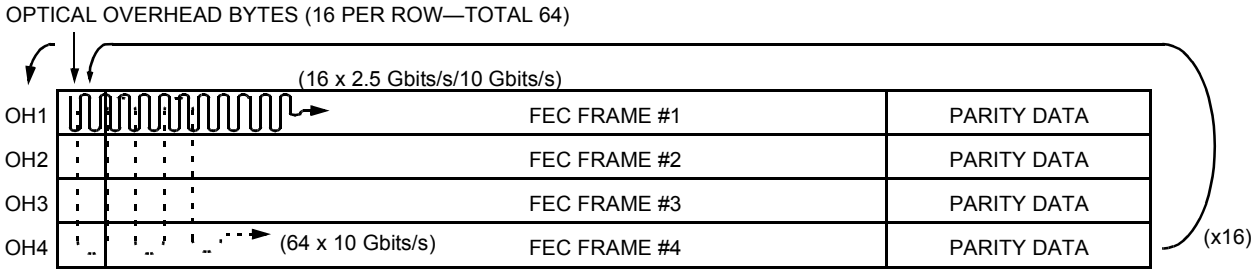


Figure 28. Digital Wrapper—Optical Channel Overhead (16-Way/64-Way Interleaving)

Table 15 on page 41 shows a summary of the DWFEC_MODE control registers.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.2 Functional Description of Strong FEC (continued)

Table 15. DWFEC_MODE Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.[1]	1st Addr† (hex)
Transmit FEC Payload Type Indication (2.5 Gbits/s or 10 Gbits/s)	DWFEC_MODE0 (R/W)	DWFEC_TX_10G_2G5	1	0×20F0
Transmit Interleaving Depth Control (16-way or 64-way for 10 Gbits/s mode only)	DWFEC_MODE0 (R/W)	DWFEC_TX_16_64	1	0×20F0
Transmit Frame Indication (FEC or DW mode)	DWFEC_MODE1_S0 (R/W)	DWFEC_TX_FEC_DW	4	0×20F1
Receive FEC Payload Type Indication (2.5 Gbits/s or 10 Gbits/s)	DWFEC_MODE0 (R/W)	DWFEC_RX_10G_2G5	1	0×20F0
Receive Interleaving Depth Control (16-way or 64-way for 10 Gbits/s mode only)	DWFEC_MODE0 (R/W)	DWFEC_RX_16_64	1	0×20F0
Receive Frame Indication (FEC or DW mode)	DWFEC_MODE1_S0 (R/W)	DWFEC_RX_FEC_DW	4	0×20F1

1. Qty. refers to the number of registers that are similar to the one shown in the table. There may be more registers to control different channels, or several registers of similar type used for a particular function.
† 1st Addr (hex) refers to the address (in hex) of the first occurrence of this type of register.

5.2.2 Strong FEC Overhead and Digital Wrapper Overhead Definition

- The entire overhead for both FEC and DW frames is programmable through the DWAC. This allows flexibility in its definition for future changes in the standards. Internally, 4 bytes can be monitored with continuous N-times detect (CNTD) monitors. These monitors can be combined in four different configurations. They can be grouped as the following:
  - Four 1-byte monitors.
  - Two 2-byte monitors.
  - One 3-byte and one 1-byte monitor.
  - One 4-byte monitor.

The multiple bytes do not need to be contiguous. Four bytes per stream can be inserted from internal registers.

Table 16 on page 42 summarizes the overhead sources for each byte in the FEC or DW frame. The FEC overhead repeats every FEC frame. The position and location of the framing bytes are provisionable from a minimum of 2 bytes to a maximum of 16 bytes in steps of 2 bytes. All other bytes that have not been assigned as framing bytes can come from the four internal registers for each 2.5 Gbits/s signal or from the DWAC. This function can also be provided through software in conjunction with the DWAC insert channel.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.2 Functional Description of Strong FEC (continued)

Table 16. FEC/Digital Wrapper Overhead Source

Row Number	Frame N	Frame N + 1	Frame N + 2	Frame N + 3
	FEC/DW Internal/DWAC	FEC (N)/DW Internal/DWAC	FEC (N)/DW Internal/DWAC	FEC (N)/DW Internal/DWAC
1	Programmable framing bytes (location/value—internal), and others from DWAC or internal registers (4 MAX).	Programmable framing bytes (location/value—internal), and others from DWAC or internal registers (4 MAX).	Programmable framing bytes (location/value—internal), and others from DWAC or internal registers (4 MAX).	Programmable framing bytes (location/value—internal), and others from DWAC or internal registers (4 MAX).
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				

Notes: Any value not from an internal register or the DWAC is set to zero.

Three BIP-8 calculations are provided over the OPUk overhead and payload bytes only; other overhead and check bits are excluded from the calculation. The calculated value can be compared against a selected overhead byte. Errors are accumulated in three different 27-bit saturating counters.

The software and hardware overhead insert priority is defined in Table 17.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

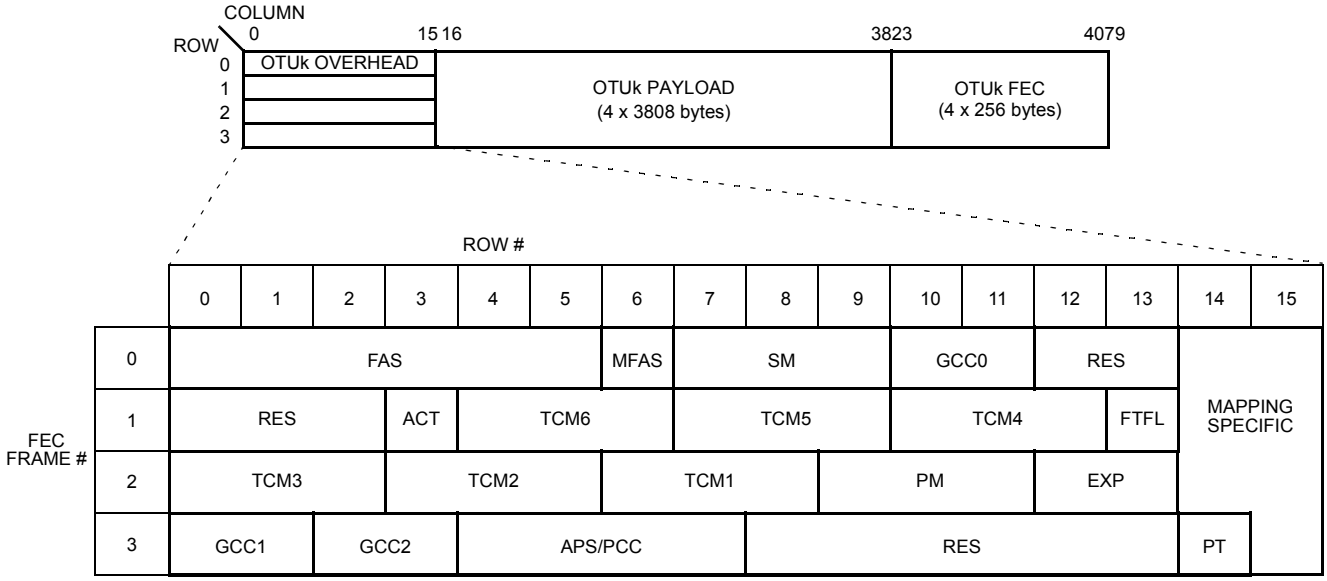
5.2 Functional Description of Strong FEC (continued)

Table 17. Software/Hardware Overhead Insert Priority

Priority (Highest = 1)	Feature
1	OA1/OA2/MFAS byte (software) (Section 7 on page 55).
2	AIS, OCI, or other fixed pattern insert (software, hardware).
3	OH3 (software).
4	OH2 (software).
5	OH1 (software).
6	OH0 (software).
7	BIP-8 insert (software).
	SM (BIP0).
	PM (BIP1).
	TCM (BIP2).
8	BEI, BDI, IAE, or STAT insert (software).
	SM (BEI0, BDI0, IAE0).
	PM (BEI1, BDI1, STAT1).
	TCM (BEI2, BDI2, STAT2).
9	DWAC insert (DWAC, default, passthrough).
10	Passthrough (see text on page 61).

Note: In 10 Gbits/s mode, only slice 0 is valid for digital wrapper overhead insert.

An OTUk overhead format is defined in Figure 29. This format (and many others) are permitted (and created) from the internal and DWAC capabilities.



Note: Column and row are defined as row and frame, respectively, for register definitions.

Figure 29. OTUk Overhead Frame Structure

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.3 Strong FEC Supermacro Clocking Domain Specification

In quad 2.5 Gbits/s mode, each slice is independent of the others. In loopback mode, clock selection is done in the top-level clock generation block.

In 10 Gbits/s mode, slice 0 acts as the master slice and all other slices sync to its frame position. In loopback mode, clock selection is done in the top-level clock generation block.

5.4 Alarm Definition Table

Table 18 summarizes all the service-affecting alarms in the device.

Table 18. DWFEC Service-Affecting Alarm Summary

Interface	Name	Definition
Receive Line	RxL_LOC	Loss-of-Clock (DEV_LOC_LINE_RXCLK)
	RxL_LOS	Loss-of-Signal (FRM_RXLOS)
	RxL_OOF	Out-of-Frame (FRM_RXOOF)
	RxL_LOF	Loss-of-Frame (FRM_RXLOF)
	RxL_BER_SD	BER Signal Degrade (RS_RXBER_SD_DET)
	RxL_BER_SF	BER Signal Fail (RS_RXBER_SF_DET)
	RxL_SM_IAE	SM Incoming Alignment Error (DW_RXIAE0_DET and DW_TXAIS_TCMSTAT_IAEINH0)
	RxL_PM(TCMi)_OCI/LCK/AIS	PM (TCMi) STAT OCI/LCK/AIS Detected (DW_RXOCI_DET)
Receive System	RxS_ES_OVRFLW	Elastic Store Overflow Indicator (ES_RX_OVERFLW_A)
	RxS_ES_UNDRFLW	Elastic Store Underflow Indicator (ES_RX_UNDRFLW_A)
Transmit System	TxS_ES_OVRFLW	Elastic Store Overflow Indicator (ES_TX_OVERFLW_A)
	TxS_ES_UNDRFLW	Elastic Store Underflow Indicator (ES_TX_UNDRFLW_A)
Transmit Line	TxL_LOC	Loss-of-Clock (DEV_LOC_LINE_TXCLK)
	TxL_LOS	Loss-of-Signal (FRM_TXLOS)
	TxL_OOF	Out-of-Frame (FRM_TXOOF)
	TxL_LOF	Loss-of-Frame (FRM_TXLOF)

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.5 OTUk Overhead Generation

Table 19. OTUk Overhead/Alarm Generation Equations

Bytes	Subfields	Generation Equation
FAS	—	MPU/DWAC
MFAS	—	0 to 255 Repeating Sequence
SM	TTI	DWAC Insert
	BIP	Calculated
	BEI	RxL_BIP[1] Errors
	BDI	OTUk_SF[2]
	IAE	OTUk_SF[2] OR TxS_CF[3]
PM	TTI	DWAC Insert
	BIP	Calculated
	BEI	RxL_BIP[1] Errors
	BDI	OTUk_SF[2]
	STAT	AIS—OTUk-AIS
		OCI—MPU Control
		LCK—MPU Control
PSI	PT	DWAC Insert
	MSI	DWAC Insert
GCC0—GCC2	—	DWAC Insert
TCMi (one at a time internally)	TTIi	DWAC Insert
	BIPi	Calculated
	BEIi	RxL_BIP[1] Errors
	BDIi	OTUk_SF[2]
	STATi	AIS—OTUk-AIS Gen
		OCI—MPU Control
		LCK—MPU Control
FTFL	—	MPU/DWAC
EXP	—	MPU/DWAC
APS/PCC	—	MPU/DWAC

1. RxL_BIP = RX_POST_CVL_U or RX_POST_CVL_L or RX_PRE_CVL_U or RX_PRE_CVL_L.
2. OTUk_SF = RxL_LOC or RxL_LOS or RxL_OOF or RxL_LOF or RxL_BER_SF or RxL_BER_SD or RxL_PM_STAT_AIS or RxL_TCMi_STAT_AIS.
3. TxS_CF (TxS_Client_Failure) = TxLOC.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.5 OTUk Overhead Generation (continued)

Table 20. Transmit OTUk Overhead Alarm Generation and Insert Control Registers

Bytes	Subfields	Generation Equation	Alarm Register	Control Register
Transmit Side				
FAS	—	MPU/DWAC Insert	—	DW_TXOA12_INS, DW_TXOA1_VAL, DW_TXOA2_VAL, DW_TXOA12_PAIRS
MFAS	—	0 to 255 Repeating Sequence (available synchronization in loopback mode), MPU/DWAC Insert	—	DW_TXMFAS_INS, DW_TXOA12_MFAS
SM	TTI	DWAC Insert	—	OH_TxL[1]
	BIP	Calculated	—	BIP_TxL[2] [0]
	BEI	RxL_BIP Errors	—	BEI_TxL[3] [0]
	BDI	OTUk_SF_TxL[4]	DW_TXBDI0_DET	BDI_TxL[5] [0]
	IAE	OTUk_IAE_TxL[6]	DW_TXIAE0_DET	DW_TXIAE0_INS, DW_TXIAE0_INH, DW_TXIAE0_LOFINH, DW_TXIAE0_OOFINH
PSI	PT	DWAC Insert	—	OH_TxL[1]
	MSI	DWAC Insert	—	OH_TxL[1]
GCC0—2	—	DWAC Insert	—	OH_TxL[1]
FTFL	—	MPU/DWAC	—	OH_TxL[1]
EXP	—	MPU/DWAC	—	OH_TxL[1]
APS/PCC	—	MPU/DWAC	—	OH_TxL[1]

1. OH_TxL = DW_TXOH[0—3]_INS, DW_TXOH[0—3]_VAL, DW_TXOH[0—3]_FRM, DW_TXOH[0—3]_ROW.
2. BIP_TxL = DW_TXBIP[0—2]_INS, DW_TXBIP[0—2]_ERRINS, DW_TXBIP[0—2]_FRM, DW_TXBIP[0—2]_ROW.
3. BEI_TxL = DW_TXBEI[0—2]_INS, DW_TXBEI[0—2]_ERRINS, DW_TXBII[0—2]_FRM, DW_TXBII[0—2]_ROW.
4. OTUk_SF_TxL = RxL_LOC or RxL_LOS or RxL_OOF or RxL_LOF or RxL_BER_SF or RxL_BER_SD or RxL_PM_STAT_AIS or RxL_TCMi_STAT_AIS.
5. BDI_TxL = DW_TXBDI[0—2]_INS, DW_TXBDI[0—2]_INH, DW_TXBDI[0—2]_LOCINH, DW_TXBDI[0—2]_OOFINH, DW_TXBDI[0—2]_LOFINH, DW_TXBDI[0—2]_LOSINH, DW_TXBDI[0—2]_SFINH, DW_TXBDI[0—2]_SDINH, DW_TXBDI[0—2]_AISINH, DW_TXBDI[0—2]_OCIINH, DW_TXBDI[0—2]_FIXINH, DW_TXBDI[0—2]_TIMERINH.
6. OTUk_IAE_TxL = RxL_OOF or RxL_LOF.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.5 OTUk Overhead Generation (continued)

Table 20. Transmit OTUk Overhead Alarm Generation and Insert Control Registers (continued)

Bytes	Subfields	Generation Equation	Alarm Register	Control Register
PM	TTI	DWAC Insert	—	OH_TxL[1]
	BIP	Calculated	—	BIP_TxL[2] [1]
	BEI	RxL_BIP Errors	—	BEI_TxL[3] [1]
	BDI	OTUk_SF_TxL[4]	DW_TXBDI1_DET	BDI_TxL[5] [1]
	STAT	AIS—OTUk-AIS Generation: OTUk_AIS_TxL = **FRM** = TxL_LOC OR TxL_LOS OR TxL_OOF OR TxL_LOF **ES** or **LB** = TxL_LOC OR DW_RXAIS_COND[7]	—	DW_TXBII1_STAT_INS, DW_TXAIS_INS, DW_TXOA12_MFAS, DW_TXLOC_AISINH, DW_TXOOF_AISINH, DW_TXLOF_AISINH, DW_TXLOS_AISINH, DW_TXRXCOND_AISINH, FTFL/TCM/GCC/APS Inhibit[8]
		OCI—MPU Control: DW_RXOCI_COND[9]	—	DW_TXOCI_INS, DW_TXRXCOND_OCIINH, FTFL/TCM/GCC/APS Inhibit[8]
		LCK—MPU Control: DW_RXFIX_COND[10]	—	DW_TXFIX_INS, DW_TXLCK_FIX, DW_TXFIX_VAL, DW_TXRXCOND_FIXINH, FTFL/TCM/GCC/APS Inhibit[8]
TCMi	TTIi	DWAC Insert	—	OH_TxL[1]
	BIPi	Calculated	—	BIP_TxL[2] [2]
	BEIi	RxL_BIP Errors	—	BEI_TxL[3] [2]
	BDIi	OTUk_SF_TxL[4]	DW_TXBDI2_DET	BDI_TxL[5] [2]
	STATi	AIS—OTUk-AIS Generation	—	DW_TXBII2_STAT_INS, FTFL/TCM/GCC/APS Inhibit[8]
		OCI—MPU Control	—	FTFL/TCM/GCC/APS Inhibit[8]
		LCK—MPU Control	—	FTFL/TCM/GCC/APS Inhibit[8]

1. OH_TxL = DW_TXOH[0—3]_INS, DW_TXOH[0—3]_VAL, DW_TXOH[0—3]_FRM, DW_TXOH[0—3]_ROW.
2. BIP_TxL = DW_TXBIP[0—2]_INS, DW_TXBIP[0—2]_ERRINS, DW_TXBIP[0—2]_FRM, DW_TXBIP[0—2]_ROW.
3. BEI_TxL = DW_TXBEI[0—2]_INS, DW_TXBEI[0—2]_ERRINS, DW_TXBII[0—2]_FRM, DW_TXBII[0—2]_ROW.
4. OTUk_SF_TxL = RxL_LOC or RxL_LOS or RxL_OOF or RxL_LOF or RxL_BER_SF or RxL_BER_SD or RxL_PM_STAT_AIS or RxL_TCMi_STAT_AIS.
5. BDI_TxL = DW_TXBDI[0—2]_INS, DW_TXBDI[0—2]_INH, DW_TXBDI[0—2]_LOCINH, DW_TXBDI[0—2]_OOFINH, DW_TXBDI[0—2]_LOFINH, DW_TXBDI[0—2]_LOSINH, DW_TXBDI[0—2]_SFINH, DW_TXBDI[0—2]_SDINH, DW_TXBDI[0—2]_AISINH, DW_TXBDI[0—2]_OCIINH, DW_TXBDI[0—2]_FIXINH, DW_TXBDI[0—2]_TIMERINH.
6. OTUk_IAE_TxL = RxL_OOF or RxL_LOF.
7. DW_RXAIS_COND = RxL_LOC or RxL_LOS or RxL_OOF or RxL_LOF or RxL_BER_SF or RxL_BER_SD or RxL_PM_STAT_AIS or RxL_TCMi_STAT_AIS or RxL_AIS_BYTE.
8. DW_TXAIS_FTFLINH, DW_TXAIS_TCMINH, DW_TXAIS_GCCINH, DW_TXAIS_APSINH.
9. DW_RXOCI_COND = RxL_PM_STAT_OCI or RxL_TCMi_STAT_OCI or RxL_OCI_BYTE.
10. DW_RXFIX_COND = RxL_PM_STAT_LCK or RxL_TCMi_STAT_LCK or RxL_FIX_BYTE.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.5 OTUk Overhead Generation (continued)

Table 21. Receive OTUk Overhead Alarm Generation and Insert Control Registers

Bytes	Subfields	Generation Equation	Alarm/Report Register	Control Register
Received Side				
FAS	—	MPU/DWAC Drop	—	—
MFAS	—	MPU/DWAC Drop	—	DW_RXOA12_MFAS
SM	TTI	Continuous N-Time Detect, MPU/DWAC Drop	OH_ALARM_RxL[4]	OH_RxL[1]
	BIP	Calculated	DW_RXBIP01_ECNT	BIP_RxL[2] [0]
	BEI	RxL_BIP Errors	DW_RXBEI01_ECNT	BEI_RxL[3] [0]
		Overwritten Before DWAC Drop (with current calculated BIP error per frame value)	—	DWAC_RXBEI0_OVWR
	BDI	Continuous N-Time Detect, MPU/DWAC	DW_RXBDI0_DET	DW_RXBDI0_CNTD
		Overwritten Before DWAC Drop (with DW_TXBDI0_DET)	—	DWAC_RXBDI0_OVWR
	IAE	Continuous N-Time Detect, MPU/DWAC	DW_RXIAE0_DET	DW_RXIAE0_CNTD
		Overwritten Before DWAC Drop (with DW_TXIAE0_DET)	—	DWAC_RXIAE0_OVWR

1. OH_RxL = DW_RXOH0123_GRP, DW_RXOH[0—3]_CNTD, DW_RXOH[0—3]_FRM, DW_RXOH[0—3]_ROW.
2. BIP_RxL = DW_RXBIP[0—2]_DISABLE, DW_RXBIP[0—2]_BIT_BLK, DW_RXBIP[0—2]_FRM, DW_TXBIP[0—2]_ROW.
3. BEI_RxL = DW_RXBEI[0—2]_DISABLE, DW_RXBEI[0—2]_BIT_BLK, DW_RXBII[0—2]_FRM, DW_TXBII[0—2]_ROW.
4. OH_ALARM_RxL = DW_RXOH[0—3]_DET, DW_RXOH[0—3]_VAL.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.5 OTUk Overhead Generation (continued)

Table 21. Receive OTUk Overhead Alarm Generation and Insert Control Registers (continued)

Bytes	Subfields	Generation Equation	Alarm/Report Register	Control Register
PM	TTI	Continuous N-Time Detect, MPU/DWAC Drop	OH_ALARM_RxL[4]	OH_RxL[1]
	BIP	Calculated	DW_RXBIP11_ECNT	BIP_RxL[2] [1]
	BEI	RxL_BIP Errors	DW_RXBEI11_ECNT	BEI_RxL[3] [1]
		Overwritten Before DWAC Drop (with current calculated BIP error per frame value)	—	DWAC_RXBEI1_OVWR
	BDI	Continuous N-Time Detect, MPU/DWAC	DW_RXBDI1_DET	DW_RXBDI1_CNTD
		Overwritten Before DWAC Drop (with DW_TXBDI1_DET)	—	DWAC_RXBDI1_OVWR
	STAT	Continuous N-Time Detect, OTUk_AIS_RxL MPU Insert and Monitor/DWAC Drop	DW_RX_BII1_STAT_NEW_A, DW_RX_BII1_STAT, DW_RXAIS_DET[5]	DW_RXBII1_STAT_CNTD, DW_RXAIS_SETCNTD, DW_RXAIS_CLRCNTD, DW_RXAIS_ROW, DW_RXAIS_FRM, DW_RXAIS_INS, DW_RXAIS_DETINH, DW_RXLOC_AISINH, DW_RXOOF_AISINH, DW_RXLOF_AISINH, DW_RXLOS_AISINH, DW_RXSF_AISINH, DW_RXSD_AISINH, FTFL/TCM/GCC/APS Inhibit[6]
		OTUk_OCI_RxL MPU Insert and Monitor/DWAC Drop	DW_RXOCI_DET[7]	DW_RXOCI_INS, DW_RXOCI_DETINH, FTFL/TCM/GCC/APS Inhibit[7]
		OTUk_LCK_RxL MPU Insert and Monitor/DWAC Drop	DW_RXFIX_DET[8]	DW_RXFIX_VAL, FTFL/TCM/GCC/APS Inhibit[7]
PSI	PT	DWAC Drop	—	—
	MSI	DWAC Drop	—	—
GCC0—2	—	DWAC Drop	OH_ALARM_RxL[4]	OH_RxL[1]

1. OH_RxL = DW_RXOH0123_GRP, DW_RXOH[0—3]_CNTD, DW_RXOH[0—3]_FRM, DW_RXOH[0—3]_ROW.
2. BIP_RxL = DW_RXBIP[0—2]_DISABLE, DW_RXBIP[0—2]_BIT_BLK, DW_RXBIP[0—2]_FRM, DW_TXBIP[0—2]_ROW.
3. BEI_RxL = DW_RXBEI[0—2]_DISABLE, DW_RXBEI[0—2]_BIT_BLK, DW_RXBII[0—2]_FRM, DW_TXBII[0—2]_ROW.
4. OH_ALARM_RxL = DW_RXOH[0—3]_DET, DW_RXOH[0—3]_VAL.
5. DW_RXAIS_DET = RxL_PM_STAT_AIS or RxL_TCMi_STAT_AIS or RxL_AIS_BYTE.
6. DW_RXAIS_FTFLINH, DW_RXAIS_TCMINH, DW_RXAIS_GCCINH, DW_RXAIS_APSINH.
7. DW_RXOCI_DET = RxL_PM_STAT_OCI or RxL_TCMi_STAT_OCI or RxL_OCI_BYTE.
8. DW_RXFIX_DET = RxL_PM_STAT_LCK or RxL_TCMi_STAT_LCK or RxL_FIX_BYTE.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.5 OTUk Overhead Generation (continued)

Table 21. Receive OTUk Overhead Alarm Generation and Insert Control Registers (continued)

Bytes	Subfields	Generation Equation	Alarm/Report Register	Control Register
TCMi	TTI	Continuous N-Time Detect, MPU/DWAC Drop	OH_ALARM_RxL[4]	OH_RxL[1]
	BIP	Calculated	DW_RXBIP21_ECNT	BIP_RxL[2] [2]
	BEI	RxL_BIP Errors	DW_RXBEI21_ECNT	BEI_RxL[3] [2]
		Overwritten Before DWAC Drop (with current calculated BIP error per frame value)	—	DWAC_RXBEI2_OVWR
	BDI	Continuous N-Time Detect, MPU/DWAC	DW_RXBDI2_DET	DW_RXBDI2_CNTD
		Overwritten Before DWAC Drop (with DW_TXBDI2_DET)	—	DWAC_RXBDI2_OVWR
	STAT	Continuous N-Time Detect, OTUk_AIS_RxL MPU Insert and Monitor/DWAC Drop	DW_RX_BII2_STAT_NEW_A, DW_RX_BII2_STAT, DW_RXAIS_DET[6]	DW_RXBII2_STAT_CNTD, FTFL/TCM/GCC/APS Inhibit[7]
		OTUk_OCI_RxL MPU Insert and Monitor/DWAC Drop	DW_RXOCI_DET[7]	FTFL/TCM/GCC/APS Inhibit[7]
		OTUk_LCK_RxL MPU Insert and Monitor/DWAC Drop	DW_RXFIX_DET[8]	FTFL/TCM/GCC/APS Inhibit[7]
FTFL	—	MPU/DWAC Drop	—	OH
EXP	—	MPU/DWAC Drop	—	OH
APS/PCC	—	MPU/DWAC Drop	OH_ALARM_RxL[4]	OH_RxL[1]

1. OH_RxL = DW_RXOH0123_GRP, DW_RXOH[0—3]_CNTD, DW_RXOH[0—3]_FRM, DW_RXOH[0—3]_ROW.
2. BIP_RxL = DW_RXBIP[0—2]_DISABLE, DW_RXBIP[0—2]_BIT_BLK, DW_RXBIP[0—2]_FRM, DW_TXBIP[0—2]_ROW.
3. BEI_RxL = DW_RXBEI[0—2]_DISABLE, DW_RXBEI[0—2]_BIT_BLK, DW_RXBII[0—2]_FRM, DW_TXBII[0—2]_ROW.
4. OH_ALARM_RxL = DW_RXOH[0—3]_DET, DW_RXOH[0—3]_VAL.
5. DW_RXAIS_DET = RxL_PM_STAT_AIS or RxL_TCMi_STAT_AIS or RxL_AIS_BYTE.
6. DW_RXAIS_FTFLINH, DW_RXAIS_TCMINH, DW_RXAIS_GCCINH, DW_RXAIS_APSINH.
7. DW_RXOCI_DET = RxL_PM_STAT_OCI or RxL_TCMi_STAT_OCI or RxL_OCI_BYTE.
8. DW_RXFIX_DET = RxL_PM_STAT_LCK or RxL_TCMi_STAT_LCK or RxL_FIX_BYTE.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.6 Strong FEC Alarm Actions

Table 22. Alarm Actions

Interface	Name	Action on Detection	
		Monitoring (All Modes)	**Maintence Signal Generation (Terminal/Regenerator/ Bidirectional Modes)**
Receive Line (OTUk input data interface)	RxL_LOC	Disable All Monitoring	ODUk-AIS if Enabled
	RxL_LOS	Disable All Monitoring	ODUk-AIS if Enabled
	RxL_OOF	Disable All Monitoring	ODUk-AIS if Enabled
	RxL_LOF	Disable All Monitoring	ODUk-AIS if Enabled
	RxL_BER_SF	Allow Monitoring	ODUk-AIS if Enabled
	RxL_BER_SD	Allow Monitoring	ODUk-AIS if Enabled
	RxL_IAE	Allow Monitoring	No Action
	RxL_TCMi_STAT_AIS	Disable All Monitoring	Regenerate ODUk-X Maintenance Signal if Enabled
	RxL_TCMi_STAT_OCI		
	RxL_TCMi_STAT_LCK		
	RxL_PM_STAT_AIS	Disable All Monitoring	Regenerate ODUk-X Maintenance Signal if Enabled
	RxL_PM_STAT_OCI		
	RxL_PM_STAT_LCK		
Receive System (client output data interface)	RxS_ES_OVRFLW	NA	No Action
	RxS_ES_UNDRFLW	NA	No Action
Transmit System (client input data interface)	TxS_ES_OVRFLW	NA	No Action
	TxS_ES_UNDRFLW	NA	No Action
Transmit Line (OTUk output data interface)	TxL_LOC	NA	ODUk-AIS if Enabled
	TxL_OOF (bidirectional mode only)	NA	ODUk-AIS if Enabled
	TxL_LOF (bidirectional mode only)	NA	ODUk-AIS if Enabled
	TxL_LOS (bidirectional mode only)	NA	ODUk-AIS if Enabled

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.7 Overview, General Functional Description, and Block Diagram of Strong FEC Supermacro Submacros

5.7.1 Elastic Store (ES) Macro

The ES macro performs rate conversion between two different clocks. One clock (83 MHz) is faster than the other (78 MHz), but the effective clock rates are the same because the faster clock has overhead bytes; therefore, there is no stuffing mechanism.

The transmit ES buffers system rate data and outputs gapped line rate data to create space for FEC/DW overhead and FEC check bytes. Data arrives at the transmit ES grouped as 32 bits in each slice. Each group of 32 bits is written into the associated ES location (128 locations $\times$ 32 bits). In 2.5 Gbits/s mode, data is read from the ES by 238 clock cycles per 255 clock cycles. In 10 Gbits/s mode, data can either be read by 237 or 238 clock cycles per 255 clock cycles depending on the phase detector divide ratio settings.

The receive ES buffers gapped data at the line rate and outputs data at the system rate to absorb clock gapping of the FEC/DW overhead and FEC check bytes. Data arrives to the receive ES grouped as 32 bits in each slice. Each group of 32 bits is written into the associated ES location (128 locations $\times$ 32 bits) by 238 clock cycles (for 2.5 Gbits/s mode) or 237/238 clock cycles (depending on the phase detector divide ratio settings for 10 Gbits/s FEC/DW frame) per 255 clock cycles per the system rate clock. An optional fixed stuff row can be placed in row 120 of 255 in 10 Gbits/s mode.

5.7.2 DW Macro

This block controls the creation of the FEC/DW frame by controlling the read/write pointers to the elastic store. This control allows gap to be inserted into the outgoing frame for overhead, stuff column, and check byte insertion. The overhead is provisionable through internal registers or through the DWAC channel.

5.7.3 Reed-Solomon (RS) Macro

The RS macro performs out-of-band forward error correction using the RS (255, 239) code. The RS encoder accepts 239 bytes of payload and overhead data followed by 16 bytes of all-zero check bytes, and generates 16 bytes of check data. The RS decoder detects and corrects transmission errors, then calculates and reports the incoming BER based on the exact number of corrected bits.

5.7.4 Scrambler/Descrambler Macro

The scrambler/descrambler optionally scrambles/descrambles data. The scrambling sequence can be selected between two different polynomials: $x^7 + x + 1$ or $x^{16} + x^{12} + x^3 + x + 1$. Once a scrambling/descrambling pattern is requested, the entire frame (with the exception of the framing bytes) is scrambled/descrambled by the selected polynomial, starting at each frame on the first bit which follows the last framing byte.

5 Strong FEC (Reed-Solomon and Digital Wrapper) Supermacro (continued)

5.7 Overview, General Functional Description, and Block Diagram of Strong FEC Supermacro Submacros (continued)

5.7.5 Error Insert Macro

The error insert macro inserts various types of errors for RS codec testing. Errors can be inserted in 32-bit format in quad 2.5 Gbits/s mode, or in 128-bit format in 10 Gbits/s mode.

5.7.6 Framer Macro

Data arrives to the FEC/DW framer grouped as 4 slices of 4 bytes (32 bits) in quad 2.5 Gbits/s mode, and 16 bytes (128 bits) in single 10 Gbits/s mode. The FEC/DW framer performs the following:

- Framing
- Detects LOS, OOF, LOF
- Descrambles the data
- Inserts AIS

In 10 Gbits/s mode, a single FEC/DW framer works on a 128-bit wide data bus. In quad 2.5 Gbits/s mode, a separate FEC/DW framer works on each 32-bit wide data bus; therefore, there are four separate FEC/DW framers for four different slices.

5.7.7 Interleaver/Deinterleaver Macro

The RS encoder/decoder performs byte interleaving/deinterleaving of code blocks in order to enhance the immunity of transmission system to burst errors (in byte manner).

6 Strong FEC Supermacro Elastic Store (Transmit Direction)

6.1 Elastic Store (Tx) Functional Description

The transmit ES buffers system rate data and outputs gapped line rate data to allocate space for FEC/DW overhead and FEC check bytes. It is assumed that the effective clocks of both write and read are the same; therefore, there is no stuffing mechanism. Data arrives to the transmit ES grouped as 32 bits in each slice. Each group of 32 bits is always written into the associated ES location (128 locations × 32 bits), even if the ES will overflow/underflow. Data is read from the ES by the line rate clock for 238 or 237 out of 255 clock cycles for each FEC frame.

The relationship between read and write address is controlled in order to simultaneously minimize signal delay and to guarantee data integrity. At the initial state, or after overflow/underflow, the read address is automatically reset to the predefined position (32 locations ahead of the write address), when the first sync pulse is received.

In 10 Gbits/s mode, all four elastic stores work in synchronization.

In some applications, the transmit ES is disabled and data is bypassed. In this case, the overflow/underflow alarm is not declared. The ES can be forced to restart by software control.

Table 23. Elastic Store (Tx) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Tx ES Overflowing Interrupt Alarm	ES_ALARM_S0 (W1C)	ES_TX_OVERFLW_A	4	0×201C
Tx ES Underflowing Interrupt Alarm	ES_ALARM_S0 (W1C)	ES_TX_UNDRFLW_A	4	0×201C
Tx ES Overflowing Interrupt Alarm Mask	ES_MASK_S0 (R/W)	ES_TX_OVERFLW_M	4	0×2058
Tx ES Underflowing Interrupt Alarm Mask	ES_MASK_S0 (R/W)	ES_TX_UNDRFLW_M	4	0×2058
Tx ES Forced Restart	ES_CTL_S0 (R/W)	ES_TX_RESTART	4	0×2130

7 Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF)

7.1 Functional Description of FEC/DW Framer

The FEC/DW framer consists of three subblocks: a loss-of-signal (LOS) detector, FEC/DW framer (OA1 and OA2), and a frame state machine (for detection of OOF and LOF). The LOS detector monitors the data for loss of signal (fixed all-zeros pattern over a programmable time interval). The FEC/DW framer block allows the framing on a DW or FEC frame based on a programmable value/number of OA1 and OA2 bytes. The LOF detector monitors the OOF state for a continuous in-frame or out-of-frame state.

7.1.1 Loss-of-Signal (LOS) Detector

The data is monitored by the LOS detector macro for loss of signal (LOS). In 10 Gbits/s mode, there is a single LOS detector. In quad 2.5 Gbits/s mode, there is a separate LOS detector on each quad input. On powerup, an LOS defect is declared if all-zeros data is received continuously for a programmable time threshold. This time threshold is provisionable through the loss-of-signal (LOS) threshold register (FRM_TX_CTL_LOSDET, 0x22B4) for each slice. The default value is 0 (disabled).

Assuming that the client signal is operating at SONET or SDH clock rates, the threshold can be set to any value from 0 µs (i.e., LOS detection disabled) to 98.32 µs, with a resolution of 96.02 ns. In the event that other line clock rates are used, the resolution of the threshold is determined by multiplying the period of the line clock by 64.

An LOS defect is subsequently cleared when two successive valid framing patterns are received with no period of all zeros exceeding the time threshold. Detection of an LOS defect is indicated by a latched alarm status bit and a persistency bit.

Four LOS detectors are implemented, corresponding to each slice. In quad 2.5 Gbits/s mode, all the LOS detectors function independently on 32 bits of data. In 10 Gbits/s mode, the slice 0 LOS detector functions on 128 bits of data and the other LOS detectors are disabled. If the LOS detect threshold is set to zero, LOS detection is disabled and LOS and LOS_PM outputs are deasserted regardless of the LOS condition. The slice 0 LOS detector pin description is given in Table 24.

If an optical transponder is connected to the receive line interface, the most appropriate method to declare LOS is by monitoring the power level monitor of the received signal from the transponder. In some transponders, the amplifier gain is high enough to cause the LVDS receive data lines to move above zero, even when there is no optical output. If this should occur, the TFEC0410G may not indicate an LOS defect. This is not a deficiency of the device, but a characteristic of the LOS detection methods. If an optical transponder is used, the LOS detector of the TFEC0410G monitors the connection from the transponder to the receive line interface. The LOS detector in the TFEC0410G is appropriate for electrical monitoring of LOS.

Table 24. LOS Detector Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
LOS Detect Time Threshold	FRM_TX_CTL_LOSDET_S0 (R/W)	FRM_TXLOS_DET	4	0×22B4
LOS Interrupt Alarm	FRM_ALARM_S0 (W1C)	FRM_TXLOS_A	4	0×202C
LOS Alarm Mask	FRM_MASK_S0 (R/W)	FRM_TXLOS_M	4	0×2068
LOS Persistency	FRM_PERSIST_S0 (RO)	FRM_TXLOS_P	4	0×209C
LOS State	FRM_STATE_S0 (RO)	FRM_TXLOS	4	0×20CC

7 Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF) (continued)

7.1 Functional Description of FEC/DW Framer (continued)

7.1.2 Framer (A1 and A2)

In 10 Gbits/s mode, framing is performed on a single channel. In quad 2.5 Gbits/s mode, framing is performed on four independent channels.

The frame alignment is found by searching for the OA1 and OA2 bytes contained in the FEC/DW (OCh) signal. The framing pattern searched for, or checked, may be a subset of the OA1 and OA2 bytes contained in the FEC/DW (OCh) signal. The framed signal is continuously checked with the presumed frame start position for the alignment. If in the in-frame state (OOF = 0), the maximum out-of-frame (OOF) detection time will be equal to a programmable period of FEC/DW (OCh) frames (superframes). If in the OOF state, the maximum frame alignment time will be equal to a programmable number of the FEC/DW (OCh) frame (superframe) periods of an error-free signal with no emulated framing patterns. The number of OA1 and OA2 bytes are programmable independently while in the in-frame state and out-of-frame state. The framer outputs frame-aligned data and an 8 kHz sync and reference (free-running) signals. The OA1 pattern cannot be aliased within the OA1 and OA2 pattern boundary. Also, under no circumstances can the two patterns, OA1 and OA2, be the same.

Four framers are implemented, corresponding to each slice. In quad 2.5 Gbits/s mode, all framers function independently on 32 bits of data. In 10 Gbits/s mode, the slice 0 framer functions on 128 bits of data and the other framers are disabled. If the FRM_DIS signal is asserted, framing is disabled. In loopback mode, the framer outputs are disabled and the output sync follows the incoming sync.

7.1.2.1 Frame State Machine (FSM)

The FSM is responsible for bit/byte rotation and for determining the out-of-frame state (OOF) and loss-of-frame (LOF) alarms for each channel. The FSM comes out of reset in the OOF state with the OOF and LOF alarms active. The framining parameters are summarized below:

1. OA1, OA2 programmable value per slice (MPU_DW_FRM_OA1_VAL[3—0][7:0], MPU_DW_FRM_OA2_VAL[3—0][7:0]).
2. Number of framing pattern pairs (OA1/OA2) in the FEC/DW (OCh) frame (MPU_DW_FRM_OA12_PAIRS[3—0][2:0]; see Table 25).
3. Number of framing pattern pairs (OA1/OA2) used to transition between out-of-frame to in-frame state (OOF, 1 $\Rightarrow$ 0), MPU_DW_FRM_OA12_PAIRCLR[3—0][2:0].
4. Number of framing pattern pairs (OA1/OA2) used to transition between in-frame to out-of-frame state (OOF, 0 $\Rightarrow$ 1), MPU_DW_FRM_OA12_PAIRSET[3—0][2:0].
5. Number of valid consecutive framing pairs (OA1/OA2) required to transition from out-of-frame to the in-frame state (MPU_DW_FRM_OOF_CLR[3—0][4:0]). When a portion of the frame alignment word is used, the pattern is always equally centered around the OA1/OA2 border.
6. Number of valid consecutive framing patterns (OA1/OA2) required to transition from in-frame to the out-of-frame state (MPU_DW_FRM_OOF_SET[3—0][4:0]). When a portion of the frame alignment word is used, the pattern is always equally centered around the OA1/OA2 border.

7 Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF) (continued)

7.1 Functional Description of FEC/DW Framer (continued)

Table 25. Frame Alignment (OA1, OA2) Pattern Positions

Value (pairs)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0x0 (1)[1]	OA1	OA2	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0x1 (2)	OA1	OA1	OA2	OA2	—	—	—	—	—	—	—	—	—	—	—	—
0x2 (3)[2]	OA1	OA1	OA1	OA2	OA2	OA2	—	—	—	—	—	—	—	—	—	—
0x3 (4)	OA1	OA1	OA1	OA1	OA2	OA2	OA2	OA2	—	—	—	—	—	—	—	—
0x4 (5)	OA1	OA1	OA1	OA1	OA1	OA2	OA2	OA2	OA2	OA2	—	—	—	—	—	—
0x5 (6)	OA1	OA1	OA1	OA1	OA1	OA1	OA2	OA2	OA2	OA2	OA2	OA2	—	—	—	—
0x6 (7)	OA1	OA1	OA1	OA1	OA1	OA1	OA1	OA2	OA2	OA2	OA2	OA2	OA2	OA2	—	—
0x7 (8)	OA1	OA1	OA1	OA1	OA1	OA1	OA1	OA1	OA2	OA2	OA2	OA2	OA2	OA2	OA2	OA2

1. 0x0 (1) is the default value.
2. 0x2 (3) is defined by ITU-T/G.709.

The following example defines a frame pattern that contains three OA1 and three OA2 frame alignment words (A in Figure 30, Framing Algorithm with Example, on page 58) with values 0xF6 and 0x28 (B, C), respectively. All six framing values are required to be error free for two consecutive frames for transition from the out-of-frame state to the in-frame state (D). After six consecutive mismatches (E), the out-of-frame state is entered. Only two of the frame alignment words (containing the OA1/OA2 border) are tested for mismatches. Note that the framer will not generate sync pulses during the OOF state.

Note: The minimum OOF set value is 0×2. If OOF_SET is programmed to 0×0 or 0×1, OOF will be declared after two consecutive mismatches.

7 Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF) (continued)

7.1 Functional Description of FEC/DW Framer (continued)

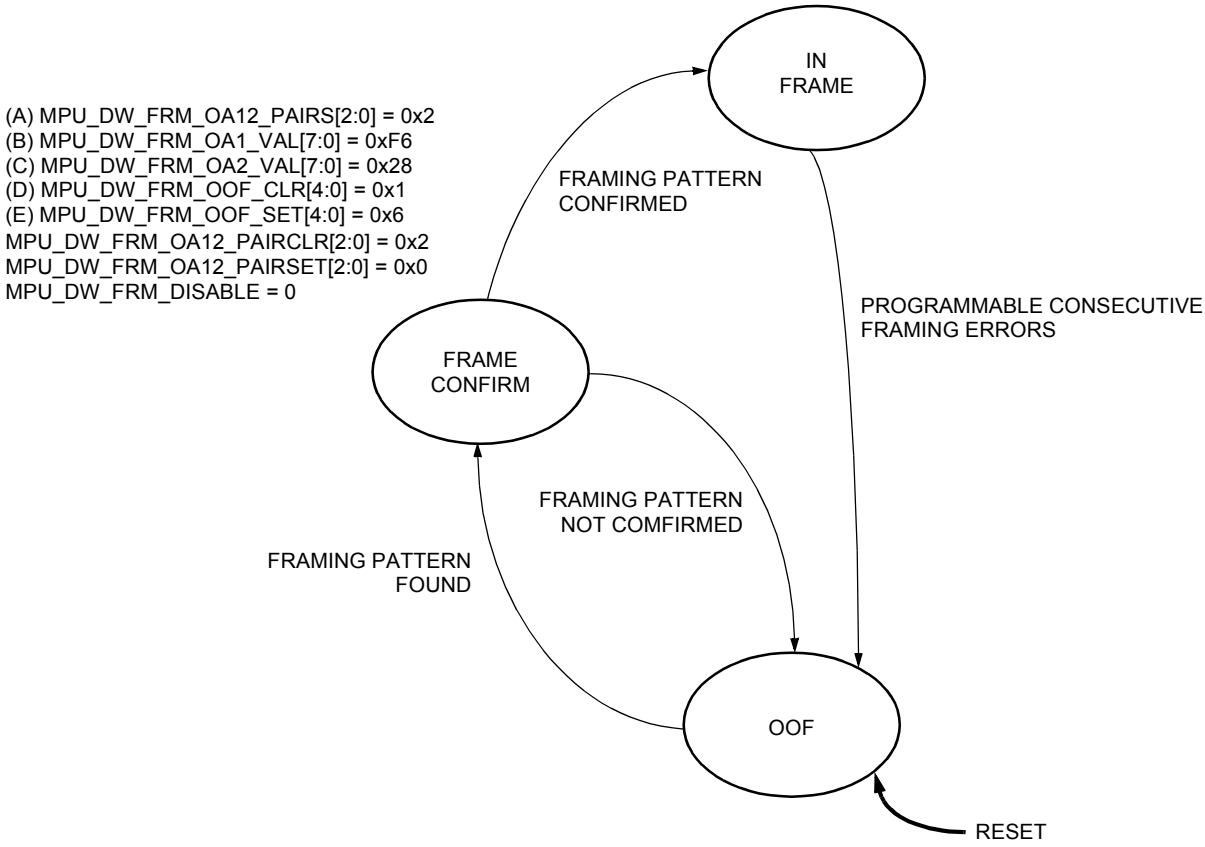


Figure 30. Framing Algorithm with Example

7 Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF) (continued)

7.1 Functional Description of FEC/DW Framer (continued)

Table 26. Framer Control Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Framer Disable	FRM_TX_CTL_OOF_3_S0 (R/W)	FRM_TX_DISABLE	4	0×22C0
OA1 Frame Byte Value	FRM_TX_CTL_OA12_S0 (R/W)	FRM_TXOA1_VAL	4	0×22B8
OA2 Frame Byte Value	FRM_TX_CTL_OA12_S0 (R/W)	FRM_TXOA2_VAL	4	0×22B8
Number of Repeat OA1 Bytes (same as OA2) Ex: 0 = One OA1, one OA2s 7 = Eight OA1s, eight OA2s See Table 25 on Page 57	FRM_TX_CTL_OA12_PAT_3_S0 (R/W)	FRM_TXOA12_PAIRS	4	0×22BC
Number of Framing Pattern Pairs (OA1/OA2) Used to Transition Between Out-of-Frame to In-Frame State (OOF, 1 → 0)	FRM_TX_CTL_OA12_PAT_3_S0 (R/W)	FRM_TXOA12_PAIRCLR	4	0×22BC
Number of Framing Pattern Pairs (OA1/OA2) Used to Transition Between In-Frame to Out-of-Frame State (OOF, 0 → 1)	FRM_TX_CTL_OA12_PAT_3_S0 (R/W)	FRM_TXOA12_PAIRSET	4	0×22BC
Out-of-Frame Set	FRM_TX_CTL_OOF_3_S0 (R/W)	FRM_TXOOF_SET	4	0×22C0
Out-of-Frame Clear	FRM_TX_CTL_OOF_3_S0 (R/W)	FRM_TXOOF_CLR	4	0×22C0
Out-of-Frame Interrupt Alarm	FRM_ALARM_S0 (W1C)	FRM_TXOOF_A	4	0×202C
Out-of-Frame Interrupt Alarm Mask	FRM_MASK_S0 (R/W)	FRM_TXOOF_M	4	0×2068
Out-of-Frame Persistency	FRM_PERSIST_S0 (RO)	FRM_TXOOF_P	4	0×209C
Out-of-Frame State	FRM_STATE_S0 (RO)	FRM_TXOOF	4	0×20CC

7 Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF) (continued)

7.1 Functional Description of FEC/DW Framer (continued)

7.1.3 Loss-of-Frame (LOF) Detector

The LOF alarm is asserted if OOF persists for a programmable number of frames. The LOF alarm is terminated a programmable number of frames after the OOF alarm is terminated. An interrupt alarm, persistency, and state are provided per slice.

Table 27. Loss-of-Frame Control Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Loss-of-Frame Set	FRM_RX_CTL_LOF_2_S0 (R/W)	FRM_TXLOF_SET	4	0×22C4
Loss-of-Frame Clear	FRM_RX_CTL_LOF_2_S0 (R/W)	FRM_TXLOF_CLR	4	0×22C4
Loss-of-Frame Interrupt Alarm	FRM_ALARM_S0 (W1C)	FRM_TXLOF_A	4	0×202C
Loss-of-Frame Interrupt Alarm Mask	FRM_MASK_S0 (R/W)	FRM_TXLOF_M	4	0×2068
Loss-of-Frame Persistency	FRM_PERSIST_S0 (RO)	FRM_TXLOF_P	4	0×209C
Loss-of-Frame State	FRM_STATE_S0 (RO)	FRM_TXLOF	4	0×20CC

7.1.4 Provisioning and Alarm Operation in 10 Gbits/s Mode

Only slice 0 alarms and control parameters are valid in 10 Gbits/s mode. All other slice information is ignored and all alarms from slice 1, slice 2, and slice 3 are disabled.

8 Digital Wrapper Insert

8.1 Functional Description of Digital Wrapper Insert

The digital wrapper insert is used for overhead processing before the Reed-Solomon (RS) encoder (check byte insert).

All overhead and data can be retimed and passed through by enabling the control bit, DW_TX_PASSTHRU. Passthrough mode is only available when the data is coming from the transmit framer or is looped back from the receive direction. See Table 17, Software/Hardware Overhead Insert Priority, on page 43 and Figure 26, Strong FEC Supermacro, on page 38 for more information.

Table 28. Digital Wrapper Input MUX Control Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Transmit input MUX. The DW insert block will take the following data to process: 0 = ES_DW_TXDATA (from Tx ES). 1 = FRM_DW_TXDATA (from Tx framer).	DWFEC_MUX_S0 (R/W)	DW_TX_ES_FRM	4	0×20F5
Transmit overhead passthrough mode: 0 = Disable. 1 = Enable. Overhead passthrough should only be enabled when data is coming from the Tx framer or from the Rx direction loopback (RDW2TDW_LB).	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TX_PASSTHRU	4	0×2178

All FEC/DW frame overhead insert functions supported by the DW in the transmit direction are summarized as follows:

- Frame bytes insert.
- Multiframe byte (free-running) insert.
- Internal FEC overhead bytes insert.
- BIP-8 calculation.
- BEI/BDI insert and monitor.
- IAE/STAT insert and monitor.
- AIS, OCI, or other pattern insert.
- DWAC insert.
- PRBS payload insert.
- Check bits insert.
- Fixed stuff column enable/disable.

The 128-bit input data can be selected from either ES_DW_TXDATA[127:0] or FRM_DW_TXDATA[127:0] via the microprocessor.

In loopback mode, the 128-bit input data can be selected from the output of the receive direction (DW_ES_RXDATA) to pass through to the digital wrapper insert, which is controlled by the top-level input pin (MPU_DW_R2T_LB). The digital wrapper insert should synchronize its frame by monitoring DW_ES_RXSYNC.

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.1 Framing Bytes Insert

The DW macro allows programmable framing bytes (OA1, OA2) in both FEC frame and DW (multiframe) mode. For G.709 compliance, the framing bytes should be set as follows:

- Set the OA1 byte to 0xF6.
- Set the OA2 byte to 0x28.
- Set the insertion count to 0x2.
- Set the number of MFAS bytes to 0x1.

In the transmit direction, a free-running counter generates the MFAS bytes. In loopback or bidirectional mode, the MFAS counter is synchronized to the incoming MFAS. The DWAC sync output is asserted for two DWAC clock cycles wide to indicate that the current overhead is for MFAS 0x0. (See Figure 40 on Page 79.)

All framing bytes can be inserted by either the DWAC insert channel or by one or all of the overhead (OHx) insert bytes. When neither OA1 nor OA2 is inserted, either the DWAC insert byte, overhead (OHx) insert bytes, or default will be inserted.

DW_TXDEFAULT will set all overhead bytes to a default value of all 1s or 0s if no specific overhead insertion is enabled.

Table 29. Framing Byte (OA1 and OA2) Insert Control Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
OA1 OA2 Frame Byte Insert Enable	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXOA12_INS	4	0×2178
OA1 Frame Byte Value	DW_TX_CTL_OA12_S0 (R/W)	DW_TXOA1_VAL	4	0×217C
OA2 Frame Byte Value	DW_TX_CTL_OA12_S0 (R/W)	DW_TXOA2_VAL	4	0×217C
Number of Repeat OA1 and OA2 Byte Pairs (see Table 25 on Page 57)	DW_TX_CTL_OA12_PAT_S0 (R/W)	DW_TXOA12_PAIRS	4	0×2180
Insert Free-Running MFAS Counter	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXMFAS_INS	4	0×2514
Default Value for Overhead Bytes (all 0s or all 1s)	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXDEFAULT	4	0×2178
Sync MFAS Counter to Incoming MFAS Value Enable	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXMFAS_SYNC	4	0×2514

8 Digital Wrapper Insert (continued)

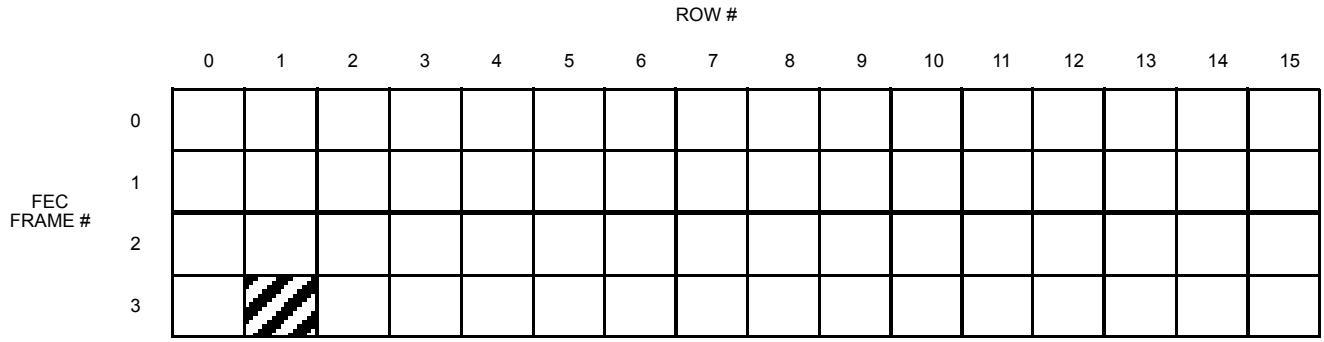
8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.2 Internal FEC Overhead Byte Insert (OH0 to OH3)

There are four internal programmable bytes (OH0, OH1, OH2, OH3) that can be inserted or overwritten in digital wrapper overhead locations for each slice.

Each overhead (OHx) can be inserted by programming its 8-bit wide value. The location of the overhead byte can be specified by using frame location and row location.

EXAMPLE: INSERT OH0 VALUE 0×20 INTO GCC1, BYTE 0; OH LOCATION IS FRM 3, ROW 1
DW_OH0_INS[0] = 1
DW_TXOH0_VAL[0][7:0] = 0×20
DW_TXOH0_FRM[0][1:0] = 01 (0×1)
DW_TXOH0_ROW[0]03:0] = 0100 (0×4)



Note: Column and row are defined as row and frame, respectively, for register definitions.

Figure 31. Internal DWFEC Overhead Byte Insert Programmable Location Example

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

Table 30. Transmit DW OH0 to OH3 Bytes Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Overhead Byte Insertion Enable	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXOH0_INS	4	0×2178
Overhead Byte Insertion Value	DW_TX_CTL_OH0_2_S0 (R/W)	DW_TXOH0_VAL	4	0×2184
Overhead Byte Insertion Frame Location (DW mode only)	DW_TX_CTL_OH0_2_S0 (R/W)	DW_TXOH0_FRM	4	0×2184
Overhead Byte Insertion Row Location	DW_TX_CTL_OH0_2_S0 (R/W)	DW_TXOH0_ROW	4	0×2184
Overhead Byte Insertion Enable	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXOH1_INS	4	0×2178
Overhead Byte Insertion Value	DW_TX_CTL_OH1_2_S0 (R/W)	DW_TXOH1_VAL	4	0×2188
Overhead Byte Insertion Frame Location (DW mode only)	DW_TX_CTL_OH1_2_S0 (R/W)	DW_TXOH1_FRM	4	0×2188
Overhead Byte Insertion Row Location	DW_TX_CTL_OH1_2_S0 (R/W)	DW_TXOH1_ROW	4	0×2188
Overhead Byte Insertion Enable	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXOH2_INS	4	0×2178
Overhead Byte Insertion Value	DW_TX_CTL_OH2_2_S0 (R/W)	DW_TXOH2_VAL	4	0×218C
Overhead Byte Insertion Frame Location (DW mode only)	DW_TX_CTL_OH2_2_S0 (R/W)	DW_TXOH2_FRM	4	0×218C
Overhead Byte Insertion Row Location	DW_TX_CTL_OH2_2_S0 (R/W)	DW_TXOH2_ROW	4	0×218C
Overhead Byte Insertion Enable	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXOH3_INS	4	0×2178
Overhead Byte Insertion Value	DW_TX_CTL_OH3_2_S0 (R/W)	DW_TXOH3_VAL	4	0×2190
Overhead Byte Insertion Frame Location (DW mode only)	DW_TX_CTL_OH3_2_S0 (R/W)	DW_TXOH3_FRM	4	0×2190
Overhead Byte Insertion Row Location	DW_TX_CTL_OH3_2_S0 (R/W)	DW_TXOH3_ROW	4	0×2190

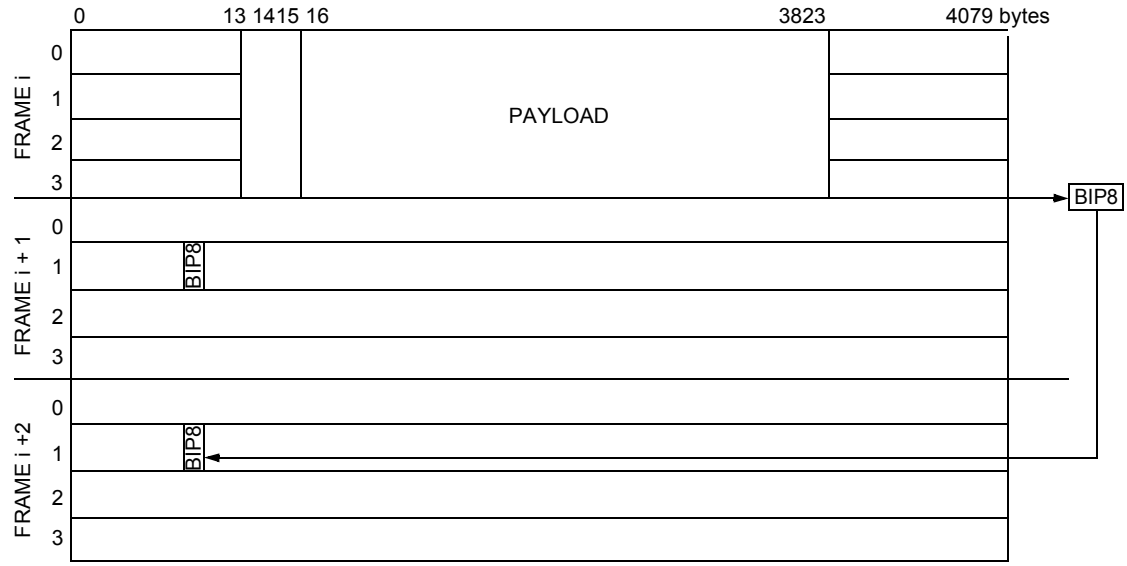
Note: Refer to Table 12 on page 35 for the priority of overhead byte insert. In FEC frame, only row location control registers are used.

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.3 BIP-8 Calculation

Three BIP-8 calculations are provided every frame (OPU overhead (row 14—15), payload, and fix stuff; other bytes are excluded from calculation). The bit interleaved parity code (BIP-8) byte is even parity, which is placed in the BIP byte of the second frame following the frame as shown in Figure 32.



Note: Refer to Table 17 on page 43 for the priority of overhead byte insert. In FEC frame, only row location control registers are used.

Figure 32. G.709 BIP-8 Computation and Transport for One Connection Monitoring Level

The BIP-8 byte can be inserted via microprocessor control. The BIP-8 byte can be inserted in both FEC and DW frames by specifying the location (time slot) of any frame. This is identical to the example in Figure 32. BIP-8 insert is suggested to be inserted at the corresponding locations of the SM/TCM and PM bytes.

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.4 General Definition of BEI, BDI, and IAE Insert and Monitor

Three BII bytes can be inserted in every frame. A BII byte includes BEI (the number of BIP errors per frame in the receive direction) and BDI interrupt alarm state. The BEI value is between 0 to 8 in each frame. When BEI insert is disabled, BEI location is set to zero. When BEI error insert is enabled, BEI location is set to a nonzero fixed value.

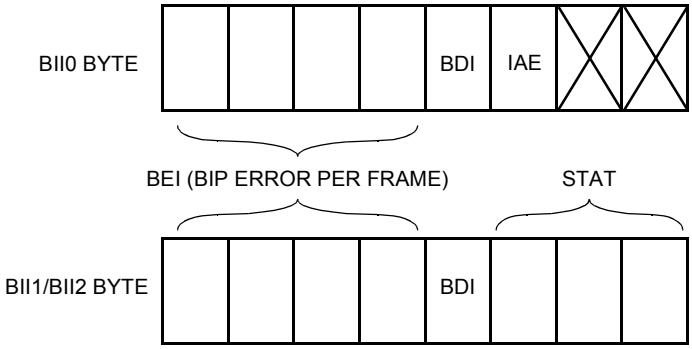


Figure 33. BII Byte Description

Each BDI-failure (DW_TXBDI0_INS, DW_TXBDI1_INS, and DW_TXBDI2_INS) contributes to a state bit. Transmit BDI-failure is inserted into the data signal using the following equation:

- DW_TXBDI_DET = (LINE_RX83LOC and not (DW_TXBDI_LOCINH)) or—input loss of clock
  (FRM_RXLOS and not (DW_TXBDI_LOSINH)) or—loss-of-signal
  (FRM_RXOOF and not (DW_TXBDI_OOFINH)) or—out-of-frame
  (FRM_RXLOF and not (DW_TXBDI_LOFINH)) or—loss-of-frame
  (RS_RXBER_SF_DET and not (DW_TXBDI_SFINH)) or—BER signal fail
  (RS_RXBER_SD_DET and not (DW_TXBDI_SDINH)) or—BER signal degrade
  (DW_RXAIS_COND and not (DW_TXBDI_AISINH)) or—PM-AIS or TCM-AIS
  (DW_RXOCI_COND and not (DW_TXBDI_OCIINH)) or—PM-OCI or TCM-OCI
  (DW_RXFIX_COND and not (DW_TXBDI_FIXINH)) or—PM-FIX/LCK or TCM-LCK
  (TIMER20Frames and not (DW_TXBDI_TIMERINH)) or—20 frame timer
  (DW_TXBDI_INS)—software insert

Only receive alarms can contribute to transmit BDI failure generation. Transmit framer alarms and loss-of-transmit clock do not contribute to transmit BDI.

Note: Refer to Table 17, Software/Hardware Overhead Insert Priority, on page 43 for the priority of overhead byte insert. In FEC frame mode, only row location control registers are used. For BEI error insert, set BEI to a value of 0x3 regardless of the number of receive direction BIP errors per frame. BEI and BDI can be passthrough or inserted indepedently by using the DWAC insert. If BDI is inserted for a BDI overwritten byte in DWAC drop in the receive direction, and it is not desired to generate BDI in the transmit direction, the BII byte location can be programmed to an invalid location; BEI insert is also disabled.

SONET/SDH equipment has the ability to generate an RDI-P alarm for a minimum number of frames. The 20-frame timer allows for a similar function in BDI generation. This may be inhibited through software if not desired.

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

A single-bit IAE is also generated in the transmit direction. It is generated under OOF/LOF conditions in the receive direction. Only receive alarms can contribute to transmit IAE failure generation. Transmit framer alarms do not contribute to transmit IAE.

- DW_TXIAE_DET = (FRM_RXOOF and NOT (DW_TXIAE_OOFINH)) or—out-of-frame
  (FRM_RXLOF and NOT (DW_TXIAE_LOFINH)) or—loss-of-frame
  (DW_TXIAE_INS)—software insert

BDI/BEI/IAE are controlled individually by the corresponding SM/PM and TCM control signals described in Section 8.1.5 on page 68 through Section 8.1.9 on page 76.

Table 31. BDI/IAE Overhead Insert Priority

Priority (Highest = 1)	Feature
1	Software BDI/IAE Insert (ex., DW_TXBDI0_INS is set high)
2	Hardware BDI/IAE Detect = DW_TXBDI0_DET (ex., DW_TXBDI0_INH or DW_TXIAE0_INH is set low)
3	DWAC Insert
4	Passthrough

Figure 34 shows the BDI and IAE alarm detection and insertion structure.

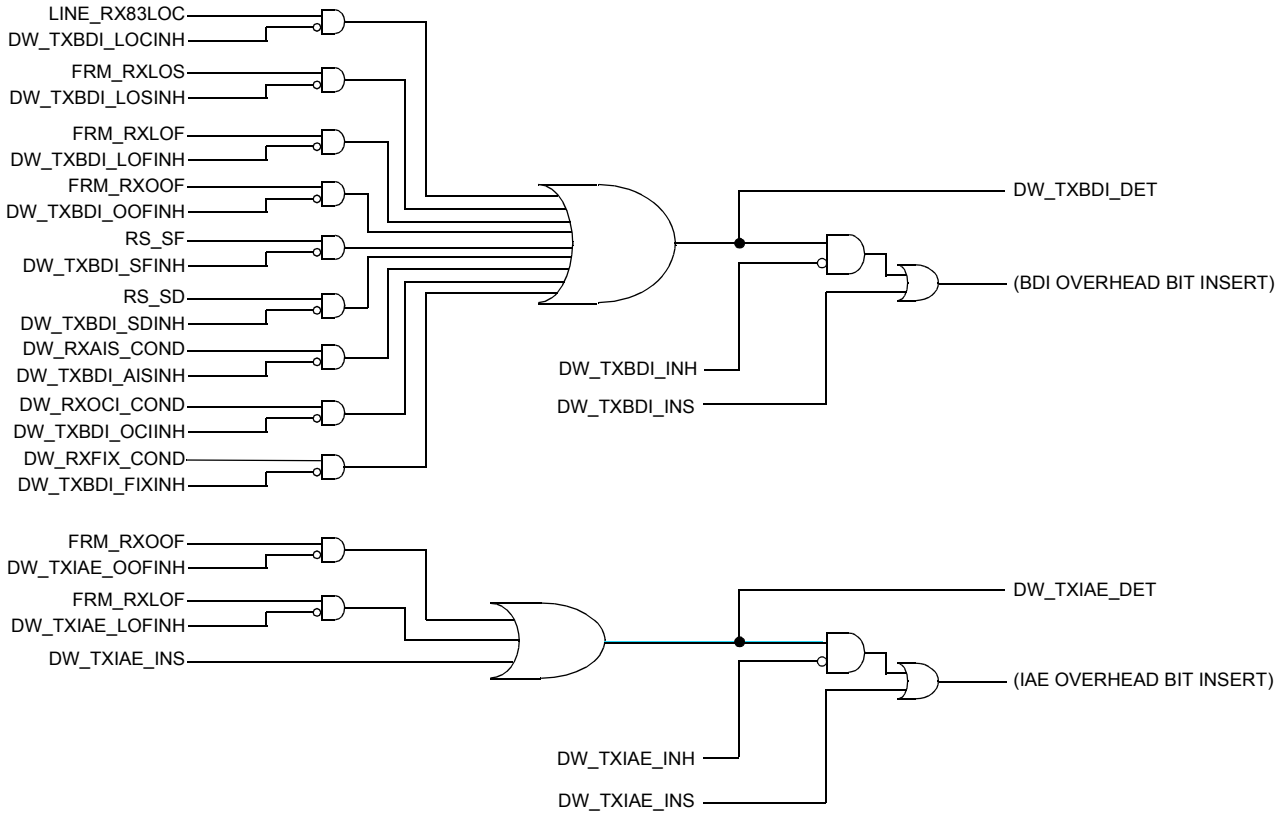


Figure 34. BDI and IAE Alarm Structure (per Slice)

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

Table 32. ODUk TCM-STAT Overhead Interpretation

If (AIS_COND_INSERT = 1), then:

STAT[2:0]	Status
000	No Source TC
001	In Use without IAE Condition (normal or OTUk-AIS[1])
010	In Use with IAE Condition (DW_TXIAE0_DET and not DW_TXAIS_TCMSTAT_IAEINH)
011	Reserved for Future International Standardization
100	Reserved for Future International Standardization
101	Maintenance Signal: ODUk-LCK
110	Maintenance Signal: ODUk-OCI
111	Maintenance Signal: ODUk-AIS

1. During OTUk-AIS, DW_TXAIS_TCMSTAT_IAEINH is set high.

8.1.5 OTU Section Monitoring (SM)

One field of section monitoring overhead (SM) is defined in FEC frame 0, rows 7 to 9, to support section monitoring. The SM field contains the following subfields (Figure 35). These bytes will use the BIP0 set of register bits (DW_TXBIP0_INS, etc.) in the insert control registers.

- Bit interleaved parity (BIP-8).
- Backward defect indication (BDI).
- Backward error indication (BEI).
- Incoming alignment error overhead (IAE).
- Reserved for future international standardization (RES).

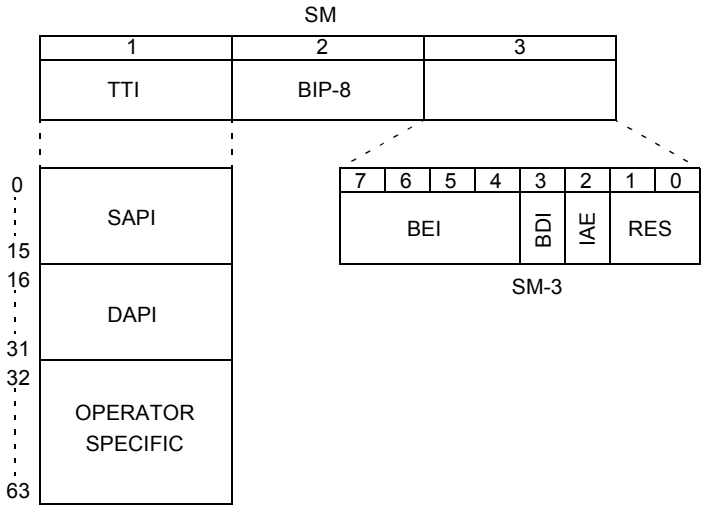


Figure 35. G.709 ODUk Section Monitor Overhead

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.5.1 SM Bit Interleaved Parity (BIP-8)

One BIP-8 calculation is provided in the section monitoring (SM) field (over payload and OPU overhead, check bits are excluded from calculation of the frames); see Figure 32. The section (even parity) bit interleaved (BIP-8) byte's value is calculated over the entire OPU signal in the nth frame and then inserted in the BIP byte of the n + 2nd frame as shown in Figure 32 on Page 65. The computed BIP-8 byte can then be error inserted (bits are inverted) via microprocessor control.

Table 33. Transmit SM BIP Byte Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BIP Byte Insertion Enable	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP0_INS	4	0×2198
BIP Byte Error Insertion Enable	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP0_ERRINS	4	0×2198
BIP Byte Insertion Frame Location	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP0_FRM	4	0×2198
BIP Byte Insertion Row Location	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP0_ROW	4	0×2198

8.1.5.2 SM Backward Error Indication (BEI)

The BEI (BIP errors per frame in the receive direction) can be inserted in every frame to indicate to the far end the received BIP errors. The valid BEI value is between 0 and 8 in each frame; invalid values that are greater than 0x8 are set as zero. When BEI insert is disabled, BEI value is set to zero. When BEI error insert is enabled, BEI value is set to a 0x3 regardless of the number of received BIP errors per frame.

Table 34. Transmit SM BEI Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BEI Insertion Enable	DW_TX_CTL_BII_S0 (R/W)	DW_TXBEI0_INS	4	0×219C
BEI Error Insertion Enable	DW_TX_CTL_BII_S0 (R/W)	DW_TXBEI0_ERRINS	4	0×219C
BII Byte Insertion Frame Location	DW_TX_CTL_BII_S0 (R/W)	DW_TXBII0_FRM	4	0×219C
BII Byte Insertion Row Location	DW_TX_CTL_BII_S0 (R/W)	DW_TXBII0_ROW	4	0×219C

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.5.3 SM Backward Defect Indication (BDI)

Transmit BDI is inserted into the OTU frame under the same conditions described in Section 8.1.4, General Definition of BEI, BDI, and IAE Insert and Monitor, on page 66. If a BDI insertion condition occurs, software can program BDI to be inserted for twenty consecutive frames regardless of BDI conditions.

Table 35. Transmit SM BDI Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI Failure Interrupt Alarm	DW_ALARM_S0 (W1C)	DW_TXBDI0_DET_A	4	0×2020
BDI Failure Interrupt Alarm Mask	DW_MASK_S0 (R/W)	DW_TXBDI0_DET_M	4	0×205C
BDI Failure Persistency	DW_PERSIST_2_S0 (RO)	DW_TXBDI0_DET_P	4	0×2090
BDI Failure State	DW_STATE_2_S0 (RO)	DW_TXBDI0_DET	4	0×20C0
BDI Failure Condition Not Detect when Detect LOC Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_LOCINH	4	0×21A0
BDI Failure Condition Not Detect when Detect OOF Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_OOFINH	4	0×21A0
BDI Failure Condition Not Detect when Detect LOF Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_LOFINH	4	0×21A0
BDI Failure Condition Not Detect when Detect LOS Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_LOSINH	4	0×21A0
BDI Failure Condition Not Detect when Detect SF Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_SFINH	4	0×21A0
BDI Failure Condition Not Detect when Detect SD Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_SDINH	4	0×21A0
BDI Failure Condition Not Detect when Detect AIS Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_AISINH	4	0×21A0
BDI Failure Condition Not Detect when Detect OCI Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_OCIINH	4	0×21A0
BDI Failure Condition Not Detect when Detected FIX Pattern Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_FIXINH	4	0×21A0
BDI Failure Condition Not Detect After at Least 20 Frames Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_TIMERINH	4	0×21A0
BDI Detect Inhibit	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_INH	4	0×21A0
BDI Insertion Enable	DW_TX_CTL_BDI0INH_2_S0 (R/W)	DW_TXBDI0_INS	4	0×21A0

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.5.4 SM Incoming Alignment Error Overhead (IAE)

Transmit IAE is inserted into the OTU frame under the same conditions described in Section 8.1.4 on page 66.

Table 36. Transmit IAE Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
IAE Insertion Enable	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXIAE0_INS	4	0×2514
IAE Detect Inhibit	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXIAE0_INH	4	0×2514
IAE Insert Inhibit Due to Rx LOF Condition	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXIAE0_LOFINH	4	0×2514
IAE Insert Inhibit Due to Rx OOF Condition	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXIAE0_OOFINH	4	0×2514
IAE Failure Interrupt Alarm	DW_ALARM_V2_S0 (W1C)	DW_TXIAE0_DET_A	4	0×2030
IAE Failure Interrupt Alarm Mask	DW_MASK_V2_S0 (R/W)	DW_TXIAE0_DET_M	4	0×206C
IAE Failure Persistency	DW_PERSIST_V2_S0 (RO)	DW_TXIAE0_DET_P	4	0×20A0
IAE Failure State	DW_STATE_V2_S0 (RO)	DW_TXIAE0_DET	4	0×20D0

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.6 Path Monitoring Insert (PM)

The path monitoring bytes have identical functionality as the SM byte with (3-bit) STAT available. These bytes will use the BIP1 set of register bits (DW_TXBIP1_INS, etc.) in the insert control registers.

8.1.6.1 PM—Bit Interleaved Parity (BIP-8)

The BIP-8 byte is processed identically to the SM-BIP8 byte (see Section 8.1.5.1 on page 69).

Table 37. Transmit PM BIP Byte Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BIP Byte Insertion Enable	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP1_INS	4	0×2198
BIP Byte Error Insertion	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP1_ERRINS	4	0×2198
BIP Byte Insertion Frame Location	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP1_FRM	4	0×2198
BIP Byte Insertion Row Location	DW_TX_CTL_BIP_S0 (R/W)	DW_TXBIP1_ROW	4	0×2198

8.1.6.2 PM—Backward Error Indication (BEI)

The BEI bits are processed identically to the SM-BEI bits (see Section 8.1.5.2 on page 69).

Table 38. Transmit PM BEI Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BEI Insertion Enable	DW_TX_CTL_BII_S0 (R/W)	DW_TXBEI1_INS	4	0×219C
BEI Error Insertion	DW_TX_CTL_BII_S0 (R/W)	DW_TXBEI1_ERRINS	4	0×219C
BII Byte Insertion Frame Location	DW_TX_CTL_BII_S0 (R/W)	DW_TXBII1_FRM	4	0×219C
BII Byte Insertion Row Location	DW_TX_CTL_BII_S0 (R/W)	DW_TXBII1_ROW	4	0×219C

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.6.3 PM—Backward Defect Indication (BDI)

The BDI bit is processed identically to the SM-BDI bit (see Section 8.1.5.3 on page 70).

Table 39. Transmit PM BDI Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI Failure Interrupt Alarm	DW_ALARM_S0 (W1C)	DW_TXBDI1_DET_A	4	0×2020
BDI Failure Interrupt Alarm Mask	DW_MASK_S0 (R/W)	DW_TXBDI1_DET_M	4	0×205C
BDI Failure Persistency	DW_PERSIST_2_S0 (RO)	DW_TXBDI1_DET_P	4	0×2090
BDI Failure State	DW_STATE_2_S0 (RO)	DW_TXBDI1_DET	4	0×20C0
BDI Failure Condition Not Detect when Detect LOC Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_LOCINH	4	0×2518
BDI Failure Condition Not Detect when Detect OOF Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_OOFINH	4	0×2518
BDI Failure Condition Not Detect when Detect LOF Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_LOFINH	4	0×2518
BDI Failure Condition Not Detect when Detect LOS Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_LOSINH	4	0×2518
BDI Failure Condition Not Detect when Detect SF Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_SFINH	4	0×2518
BDI Failure Condition Not Detect when Detect SD Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_SDINH	4	0×2518
BDI Failure Condition Not Detect when Detect AIS Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_AISINH	4	0×2518
BDI Failure Condition Not Detect when Detect OCI Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_OCIINH	4	0×2518
BDI Failure Condition Not Detect when Detected FIX Pattern Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_FIXINH	4	0×2518
BDI Failure Condition Not Detect After at Least 20 Frames Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_TIMERINH	4	0×2518
BDI Detect Inhibit	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_INH	4	0×2518
BDI Insertion Enable	DW_TX_CTL_BDI1INH_V2_S0 (R/W)	DW_TXBDI1_INS	4	0×2518

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.7 PM Statistics

The STAT bits are set to 0x1 to indicate normal data signal and are overwritten under AIS/OCI and LCK conditions. The generation of these maintenance signals is described in Section 8.1.10 on page 76.

Table 40. Transmit PM AIS, OCI, and LCK Insert Register Summary

Function	Register Name	Register Bits	Qty.	1st Addr (hex)
STAT 0x1 Insert Enable (if no error)	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXBII1_STAT_INS	4	0×2514

8.1.8 Tandem Connection Insert (TCMi)

There are 6 TCM bytes in an OTUk frame. The software can program any one of the TCM bytes to be processed in the transmit direction. The processing of the selected TCM bytes is identical to the PM bytes. These bytes will use the BIP3 set of register bits (DW_TXBIP2_INS, etc.) in the insert control registers.

8.1.8.1 TCMi—Bit Interleaved Parity (BIP-8)

The BIP-8 byte is processed identically to the SM-BIP8 byte (see Section 8.1.5.1 on page 69).

Table 41. Transmit TCM BIP Byte Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BIP Byte Insertion Enable	DW_TX_CTL_BIP_V2_S0 (R/W)	DW_TXBIP2_INS	4	0×2524
BIP Byte Error Insertion	DW_TX_CTL_BIP_V2_S0 (R/W)	DW_TXBIP2_ERRINS	4	0×2524
BIP Byte Insertion Frame Location	DW_TX_CTL_BIP_V2_S0 (R/W)	DW_TXBIP2_FRM	4	0×2524
BIP Byte Insertion Row Location	DW_TX_CTL_BIP_V2_S0 (R/W)	DW_TXBIP2_ROW	4	0×2524

8.1.8.2 TCMi—Backward Error Indication (BEI)

The BEI bits are processed identically to the SM-BEI bits (see Section 8.1.5.2 on page 69).

Table 42. Transmit TCM BEI Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BEI Insertion Enable	DW_TX_CTL_BII_V2_S0 (R/W)	DW_TXBEI2_INS	4	0×2520
BEI Error Insertion	DW_TX_CTL_BII_V2_S0 (R/W)	DW_TXBEI2_ERRINS	4	0×2520
BII Byte Insertion Frame Location	DW_TX_CTL_BII_V2_S0 (R/W)	DW_TXBII2_FRM	4	0×2520
BII Byte Insertion Row Location	DW_TX_CTL_BII_V2_S0 (R/W)	DW_TXBII2_ROW	4	0×2520

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.8.3 TCMi—Backward Defect Indication (BDI)

The BDI bit is processed identically to the SM-BDI bit (see Section 8.1.5.3 on page 70).

Table 43. Transmit TCM BDI Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI Failure Interrupt Alarm	DW_ALARM_S0 (W1C)	DW_TXBDI2_DET_A	4	0×2020
BDI Failure Interrupt Alarm Mask	DW_MASK_S0 (R/W)	DW_TXBDI2_DET_M	4	0×205C
BDI Failure Persistency	DW_PERSIST_2_S0 (RO)	DW_TXBDI2_DET_P	4	0×2090
BDI Failure State	DW_STATE_2_S0 (RO)	DW_TXBDI2_DET	4	0×20C0
BDI Failure Condition Not Detect when Detect LOC Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_LOCINH	4	0×251C
BDI Failure Condition Not Detect when Detect OOF Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_OOFINH	4	0×251C
BDI Failure Condition Not Detect when Detect LOF Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_LOFINH	4	0×251C
BDI Failure Condition Not Detect when Detect LOS Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_LOSINH	4	0×251C
BDI Failure Condition Not Detect when Detect SF Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_SFINH	4	0×251C
BDI Failure Condition Not Detect when Detect SD Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_SDINH	4	0×251C
BDI Failure Condition Not Detect when Detect AIS Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_AISINH	4	0×251C
BDI Failure Condition Not Detect when Detect OCI Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_OCIINH	4	0×251C
BDI Failure Condition Not Detect when Detected FIX Pattern Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_FIXINH	4	0×251C
BDI Failure Condition Not Detect After at Least 20 Frames Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_TIMERINH	4	0×251C
BDI Detect Inhibit	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_INH	4	0×251C
BDI Insertion Enable	DW_TX_CTL_BDI2INH_V2_S0 (R/W)	DW_TXBDI2_INS	4	0×251C

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.9 TCM Statistics

The STAT bits are set to 0x0 to indicate no TC signal and are overwritten under AIS/OCI and LCK conditions. The generation of these maintenance signals is described in later sections.

Table 44. Transmit TCM AIS, OCI, and LCK Insert Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
STAT 0x1 Insert Enable (if no error)	DW_TX_CTL_TOP_V2_S0 (RW)	DW_TXBII2_STAT_INS	4	0×2514

8.1.10 Alarm Indication Signal (AIS), Open Connection Indication (OCI), Locked (LCK), and Fixed Pattern Insert

The macro automatically generates hardware AIS in transmit direction insert when the alarms (i.e., LOC, LOS, OOF, or LOF state bits) are active and the appropriate inhibit signals are inactive or software insert is active.

The AIS, OCI, LCK, or other pattern insert priority is defined in Table 45.

Table 45. AIS, OCI, Locked (LCK), and Fixed Pattern Insert Priority

<table>
<tr><th>Priority (Highest = 1)</th><th colspan="2">AIS, OCI, or Other Pattern</th></tr>
<tr><td>1</td><td colspan="2">AIS Insert (Software)</td></tr>
<tr><td>2</td><td colspan="2">OCI Insert (Software)</td></tr>
<tr><td>3</td><td colspan="2">Fixed Pattern Insert (Software)</td></tr>
<tr><td rowspan="6">4</td><td colspan="2">AIS Insert (Hardware)</td></tr>
<tr><td>FRM (Tx)</td><td>ES (Tx) or LB (Rx to Tx)</td></tr>
<tr><td rowspan="5">(LINE_TX83LOC and not (DW_TXLOC_AISINH))
or
(FRM_DW_TXLOS and not (DW_TXLOS_AISINH))
or
(FRM_DW_TXOOF and not (DW_TXOOF_AISINH))
or
(FRM_DW_TXLOF and not (DW_TXLOF_AISINH))</td><td>(LINE_TX83LOC and not (DW_TXLOC_AISINH))
or
(DW_RXAIS_COND and not (DW_TXRXCOND_AISINH))</td></tr>
<tr><td rowspan="2">5</td><td>OCI Insert (Hardware)</td></tr>
<tr><td>(DW_RXOCI_COND and not (DW_TXRXCOND_OCIINH)</td></tr>
<tr><td rowspan="2">6</td><td>Locked or Fixed Pattern Insert (Hardware)</td></tr>
<tr><td>(DW_RXFIX_COND and not (DW_TXRXCOND_FIXINH))</td></tr>
</table>

Note: See page 107 for description of DW_RXAIS_COND, DW_RXOCI_COND, and DW_RXFIX_COND.

All frames are generated with a valid FEC/DW framing pattern, OTUk overhead, and the remaining frame bytes set to 0xFF for AIS insert, 0x66 for OCI insert, or all fixed pattern (0x55—OTUk-LCK).

At programmable MFAS location bytes, overhead insert (such as DWAC insert or OH0) in the OTU OH field, is valid and is not overwritten by the AIS generator.

TCM0—TCM5, GCC0—GCC2, and APS/PCC inhibits are available.

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

The frame structures for AIS, OCI, and LCK are shown below.

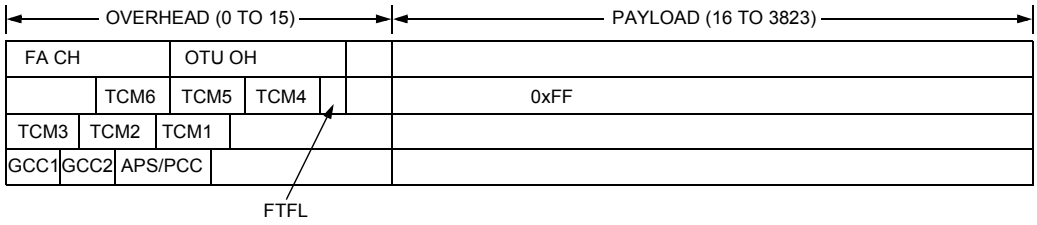


Figure 36. ODUk-AIS (TCMi, GCC1, GCC2, APS/PCC Can Be Modified/Monitored)

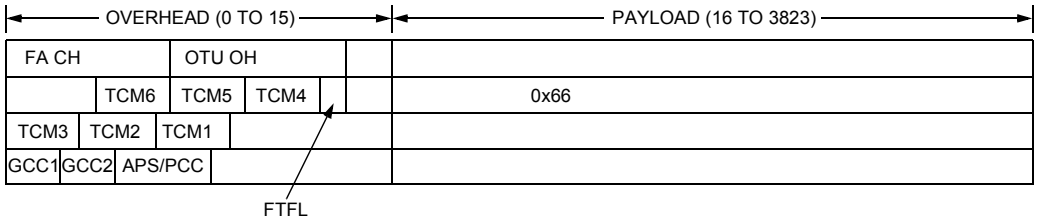


Figure 37. ODUk-OCI (TCMi, GCC1, GCC2, APS/PCC Can Be Modified/Monitored)

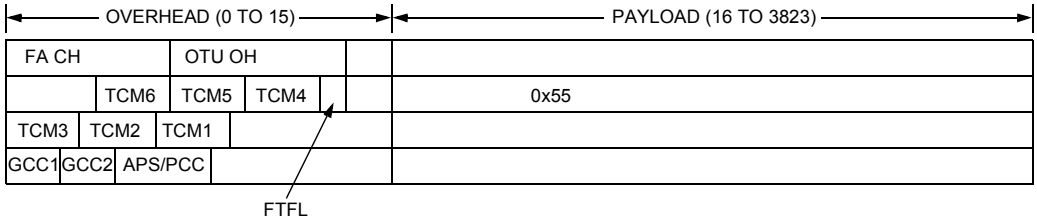
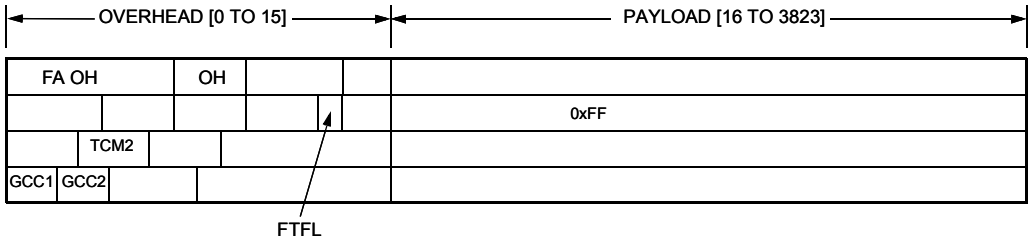


Figure 38. ODUk-LCK (TCMi, GCC1, GCC2, APS/PCC Can Be Modified/Monitored)

Figure 39 is an example of MFAS, SM, FTFL, TCM2, GCC1, and GCC2 when inhibited during ODUk-AIS.



Example: DW_TXOA12_PAIR = 0x2, DW_TXOA12_MFAS = 0x4, DW_RXAIS_FTFLINH = 0x1, DW_RXAIS_GCCINH = 0x6, DW_TXAIS_TCMINH = 0x2, and DW_TXAIS_APSINH = 0x0.

Figure 39. ODUk-AIS (MFAS, SM, FTFL, TCM2, GCC1, and GCC2 are Inhibited)

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

An AIS signal is generated in case of a layer defect or an open connection.

Table 46. Digital Wrapper AIS Insert Byte Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
AIS Insertion Enable.	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXAIS_INS	4	0×2178
OCI Insertion Enable.	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXOCI_INS	4	0×2178
Fixed Pattern Byte Insertion Enable.	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXFIX_INS	4	0×2178
Locked or Fixed Signal Pattern to Be Inserted: 0 = Locked. 1 = Fixed.	DW_TX_CTL_TOP_V2_S0 (R/W)	DW_TXLCK_FIX	4	0×2514
Fixed Pattern Byte: 0x00 = Open Connection Indication/All 0s. 0xFF = Layer Defect/All 1s (default).	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXFIX_VAL	4	0×2194
Number of Multiframe (MFAS) Bytes After OA2 (see Table 25 on Page 57).	DW_TX_CTL_OA12_PAT_S0 (R/W)	DW_TXOA12_MFAS	4	0×2180
Loss-of-Clock AIS Inhibit. When Set to Logic 1, the AIS Insert is Inhibited in Case of Loss-of-Clock (LINE_TX83LOC).	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXLOC_AISINH	4	0×2194
Out-of-Frame AIS Inhibit. When Set to Logic 1, the AIS Insert is Inhibited in Case of Out-of-Frame (FRM_TXOOF).	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXOOF_AISINH	4	0×2194
Loss-of-Frame AIS Inhibit. When Set to Logic 1, the AIS Insert is Inhibited in Case of Loss-of-Frame (FRM_TXLOF).	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXLOF_AISINH	4	0×2194
Loss-of-Signal AIS Inhibit. When Set to Logic 1, the AIS Insert is Inhibited in Case of Loss-of-Signal (FRM_TXLOS).	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXLOS_AISINH	4	0×2194
Receive AIS Condition Inhibit.	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXRXCOND_AISINH	4	0×2194
Receive OCI Condition Inhibit.	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXRXCOND_OCIINH	4	0×2194
Receive Other Fixed Pattern Condition Inhibit.	DW_TX_CTL_AIS_2_S0 (R/W)	DW_TXRXCOND_FIXINH	4	0×2194
FTFL Inhibit during AIS.	DW_TX_CTL_AIS_V2_S0 (R/W)	DW_TXAIS_FTFLINH	4	0×2528
Inhibit TCM0—TCM5 overwritten by AIS/OCI/LCK[1].	DW_TX_CTL_AIS_V2_S0 (R/W)	DW_TXAIS_TCMINH	4	0×2528
Inhibit GCC0—GCC2 overwritten by AIS/OCI/LCK.	DW_TX_CTL_AIS_V2_S0 (R/W)	DW_TXAIS_GCCINH	4	0×2528
Inhibit APS/PCC inhibit overwritten by AIS/OCI/LCK.	DW_TX_CTL_AIS_V2_S0 (R/W)	DW_TXAIS_APSINH	4	0×2528
Inhibit TCM0—TCM5 overwritten by AIS/OCI/LCK[1] Inhibit.	DW_TX_CTL_AIS_V2_S0 (R/W)	DW_TXAIS_TCMSTAT_IAEINH	4	0×2514

1. If TCM insert during AIS/OCI/LCK, STAT [2:0] will be inserted 001 for normal operation mode. (IAE in-use is not available.)

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.11 DWAC Insert

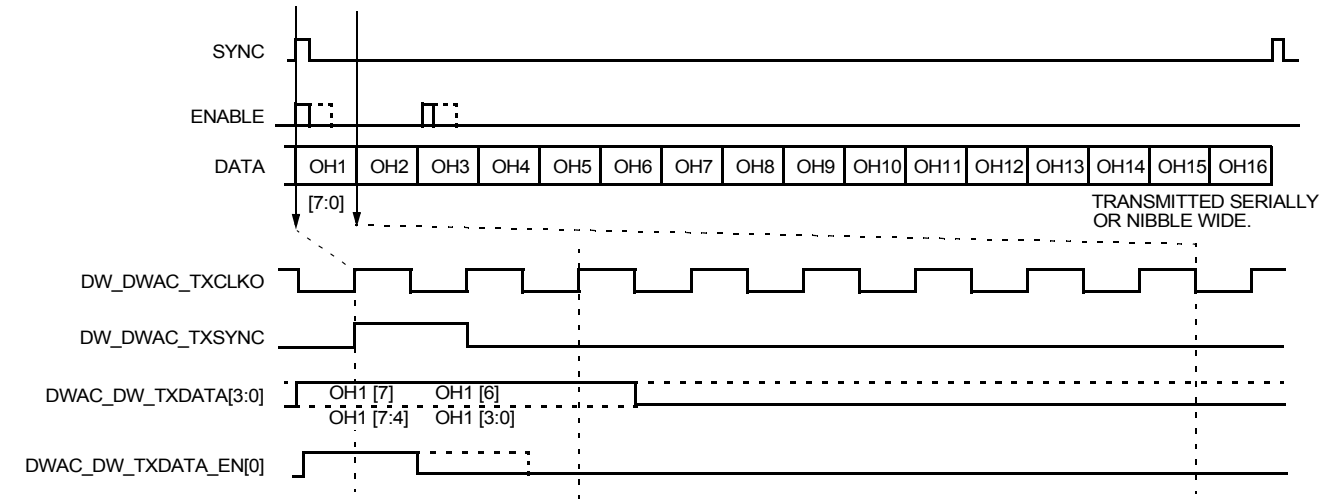
Four insert digital wrapper access channels (DWAC) are provided on chip along with four drop DWACs. These channels provide most of the monitoring and insert capabilities for the FEC/DW overhead bytes.

The insert DWAC consists of four signals per channel (total of four DWAC channels):

— Output clock at ~10.455 MHz (10 Gbits/s mode (slice 0 only) and quad 2.5 Gbits/s mode).
— Output superframe sync (~326.7/~81.68 kHz—10 Gbits/s (FEC/DW), ~81.68/~20.42 kHz—quad 2.5 Gbits/s (FEC/DW)) coincident with the MSB (most significant bit) in quad 2.5 Gbits/s mode, or MSN (most significant nibble) in 10 Gbits/s mode of the first byte in frame 0. The sync pulse is provided on the rising edge of DWAC clock. At MFAS = 0x00, sync pulse is set high for two clock cycles.
— Input data: 4 bits (a nibble) in 10 Gbits/s mode and 1 bit per stream in quad 2.5 Gbits/s mode.
— Input insert enable signal: active-high signal coincident with the first two MSB[7:6] of the byte to insert in quad 2.5 Gbits/s mode or coincident with the two MSNs in 10 Gbits/s mode. See Table 28 on page 61.

All the DWAC bytes insertion control is described below.

The data stream format from the device is identical to Figure 33 on page 66.



Note: See the Timing Characteristics section in the Hardware Design Guide for the Transmit Transport Overhead Access Channel section.

Figure 40. Transmit DWAC Frame Definition

Table 47. DWAC Byte Insertion Control

DWAC Enable Data	Value	Description
DWAC_DW_TXDATA_EN[3:0]/[0] Sampled at [MSB], [MSB – 1]/[MSN], [MSN – 1] Positions Only.	11	Insert data from the serial DWAC input.
	00	Default standards.
	01/10	Passthrough (if enabled, otherwise default standard is inserted).

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

Table 48. Transmit DWAC Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
DWAC Byte Insertion Enable	DW_DWAC_TX_CTL_S0 (R/W)	DWAC_TXINS	4	0×21C4

8.1.12 PRBS Insert and Monitor

A pseudorandom sequence (PRBS: $2^{29} – 1$ or $2^{31} – 1$) data can be inserted into payload locations (exclude overhead and check bits locations). When the pseudorandom sequence is inserted, a $2^{29} – 1$ or a $2^{31} – 1$ sequence is used in the payload data bytes with the pattern starting after each of the overhead bytes. In addition, all overhead bytes function normally.

The pseudorandom pattern uses either a $2^{29} – 1$ (536, 870, 911 bits), or a $2^{31} – 1$ (2, 147, 483, 647 bits) pattern length specified in O.150. The $2^{29} – 1$ sequence is generated by a 29-stage shift register whose twenty-seventh and twenty-ninth stage outputs are added and fed back to the first stage. The output of the last stage can be inverted (which yields a sequence with up to 29 zeros). The $2^{31} – 1$ sequence is generated by a 31-stage shift register whose twenty-eighth and thirty-first stage outputs are added and fed back to the first stage. The output of the last stage can be inverted (which yields a sequence with up to 31 zeros).

In quad 2.5 Gbits/s mode, the PRBS macro generates four independent 32-bit PN sequences. In 10 Gbits/s mode, all 128 bits are generated as one PN sequence.

The PRBS pattern can be inverted by setting a single control bit. Only the slice 0 control bit is valid in 10 Gbits/s mode. A single-bit error can be inserted. The PRBS generator injects a single error bit at the MSB in the test pattern. The most significant bit (MSB) of each slice is inverted. For example, in quad 2.5 Gbits/s, the 127th (slice 3), 95th (slice 2), 64th (slice 1), and 31th (slice 0) are used. In 10 Gbits/s mode, only the 127th is used.

Table 49. PRBS Insert Control Bit Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Transmit PRBS Pattern (Payload Only) Insertion Enable	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TXPRBS_INS	4	0×2178
Transmit PRBS Pattern Sequence Selection: 0 = $2^{29} – 1$ 1 = $2^{31} – 1$	DW_PRBS_CTL_S0 (R/W)	DW_TXPRBS_29_31_PAT	4	0×21E0
Transmit PRBS Inverted Pattern (Payload Only) Insertion Enable	DW_PRBS_CTL_S0 (R/W)	DW_TXPRBS_INV	4	0×21E0
Transmit PRBS Error Insert Bit (1 error bit per 128 bits in 10 Gbits/s mode, and 1 bit per 32 bits in 2.5 Gbits/s mode)	DW_PRBS_CTL_S0 (R/W)	DW_TXPRBS_1BERRINS	4	0×21E0

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

PRBS data in payload locations (exclude overhead and check bytes location) can be monitored by the PRBS monitor at the input pins. A pseudorandom sequence pattern (either $2^{31} – 1$ or $2^{29} – 1$) can be detected.

When 32 consecutive bits match the pattern, the pattern sync state declares itself in-sync. If eight or more consecutive mismatches are in the payload sequence, the corresponding pattern sync state declares itself out-of-sync. In 10 Gbits/s mode, the payload goes into sync if the most up-to-date 32 bits (LSB) are matched, and declares out-of-sync if the most up-to-date of the last 32 bits (LSB) has eight or more consecutive mismatches in the payload sequence.

Note: If 32 bits match and/or eight mismatches occur in less up-to-date patterns [127:32], sync state will be ignored.

The pattern sync state also provides an interrupt alarm and persistency. The PRBS can also monitor for an inverted pattern via the microprocessor. Any bit error occurring after the monitor is in the in-sync state is reported by an 8-bit counter. This counter (DW_TXPRBS_ECNT) will contain the number of bit errors (clear-on-read toggle from the microprocessor).

Table 50. PRBS Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Transmit PRBS Monitor Pattern (payload only) Monitor is Expected to be Inverted When Set	DW_PRBS_CTL_V2_S0 (RW)	DW_TXPRBS_MON_INV	4	0×2530
Transmit PRBS Monitor Pattern Sequence Selection: 0 = $2^{29} – 1$ 1 = $2^{31} – 1$	DW_PRBS_CTL_V2_S0 (RW)	DW_TXPRBS_MON_29_31_PAT	4	0×2530
Monitored PRBS Pattern Sync Interrupt Alarm Bit	DW_ALARM_V2_S0 (W1C)	DW_TXPRBS_SYNC_A	4	0×2030
Monitored PRBS Pattern Sync Mask Bit	DW_MASK_V2_S0 (RW)	DW_TXPRBS_SYNC_M	4	0×206C
Monitored PRBS Pattern Sync Persistency Bit	DW_PERSIST_V2_S0 (RO)	DW_TXPRBS_SYNC_P	4	0×20A0
When the PRBS Pattern (Payload Only) Detects 32 Matches in a Row, It Declares Itself In-Sync and the Error Detector is Enabled. If the Device Detects Eight Consecutive Mismatches, the Test Pattern Detector Declares Itself Out-of-Sync and Starts Searching Again. 0 = In-Sync. 1 = Out-of-Sync.	DW_STATE_V2_S0 (RO)	DW_TXPRBS_SYNC	4	0×20D0
Monitored PRBS Error Pattern Counter. The PRBS Monitor Counts the number of Times the Input Data Differs from the Expected Value in an 8-Bit Counter that Holds its Count when it Reaches the Maximum Value of 255. This Counter is Reset when Ready by the Microprocessor, and is not Affected by the PMRST Signal (clear-on-read).	DW_TX_CNT_PRBS_V2_S0 (COR)	DW_TXPRBS_ECNT	4	0×2604

8 Digital Wrapper Insert (continued)

8.1 Functional Description of Digital Wrapper Insert (continued)

8.1.13 Digital Wrapper Check Byte Insert

The check bits location can be set to pass through its value by setting a control bit. Otherwise, all check bits are set to zero. Check byte passthrough is not available when the transmit data is generated from the transmit elastic store.

Table 51. DW Insert Check Byte Insertion Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Transmit Check Bits Location Zero Insertion: 0 = Check Bits are Set to Zero 1 = Check Bits Pass Through.	DW_TX_CTL_TOP_2_S0 (R/W)	DW_TX_CBPASS	4	0×2178
Transmit No Fix Stuff Enable (10 Gbits/s DW mode only) i.e., 119th of 0—254 Columns is Reserved for a Stuff Column	DW_TX_CTL_TOP_V2_S0 (RW)	DW_TX_NO_FS	4	0×2514

9 Strong FEC Supermacro Reed-Solomon (RS) Encoder

9.1 Functional Description of RS Encoder

The RS encoder calculates and inserts check bytes which are remainders after polynomial division of the payload by generating polynomial, $g(z) = (z + 1)(z + a^1) \ldots (z + a^{15})$, where a is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$.

Data arrives to the RS encoder grouped as four slices of 32 bits. Each slice has four independent check byte calculators. Each calculator accepts 239 bytes of payload data followed by 16 bytes of all-zeros data, and generates 16 bytes of check data. The check bytes replace all 16 incoming zero bytes unless the RS encoder is in bypass mode.

Table 52. RS Encoder Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
RS Encoder Mode Control: 0 = Normal. 1 = Bypass.	RS_TX_CTL_TOP_S0 (R/W)	RS_TX_ENC	4	0×221A

10 Strong FEC Supermacro Scrambler

10.1 Functional Description of Strong FEC Supermacro Scrambler

The scrambler optionally scrambles incoming data. The scrambling sequence can be selected between two different polynomials: $x^7 + x + 1$ and $x^{16} + x^{12} + x^3 + x + 1$.

When scrambling is enabled, the whole FEC/DW frame is scrambled, with the exception of the framing byte, by a selected polynomial ($x^7 + x + 1$ or $x^{16} + x^{12} + x^3 + x + 1$). Scrambling is initiated at each frame on the first bit which follows the framing byte. The first bit sequence of the scrambler is all 1s.

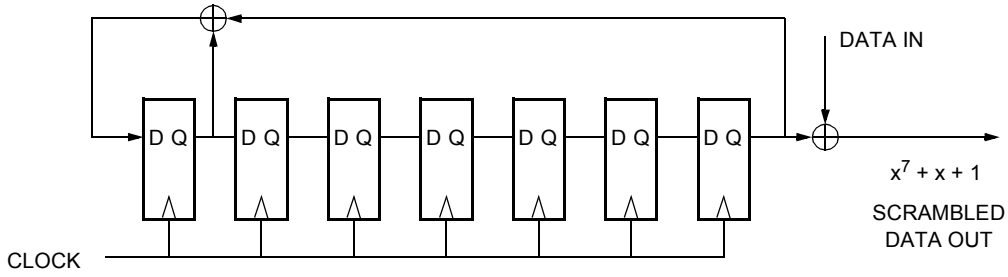


Figure 41. $x^7 + x + 1$ Frame Synchronous Scrambler (G.975)

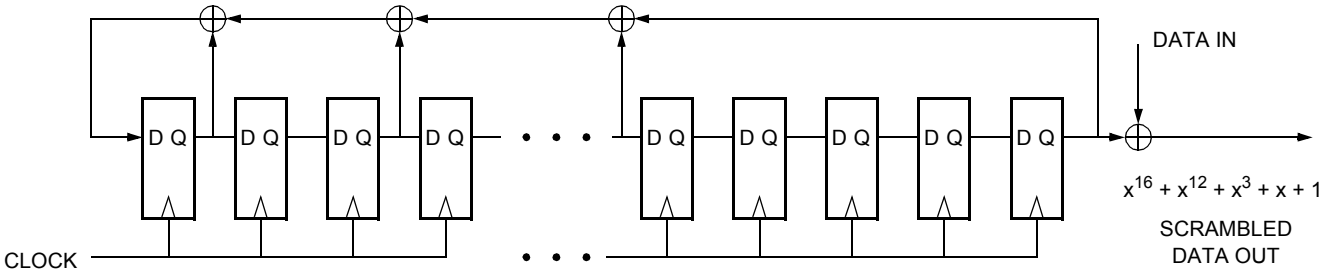


Figure 42. $x^{16} + x^{12} + x^3 + x + 1$ Frame Synchronous Scrambler (G.709)

Table 53. Scrambler Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Scrambling Control: 0 = Off. 1 = On.	RS_TX_CTL_TOP_S0 (R/W)	RS_TX_SCR	4	0×221A
Scrambling Sequence Select: 0 = 7-bit ($x^7 + x + 1$). 1 = 16-bit ($x^{16} + x^{12} + x^3 + x + 1$).	RS_TX_CTL_TOP_S0 (R/W)	RS_TX_SCR_7_16_POL	4	0×221A

11 Strong FEC Supermacro Error Insert

11.1 Functional Description of Error Insert

The error insert inserts various types of errors for RS code testing. For each slice, an error insert block accepts 32 bits of data. There is a total of four slices instantiated to make the 128-bit wide data for 16-way and 64-way 10 Gbits/s mode.

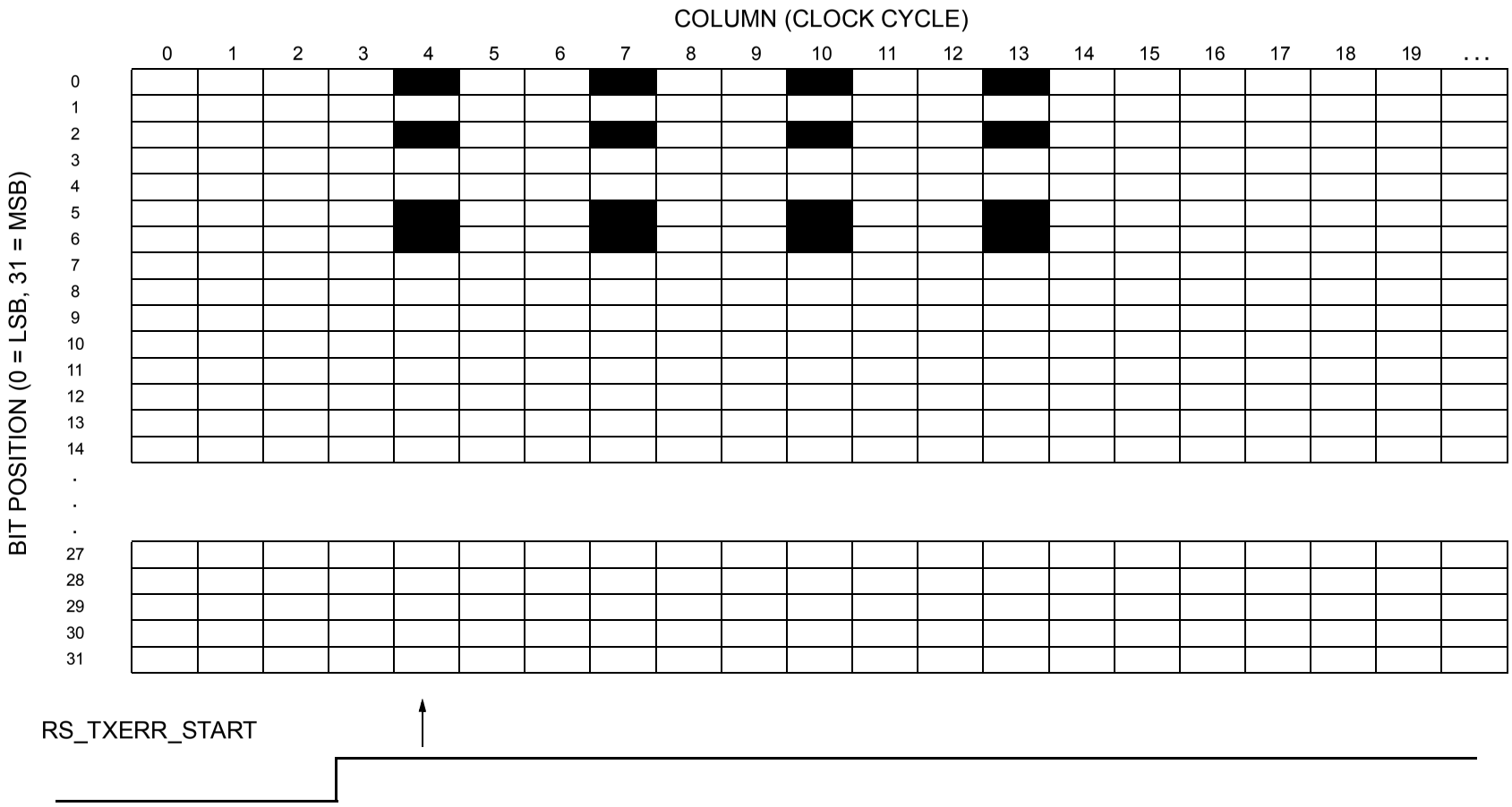
A 32-bit mask register corresponds to the 32-bit wide data bus for the error insertion. When the mask bit is set to logic 1, the corresponding data bit is inverted. The number of skipping clock cycles can be programmed through the microprocessor. Error bits combining with the number of skipping clock cycles can be repeated by using a control bit bus. The first column of error can be chosen via the microprocessor. The stream of errors start when there is a 0 ⇒ 1 transition. See Figure 43, Example of Error Insert Setup Diagram, on page 85. Ensure the inserted error bits are within the range as noted in Table 54.

Table 54. Error Insert Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Mask for the Error Insertion on the 32-Bit Data Bus	RS_TX_CTL_ERRMSK1_S0/ RS_TX_CTL_ERRMSK0_S0 (R/W)	RS_TXERR1_MASK/ RS_TXERR0_MASK	4	0×2226/ 0×2227
Number of Skipping Clock Cycles Between 32-Bit Error Pattern	RS_TX_CTL_ERRSKIP_S0 (R/W)	RS_TXERR_SKIP	4	0×221E
Number of Repeating Clock Cycles Between 32-Bit Error Pattern	RS_TX_CTL_ERRREPT_S0 (R/W)	RS_TXERR_REPEAT	4	0×2222
Start Column (Note: In 16×2.5G mode, 0—1019; 16×10G mode, 0—254; 64×10G mode, 0—1019. Out of range values default to 0.)	RS_TX_CTL_ERRCOL_S0 (R/W)	RS_TXERR_COL	4	0×222F
Error Start Control Bit	RS_TX_CTL_TOP_S0 (R/W)	RS_TXERR_START	4	0×221A
Error Insert Finish Alarm	RS_ALARM_S0 (W1C)	RS_TXERR_A	4	0×2028
Error Insert Finish Mask	RS_MASK_2_S0 (R/W)	RS_TXERR_M	4	0×2064
Error Insert Finish State	RS_STATE_S0 (RO)	RS_TXERR	4	0×20C8

11 Strong FEC Supermacro Error Insert (continued)

11.1 Functional Description of Error Insert (continued)



Example:

RS_TXERR_SKIP[7:0] = 0×2
RS_TXERR_REPEAT[9:0] = 0×4
RS_TXERR_COL[11:0] = 0×4
RS_TXERR1_MASK = 0×0
RS_TXERR0_MASK = 0×0065

Figure 43. Example of Error Insert Setup Diagram

12 Interleaver

12.1 Functional Description of Interleaver

The RS encoder performs interleaving of code blocks in order to enhance the immunity of a transmission system to burst errors, in byte manner.

In 10 Gbits/s mode, all four interleavers work in synchronization. The read/write addresses of slice 1, slice 2, and slice 3 are synchronized with slice 0, which is a master slice.

13 Deinterleaver

13.1 Functional Description of Deinterleaver

The RS decoder performs deinterleaving of code blocks in order to enhance the immunity of the transmission system to burst errors, in byte manner.

In 10 Gbits/s mode, all four deinterleavers work in synchronization. The read/write addresses of slice 1, slice 2, and slice 3 are synchronized with slice 0, which is a master slice.

14 Framer Receive Direction Requirements

The framer functionality of the receive direction is identical to the transmit direction in Section 7, Strong FEC Supermacro FEC/DW Framer (LOS, OOF, LOF), on page 55.

Table 55. LOS Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
LOS Detect Time Threshold	FRM_RX_CTL_LOSDET_S0 (R/W)	FRM_RXLOS_DET	4	0×22A0
LOS Interrupt Alarm	FRM_ALARM_S0 (W1C)	FRM_RXLOS_A	4	0×202C
LOS Alarm Mask	FRM_MASK_S0 (R/W)	FRM_RXLOS_M	4	0×2068
LOS Persistency	FRM_PERSIST_S0 (RO)	FRM_RXLOS_P	4	0×209C
LOS State	FRM_STATE_S0 (RO)	FRM_RXLOS	4	0×20CC

14 Framer Receive Direction Requirements (continued)

Table 56. Framer Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Framer Disable	FRM_RX_CTL_OOF_3_S0 (R/W)	FRM_RX_DISABLE	4	0×22AC
OA1 Frame Byte Value	FRM_RX_CTL_OA12_S0 (R/W)	FRM_RXOA1_VAL	4	0×22A4
OA2 Frame Byte Value	FRM_RX_CTL_OA12_S0 (R/W)	FRM_RXOA2_VAL	4	0×22A4
Number of Repeat OA1 Byte (same as OA2): 0 = One OA1's, One OA2's 7 = Eight OA1's, Eight OA2's See Table 25 on Page 57	FRM_RX_CTL_OA12_PAT_3_S0 (R/W)	FRM_RXOA12_PAIRS	4	0×22A8
Number of Framing Pattern Pairs (OA1/OA2) Used to Transition Between Out-of-Frame to In-Frame State (OOF, 1 ⇒ 0)	FRM_RX_CTL_OA12_PAT_3_S0 (R/W)	FRM_RXOA12_PAIRCLR	4	0×22A8
Number of Framing Pattern Pairs (OA1/OA2) Used to Transition Between In-Frame to Out-of-Frame State (OOF, 0 ⇒ 1)	FRM_RX_CTL_OA12_PAT_3_S0 (R/W)	FRM_RXOA12_PAIRSET	4	0×22A8
Out-of-Frame Set	FRM_RX_CTL_OOF_3_S0 (R/W)	FRM_RXOOF_SET	4	0×22AC
Out-of-Frame Clear	FRM_RX_CTL_OOF_3_S0 (R/W)	FRM_RXOOF_CLR	4	0×22AC
Out-of-Frame Interrupt Alarm	FRM_ALARM_S0 (W1C)	FRM_RXOOF_A	4	0×202C
Out-of-Frame Interrupt Alarm Mask	FRM_MASK_S0 (R/W)	FRM_RXOOF_M	4	0×2068
Out-of-Frame Persistency	FRM_PERSIST_S0 (RO)	FRM_RXOOF_P	4	0×209C
Out-of-Frame State	FRM_STATE_S0 (RO)	FRM_RXOOF	4	0×20CC

14 Framer Receive Direction Requirements (continued)

Table 57. Loss-of-Frame Control Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Loss-of-Frame Set	FRM_RX_CTL_LOF_2_S0 (R/W)	FRM_RXLOF_SET	4	0×22B0
Loss-of-Frame Clear	FRM_RX_CTL_LOF_2_S0 (R/W)	FRM_RXLOF_CLR	4	0×22B0
Loss-of-Frame Interrupt Alarm	FRM_ALARM_S0 (W1C)	FRM_RXLOF_A	4	0×202C
Loss-of-Frame Interrupt Alarm Mask	FRM_MASK_S0 (R/W)	FRM_RXLOF_M	4	0×2068
Loss-of-Frame Persistency	FRM_PERSIST_S0 (RO)	FRM_RXLOF_P	4	0×209C
Loss-of-Frame State	FRM_STATE_S0 (RO)	FRM_RXLOF	4	0×20CC

15 Strong FEC Supermacro Descrambler

15.1 Functional Description of Descrambler

The descrambler optionally descrambles incoming data. The scrambling sequence can be selected between two different polynomials: $x^7 + x + 1$ or $x^{16} + x^{12} + x^3 + x + 1$.

Once descrambling is requested, the whole FEC/DW frame is descrambled, with the exception of the framing byte, by a selected polynomial initiated at each frame on the first bit which follows the framing byte. The first bit sequence of the descrambler is all ones.

Table 58. Descrambler Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Rx Descrambling Control: 0 = Off. 1 = On.	RS_RX_CTL_TOP_S0 (R/W)	RS_RX_DSCR	4	0×2200
Rx Descrambling Sequence Select: 0 = 7-bit ($x^7 + x + 1$). 1 = 16-bit ($x^{16} + x^{12} + x^3 + x + 1$).	RS_RX_CTL_TOP_S0 (R/W)	RS_RX_DSCR_7_16_POL	4	0×2200

16 Reed-Solomon (RS) Decoder

16.1 Functional Description of RS Decoder

The RS decoder detects and corrects transmission errors, and calculates and reports incoming BER based on the exact number of corrected bits. When the FEC/DW framer is in the OOF, LOF, or LOS state, the associated decoder is disabled.

16.1.1 Error Detect and Correct

Data arrives to the RS decoder grouped as four slices of 32 bits. Each slice has four independent error detect-and-correct blocks. Each block accepts 8-bit wide RS code blocks, and outputs 8-bit wide corrected code blocks.

The number of corrected bits and the number of uncorrectable blocks are counted and reported to the BER monitor block, per slice. If uncorrectable errors are detected, correction operation is turned off automatically on a block-by-block basis and the number of corrected bit errors is not counted.

There are four operational decoding modes

- Monitor
- Shutdown
- Decode Only
- Correct

When the RS decoder is set to the monitoring mode, the error is detected and monitored, but data is not corrected without delay. When set to shut-down mode, the decoding function is disabled and data is bypassed without delay. When set to decode-only mode, the error is detected and monitored, but data is not corrected with delay. When set to correct mode, the error is detected and corrected. The transition between decode-only and correct are hitless.

Table 59. RS Decoder Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
RS Decoder Mode Control	RS_RX_CTL_TOP_S0 (R/W)	RS_RX_DEC	4	0×2200

16.1.2 BER Monitor

The Reed Solomon statistics count correctable errors that are detected and corrected in the RS decoder. The monitoring of the line BER before correction can be done through the knowledge of the exact number of corrected bits. The errors that remain uncorrected after forward error correction can be considered negligible in the computation of BER, for low error rates.

16 Reed-Solomon (RS) Decoder (continued)

16.1 Functional Description of RS Decoder (continued)

16.1.3 Error Count

The corrected bits and the uncorrectable blocks are accumulated per slice in 16-bit saturating counters based on either bit or block errors. In bit mode, each corrected error (or uncorrectable block) causes the counter to increment.

If block error is selected, each FEC/DW frame which has a corrected error (or uncorrectable block) causes the counter to increment by only one. The counter stops at the maximum value and will not roll over, and is cleared by the PMRST signal.

Table 60. RS Error Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
RS Error Count Control	RS_RX_CTL_TOP_S0 (R/W)	RS_ERR_BITBLK	4	0×2200
RS Rx 0 ⇒ 1 Corrected Bit Counter	RS_RX_CNT_0TO1_ERRBIT0_S0/ RS_RX_CNT_0TO1_ERRBIT1_S0 (RO)	RS_RX_ERR00_0TO1_BITCNT/ RS_RX_ERR01_0TO1_BITCNT	4	0×254A/ 0×254B
RS Rx 1 ⇒ 0 Corrected Bit Counter	RS_RX_CNT_1TO0_ERRBIT0_S0/ RS_RX_CNT_1TO0_ERRBIT1_S0 (RO)	RS_RX_ERR0_1TO0_BITCNT/ RS_RX_ERR1_1TO0_BITCNT	4	0×2553/ 0×2554
RS Rx Corrected Bit Counter	RS_RX_CNT_ERRBIT0_S0/ RS_RX_CNT_ERRBIT1_S0 (RO)	RS_RX_ERR0_BITCNT/ RS_RX_ERR1_BITCNT	4	0×234C/ 0×234D
RS Rx Uncorrectable Block Counter	RS_RX_CNT_ERRBLK0_S0/ RS_RX_CNT_ERRBLK1_S0 (RO)	RS_RX_UNC0_BLKCNT/ RS_RX_UNC1_BLKCNT	4	0×2355/ 0×2356

16.1.3.1 BER Detecting and Reporting

The corrected errors are used to detect SF and SD conditions. The BER threshold for each defect is separately provisionable for each slice over a range of 1×10^{-N} values, where N = 3 to 9.

The detection times and error limits used to detect and clear both defects are dependent on the provisioned BER threshold, as shown in Table 61. The values shown in Table 61 are the powerup defaults and are dependent on the mode selected (2.5 Gbits/s or 16-way/64-way 10 Gbits/s). These values can be changed through the corresponding registers and are common to all slices.

The clearing BER threshold for each defect is always one-tenth of the detection threshold. As can be seen in Table 61, the range of possible detect threshold are 1×10^{-3} to 1×10^{-9}, which results in clear thresholds of 1×10^{-4} to 1×10^{-10}. For example, to detect SD at 1×10^{-5} BER in 2.5 Gbits/s mode, the detection time is 3.2 ms and the detect error limit is 83. The clearing would take place at 1×10^{-6} BER, with a clearing time of 51.2 ms and a clearing error limit of 665. Figure 44 on page 91 illustrates SD detection and clearing using the default values.

16 Reed-Solomon (RS) Decoder (continued)

16.1 Functional Description of RS Decoder (continued)

Table 61. BER Threshold Time and Error Limits for Line SD and SF Detection

Provisioned BER Threshold	Detection Time		Detect Error Limit		Clear Error Limit	
	2.5 Gbits/s	10 Gbits/s	2.5 Gbits/s	10 Gbits/s	2.5 Gbits/s	10 Gbits/s
1×10^{-3}	0.4 ms	0.1 ms	1044	1044	—	—
1×10^{-4}	0.4 ms	0.1 ms	104	104	520	520
1×10^{-5}	3.2 ms	0.8 ms	83	83	415	415
1×10^{-6}	51.2 ms	10.3 ms	133	133	665	665
1×10^{-7}	409.6 ms	102.4 ms	106	106	530	530
1×10^{-8}	3200 ms	800 ms	85	85	425	425
1×10^{-9}	52.4 s	10.6 s	136	136	680	680
1×10^{-10}	419.4 s	104.8 s	—	—	545	545

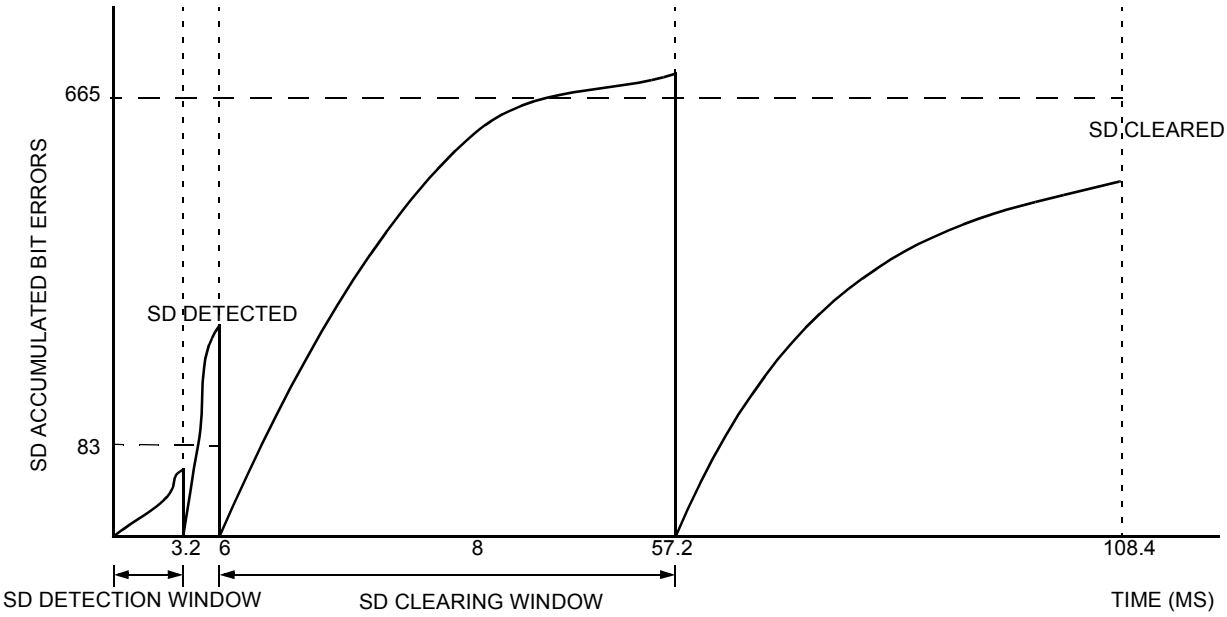


Figure 44. Example of SD Detection (10^{-5} BER) and Clearing (10^{-6} BER)

In 10 Gbits/s mode, the thresholds are compared against the sum of the four slice SF and SD counts. A detected SF or SD defect causes a corresponding maskable interrupt status bit to be set.

The SD/SF BER control bits select the bit error rate for a particular slice. These control bits then select the detection time, the detect error limit, and the clear error limits for each slice. The detect error limit and the clear error limit registers contain 16-bit values, while the detection time registers use the lower 15 bits for a value and the upper bit for a time unit specifier. For the detection time register, the value contained in the lower 15 bits is either specified in 0.1 ms units (upper bit = 0) or in 0.1 s units (upper bit = 1). Note that the receive sync pulse is used as the timing reference.

16 Reed-Solomon (RS) Decoder (continued)

16.1 Functional Description of RS Decoder (continued)

A fixed windowing scheme is used for SD/SF detection. The window size is determined by the value in the detection time register for the specified bit error rate. An SD or SF alarm is declared immediately when the accumulated error count exceeds the value specified in the detect error limit register.

If this error limit is not reached by the end of the window, then the accumulated error count is reset to zero. When an SD or SF alarm is declared, the accumulated error count resets and clearing begins using the bit error rate threshold that is one-tenth of the specified value, along with the corresponding detection time registers. Clearing of the SD or SF alarm only occurs at the end of the window when the accumulated error count is less than the value specified in the clear error limit register.

The RS decoder reports current BER so the customer knows which is a current BER. For this, seven BERs are monitored at the same time. Once a certain level BER is detected, lower-level BERs are ignored and the highest-level of BER is reported as a current BER, i.e., when 1 x 10^{-4} BER is detected, BERs from 1 x 10^{-5} to 1 x 10^{-9} are ignored and 1 x 10^{-4} is reported as a current BER.

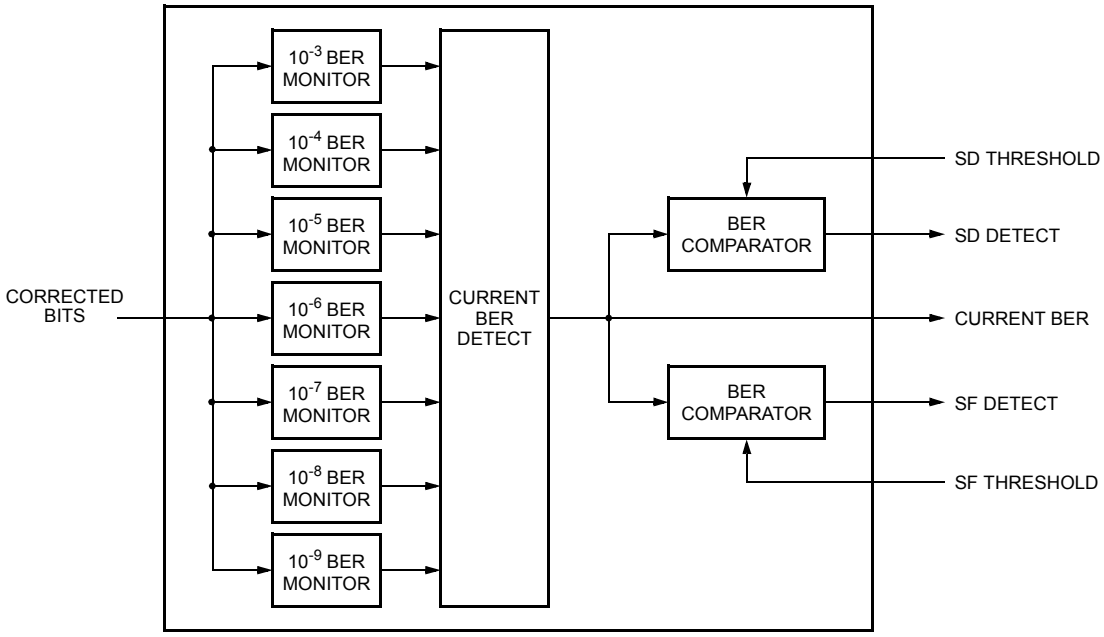


Figure 45. RS Decoder Block Diagram

16 Reed-Solomon (RS) Decoder (continued)

16.1 Functional Description of RS Decoder (continued)

Table 62. RS Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
RS SD Threshold Select	RS_RX_CTL_TOP_S0 (R/W)	RS_RXBER_SD_ THRESHOLD	4	0×2200
RS SF Threshold Select	RS_RX_CTL_TOP_S0 (R/W)	RS_RXBER_SF_ THRESHOLD	4	0×2200
RS SD Detect Interrupt Alarm	RS_ALARM_S0 (W1C)	RS_RXBER_SD_DET_A	4	0×2028
RS SF Detect Interrupt Alarm	RS_ALARM_S0 (W1C)	RS_RXBER_SF_DET_A	4	0×2028
RS SD Detect Mask	RS_MASK_2_S0 (R/W)	RS_RXBER_SD_DET_M	4	0×2064
RS SF Detect Mask	RS_MASK_2_S0 (R/W)	RS_RXBER_SF_DET_M	4	0×2064
RS SD Detect Persistence	RS_PERSIST_S0 (RO)	RS_RXBER_SD_DET_P	4	0×2098
RS SF Detect Persistence	RS_PERSIST_S0 (RO)	RS_RXBER_SF_DET_P	4	0×2098
RS SD Detect State	RS_STATE_S0 (RO)	RS_RXBER_SD_DET	4	0×20C8
RS SF Detect State	RS_STATE_S0 (RO)	RS_RXBER_SF_DET	4	0×20C8
RS BER Report	RS_RX_CNT_BERREP_S0 (RO)	RS_RXBER_REPORT	4	0×235E
RS BER-3 Detection Time	RS_RX_CTL_BERDT0 (R/W)	RS_RXBER_DETTIME0	1	0×2204
RS BER-4 Detection Time	RS_RX_CTL_BERDT1 (R/W)	RS_RXBER_DETTIME1	1	0×2205
RS BER-5 Detection Time	RS_RX_CTL_BERDT2 (R/W)	RS_RXBER_DETTIME2	1	0×2206
RS BER-6 Detection Time	RS_RX_CTL_BERDT3 (R/W)	RS_RXBER_DETTIME3	1	0×2207
RS BER-7 Detection Time	RS_RX_CTL_BERDT4 (R/W)	RS_RXBER_DETTIME4	1	0×2208
RS BER-8 Detection Time	RS_RX_CTL_BERDT5 (R/W)	RS_RXBER_DETTIME5	1	0×2209
RS BER-9 Detection Time	RS_RX_CTL_BERDT6 (R/W)	RS_RXBER_DETTIME6	1	0×220A
RS BER-10 Detection Time	RS_RX_CTL_BERDT7 (R/W)	RS_RXBER_DETTIME7	1	0×220B
RS BER-3 Detect Error Limit	RS_RX_CTL_BERSET0 (R/W)	RS_RXBER_SET0	1	0×220C
RS BER-4 Detect Error Limit	RS_RX_CTL_BERSET1 (R/W)	RS_RXBER_SET1	1	0×220E
RS BER-5 Detect Error Limit	RS_RX_CTL_BERSET2 (R/W)	RS_RXBER_SET2	1	0×2210
RS BER-6 Detect Error Limit	RS_RX_CTL_BERSET3 (R/W)	RS_RXBER_SET3	1	0×2212
RS BER-7 Detect Error Limit	RS_RX_CTL_BERSET4 (R/W)	RS_RXBER_SET4	1	0×2214
RS BER-8 Detect Error Limit	RS_RX_CTL_BERSET5 (R/W)	RS_RXBER_SET5	1	0×2216
RS BER-9 Detect Error Limit	RS_RX_CTL_BERSET6 (R/W)	RS_RXBER_SET6	1	0×2218
RS BER-4 Clear Error Limit	RS_RX_CTL_BERCLR0 (R/W)	RS_RXBER_CLR0	1	0×220D
RS BER-5 Clear Error Limit	RS_RX_CTL_BERCLR1 (R/W)	RS_RXBER_CLR1	1	0×220F
RS BER-6 Clear Error Limit	RS_RX_CTL_BERCLR2 (R/W)	RS_RXBER_CLR2	1	0×2211
RS BER-7 Clear Error Limit	RS_RX_CTL_BERCLR3 (R/W)	RS_RXBER_CLR3	1	0×2213
RS BER-8 Clear Error Limit	RS_RX_CTL_BERCLR4 (R/W)	RS_RXBER_CLR4	1	0×2215
RS BER-9 Clear Error Limit	RS_RX_CTL_BERCLR5 (R/W)	RS_RXBER_CLR5	1	0×2217
RS BER-10 Clear Error Limit	RS_RX_CTL_BERCLR6 (R/W)	RS_RXBER_CLR6	1	0×2219

17 Digital Wrapper Drop

17.1 Functional Description of Digital Wrapper Drop

The digital wrapper drop is used for overhead monitoring after the RS decoder (checkbyte calculate and correct). For each slice, the digital wrapper drop block accepts 32 bits of data. There is a total of four slices instantiated to create a 128-bit wide block for 16-way and 64-way 10 Gbits/s mode.

- All FEC/DW frame overhead dropping and monitoring functions supported by the DW in the receive direction are summarized in the following list:
  - Internal FEC overhead bytes monitor.
  - BIP-8 monitor (also has an available TCM byte).
  - BII monitor, BDI detect, IAE detect, and BEI monitor (also has an available TCM byte).
  - AIS, OCI, or other fixed pattern detect (STAT monitor in TCMi and PM bytes).
  - DWAC drop.
  - Insertion of AIS, OCI, or other fixed pattern.
  - PRBS monitor (also provides insert).

All monitors are disabled if the receive direction, loss-of-signal, loss-of-clock, and out-of-frame alarms are disabled. In the loss-of-frame case, the monitor continues functioning if its associate AIS inhibit is set.

Whenever the continuous N-times detect (CNTD) signals are defined, they require not only that the monitored signal be consistent for N consecutive frames, but also that the frame bytes be error free for all N frames before the status can be updated. N can range from 1 to 15. Programming a CNTD block with a value of 0 turns off the CNTD detection.

In the receive direction, 128-bit input data will be retimed and passed through without any processing to either DW_ES_RXDATA[127:0] or DWFEC_SYS_RX83DATA[127:0]. (Note that AIS insertion may need to be inhibited.)

In a loopback mode, the 128-bit input data can be selected from DW_RS_TXDATA[127:0].

17.1.1 Internal FEC Overhead Bytes Monitor (OH0 to OH3)

There are up to four overhead bytes per FEC or DW frame which can be detected and reported via the microprocessor. The provisioning location is programmable and operates identically to the digital wrapper OH0 to OH3 insert. See Section 8.1, Functional Description of Digital Wrapper Insert, on page 61 for the programming example.

- The monitored overhead byte is updated via a microprocessor after N consecutive consistent occurrences (frames) of a new pattern overhead byte is received. They can be grouped as the following:
  - Four 1-byte monitors.
  - Two 2-byte monitors.
  - One 3-byte and one 1-byte monitor.
  - One 4-byte monitor.

Multiple bytes do not need to be contiguous. Four bytes can be inserted from internal register per stream.

Table 63. OH0—OH3 Monitor Byte Group Indication Summary

Control Bits DW_RXOH0123_GRP[1:0]	Description	Valid CNTD Control Value
00	Four 1-Byte Group	OH3, OH2, OH1, OH0
01	Two 2-Byte Groups	OH2, OH0
10	One 1-Byte and One 3-Byte Group	OH1, OH0
11	One 4-Byte Group	OH0

Any changes to the receive overhead byte state must be reported to its interrupt alarm and persistency register bit. The interrupt alarm mask bit is also provided.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

Table 64. Internal FEC Overhead Byte Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Overhead Byte Monitor Group Indication: 00 = Four 1-byte. 01 = Two 2-byte. 10 = One 1-byte and one 3-byte. 11 = One 4-byte.	DW_RX_CTL_TOP_S0 (R/W)	DW_RXOH0123_GRP	4	0×2150
Overhead Byte Monitor Interrupt Alarm.	DW_ALARM_S0 (W1C)	DW_RXOH0_DET_A	4	0×2020
Overhead Byte Monitor Interrupt Alarm Mask.	DW_MASK_S0 (R/W)	DW_RXOH0_DET_M	4	0×205C
Overhead Byte Monitor Value.	DW_RX_VAL_OH01_S0 (RO)	DW_RXOH0_VAL	4	0×2320
Continuous N-Times Detect for Receive Overhead Byte (OH0). (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_OH0_2_S0 (R/W)	DW_RXOH0_CNTD	4	0×2154
Overhead Byte Monitor Frame Location (DW Mode Only).	DW_RX_CTL_OH0_2_S0 (R/W)	DW_RXOH0_FRM	4	0×2154
Overhead Byte Monitor Row Location.	DW_RX_CTL_OH0_2_S0 (R/W)	DW_RXOH0_ROW	4	0×2154
Overhead Byte Monitor Interrupt Alarm.	DW_ALARM_S0 (W1C)	DW_RXOH1_DET_A	4	0×2020
Overhead Byte Monitor Interrupt Alarm Mask.	DW_MASK_S0 (R/W)	DW_RXOH1_DET_M	4	0×205C
Overhead Byte Monitor Value.	DW_RX_VAL_OH01_S0 (RO)	DW_RXOH1_VAL	4	0×2320
Continuous N-Times Detect for Receive Overhead Byte (OH1). (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_OH1_2_S0 (R/W)	DW_RXOH1_CNTD	4	0×2158
Overhead Byte Monitor Frame Location (DW Mode Only).	DW_RX_CTL_OH1_2_S0 (R/W)	DW_RXOH1_FRM	4	0×2158
Overhead Byte Monitor Row Location.	DW_RX_CTL_OH1_2_S0 (R/W)	DW_RXOH1_ROW	4	0×2158
Overhead Byte Monitor Interrupt Alarm.	DW_ALARM_S0 (W1C)	DW_RXOH2_DET_A	4	0×2020
Overhead Byte Monitor Interrupt Alarm Mask.	DW_MASK_S0 (R/W)	DW_RXOH2_DET_M	4	0×205C
Overhead Byte Monitor Value.	DW_RX_VAL_OH23_S0 (RO)	DW_RXOH2_VAL	4	0×2324

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

Table 64. Internal FEC Overhead Byte Monitor Register Summary (continued)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Continuous N-Times Detect for Receive Overhead Byte (OH2). (The valid range for this register is 0x1—0xF. 0x0 is used to turn-off the monitor.)	DW_RX_CTL_OH2_2_S0 (R/W)	DW_RXOH2_CNTD	4	0×215C
Overhead Byte Monitor Frame Location (DW Mode Only).	DW_RX_CTL_OH2_2_S0 (R/W)	DW_RXOH2_FRM	4	0×215C
Overhead Byte Monitor Row Location.	DW_RX_CTL_OH2_2_S0 (R/W)	DW_RXOH2_ROW	4	0×215C
Overhead Byte Monitor Interrupt Alarm.	DW_ALARM_S0 (W1C)	DW_RXOH3_DET_A	4	0×2020
Overhead Byte Monitor Interrupt Alarm Mask.	DW_MASK_S0 (R/W)	DW_RXOH3_DET_M	4	0×205C
Overhead Byte Monitor Value.	DW_RX_VAL_OH23_S0 (RO)	DW_RXOH3_VAL	4	0×2324
Continuous N-Times Detect for Receive Overhead Byte (OH3). (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_OH3_2_S0 (R/W)	DW_RXOH3_CNTD	4	0×2160
Overhead Byte Monitor Frame Location (DW Mode Only).	DW_RX_CTL_OH3_2_S0 (R/W)	DW_RXOH3_FRM	4	0×2160
Overhead Byte Monitor Row Location.	DW_RX_CTL_OH3_2_S0 (R/W)	DW_RXOH3_ROW	4	0×2160

17.1.2 BIP-8 Monitor (See Figure 32 on Page 65)

For each FEC or DW frame, up to three single BIP-8 bytes per slice, even parity, is computed over the i – 2 frame (overhead and check bytes). In every FEC or DW frame, the received BIP-8 value is extracted and compared to the calculated BIP-8 byte for the previous frame.

Three per-slice BIP-8 bytes' locations for monitoring are programmable. In FEC frame, only the row location is used. Errors in the BIP-8 code are tabulated in an internal 27-bit counter based on either bit or block errors, as provisioned for each slice through the BIP-8 mode control bit.

In bit mode (selected by default), each BIP-8 bit in error causes the counter to increment. If block error is selected, each BIP-8 code in error causes the counter to increment only once. Regardless of which mode is selected, the value in the counter is transferred to maintenance register on the rising edge of the performance monitoring clock, at which point the counter is cleared. The counter will stop at the maximum value and will not roll over.

Twelve BIP-8 monitoring blocks are implemented, corresponding to each slice. In quad 2.5 Gbits/s mode, all these blocks function independently on 32 bits of data. In 10 Gbits/s mode, the slice 0 block functions on 128 bits of data and the other blocks are disabled.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.3 BII Monitor—BDI Detect and BEI Monitor

BDI can be detected via microprocessor control. There are 3 BDI bits per slice, for a total of 12 bits of BDI indication bytes, which can be detected by specifying the location of the frame and the row. In FEC frame mode, only the row location is used. See Figure 33 on Page 66 for BEI and BDI locations in the BII byte.

BEI (BIP error per frame) will be accumulated in a counter. BDI bit detect is declared when the monitored BDI bit is set after a number of N consecutive consistent occurrences (frames). Three sets of BII byte can be monitored.

17.1.4 OTU Section Monitoring (SM)

The following subfields in the SM bytes are monitored. These bytes will use the BIP0 set of register bits (DW_RXBIP0_DISABLE, etc.) in the monitor control registers.

17.1.4.1 SM—BIP-8

The BIP-8 is computed over all the bytes of OPUk (overhead and payload) in the nth frame and is compared against the received BIP in the n + 2 frame. The BIP errors (if any) are reported to the transmit overhead processor for insertion of BEI in the corresponding transmit SM byte. These bit errors are also accumulated in an internal register. The content of this internal register is transferred to the corresponding reporting register on performance monitoring reset. The internal accumulating register is then cleared. The internal accumulating counter can be set to count the number of bits (0x0) or blocks (0x1) in error.

Table 65. SM BIP-8 Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BIP Calculation Disable.	DW_RX_CTL_TOP_S0 (R/W)	DW_RXBIP0_DISABLE	4	0×2150
BIP Byte Counter Mode: 0 = Bit Count Mode. 1 = Block Count Mode.	DW_RX_CTL_BIP_S0 (R/W)	DW_RXBIP0_BIT_BLK	4	0×216C
BIP Byte Monitor Frame Location (DW mode only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_BIP_S0 (R/W)	DW_RXBIP0_FRM	4	0×216C
BIP Monitor Byte Row Location.	DW_RX_CTL_BIP_S0 (R/W)	DW_RXBIP0_ROW	4	0×216C
DW BIP-8 Error Counter.	DW_RX_CNT_BIP00_S0/ DW_RX_CNT_BIP01_S0 (RO)	DW_RXBIP00_ECNT/ DW_RXBIP01_ECNT	4	0×2328/ 0×2329

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.4.2 SM—Backward Error Indication (BEI)

These bits indicate the BIP errors in the far end and are accumulated in an internal register. The content of this internal register is transferred to the corresponding reporting register on performance monitoring reset. The internal accumulating register is then cleared. The internal accumulating counter can be set to count the number of bits (0x0) or blocks (0x1) in error.

Table 66. SM BEI Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BEI Calculation Disable.	DW_RX_CTL_TOP_S0 (R/W)	DW_RXBEI0_DISABLE	4	0×2150
BEI Counter Mode: 0 = Bit Count Mode. 1 = Block Count Mode.	DW_RX_CTL_BII_S0 (R/W)	DW_RXBEI0_BIT_BLK	4	0×2170
BII Byte Monitor Frame Location (DW Mode Only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_BII_S0 (R/W)	DW_RXBII0_FRM	4	0×2170
BII Monitor Byte Row Location.	DW_RX_CTL_BII_S0 (R/W)	DW_RXBII0_ROW	4	0×2170
DW BEI Error Counter.	DW_RX_CNT_BEI00_S0/ DW_RX_CNT_BEI01_S0 (RO)	DW_RXBEI00_ECNT/ DW_RXBEI01_ECNT	4	0×233A/ 0×233B

17.1.4.3 SM—Backward Defect Indication (BDI)

This bit is captured in the corresponding register. A new value is only validated after it has been received for a programmable N consecutive frames.

Table 67. SM BDI Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI Bit Monitor Interrupt Alarm.	DW_ALARM_S0 (W1C)	DW_RXBDI0_DET_A	4	0×2020
BDI Bit Monitor Interrupt Alarm Mask.	DW_MASK_S0 (R/W)	DW_RXBDI0_DET_M	4	0×205C
BDI Bit Monitor Persistency.	DW_PERSIST_2_S0 (RO)	DW_RXBDI0_DET_P	4	0×2090
BDI Bit Monitor State.	DW_STATE_2_S0 (RO)	DW_RXBDI0_DET	4	0×20C0
Continuous N-Times Detect and Clear BDI Monitor Byte Detect Condition. (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_BIICNTD_S0 (R/W)	DW_RXBDI0_CNTD	4	0×2174

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.4.4 SM—Incoming Alignment Error (IAE)

This bit indicates the alignment error in the far end and is captured in the corresponding register. A new value is only validated after it has been received for a programmable N consecutive frames. The bit location for the IAE value is fixed in the SM byte at row 0, column 9, bit 2.

Table 68. SM IAE Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
IAE Bit Monitor Interrupt Alarm	DW_ALARM_V2_S0 (W1C)	DW_RXIAE0_DET_A	4	0×2030
IAE Bit Monitor Interrupt Alarm Mask	DW_MASK_V2_S0 (R/W)	DW_RXIAE0_DET_M	4	0×206C
IAE Bit Monitor Persistency	DW_PERSIST_V2_S0 (RO)	DW_RXIAE0_DET_P	4	0×20A0
IAE Bit Monitor State	DW_STATE_V2_S0 (RO)	DW_RXIAE0_DET	4	0×20D0
Continuous N-Times Detect and Clear IAE Monitor Byte Detect Condition (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_V2_S0 (R/W)	DW_RXIAE0_CNTD	4	0×2500

17.1.5 ODU Path Monitoring (PM)

The PM bytes are processed identically to the SM/TCM byte (see Section 7.1.4 on page 60). These bytes will use the BIP1 set of register bits (DW_RXBIP1_DISABLE, etc.) in the monitor control registers.

17.1.5.1 PM—BIP-8

Table 69. PM BIP-8 Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BIP Calculation Disable	DW_RX_CTL_TOP_S0 (R/W)	DW_RXBIP1_DISABLE	4	0×2150
BIP Byte Counter Mode: 0 = Bit Count Mode. 1 = Block Count Mode.	DW_RX_CTL_BIP_S0 (R/W)	DW_RXBIP1_BIT_BLK	4	0×216C
BIP Byte Monitor Frame Location (DW Mode Only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_BIP_S0 (R/W)	DW_RXBIP1_FRM	4	0×216C
BIP Monitor Byte Row Location	DW_RX_CTL_BIP_S0 (R/W)	DW_RXBIP1_ROW	4	0×216C
DW BIP-8 Error Counter	DW_RX_CNT_BIP10_S0/ DW_RX_CNT_BIP11_S0 (RO)	DW_RXBIP10_ECNT/ DW_RXBIP11_ECNT	4	0×2331/ 0×2332

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.5.2 PM—Backward Error Indication (BEI)

Table 70. PM BEI Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BEI Calculation Disable	DW_RX_CTL_TOP_S0 (R/W)	DW_RXBEI1_DISABLE	4	0×2150
BEI Counter Mode: 0 = Bit Count Mode. 1 = Block Count Mode.	DW_RX_CTL_BII_S0 (R/W)	DW_RXBEI1_BIT_BLK	4	0×2170
BII Byte Monitor Frame Location (DW Mode Only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_BII_S0 (R/W)	DW_RXBII1_FRM	4	0×2170
BII Monitor Byte Row Location	DW_RX_CTL_BII_S0 (R/W)	DW_RXBII1_ROW	4	0×2170
DW BEI Error Counter	DW_RX_CNT_BEI10_S0/ DW_RX_CNT_BEI11_S0 (RO)/	DW_RXBEI10_ECNT/ DW_RXBEI11_ECNT	4	0×2343/ 0×2344

17.1.5.3 PM—Backward Defect Indication (BDI)

Table 71. PM BDI Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI Bit Monitor Interrupt Alarm.	DW_ALARM_S0 (W1C)	DW_RXBDI1_DET_A	4	0×2020
BDI Bit Monitor Interrupt Alarm Mask.	DW_MASK_S0 (R/W)	DW_RXBDI1_DET_M	4	0×205C
BDI Bit Monitor Persistency.	DW_PERSIST_2_S0 (RO)	DW_RXBDI1_DET_P	4	0×2090
BDI Bit Monitor State.	DW_STATE_2_S0 (RO)	DW_RXBDI1_DET	4	0×20C0
Continuous N-Times Detect and Clear BDI Monitor Byte Detect Condition. (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_BIICNTD_S0 (R/W)	DW_RXBDI1_CNTD	4	0×2174

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.5.4 PM—Status (STAT)

Table 72. STAT Bits Monitoring

MS Value	Maintenance Signal
0x66	ODUk-OCI
0x55	ODUk-LCK
0xFF	ODUk-AIS

AIS, OCI, or other fixed patterns can be detected via microprocessor control. One indication byte can be detected by specifying the frame location, row location, and expected value. In FEC frame mode, only the row location is used.

The AIS, OCI, or other pattern byte detect is declared when the monitored byte is AIS (all 1s), OCI (all 6s), or other fixed pattern byte pattern after setting a number of N consecutive consistent occurrences (frames).

The AIS, OCI, or other pattern byte detect is cleared when the monitored byte is found to be a mismatch from AIS (all 1s), OCI (all 6s), or other pattern byte for a clearing number of N consecutive consistent occurrences (frames).

AIS, OCI, or other pattern byte detects report the interrupt alarm, persistency, and state bit via the microprocessor.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

Table 73. PM STAT Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (Hex)
AIS Monitor Byte Detect Condition Interrupt Alarm	DW_ALARM_S0 (W1C)	DW_RXAIS_DET_A	4	0×2020
AIS Monitor Byte Detect Condition Interrupt Alarm Mask	DW_MASK_S0 (R/W)	DW_RXAIS_DET_M	4	0×205C
AIS Monitor Byte Detect Condition Persistence	DW_PERSIST_2_S0 (RO)	DW_RXAIS_DET_P	4	0×2090
AIS Monitor Byte Detect Condition State	DW_STATE_2_S0 (RO)	DW_RXAIS_DET[1]	4	0×20C0
OCI Monitor Byte Detect Condition Interrupt Alarm	DW_ALARM_S0 (W1C)	DW_RXOCI_DET_A	4	0×2020
OCI Monitor Byte Detect Condition Interrupt Alarm Mask	DW_MASK_S0 (R/W)	DW_RXOCI_DET_M	4	0×205C
OCI Monitor Byte Detect Condition Persistence	DW_PERSIST_2_S0 (RO)	DW_RXOCI_DET_P	4	0×2090
OCI Monitor Byte Detect Condition State	DW_STATE_2_S0 (RO)	DW_RXOCI_DET[2]	4	0×20C0
FIX Monitor Byte Detect Condition Interrupt Alarm	DW_ALARM_S0 (W1C)	DW_RXFIX_DET_A	4	0×2020
FIX Monitor Byte Detect Condition Interrupt Alarm Mask	DW_MASK_S0 (R/W)	DW_RXFIX_DET_M	4	0×205C
FIX Monitor Byte Detect Condition Persistence	DW_PERSIST_2_S0 (RO)	DW_RXFIX_DET_P	4	0×2090
FIX Monitor Byte Detect Condition State	DW_STATE_2_S0 (RO)	DW_RXFIX_DET[3]	4	0×20C0
Fixed Pattern Monitor And Insert Byte Value	DW_RX_CTL_AISBYTE_S0 (R/W)	DW_RXFIX_VAL	4	0×2168
Continuous N-Times Detect for Setting AIS, OCI, or Other Fixed Pattern Monitor Byte Detect Condition. (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_AIS_2_S0 (R/W)	DW_RXAIS_SETCNTD	4	0×2164

1. DW_RXAIS_DET is when AIS byte or PM-STAT or TCM-STAT detected AIS.
2. DW_RXOCI_DET is when AIS byte or PM-STAT or TCM-STAT detected OCI.
3. DW_RXFIX_DET is when AIS byte or PM-STAT or TCM-STAT detected LCK or fixed pattern is detected.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

Table 73. PM STAT Register Summary (continued)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (Hex)
Continuous N-Times Detect for Clearing AIS, OCI, or Other Fixed Pattern Monitor Byte Detect Condition. (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_AIS_2_S0 (R/W)	DW_RXAIS_CLRCNTD	4	0×2164
AIS, OCI, or Other Fixed Pattern Byte Monitor Frame Location (DW Mode Only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_AIS_2_S0 (R/W)	DW_RXAIS_FRM	4	0×2164
AIS, OCI, or Other Fixed Pattern Monitor Byte Row Location	DW_RX_CTL_AIS_2_S0 (R/W)	DW_RXAIS_ROW	4	0×2164
STAT N-Time	DW_RX_CTL_OH_V2_S0 (RW)	DW_RXBII1_STAT_CNTD	4	0×2504
New Validated STAT Value Interrupt Alarm	DW_ALARM_V2_S0 (RO)	DW_RX_BII1_STAT_NEW_A	4	0×2030
New Validated STAT Value Persistency Mask	DW_MASK_V2_S0 (RO)	DW_RX_BII1_STAT_NEW_M	4	0×206C
New Validated STAT Value Persistency	DW_PERSIST_V2_S0 (RO)	DW_RX_BII1_STAT_NEW_P	4	0×20A0
STAT Value	DW_RX_MON_V2_S0 (RO)	DW_RX_BII1_STAT	4	0×2546

1. DW_RXAIS_DET is when AIS byte or PM-STAT or TCM-STAT detected AIS.
2. DW_RXOCI_DET is when AIS byte or PM-STAT or TCM-STAT detected OCI.
3. DW_RXFIX_DET is when AIS byte or PM-STAT or TCM-STAT detected LCK or fixed pattern is detected.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.6 ODUk Tandem Connection Monitoring (TCM)

There are 6 TCM bytes in an OTU frame. Any one of these 6 TCM bytes can be monitored by selecting it via the microprocessor. The selected TCM bytes are then processed identically to the SM byte (Section 7.1.4 on page 60). These bytes will use the BIP2 set of register bits (DW_RXBIP2_DISABLE, etc.) in the monitor control registers

17.1.6.1 TCMi—BIP-8

Table 74. TCM BIP-8 Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BIP Calculation Disable	DW_RX_CTL_V2_S0 (R/W)	DW_RX_BIP2_DISABLE	4	0×2500
BIP Byte Counter Mode: 0 = Bit Count Mode. 1 = Block Count Mode.	DW_RX_CTL_V2_S0 (R/W)	DW_RX_BIP2_BIT_BLK	4	0×2500
BIP Byte Monitor Frame Location (DW Mode Only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_BII2_V2_2_S0 (R/W)	DW_RXBIP2_FRM	4	0×2508
BIP Monitor Byte Row Location	DW_RX_CTL_BII2_V2_2_S0 (R/W)	DW_RXBIP2_ROW	4	0×2508
DW BIP-8 Error Counter	DW_RX_CNT_BIP20_V2_S0/ DW_RX_CNT_BIP21_V2_S0 (RO)	DW_RXBIP20_ECNT/ DW_RXBIP21_ECNT	4	0×2534/ 0×2535

17.1.6.2 TCMi—Backward Error Indication (BEI)

Table 75. TCM BEI Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BEI Calculation Disable	DW_RX_CTL_V2_S0 (R/W)	DW_RX_BEI2_DISABLE	4	0×2500
BEI Counter Mode: 0 = Bit Count Mode. 1 = Block Count Mode.	DW_RX_CTL_V2_S0 (R/W)	DW_RX_BEI2_BIT_BLK	4	0×2500
BII Byte Monitor Frame Location (DW Mode Only): 00 = Frame N. 01 = Frame N + 1. 10 = Frame N + 2. 11 = Frame N + 3.	DW_RX_CTL_BII2_V2_2_S0 (R/W) Used for BEI, BDI, and STAT Locations	DW_RXBII2_FRM	4	0×2508
BII Monitor Byte Row Location	DW_RX_CTL_BII2_V2_2_S0 (R/W) Used for BEI, BDI, and STAT Locations	DW_RXBII2_ROW	4	0×2508
DW BEI Error Counter	DW_RX_CNT_BEI20_V2_S0/ DW_RX_CNT_BEI21_V2_S0 (RO)	DW_RXBEI20_ECNT/ DW_RXBEI21_ECNT	4	0×253D/ 0×253E

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.6.3 TCMi—Backward Defect Indication (BDI)

Table 76. TCM BDI Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI Bit Monitor Interrupt Alarm	DW_ALARM_V2_S0 (W1C)	DW_RXBDI2_DET_A	4	0×2030
BDI Bit Monitor Interrupt Alarm Mask	DW_MASK_V2_S0 (R/W)	DW_RXBDI2_DET_M	4	0×206C
BDI Bit Monitor Persistency	DW_PERSIST_V2_S0 (RO)	DW_RXBDI2_DET_P	4	0×20A0
BDI Bit Monitor State	DW_STATE_V2_S0 (RO)	DW_RXBDI2_DET	4	0×20D0
Continuous N-Times Detect and Clear BDI Monitor Byte Detect Condition (The valid range for this register is 0x1—0xF. 0x0 is used to turn off the monitor.)	DW_RX_CTL_CNTD_V2_S0 (R/W)	DW_RXBDI2_CNTD	4	0×2510

17.1.6.4 Status (STAT)

Table 77. STAT Bits Monitoring

MS Value	Maintenance Signal
0x66	ODUk-OCI
0x55	ODUk-LCK
0xFF	ODUk-AIS

Table 78. TCM STAT Register Summary

Function	Register Name	Register Bits	Qty.	1st Addr (Hex)
STAT N-Time	DW_RX_CTL_CNTD_V2_S0 (RW)	DW_RXBII2_STAT_CNTD	4	0×2510
New Validated STAT Value Interrupt Alarm	DW_ALARM_V2_S0 (RO)	DW_RX_BII2_STAT_NEW_A	4	0×2030
New Validated STAT Value Persistency Mask	DW_MASK_V2_S0 (RO)	DW_RX_BII2_STAT_NEW_M	4	0×206C
New Validated STAT Value Persistency	DW_PERSIST_V2_S0 (RO)	DW_RX_BII2_STAT_NEW_P	4	0×20A0
STAT Value	DW_RX_MON_V2_S0 (RO)	DW_RX_BII2_STAT	4	0×2546

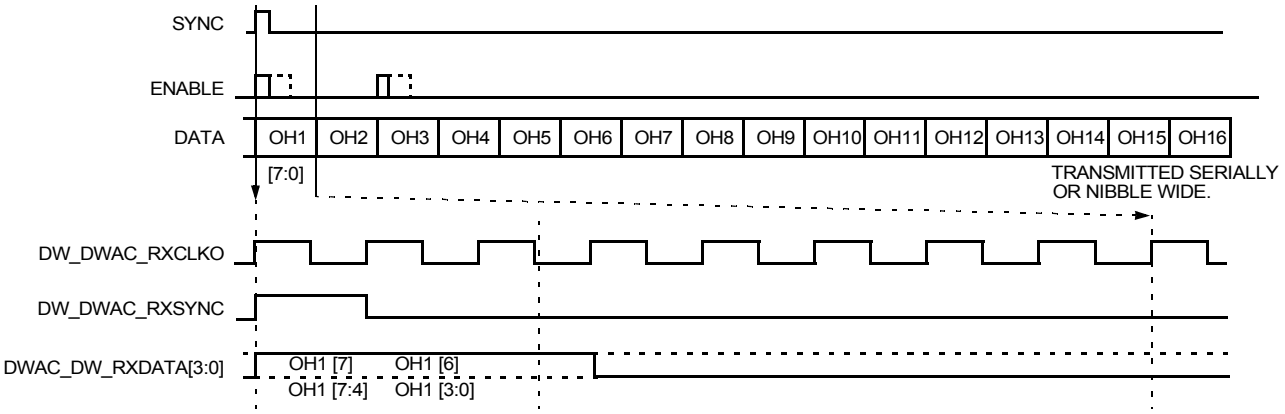
17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.7 DWAC Drop

The drop DWAC consists of the following three signals per channel (total of four DWAC channels):

— Output clock at ~10.455 MHz (10 Gbits/s mode and quad 2.5 Gbits/s mode).
— Output superframe sync (~326.7/~81.68 kHz—10 Gbits/s (FEC/DW), ~81.68/~20.42 kHz—quad 2.5 Gbits/s (FEC/DW)) coincident with the MSB (most significant bit) of the first byte in frame 0.
— Output data: 4 bits in 10 Gbits/s mode and 1 bit per stream in quad 2.5 Gbits/s mode.



Note: See the Timing Characteristics section in the Hardware Design Guide for the Transmit Transport Overhead Access Channel section. DW_DWAC_RXCLKO is not 50% duty cycle.

Figure 46. Receive DWAC Frame Definition

Three BII bytes can be overwritten to BII byte locations using monitored BIP-8 error per frame and DW_TXBDI_DET information (signal from transmit direction). The BII overwritten byte capability is provided for a regenerator mode.

Table 79. Receive DWAC Drop Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BDI (Tx Detect) Overwritten to DWAC Drop (SM-BDI)	DW_DWAC_RX_CTL_S0 (R/W)	DWAC_RXBDI0_OVWR	4	0×21C0
BEI (Tx Detect) Overwritten to DWAC Drop (SM-BEI)	DW_DWAC_RX_CTL_S0 (R/W)	DWAC_RXBEI0_OVWR	4	0×21C0
IAE (Tx Detect) Overwritten to DWAC Drop (SM-IAE)	DW_DWAC_RX_CTL_V2_S0 (R/W)	DWAC_RXIAE0_OVWR	4	0×252C
BDI (Tx Detect) Overwritten to DWAC Drop (PM-BDI)	DW_DWAC_RX_CTL_S0 (R/W)	DWAC_RXBDI1_OVWR	4	0×21C0
BEI (Tx Detect) Overwritten to DWAC Drop (PM-BEI)	DW_DWAC_RX_CTL_S0 (R/W)	DWAC_RXBEI1_OVWR	4	0×21C0
BDI (Tx Detect) Overwritten to DWAC Drop (TCM-BDI)	DW_DWAC_RX_CTL_V2_S0 (R/W)	DWAC_RXBDI2_OVWR	4	0×252C
BEI (Tx Detect) Overwritten to DWAC Drop (TCM-BEI)	DW_DWAC_RX_CTL_V2_S0 (R/W)	DWAC_RXBEI2_OVWR	4	0×252C

Note: BDI/BEI/IAE value are calculated, processed, and overwritten at the corresponding location. Ex., BEI calculated value can be inserted at SM-BEI before being dropped by the DWAC.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.8 Insertion of AIS, OCI, and Other Fixed Patterns

The macro will automatically generate AIS, OCI, and other fixed pattern bytes with valid framing byte patterns by alarms (hardware) or software insert. The AIS, OCI, or other pattern insert priorities are defined in Table 23 on page 54.

Table 80. AIS, OCI, and Fixed Pattern Insert Priority

Priority (Highest = 1, Lowest = 6)	AIS, OCI, or Other Pattern
1	AIS Insert (Software)
	(DW_RXAIS_INS)
2	OCI Insert (Software)
	(DW_RXOCI_INS)
3	LCK or Fixed Pattern Insert (Software)
	(DW_RXFIX_INS)
4	AIS Alarm Detect (Hardware)
	(LINE_RX83LOC and not (DW_RXLOC_AISINH)) or (FRM_DW_RX_LOS and not (DW_RXLOS_AISINH)) or (FRM_DW_RX_OOF and not (DW_RXOOF_AISINH)) or (FRM_DW_RX_LOF and not (DW_RXLOF_AISINH)) or (RS_BER_SD and not (DW_RXSD_AISINH)) or (RS_BER_SD and not (DW_RXSD_AISINH)) or (DW_RXAIS_DET[1]) and not (DW_RXAIS_DETINH)
5	OCI Alarm Detect (Hardware)
	(DW_RXOCI_DET[2] and not (DW_RXOCI_DETINH))
6	Other Fixed Pattern Alarm Detect (Hardware)
	(DW_RXFIX_DET[3] and not (DW_RXFIX_DETINH))

1. DW_RXAIS_DET is when AIS byte or PM-STAT or TCM-STAT detected AIS.
2. DW_RXOCI_DET is when AIS byte or PM-STAT or TCM-STAT detected OCI.
3. DW_RXFIX_DET is when AIS byte or PM-STAT or TCM-STAT detected LCK or fixed pattern is detected.

- DW_RXAIS_COND is active-high (output) if AIS pattern in STAT1 or STAT2 is detected and inserted.
- DW_RXOCI_COND is active-high (output) if OCI pattern in STAT1 or STAT2 is detected.
- DW_RXFIX_COND is active-high (output) if fixed or LCK pattern in STAT1 or STAT2 is detected.

When DW_RXAIS_COND is set to logic 1, a default pattern of all 1s will be inserted. When the DW_RXOCI_DET alarm is in detect mode (active), an OCI (0x66) pattern will be inserted. When the DW_RXFIX_DET alarm is detected, all LCK (0x55) or fixed patterns in DW_RXFIX_VAL will be inserted via the microprocessor. AIS, OCI, or other fixed patterns can be inserted. AIS/OCI/LOCk signals are generated as per Table 77 on page 105.

The DW_RXAIS_COND is also an output to an elastic store (Rx). At programmable MFAS location bytes, overhead in the OTU OH field is valid and is not overwritten by AIS generator. TCM0—TCM5, GCC0—GCC2, and APS/PCC inhibit are available. In 10 Gbits/s mode, only slice 0 is valid.

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

Table 81. Insertion of AIS Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
AIS Insert Control Bit (when set to logic 1, AIS condition will be inserted)	DW_RX_CTL_TOP_S0 (R/W)	DW_RXAIS_INS	4	0×2150
OCI Insert Control Bit.	DW_RX_CTL_TOP_S0 (R/W)	DW_RXOCI_INS	4	0×2150
Fixed Pattern Insert Control Bit	DW_RX_CTL_TOP_S0 (R/W)	DW_RXFIX_INS	4	0×2150
Number of Multiframe (MFAS) Bytes After OA2 (see Table 25 on Page 57)	DW_RX_CTL_OH_V2_S0 (R/W)	DW_RXOA12_MFAS	4	0×2504
Loss-of-Clock AIS Inhibit (When set to logic 1, the AIS insert will be inhibited in case of loss-of-clock (LINE_RX83LOC))	DW_RX_CTL_TOP_S0 (R/W)	DW_RXLOC_AISINH	4	0×2150
Out-of-Frame AIS Inhibit (When set to logic 1, the AIS insert will be inhibited in case of out-of-frame (FRM_RXOOF))	DW_RX_CTL_TOP_S0 (R/W)	DW_RXOOF_AISINH	4	0×2150
Loss-of-Frame AIS Inhibit (When set to logic 1, the AIS insert will be inhibited in case of loss-of-frame (FRM_RXLOF))	DW_RX_CTL_TOP_S0 (R/W)	DW_RXLOF_AISINH	4	0×2150
Loss-of-Signal AIS Inhibit (When set to logic 1, the AIS insert will be inhibited in case of loss-of-signal (FRM_RXLOS))	DW_RX_CTL_TOP_S0 (R/W)	DW_RXLOS_AISINH	4	0×2150
AIS Failure Condition when Detect SF Inhibit	DW_RX_CTL_AIS_V2_S0 (R/W)	DW_RXSF_AISINH	4	0×250C
AIS Failure Condition when Detect SD Inhibit	DW_RX_CTL_AIS_V2_S0 (R/W)	DW_RXSD_AISINH	4	0×250C
AIS Detect, AIS Pattern Insert Inhibit	DW_RX_CTL_TOP_S0 (R/W)	DW_RXAIS_DETINH	4	0×2150
OCI Detect, OCI Pattern Insert Inhibit	DW_RX_CTL_TOP_S0 (R/W)	DW_RXOCI_DETINH	4	0×2150
Fixed Pattern Detect, Fixed Pattern Insert Inhibit	DW_RX_CTL_TOP_S0 (R/W)	DW_RXFIX_DETINH	4	0×2150
Choose Insert Pattern of LCK (0x55) or FIX Value	DW_RX_CTL_V2_S0 (RW)	DW_RXLCK_FIX	4	0×2500
FTFL Inhibit During AIS	DW_RX_CTL_AIS_V2_S0 (RW)	DW_RXAIS_FTFLINH	4	0×250C

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

Table 81. Insertion of AIS Register Summary (continued)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
TCM0 to TCM5 Insert During AIS/OCI/LCK[1]	DW_RX_CTL_AIS_V2_S0 (RW)	DW_RXAIS_TCMINH	4	0×250C
GCC0 to GCC2 Inhibit During AIS/OCI/LCK	DW_RX_CTL_AIS_V2_S0 (RW)	DW_RXAIS_GCCINH	4	0×250C
APS/PCC Inhibit During AIS/OCI/LCK	DW_RX_CTL_AIS_V2_S0 (RW)	DW_RXAIS_APSINH	4	0×250C
TCM0 to TCM5 Insert During AIS/OCI/LCK[1] Inhibit	DW_RX_CTL_OH_V2_S0 (RW)	DW_RXAIS_TCMSTAT_IAEINH	4	0×2504

1. If TCM insert during AIS/OCI/LCK, STAT [2:0] will be inserted 001 for normal operation mode. (IAE in-use is not available.)

The following figure shows the alarm structure of the AIS/OCI/FIX detection and insertion.

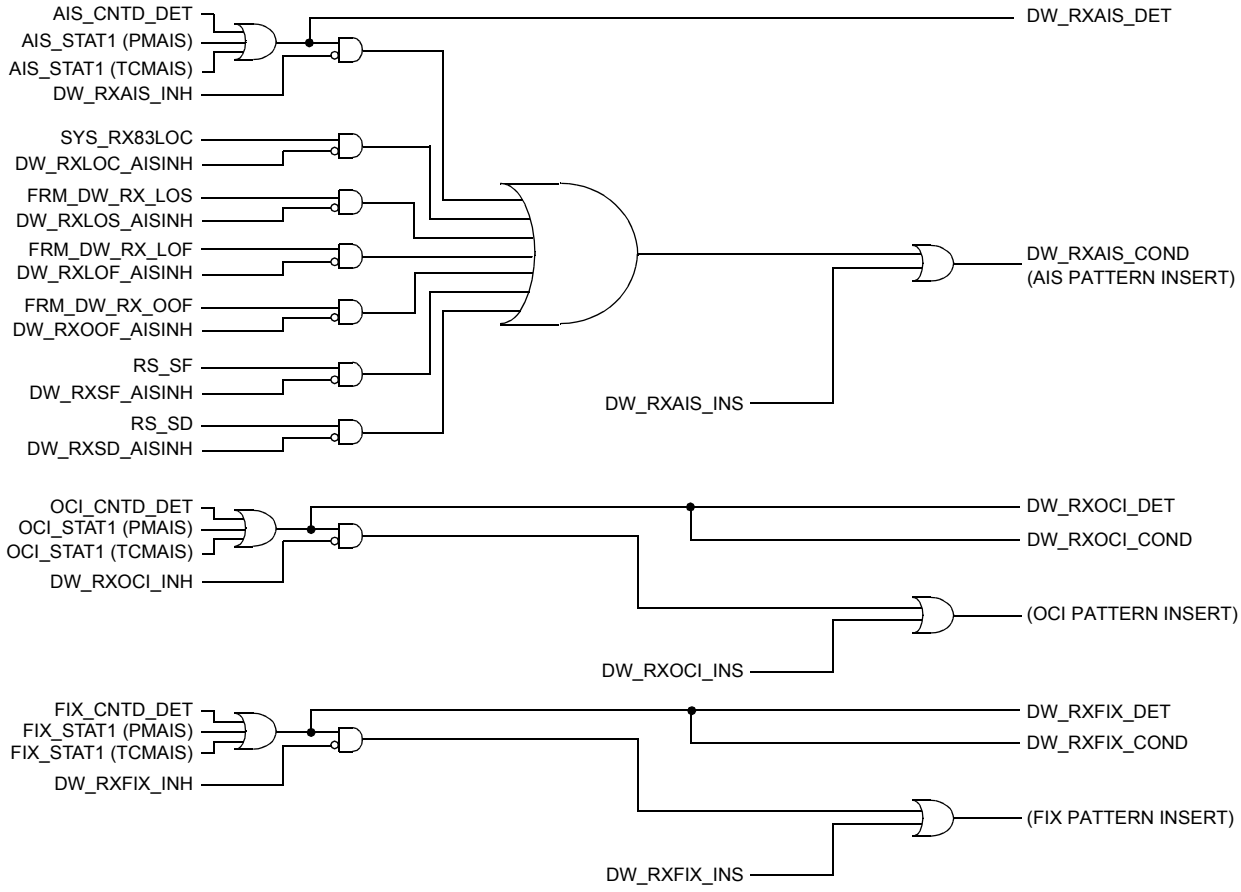


Figure 47. AIS/OCI/FIX Alarm Structure (per Slice)

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.9 PRBS Monitor

PRBS data in payload locations (excluding overhead and check bytes location) can be monitored by the PRBS monitor at the output pins (DW_RXPRBSDATA[127:0] and DW_RXPRBSDATA_EN[3:0]). A pseudorandom sequence pattern (either $2^{31} – 1$ or $2^{29} – 1$) can be detected.

When 32 consecutive bits matches in its pattern, the pattern sync state declares itself in-sync. If eight or more consecutive mismatches are in the payload sequence, the corresponding pattern sync state declares itself out-of-sync. In 10 Gbits/s mode, the payload goes into sync if the most up-to-date 32 bits (LSB) are a match, and declares itself out-of-sync if the most up-to-date of the last 32 bits (LSB) has eight or more consecutive mismatches in the payload sequence.

Note: If 32 bits match and/or eight mismatches occur in a less up-to-date pattern [127:32], it will be ignored.

The pattern sync state also provides interrupt alarm and persistence. The PRBS can also monitor for inverted patterns via the microprocessor. For any bit errors occurring after the monitor is in the in-sync state, an 8-bit counter reports the number of bit errors using clear-on-read toggle from the microprocessor.

Table 82. PRBS Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Receive PRBS Pattern (Payload Only) Monitor is Expected to be Inverted When Set	DW_PRBS_CTL_S0 (R/W)	DW_RXPRBS_INV	4	0×21E0
Receive PRBS Pattern Sequence Selection: 0 = $2^{29} – 1$. 1 = $2^{31} – 1$.	DW_PRBS_CTL_S0 (R/W)	DW_RXPRBS_29_31_PAT	4	0×21E0
Receive PRBS Error Pattern Counter. The PRBS monitor counts the number of times the input data differs from the expected value in an 8-bit counter that holds its count when it reaches the maximum value of 255. This counter is reset when ready by the microprocessor, and is not affected by the PMRST signal. (clear-on-read)	DW_RX_CNT_ PRBS_S0 (COR)	DW_RXPRBS_ECNT	4	0×2600
Receive PRBS Pattern Sync Interrupt Alarm Bit	DW_PRBS_ ALARM_S0 (W1C)	DW_RXPRBS_SYNC_A	4	0×2024
Receive PRBS Pattern Sync Mask Bit	DW_PRBS_MASK_ S0 (R/W)	DW_RXPRBS_SYNC_M	4	0×2060
Receive PRBS Pattern Sync Persistency Bit	DW_PRBS_ PERSIST_S0 (RO)	DW_RXPRBS_SYNC_P	4	0×2094
Receive PRBS Pattern Sync Alarm Bit	DW_PRBS_ ALARM_S0 (W1C)	DW_RXPRBS_SYNC	4	0×2024
When the PRBS pattern (payload only) detects 32 matches in a row, it declares itself in-sync and the error detector is enabled. if the device detects eight consecutive mismatches, the test pattern detector declares itself out-of-sync and starts searching again. 0 = In-sync. 1 = Out-of-sync.	DW_PRBS_STATE_ S0 (RO)	DW_RXPRBS_SYNC	4	0×20C4

17 Digital Wrapper Drop (continued)

17.1 Functional Description of Digital Wrapper Drop (continued)

17.1.10 PRBS Insert

Table 83. PRBS Insert Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
PRBS Pattern (payload only) Insert	DW_PRBS_CTL_V2_S0 (R/W)	DW_RXPRBS_INS	4	0×2530
PRBS Inverted Pattern Insert (payload only) Insert	DW_PRBS_CTL_V2_S0 (R/W)	DW_RXPRBS_INS_INV	4	0×2530
PRBS Pattern Sequence Insert Selection: 0 = $2^{29} – 1$ 1 = $2^{31} – 1$	DW_PRBS_CTL_V2_S0 (R/W)	DW_RXPRBS_INS_29_31_PAT	4	0×2530
Received PRBS Error Insert Bit (1 error bit per 128 bits in 10 Gbits/s mode, and 1 bit per 32 bits in 2.5 Gbits/s mode)	DW_PRBS_CTL_V2_S0 (R/W)	DW_RXPRBS_INS_1BERRINS	4	0×2530

17.1.11 No Fix Stuff Mode

A register bit can be enabled to disable the fix stuff column.

Table 84. Receive Data No Fix Stuff Mode Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Fix Column Disable (119th column is reserved for fixed stuff, 10 Gbits/s mode only)	DW_RX_CTL_V2_S0 (RW)	DW_RX_NO_FS	1	0×2500

18 Elastic Store (Receive Direction)

18.1 Functional Description of Elastic Store Receive Direction

The receive elastic store (ES) buffers gapped 83 MHz data and outputs 78 MHz data to absorb clock gapping of the FEC/DW overheads and FEC check bytes. Data arrives to the receive ES grouped as 32 bits in each slice. Each group of 32 bits is written into the associated ES location (128 locations x 32 bits) by 237/238 clock cycles (payload region of the FEC/DW frame) out of 255 clock cycles (whole FEC/DW frame) in the 83 MHz clock. Data is read from the ES by a 78 MHz clock.

The relationship between read and write addresses is controlled in order to minimize signal delay and to guarantee data integrity at the same time. In the initial state, or after over/underflow, the write address is automatically reset to the predefined position (32 locations ahead of the read address), when the first sync pulse is received.

In 10 Gbits/s mode, all four elastic stores should work in synchronization.

In some applications, the receive ES is disabled and data is bypassed. In this case, the overflow/underflow alarm is not declared. By software control, the elastic store is forced to restart.

Table 85. Elastic Store (Rx) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Rx ES Overflowing Interrupt Alarm	ES_ALARM_S0 (W1C)	ES_RX_OVERFLW_A	4	0×201C
Rx ES Underflowing Interrupt Alarm	ES_ALARM_S0 (W1C)	ES_RX_UNDRFLW_A	4	0×201C
Rx ES Overflowing Interrupt Alarm Mask	ES_MASK_S0 (R/W)	ES_RX_OVERFLW_M	4	0×2058
Rx ES Underflowing Interrupt Alarm Mask	ES_MASK_S0 (R/W)	ES_RX_UNDRFLW_M	4	0×2058
Rx ES Forced Restart	ES_CTL_S0 (R/W)	ES_RX_RESTART	4	0×2130

19 SONET FEC (BCH Weak/In Band) Supermacro

19.1 SONFEC (BCH Weak/In Band) Introduction

- The following sections provide the functional description of the SONET weak FEC supermacro core: in-band. The functional description includes requirements that must be met, as derived from various specifications. The weak FEC supermacro core consists of the following:
  - SONET STS-192/Quad STS-48 BCH Macro Core
  - SONET STS-192/Quad STS-48 Framer
  - SONET STS-192/Quad STS-48 B1 Monitoring
  - SONET STS-192/Quad STS-48 Descrambler
  - SONET STS-192/Quad STS-48 Alignment FIFO (transmit only)
  - SONET STS-192/Quad STS-48 Transpose Demultiplexer
  - SONET STS-192/Quad STS-48 B2 Monitoring
  - SONET Overhead/PRBS Payload Insert Processing
  - SONET Overhead/PRBS Payload Monitor Processing
  - SONET STS-192/Quad STS-48 B2 Computing
  - SONET STS-192/Quad STS-48 Transpose Multiplexer
  - SONET STS-192/Quad STS-48 Scrambler
  - SONET STS-192/Quad STS-48 B1 Computing

19.2 Functional Description of SONET FEC (BCH Weak/In Band) Supermacro

The SONET FEC (SONFEC) supermacro incorporates all the SONET-related functions of the TFEC0410G device. It performs the BCH encoding of the incoming STS data in the transmit direction and BCH decoding in the receive direction. In both directions, all the blocks that modify/monitor the data can be disabled.

In the transmit direction, the incoming data is framed, optionally descrambled, and monitored for B1 BIP errors. If loss of frame, loss of signal, or RDI/AIS is detected, then the AIS frames are generated and all the functions are disabled (including BCH encoding). If no AIS conditions exist, or no AIS data is received, then the data is passed on to the overhead processing macro. The overhead processor inserts the provisioned overhead bytes (software, TOAC, default, or data as received). The complete SONET frame is then BCH encoded and optionally scrambled before being sent out from this macro.

In the receive direction, the incoming data is framed, optionally descrambled, and monitored for B1 BIP errors. If loss of frame, loss of signal, or RDI/AIS is detected, then AIS frames are generated and all the functions are disabled (including BCH decoding). If no AIS conditions exist, or no AIS data is received, then the data is error corrected by the BCH decoder (if within its error correction capability) and then is passed on to the overhead processing macro. The overhead processor drops the overhead bytes on the TOAC channel and performs overhead byte analysis on individual bytes, if enabled. The complete SONET frame is then optionally scrambled before being sent out from this macro. In the receive direction, software can monitor the error correction performance through the BIP error counts provided both before and after BCH decoding. The B1 or B2 BIP errors can be monitored before BCH decoding for SD/SF detection. The B2 errors can be monitored before or after BCH decoding for SD/SF detection.

The SONET supermacro also supports two loopback modes: one on the line side and the other on the system side. Individual disable controls for all the blocks allow operational flexibility within the device. As an example, in loopback mode, one of the framers (of the two in the loop) can be disabled as the other one performs the framing. This avoids redundancy of alarm signals as well as reduces the delay in framing. Since individual macros are independently controlled by software, care must be taken to program the mode (10 Gbits/s mode/2.5 Gbits/s mode) of each block.

In virtual 10 Gbits/s mode (in the transmit direction only), the incoming four 2.5 Gbits/s mode STS-48 signals are frame aligned at the alignment FIFO and then multiplexed to form one single 10 Gbits/s mode STS-192 signal.

The structure of SONET weak FEC supermacro is shown in Figure 48 on page 114.

19 SONET FEC (BCH Weak/In Band) Supermacro (continued)

19.2 Functional Description of SONET FEC (BCH Weak/In Band) Supermacro (continued)

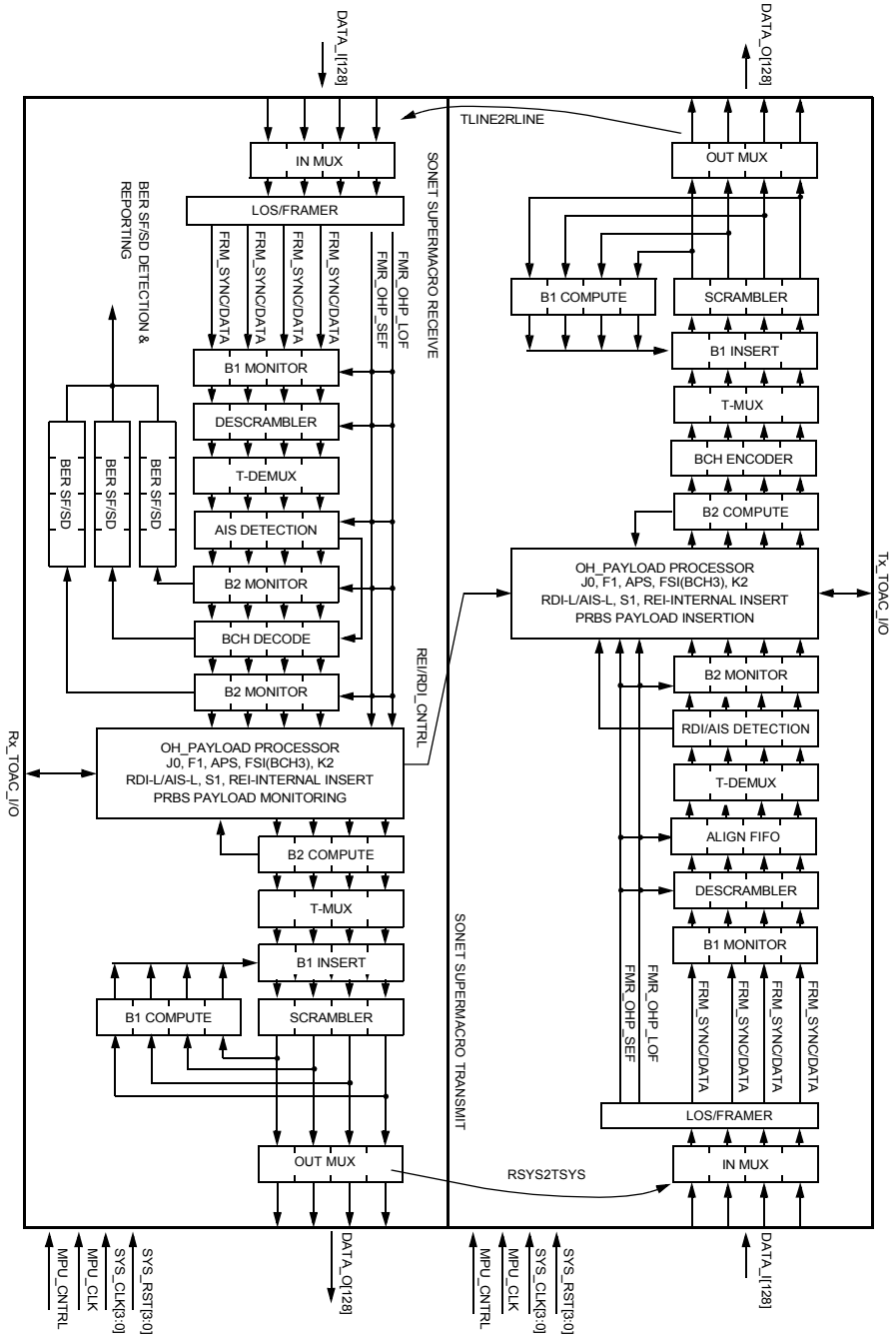


Figure 48. SONET Weak FEC Supermacro Functional Block Diagram

19 SONET FEC (BCH Weak/In Band) Supermacro (continued)

19.3 SONFEC AIS/RDI Generation

19.3.1 SONFEC (BCH Weak/In Band) Overview

In SONFEC, both transmit and receive overhead processors can generate AIS. If loss of clock or loss of signal is detected, AIS is generated and software cannot disable the AIS generation (no internal frame generation). Once the AIS condition is cleared, a subsequent one or two frames may be corrupt (BIPs).

19.3.2 Transmit AIS

The SONFEC supermacro generates AIS in the transmit direction under the following conditions:

- Loss of clock.
- Loss of signal.
- Severely errored frame (SEF) and SEF AIS generation is software enabled (TX_SEF_AIS_DIS).
- Loss of frame (LOF) and LOF AIS generation is software enabled (TX_LOF_AIS_DIS).
- Line—AIS frame is detected and line AIS generation upon detection is software enabled (TX_LINE_AIS_DIS).
- Line—AIS frame generation is software enabled (TX_LINE_AIS_INS).

Table 86. Transmit AIS Control Register Summary

Register Name	Register Bits	Function
OHP_TX_AIS_RDI	TX_SEF_AIS_DIS	AIS generation due to SEF condition disable. 0 = AIS generated under SEF. 1 = AIS generation under SEF disabled.
	TX_LOF_AIS_DIS	AIS generation due to LOF condition disable. 0 = AIS generated under LOF. 1 = AIS generation under LOF disabled.
	TX_LINE_AIS_DIS	AIS generation due to AIS detect disable. 0 = AIS generated under AIS. 1 = AIS generation under AIS disabled.
	TX_LINE_AIS_INS	AIS generation. 0 = AIS generated. 1 = AIS generation disabled.

19 SONET FEC (BCH Weak/In Band) Supermacro (continued)

19.3 SONFEC AIS/RDI Generation (continued)

19.3.3 Receive AIS

The SONFEC supermacro generates AIS in the receive direction under the following conditions:

- Loss of clock.
- Loss of signal.
- Severely errored frame (SEF) and SEF AIS generation is software enabled (RX_SEF_AIS_DIS).
- Loss of frame (LOF) and LOF AIS generation is software enabled (RX_LOF_AIS_DIS).
- Signal fail at post B2 monitoring and SF AIS generation is software enabled (RX_SF_AIS_DIS).
- Section trace—J0 mismatch and J0 mismatch AIS generation is software enabled (RX_TIM_L_AIS_DIS).
- Line—AIS frame is detected and line AIS generation upon detection is software enabled (RX_LINE_AIS_DIS).
- Line—AIS frame generation is software enabled (RX_LINE_AIS_INS).

Table 87. Receive AIS Control Register Summary

Register Name	Register Bits	Function
OHP_RX_AIS_RDI	RX_SEF_AIS_DIS	AIS generation due to SEF condition disable. 0 = AIS generation due to SEF enabled. 1 = AIS generation due to SEF disabled.
	RX_LOF_AIS_DIS	AIS generation due to LOF condition disable. 0 = AIS generation due to LOF enabled. 1 = AIS generation due to LOF disabled.
	RX_LINE_AIS_DIS	AIS generation due to AIS detection disable. 0 = AIS generation due to AIS detect enabled. 1 = AIS generation due to ASI detect disabled.
	RX_TIM_L_AIS_DIS	AIS generation due to J0 mismatch disable. 0 = AIS generation due to J0 mismatch enabled. 1 = AIS generation due to J0 mismatch disabled.
	RX_SF_AIS_DIS	AIS generation due to SF condition disable. 0 = AIS generation due to SF condition enabled. 1 = AIS generation due to SF condition disabled.
	RX_LINE_AIS_INS	AIS generation. 0 = AIS generation disabled. 1 = AIS generated.

19 SONET FEC (BCH Weak/In Band) Supermacro (continued)

19.3 SONFEC AIS/RDI Generation (continued)

19.3.4 Transmit RDI Generation

The SONFEC supermacro generates RDI in the transmit direction whenever there is a hardware AIS condition in the receive direction. Once the receive direction detects any one of the RDI generation events, K2 bytes in the transmit direction are modified under all conditions (except in the case of software bypass). If no hardware RDI generation events are present, then the lower 3 bits of the software programmed K2 byte are inserted if software insert is enabled. Once RDI is inserted, the duration can be software controlled for either 20 consecutive frames or the duration of the RDI event. Both RDI and AIS conditions are controlled by the same set of register bits. Optionally, software can be programmed to bypass the received K1/K2.

Table 88. Transmit RDI Insertion Control Register Summary

Register Name	Register Bits	Function
OHP_TX_AIS_RDI	TX_20FRM_RDI_DIS	RDI insertion disable. 0 = Enable RDI insertion on 20 frames. 1 = Disable RDI insertion on 20 frames.
OHP_TX_MAINT	TX_RDI_L_SELECT	RDI insertion from the programmed K2 byte enable. 0 = RDI insertion disabled. 1 = RDI insertion enabled.
OHP_TX_K1K2	TX_K2_BYTE[3:0]	If software enabled, then the last three bits of K2 are inserted in RDI.

19.4 SONFEC Interrupt Structure

The interrupt structure is comprised of different registers depending on the consolidation level. The structure depicts only that of the SONFEC macro. Individual interrupts sourced within the SONFEC supermacro cause the corresponding bits to be set in the interrupt service register (ALARM registers (W1C)).

If the corresponding interrupt mask register bit is set (MASK registers (R/W)), then these interrupts cause the submacro level interrupt bit to be set. These submacro level interrupts are grouped into two: overhead processor and BCH. When the mask bits corresponding to these submacro interrupts are set, they cause an interrupt to be sourced from the SONFEC supermacro. The interrupt summary is given the TFEC0410G Hardware Register Map document.

20 BCH Macro

20.1 Functional Description of BCH Macro

The BCH (Bose-Chaudhuri-Hocquenghem) macro performs in-band forward error correction (FEC). The code used for in-band FEC is a shortened, systematic binary BCH (4359, 4320) code derived from a (8191, 8162) parent code which belongs to the family of systematic linear cyclic block codes. The code block consists of 4320 information bits and 39 check bits. In order to enhance the immunity of the transmission system to the burst errors, eight code blocks are bit-interleaved.

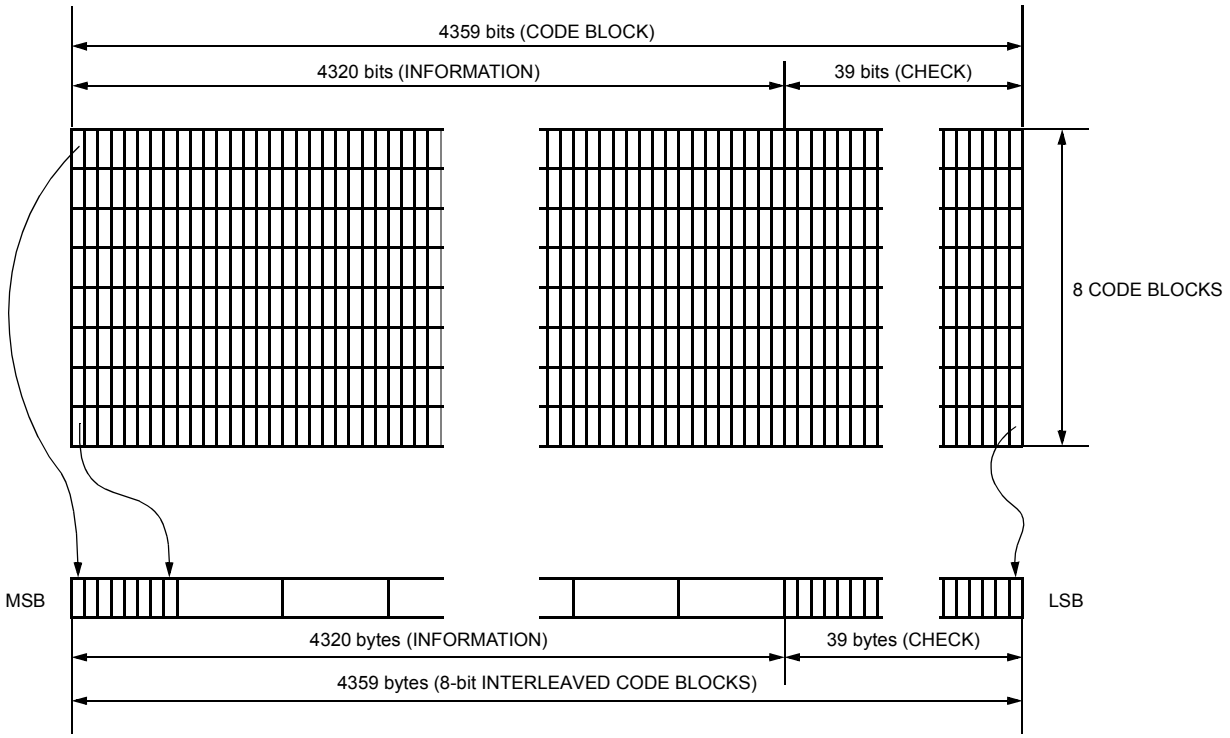


Figure 49. 8-Way Bit Interleaved BCH (4359, 4320) Frame

The 39 check bits are the remainder after polynomial division of the information polynomial by generating polynomial $G(x) = G1(x) \times G3(x) \times G5(x)$ where $G1(x) = x^{13} + x^4 + x^3 + x + 1$, $G3(x) = x^{13} + x^{10} + x^9 + x^7 + x^5 + x^4 + 1$, and $G5(x) = x^{13} + x^{11} + x^8 + x^7 + x^4 + x + 1$. Sufficient check bits are generated to support triple error correction. The 8-way bit interleaving in conjunction with BCH-3 provides 24-bit burst error correction capability per frame.

One row of an STM-16 (STS-48), which is 4320 bytes, forms the information of the BCH frame (i.e., the BCH macro encodes and decodes the STM-16 (STS-48) on a row-by-row basis). The code block definition for an STM-64 (STS-196) is identical to that for an STM-16 (STS-48). However, there are four block groups, i.e., 32 code blocks.

Conceptually, the FEC function falls below the multiplexing section (MS) layer and provides a correction service to the MS layer, and uses overhead bytes from the MSOH (multiplexing section overhead) and RSOH (regenerator section overhead) as shown in Figure 50 on page 119. Although check bytes are transported in information byte positions, they are not included in information. From this, all RSOH bytes (including undefined RSOH bytes) and all FEC check bytes are not included in the coding of the FEC and are replaced with zeros. Note that the Q1 bytes (FSI—FEC status indication bytes) are covered by the FEC, and are therefore included in the coding of the FEC.

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

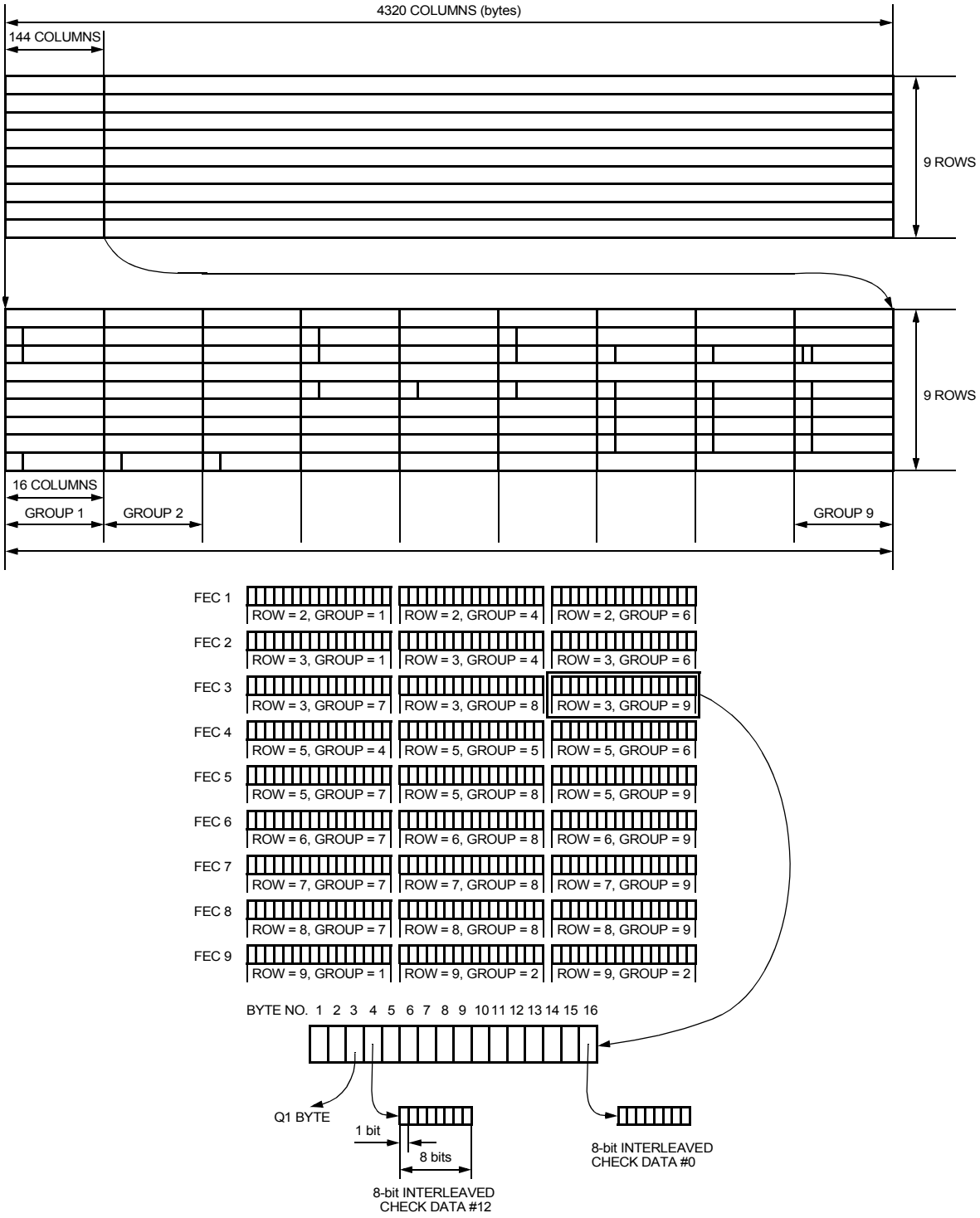


Figure 50. FEC Check Byte Allocation in STM-16 (STS-48)

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

In Figure 44 on page 91, each set of FEC bytes represents a set of FEC check bits. The number indicates the row of the payload to which each set of FEC check bytes pertains. The Q1 byte is an FEC status indicator (FSI). This is used at the FEC decoding point to determine whether FEC information is present for error correction to take place. Table 89 and Table 90 give the exact check byte locations for STM-16 and STM-64 signals.

Table 89. Location of FEC Check Bits for STM-64 (STS-192)

The numbers in the table represent row number, group number, and byte number, respectively.

FEC Row #[1]	Check Bits Set #1 (#38 ~ #26)	Check Bits Set #2 (#25 ~ #13)	Check Bits Set #3 (#12 ~ #0)	Q1 Byte
1	2, 1, 4 ~ 2, 1, 16	2, 4, 4 ~ 2, 4, 16	2, 6, 4 ~ 2, 6, 16	—
	2, 1, 20 ~ 2, 1, 32	2, 4, 20 ~ 2, 4, 32	2, 6, 20 ~ 2, 6, 32	
	2, 1, 36 ~ 2, 1, 48	2, 4, 36 ~ 2, 4, 48	2, 6, 36 ~ 2, 6, 48	
	2, 1, 52 ~ 2, 1, 64	2, 4, 52 ~ 2, 4, 64	2, 6, 52 ~ 2, 6, 64	
2	3, 1, 4 ~ 3, 1, 16	3, 4, 4 ~ 3, 4, 16	3, 6, 4 ~ 3, 6, 16	
	3, 1, 20 ~ 3, 1, 32	3, 4, 20 ~ 3, 4, 32	3, 6, 20 ~ 3, 6, 32	
	3, 1, 36 ~ 3, 1, 48	3, 4, 36 ~ 3, 4, 48	3, 6, 36 ~ 3, 6, 48	
	3, 1, 52 ~ 3, 1, 64	3, 4, 52 ~ 3, 4, 64	3, 6, 52 ~ 3, 6, 64	
3	3, 7, 4 ~ 3, 7, 16	3, 8, 4 ~ 3, 8, 16	3, 9, 4 ~ 3, 9, 16	3, 9, 3 (FSI)
	3, 7, 20 ~ 3, 7, 32	3, 8, 20 ~ 3, 8, 32	3, 9, 20 ~ 3, 9, 32	3, 9, 19 (00H)
	3, 7, 36 ~ 3, 7, 48	3, 8, 36 ~ 3, 8, 48	3, 9, 36 ~ 3, 9, 48	3, 9, 35 (00H)
	3, 7, 52 ~ 3, 7, 64	3, 8, 52 ~ 3, 8, 64	3, 9, 52 ~ 3, 9, 64	3, 9, 51 (00H)
4	5, 4, 4 ~ 5, 4, 16	5, 5, 4 ~ 5, 5, 16	5, 6, 4 ~ 5, 6, 16	—
	5, 4, 20 ~ 5, 4, 32	5, 5, 20 ~ 5, 5, 32	5, 6, 20 ~ 5, 6, 32	
	5, 4, 36 ~ 5, 4, 48	5, 5, 36 ~ 5, 5, 48	5, 6, 36 ~ 5, 6, 48	
	5, 4, 52 ~ 5, 4, 64	5, 5, 52 ~ 5, 5, 64	5, 6, 52 ~ 5, 6, 64	
5	5, 7, 4 ~ 5, 7, 16	5, 8, 4 ~ 5, 8, 16	5, 9, 4 ~ 5, 9, 16	
	5, 7, 20 ~ 5, 7, 32	5, 8, 20 ~ 5, 8, 32	5, 9, 20 ~ 5, 9, 32	
	5, 7, 36 ~ 5, 7, 48	5, 8, 36 ~ 5, 8, 48	5, 9, 36 ~ 5, 9, 48	
	5, 7, 52 ~ 5, 7, 64	5, 8, 52 ~ 5, 8, 64	5, 9, 52 ~ 5, 9, 64	
6	6, 7, 4 ~ 6, 7, 16	6, 8, 4 ~ 6, 8, 16	6, 9, 4 ~ 6, 9, 16	—
	6, 7, 20 ~ 6, 7, 32	6, 8, 20 ~ 6, 8, 32	6, 9, 20 ~ 6, 9, 32	
	6, 7, 36 ~ 6, 7, 48	6, 8, 36 ~ 6, 8, 48	6, 9, 36 ~ 6, 9, 48	
	6, 7, 52 ~ 6, 7, 64	6, 8, 52 ~ 6, 8, 64	6, 9, 52 ~ 6, 9, 64	
7	7, 7, 4 ~ 7, 7, 16	7, 8, 4 ~ 7, 8, 16	7, 9, 4 ~ 7, 9, 16	
	7, 7, 20 ~ 7, 7, 32	7, 8, 20 ~ 7, 8, 32	7, 9, 20 ~ 7, 9, 32	
	7, 7, 36 ~ 7, 7, 48	7, 8, 36 ~ 7, 8, 48	7, 9, 36 ~ 7, 9, 48	
	7, 7, 52 ~ 7, 7, 64	7, 8, 52 ~ 7, 8, 64	7, 9, 52 ~ 7, 9, 64	
8	8, 7, 4 ~ 8, 7, 16	8, 8, 4 ~ 8, 8, 16	8, 9, 4 ~ 8, 9, 16	
	8, 7, 20 ~ 8, 7, 32	8, 8, 20 ~ 8, 8, 32	8, 9, 20 ~ 8, 9, 32	
	8, 7, 36 ~ 8, 7, 48	8, 8, 36 ~ 8, 8, 48	8, 9, 36 ~ 8, 9, 48	
	8, 7, 52 ~ 8, 7, 64	8, 8, 52 ~ 8, 8, 64	8, 9, 52 ~ 8, 9, 64	
9	9, 1, 4 ~ 9, 1, 16	9, 2, 4 ~ 9, 2, 16	9, 3, 4 ~ 9, 3, 16	
	9, 1, 20 ~ 9, 1, 32	9, 2, 20 ~ 9, 2, 32	9, 3, 20 ~ 9, 3, 32	
	9, 1, 36 ~ 9, 1, 48	9, 2, 36 ~ 9, 2, 48	9, 3, 36 ~ 9, 3, 48	
	9, 1, 52 ~ 9, 1, 64	9, 2, 52 ~ 9, 2, 64	9, 3, 52 ~ 9, 3, 64	

1. See Figure 50, FEC Check Byte Allocation in STM-16 (STS-48), on page 119 for details on FEC rows.

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

Table 90. Location of FEC Check Bits for STM-16 (STS-48)

FEC Row #[1]	Check Bits Set #1 (#38 ~ #26)	Check Bits Set #2 (#25 ~ #13)	Check Bits Set #3 (#12 ~ #0)	Q1 Byte
1	2, 1, 4 ~ 2, 1, 16	2, 4, 4 ~ 2, 4, 16	2, 6, 4 ~ 2, 6, 16	—
2	3, 1, 4 ~ 3, 1, 16	3, 4, 4 ~ 3, 4, 16	3, 6, 4 ~ 3, 6, 16	
3	3, 7, 4 ~ 3, 7, 16	3, 8, 4 ~ 3, 8, 16	3, 9, 4 ~ 3, 9, 16	3, 9, 3
4	5, 4, 4 ~ 5, 4, 16	5, 5, 4 ~ 5, 5, 16	5, 6, 4 ~ 5, 6, 16	—
5	5, 7, 4 ~ 5, 7, 16	5, 8, 4 ~ 5, 8, 16	5, 9, 4 ~ 5, 9, 16	
6	6, 7, 4 ~ 6, 7, 16	6, 8, 4 ~ 6, 8, 16	6, 9, 4 ~ 6, 9, 16	
7	7, 7, 4 ~ 7, 7, 16	7, 8, 4 ~ 7, 8, 16	7, 9, 4 ~ 7, 9, 16	
8	8, 7, 4 ~ 8, 7, 16	8, 8, 4 ~ 8, 8, 16	8, 9, 4 ~ 8, 9, 16	
9	9, 1, 4 ~ 9, 1, 16	9, 2, 4 ~ 9, 2, 16	9, 3, 4 ~ 9, 3, 16	

1. See Figure 50, FEC Check Byte Allocation in STM-16 (STS-48), on page 119 for details on FEC rows.

20.1.1 BCH Encoder

The BCH encoder generates and inserts check bits of STM-16/STM-64 (STS-48/STS-192) signals. Data arrives to the BCH encoder grouped as four slices of 32 bits. Because the code block definition for an STM-64 (STS-192) is identical to that for an STM-16 (STS-48), and the transpose demultiplexer (TDMX) reorders the data so that the STM-64 (STS-192) is divided into its four constituent STS-48 data streams, each slice can operate independently even in STM-64 (STS-192) mode.

The only difference between STM-16 (STS-48) mode and STM-64 (STS-192) is Q1 byte insertion, which is explained in the next section (Section 20.1.1.1).

20.1.1.1 FSI Bit Insert

The FEC encoder is required to generate the FEC status indication (FSI) bits to enable downstream decoders. This is to prevent downstream decoders from causing miscorrection when FEC encoding is not present.

The Q1 byte is located in row 3, as shown in Figure 49 on page 118. The FSI carrying byte is located in the first Q1 byte, i.e., the Q1 byte of the first block group (which contains FSI and Q1 bytes in the remaining block groups) is unassigned and the transmitted default value is 00H in STM-64 (STS-192) mode.

The FSI bits are the bits (7 and 8) of the FSI byte, as shown in Figure 51. The remaining bits in the FSI byte are reserved, but are covered by the FEC. The transmitted default value for these remaining 6 bits is zero.

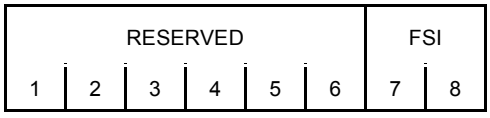


Figure 51. FEC Status Indication Byte (FSI)

The value of the FSI bits is encoded according to encoder states, and there are three operational encoder states: FEC-ON, FEC-OFF with encoder delay, and FEC-OFF without encoder delay. The encoder operational state is controlled by software.

When the encoder is in the FEC-ON state, FSI = 01 is transmitted. When the encoder is in the FEC-OFF with encoder delay state, all Q1 bytes are set to 0×00. When the encoder is in the FEC-OFF without encoder delay state, they are bypassed.

Note: 10 or 11 is not a valid encoder transmission value.

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

Table 91. BCH Macro Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH Encoder Status Control	BCH_PROV_S0 (R/W)	BCH_ENC_MODE	4	0×1144

Note: When configuring the BCH encoder in OC-192 mode, ensure that all slices are enabled. To ensure all slices are active before the FSI byte is generated, write 0×1147 last.

20.1.1.2 FEC Payload Generate

All RSOH bytes (including undefined RSOH bytes) of incoming STM-16 (STS-48) signals are not included in the encoding of the FEC and are replaced with zeros before the check bit calculation.

All Q1 bytes are included in the FEC block for correction before retransmission by correcting regenerators, and therefore are added to the incoming STM-16 (STS-48) signal for the encoding of the FEC.

20.1.1.3 Check Bit Generate

Data arrives to the BCH encoder grouped as four slices of 32 bits. The BCH encoder generates check bits in 8-way bit interleaving mode. Therefore, there are 4 bits of data which belong to the same code block at every clock cycle.

Each slice has eight independent check bit calculators. Each calculator accepts 4 bits of information data which belong to same code block during 1080 clock cycles (i.e., accepts 4320 information bits). After 1080 times polynomial division of the information data, each calculator outputs 39 bits check data, which is a remainder of the polynomial division.

Since the in-band FEC code blocks are designed to cover a single row of the STM-16 (STS-48), the starting of polynomial division is the same as starting each row of the STM-16 (STS-48).

20.1.1.4 Check Bit Insert

The check bits are inserted into designated locations as shown in Figure 44 on page 91. The check bit data is available after polynomial division of the associated information data, but FEC-3, FEC-5, FEC-6, FEC-7, FEC-8, and FEC-9 are located in the middle of the rows to which the check bit data pertains. For this reason, information data is delayed before check bit inserting.

As mentioned previously, there are three operational encoding states. The FEC insert works in synchronization with the encoding state. When the encoder operates in the FEC-OFF without encoder delay state, the information data is transmitted without delay.

In order to permit synchronized decoder switching at the receiver, the FEC insert is turned off (on) starting with the first row of the eighth frame after the FSI change.

For flexible operation, check bits are inserted either MSB first or LSB first. This is configured by software.

Table 92. BCH FEC Insert Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH FEC Insert Control	BCH_PROV_S0 (R/W)	BCH_ENC_INSERT	4	0×1144

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

20.1.1.5 B2 Compensate

Since the FEC function uses overhead bytes from the MSOH and consequently overwrites bytes currently covered by B2, the BCH encoder compensates B2 appropriately to reflect the change in the FEC MSOH bytes; the FEC check bits cover the B2 byte.

The FEC check bytes and FSI byte in the RSOH are not included in B2 compensation; only the FEC check bytes in the MSOH are included in B2 compensation. This ensures backward compatibility of B1 and B2 calculation for non-FEC equipment.

20.1.1.6 Error Insert

Various types of errors can be inserted for BCH code testing. The error insert inserts various types of errors for BCH code testing. For each slice, an error insert block accepts 32 bits of data. There are a total of 4 slices instantiated to create the 128-bit wide data for 16-way and 64-way 10 Gbits/s mode.

A 32-bit mask register corresponds to the 32-bit wide data bus for the error insertion. When the mask bit is set to logic 1, the corresponding data bit is inverted. The number of skipping clock cycles can be programmed through the microprocessor. Error bits combining with the number of skipping clock cycles can be repeated by using a control bit bus. The first column of error can be chosen via the microprocessor. The stream of errors start when there is a 0 $\Rightarrow$ 1 transition on the error control bit.

Note: To ensure all errors are inserted within the valid range, the following equation can be used:

$$(skip + 1) \times (repeat - 1) + row \times 1080 + column < 9 \times 1080$$

Table 93. BCH Error Insert Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Mask for Error Insertion on the 32-bit Data Bus	BCH_TXERR_MASKL_S0/ BCH_TXERR_MASKU_S0 (R/W)	BCH_TXERR_MASK_L/ BCH_TXERR_MASK_U	4	0×1148/ 0×114C
Number of Skipping Clock Cycles Between the 32-bit Error Patterns (valid range is 0—1023)	BCH_TXERR_SKIP_S0 (R/W)	BCH_TXERR_SKIP	4	0×1158
Number of Repeating Clock Cycles Between the 32-bit Error Patterns (valid range is 0 (no error)—255)	BCH_TXERR_REPEAT_S0 (R/W)	BCH_TXERR_REPEAT	4	0×1154
Start Row (valid range is 0—8)	BCH_TXERR_ROWCOL_S0 (R/W)	BCH_TXERR_ROW	4	0×1150
Start Column (valid range is 0—1079)	BCH_TXERR_ROWCOL_S0 (R/W)	BCH_TXERR_COL	4	0×1150
Error Start Control Bit	BCH_TXERR_START_S0 (R/W)	BCH_TXERR_START	4	0×1158
Error Insert Finish State	BCH_TX_STATE_S0 (RO)	BCH_TXERR_FINISH	4	0×10E4
Error Insert Finish Alarm	BCH_TX_ALARM_S0 (W1C)	BCH_TXERR_FINISH_A	4	0×1020
Error Insert Finish Mask	BCH_TX_MASK_S0 (R/W)	BCH_TXERR_FINISH_M	4	0×106C
Error Insert Finish Persist	BCH_TX_PERSIST_S0 (RO)	BCH_TXERR_FINISH_P	4	0×10B4

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

20.1.2 BCH Decoder

The BCH decoder detects and corrects transmission errors of STM-16/STM-64 (STS-48/STS-192) signals. Data arrives to the BCH decoder grouped as four slices of 32 bits. Because the code block definition for an STM-64 (STS-192) is identical to that of an STM-16 (STS-48), and the transpose demultiplexer (TDMX) reorders the data so that the STM-64 (STS-192) is divided into its four constituent STS-48 data streams, each slice can operate independently even in STM-64 (STS-192) mode.

One difference between STM-16 (STS-48) mode and STM-64 (STS-192) is Q1 byte interpretation, which will be explained in Section 20.1.2.3 on page 125.

When defects (LOC/LOS/OOF/LOF/MS-AIS) are found, the associated BCH decoder is disabled. The diagram of the BCH decoder, in each slice, is shown in Figure 48 on page 114.

20.1.2.1 FEC Frame Generate

All RSOH bytes (including undefined RSOH bytes) of incoming STM-16 (STS-48) signals are not included in the decoding of the FEC and are replaced with zeros before error detection. All Q1 bytes are corrected before retransmission by correcting regenerators, and therefore are included in the decoding of the FEC.

For flexible operation, check bits are extracted in either MSB first or LSB first. This is configured by software.

Table 94. BCH Frame Generate Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH FEC Extract Control	BCH_RXPROV_S0 (R/W)	BCH_DEC_EXTRACT	4	0×1140

20.1.2.2 Error Detect

Each slice has eight independent error detect blocks and each detect block consists of three subblocks: syndrome calculate, BMA (Berlekamp-Massey algorithm), and chien (time-domain error location) search.

Uncorrectable errors are detected and reported to the BCH stat as well as corrected bits, per slice.

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

20.1.2.3 FSI Bit Interpret

In hardware mode, the FEC decoder is required to interpret the FEC status indication (FSI) bits to enable correcting function. This is to prevent miscorrection when FEC encoding is not present.

The Q1 byte locations and FSI bits information are the same as those of the encoder. When the BCH decoder operates in STM-64 (STS-192) mode, the FSI carrying byte is located in the first Q1 byte, and therefore, decoding states of the slices which have the second, third, and fourth Q1 bytes follow that of the master slice, which has the first Q1 byte.

The decoding state transition according to the received FSI is as follows. The decoding state can be changed from FEC-ON to FEC-OFF with encoder delay upon receipt of third consecutive NON-01, and from FEC-OFF with encoder delay to FEC-ON upon receipt of the ninth consecutive FSI value 01.

Table 95. BCH FSI Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH Correction Status	BCH_RX_STATE_S0 (RO)	BCH_DEC_FSI	4	0×10E0
BCH Correction Status Interrupt Alarm	BCH_RX_ALARM_S0 (W1C)	BCH_DEC_FSI_A	4	0×101C
BCH Correction Status Interrupt Mask	BCH_RX_MASK_S0 (R/W)	BCH_DEC_FSI_M	4	0×1068
BCH Correction Status Persistency	BCH_RX_PERSIST_S0 (RO)	BCH_DEC_FSI_P	4	0×10B0

20.1.2.4 Error Correct

The received data is delayed before being corrected, while transmission errors are detected. There are two ways of controlling decoding states. The first is by hardware (FSI controlled) and the second is by software.

When the BCH decoder is set to hardware mode, the correcting function will follow the FSI as mentioned above. The state transition between FEC-ON and FEC-OFF is hitless.

- In software mode, there are the four following decoding states. Two are the same as hardware mode, and monitoring and shutdown modes are added:
  - FEC-ON.
  - FEC-OFF with decoder delay.
  - Monitoring (error detect and count but not correct without decoder delay).
  - Shutdown (no error detect nor correct).

In monitoring and shut-down modes, the received data is transmitted downstream without delay.

Table 96. BCH Decoding Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH Decoding Mode Select	BCH_RXPROV_S0 (R/W)	BCH_DEC_MODE	4	0×1140

20.1.3 BCH Statistics (BCH-Stat)

The BCH-stat counts correctable errors that are detected and corrected in the BCH decoder. The monitoring of the line BER before correction can be done through the knowledge of the exact number of corrected bits. The errors that remain uncorrected after forward error correction can be considered negligible in the computation of BER for low error rates.

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

20.1.3.1 Error Count

The corrected bits and the uncorrectable blocks are accumulated per slice in 16-bit saturating counters based on either bit or block errors. In bit mode, each corrected error (or uncorrectable block) causes the counter to increment. If block error is selected, each BCH frame which has a corrected error (or uncorrectable block) causes the counter to increment by one. The counter will stop at the maximum value, will not roll over, and is cleared by the PMRST signal.

Table 97. BCH Error Count Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH Error Count Control	BCH_ERR_PROV_S0 (R/W)	BCH_ERR_BITBLK	4	0×115C
BCH Rx Corrected Bit Counter	BCH_ERR_BITCNT_L_S0/ BCH_ERR_BITCNT_U_S0 (RO)	BCH_ERR_BITCNT_L/ BCH_ERR_BITCNT_U	4	0×1165/ 0×1164
BCH Rx Uncorrectable Block Counter	BCH_ERR_BLKCNT_L_S0/ BCH_ERR_BLKCNT_U_S0 (RO)	BCH_UNC_BLKCNT_L/ BCH_UNC_BLKCNT_U	4	0×116E/ 0×116D

20.1.3.2 BER Monitor

The corrected errors are used to detect SF and SD conditions. The BER threshold for each defect is separately provisionable for each slice over a range of 1×10^{-N} values, where N = 3 to 9.

The BER algorithm is the same as that of the RS decoder (refer to Section 16.1.2, BER Monitor, on page 89 for a detailed description).

Table 98. BER Threshold Time and Error Limits for Line SD and SF Detection

BER Threshold	Detection Time		Detect Error Limit		Clear Error Limit	
	STS-48/ STM-16	STS-192/ STM-64	STS-48/ STM-16	STS-192/ STM-64	STS-48/ STM-16	STS-192/ STM-64
1×10^{-3}	1.0 ms	0.25 ms	992	992	—	—
1×10^{-4}	1.0 ms	0.25 ms	248	248	496	496
1×10^{-5}	4.0 ms	1.0 ms	99	99	495	495
1×10^{-6}	32.0 ms	8.0 ms	79	79	395	395
1×10^{-7}	128.0 ms	32.0 ms	63	63	315	315
1×10^{-8}	1 s	250 ms	50	50	250	250
1×10^{-9}	8.2 s	2.1 s	40	40	200	200
1×10^{-10}	65.6 s	16.4 s	—	—	160	160

The SD/SF BER control bits select the bit error rate for a particular slice. These control bits then select the detection time, detect error limit, and clear error limit for each slice. The detect error limit and the clear error limit registers contain 16-bit values, while the detection time registers use the lower 15 bits for a value and the upper bit for a time unit specifier. For the detection time register, the value contained in the lower 15 bits is either specified in 0.125 ms units (upper bit = 0) or in 0.128 s units (upper bit = 1).

Note: The receive sync pulse is used as the timing reference.

20 BCH Macro (continued)

20.1 Functional Description of BCH Macro (continued)

Table 99. BCH BER Monitor Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
BCH SD Threshold Select	BCH_ERR_PROV_S0 (R/W)	BCH_RX_BER_SD	4	0×115C
BCH SF Threshold Select	BCH_ERR_PROV_S0 (R/W)	BCH_RX_BER_SF	4	0×115C
BCH SD Detect	BCH_STATE_S0 (RO)	BCH_RX_BER_SD_DET	4	0×10E0
BCH SF Detect	BCH_STATE_S0 (RO)	BCH_RX_BER_SF_DET	4	0×10E0
BCH SD Detect Alarm	BCH_ALARM_S0 (W1C)	BCH_RX_BER_SD_DET_A	4	0×101C
BCH SF Detect Alarm	BCH_ALARM_S0 (W1C)	BCH_RX_BER_SF_DET_A	4	0×101C
BCH SD Detect Mask	BCH_MASK_S0 (R/W)	BCH_RX_BER_SD_DET_M	4	0×1168
BCH SF Detect Mask	BCH_MASK_S0 (R/W)	BCH_RX_BER_SF_DET_M	4	0×1168
BCH SD Detect Persistency	BCH_PERSIST_S0 (RO)	BCH_RX_BER_SD_DET_P	4	0×10B0
BCH SF Detect Persistency	BCH_PERSIST_S0 (RO)	BCH_RX_BER_SF_DET_P	4	0×10B0
BCH BER Report	BCH_ERR_RPT_S0 (RO)	BCH_BER_REPORT	4	0×1160
BCH BER-3 Detection Time	BCH_BERDT3 (R/W)	BCH_BER_DT_UNIT_3/ BCH_BER_DT_VAL_3	1	0×1190
BCH BER-4 Detection Time	BCH_BERDT4 (R/W)	BCH_BER_DT_UNIT_4/ BCH_BER_DT_VAL_4	1	0×1191
BCH BER-5 Detection Time	BCH_BERDT5 (R/W)	BCH_BER_DT_UNIT_5/ BCH_BER_DT_VAL_5	1	0×1192
BCH BER-6 Detection Time	BCH_BERDT6 (R/W)	BCH_BER_DT_UNIT_6/ BCH_BER_DT_VAL_6	1	0×1193
BCH BER-7 Detection Time	BCH_BERDT7 (R/W)	BCH_BER_DT_UNIT_7/ BCH_BER_DT_VAL_7	1	0×1194
BCH BER-8 Detection Time	BCH_BERDT8 (R/W)	BCH_BER_DT_UNIT_8/ BCH_BER_DT_VAL_8	1	0×1195
BCH BER-9 Detection Time	BCH_BERDT9 (R/W)	BCH_BER_DT_UNIT_9/ BCH_BER_DT_VAL_9	1	0×1196
BCH BER-10 Detection Time	BCH_BERDT10 (R/W)	BCH_BER_DT_UNIT_10/ BCH_BER_DT_VAL_10	1	0×1197
BCH BER-3 Detect Error Limit	BCH_BERSET3 (R/W)	BCH_BER_SET_LIMIT_3	1	0×11C0
BCH BER-4 Detect Error Limit	BCH_BERSET4 (R/W)	BCH_BER_SET_LIMIT_4	1	0×11C1
BCH BER-5 Detect Error Limit	BCH_BERSET5 (R/W)	BCH_BER_SET_LIMIT_5	1	0×11C2
BCH BER-6 Detect Error Limit	BCH_BERSET6 (R/W)	BCH_BER_SET_LIMIT_6	1	0×11C3
BCH BER-7 Detect Error Limit	BCH_BERSET7 (R/W)	BCH_BER_SET_LIMIT_7	1	0×11C4
BCH BER-8 Detect Error Limit	BCH_BERSET8 (R/W)	BCH_BER_SET_LIMIT_8	1	0×11C5
BCH BER-9 Detect Error Limit	BCH_BERSET9 (R/W)	BCH_BER_SET_LIMIT_9	1	0×11C6
BCH BER-4 Clear Error Limit	BCH_BERCLR4 (R/W)	BCH_BER_CLR_LIMIT_4	1	0×11F0
BCH BER-5 Clear Error Limit	BCH_BERCLR5 (R/W)	BCH_BER_CLR_LIMIT_5	1	0×11F1
BCH BER-6 Clear Error Limit	BCH_BERCLR6 (R/W)	BCH_BER_CLR_LIMIT_6	1	0×11F2
BCH BER-7 Clear Error Limit	BCH_BERCLR7 (R/W)	BCH_BER_CLR_LIMIT_7	1	0×11F3
BCH BER-8 Clear Error Limit	BCH_BERCLR8 (R/W)	BCH_BER_CLR_LIMIT_8	1	0×11F4
BCH BER-9 Clear Error Limit	BCH_BERCLR9 (R/W)	BCH_BER_CLR_LIMIT_9	1	0×11F5
BCH BER-10 Clear Error Limit	BCH_BERCLR10 (R/W)	BCH_BER_CLR_LIMIT_10	1	0×11F6

21 SONFEC Input MUX and Output MUX

21.1 Functional Description of SONEC Input MUX and Output MUX

The SONFEC input MUX and output MUX transfer data across the slices depending upon their mode of operation. In 2.5 Gbits/s mode, they bypass the data received. In 10 Gbits/s mode, they transfer data across slices to/from four aggregate 32 bits of data on each of the slice clocks. The input MUX also performs the loopback functionality in SONFEC.

22 Loss-of-Signal (LOS) Detector and Framer

22.1 Functional Description of LOS Detector and Framer

The LOS detector monitors the data for loss of signal. The framer macro generates the frame sync and loss-of-frame outputs. These functions can be optionally disabled, allowing data to pass through unchanged. The framer also generates an 8 kHz reference output.

22.1.1 Loss-of-Signal (LOS) Detector

The data is monitored by the LOS detector macro for loss of signal (LOS). In STS-192 mode, there is a single LOS detector. In STS-48 mode, there is a separate LOS detector on each STS-48 input. On powerup, an LOS defect is declared if all zeros data is received continuously for a programmable time threshold. This time threshold is provisional through the loss-of-signal (LOS) threshold register for each channel, and can be set to any value from 0 μs (i.e., LOS detection disabled) to 105 μs, with a resolution of 102.88 ns (64 times the period of the 622.08 MHz clock).

The LOS defect is subsequently cleared when two successive valid framing patterns are received with no period of all zeros exceeding the time threshold. Detection of an LOS defect is indicated by a latched alarm status bit, a persistency bit, and a 1 s PM bit being set in the corresponding LTE receive channel registers. In addition, LOS causes alarm indication signal (AIS) generation by the overhead processor block in all STS-48 or STS-192 affected.

Both the transmit and receive LOS detectors are identical.

22.1.2 Framer (A1 and A2)

In STS-192 mode, framing is performed on a single channel. In STS-48 mode, framing is performed on four independent channels. The framer also supports enhanced framing, where every other A1 byte and A2 byte is inverted to better maintain dc balance on the optical line.

A1$\overline{A1}$A1$\overline{A1}$ . . . A1$\overline{A1}$ = F609F609 . . . F609.
A2$\overline{A2}$A2$\overline{A2}$ . . . A2$\overline{A2}$ = 28D728D7 . . . 28D7.

The STS framing bytes are present in all STS-1 time slots of the STS-48 or STS-192. When normal framing is selected, the A1 bytes are set to 0xF6, while the A2 bytes are set to 0x28. If enhanced framing is selected, using the framing mode control bit, the A1 and A2 bytes contain normal framing in odd STS-1 time slots and the inverse value in even STS-1 time slots. The framer outputs frame-aligned data and the 8 kHz reference (free-running) signal.

The STS-192 framer is described in the following sections. The STS-48 framer is similar.

22 Loss-of-Signal (LOS) Detector and Framer (continued)

22.1 Functional Description of LOS Detector and Framer (continued)

22.1.2.1 Framer FSM

The framer finite state machine (FSM) is responsible for determining the severely errored framing (SEF) and loss-of-framing (LOF) SONET framing alarms for each channel. The framer FSM is shown in Figure 52.

The FSM comes out of reset in the SEF state with the SEF and LOF alarms active. The framing pattern used is the 16-bit word consisting of the last A1 byte and the first A2 byte. The first occurrence of the framing pattern transfers the FSM to the frame confirm state. Frame timing is also synchronized. Another framing pattern that matches coincident with the expected frame timing transfers the state to in-frame (i.e., it takes two consecutive valid framing patterns to frame to an incoming signal). Outside the SEF and frame confirm states, the SEF alarm output is inactive. As shown in the FSM, when in-frame, four consecutive framing errors are required to be transferred back to the SEF state.

The LOF alarm is asserted if SEF persists for 24 frames (3 ms). The LOF alarm is terminated eight frames (1 ms) after the SEF alarm is terminated (i.e., eight frames after the FSM enters the in-frame state), provided the SEF state is not reentered (as per SONET objectives).

The framing pattern is a subset of the A1A2 STS-N pattern. This design uses the 16-bit A1A2 boundary as the framing pattern which evaluates to an average SEF defect occurrence time of 31.79 min., assuming a Poisson bit error rate (BER) of 10^{-3}. This is greater than the minimum average SONET requirement of 6 min.

The SEF alarm is reported by a latched register bit in the LTE receive nonservice-affecting alarm register for the respective channel. The LOF alarm is reported by a latched register bit in the LTE receive service-affecting alarm register for the respective channel. In addition, a persistency bit for LOF exists in the LTE receive service-affecting persistency register. Detection of LOF and SEF defects are also indicated by the LTE receive last-second PM register.

Detected LOF defect detection causes AIS to be inserted in all affected STS-48 or STS-192. This AIS insertion is disabled by default after reset and can be enabled using the LOF AIS disable control register bit for each channel, or replaced by insertion upon SEF detection using the SEF AIS disable control bit. Another control bit is the enhanced framing mode bit. These control bits are part of the LTE provisioning register for the respective channel.

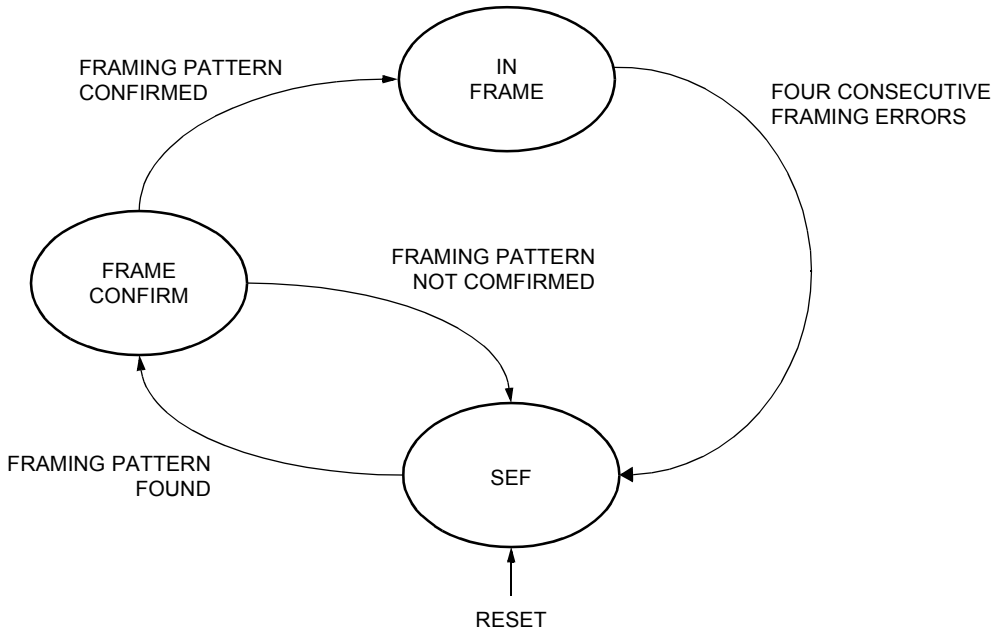


Figure 52. Framer FSM

22 Loss-of-Signal (LOS) Detector and Framer (continued)

22.1 Functional Description of LOS Detector and Framer (continued)

Table 100. Framer Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Framer Disable Control	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_FRM_DIS	4	0×1115
Framer Mode Control	SONFEC_RX_MODE (R/W)	RX_FRM_MODE	1	0×1110
Enhanced Framing Enable	OHP_RX_PROV_S0 (R/W)	RX_ENH_FRMG_ENB	4	0×1310
AIS Insertion on SEF	OHP_RX_PROV_S0 (R/W)	RX_SEF_AIS_DIS	4	0×1314
AIS Insertion on LOF	OHP_RX_PROV_S0 (R/W)	RX_LOF_AIS_DIS	4	0×1314
LOF State	OHP_RX_SA_STATE_S0 (RO)	RX_LOF	4	0×10E8
SEF State	OHP_RX_NSA_0_STATE_S0 (RO)	RX_SEF	4	0×10EC
LOF Alarm	OHP_RX_SA_ALARM_S0 (W1C)	RX_LOF_A	4	0×1024
SEF Alarm	OHP_RX_NSA_0_ALARM_S0 (W1C)	RX_SEF_A	4	0×102C
LOF Alarm Mask	OHP_RX_SA_MASK_S0 (R/W)	RX_LOF_M	4	0×1070
SEF Alarm Mask	OHP_RX_NSA_0_MASK_S0 (R/W)	RX_SEF_M	4	0×1078
LOF Persistency	OHP_RX_SA_PERSIST_S0 (RO)	RX_LOF_P	4	0×10B8
SEF Persistency	OHP_RX_NSA_0_PERSIST_S0 (RO)	RX_SEF_P	4	0×10BC
LOF PM	OHP_RX_PM_S0 (RO)	RX_LOF_PM	4	0×132C
SEF PM	OHP_RX_PM_S0 (RO)	RX_SEF_PM	4	0×132C

Table 101. LOS Detector Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
LOS Detection Mode Control	SONFEC_RX_MODE (R/W)	RX_LOS_MODE	1	0×1110
LOS Detect Time Threshold	OHP_RX_LOS_S0 (R/W)	RX_LOS_THRESHOLD	4	0×1324
LOS State	OHP_RX_SA_STATE_S0 (RO)	RX_LOS	4	0×10E8
LOS Alarm	OHP_RX_SA_ALARM_S0 (W1C)	RX_LOS_A	4	0×1024
LOS Alarm Mask	OHP_RX_SA_MASK_S0 (R/W)	RX_LOS_M	4	0×1070
LOS Persistency	OHP_RX_SA_PERSIST_S0 (RO)	RX_LOS_P	4	0×10B8
LOS PM	OHP_RX_PM_S0 (RO)	RX_LOS_PM	4	0×132C

23 Transmit Alignment FIFO

23.1 Functional Description of Transmit Alignment FIFO

The alignment FIFO block will align four independent 2.5 Gbits/s data channels into one 10 Gbits/s data channel.

Elastic buffers (FIFOs) are used to align each incoming 2.5 Gbits/s stream (slice 1, slice 2, and slice 3) to the master 77.76 MHz clock (slice 0). These FIFOs will absorb delay variations of up to 1000 ns between the first and the last incoming 2.5 Gbits/s streams, given that the four streams are byte-synchronous (on the byte boundary).

Each input 2.5 Gbits/s data channel may be inhibited from contributing to the overall alignment by setting the corresponding inhibit bit (ALGN_INH) high. When one particular channel is inhibited from being aligned with the rest, the frame pulse for that channel is aligned with the aligned frame pulses of the rest of the channels and the data is brought out as all ones.

The FIFO depths can be monitored to give an indication of the individual operating depths (write address—read address). In addition, an overflow bit, when set using FIFO_MIN and FIFO_MAX values, will indicate the FIFO fullness or emptiness for each channel.

The global resync signal will align all the channels when there is a 0 to 1 transition on the GLBL_RESYNC input. There is an alarm bit which will indicate if the alignment is not correct for a particular channel. If the alarm bit for a particular channel is high (indicating that the channel did not get aligned), the frame pulse for that channel is aligned with the pseudoframe pulse and the data is all ones. The pseudoframe pulse is the output of a free-running counter when there is no alignment performed. After alignment, the pseudoframe pulse occurs at the same position as the frame pulses from aligned channels.

Note: The global resync signal must be asserted if the original delay **increases** between the streams.

The BYPASS input signal will cause the alignment to be bypassed and the data streams will be brought out as if it came in on time. (The input bits MPU_SONFEC_TX_10G_2G5, V10G_MODE_N, and BYPASS should all be set to zeros in order for the alignment to take place. This block also supports short-frame mode.)

To use the alignment FIFO on Tx side, all four groups of four bits (16 bits total) must be frequency and phase aligned on arrival. Internally, only the slice 0 clock is used (this is related to virtual 10 Gbits/s mode). In this instance, it is important to understand that the alignment FIFO in the SONFEC block is used to frame align the four streams.

The FIFO alarm bit indicates if a stream is not correctly aligned with the other frames. A global resync is needed for alignment if the original delay increases between the inputs. While the delay between the inputs is less than the original delay, the device absorbs the delay variation automatically and no global resync is needed.

24 B1 Monitoring

24.1 Functional Description of B1 Monitoring

The section BIP-8 byte is located in the first STS-1 of the STS-48 or STS-192 only, and carries the even parity of the scrambled data in the previous STS-48 or STS-192 frame. In every frame, the received B1 value is extracted and compared to the calculated BIP-8 for the previous frame. Errors in the BIP-8 code are tabulated in an internal 16-bit counter based on either bit or block errors, as provisioned for each channel through the B1 BIP mode control bit.

In bit mode (selected by default), each BIP-8 bit in error causes the counter to increment. If block error is selected, each BIP-8 code in error causes the counter to increment only once. Regardless of which mode is selected, the value in the counter is transferred to the section coding violation (CV-S) register on the rising edge of the performance monitoring clock, at which point the counter is cleared. The counter will stop at the maximum value and will not roll over.

Table 102. B1 Monitoring Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
B1 Monitoring Disable	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_B1MON_DIS	4	0×1115
B1 Monitoring Mode	SONFEC_RX_MODE (R/W)	RX_B1MON_MODE	1	0×1110
Bit/Block Error Control	OHP_RX_PROV_S0 (R/W)	RX_B1BIP_MODE	4	0×1310
Last Second Coding Violations Count	OHP_RX_CVS_PM_S0 (RO)	RX_CVS	4	0×1353

25 Descrambler

25.1 Functional Description of the Descrambler

The data from the framer is optionally descrambled using the SONET/SDH standard generator polynomial: $1 + x^6 + x^7$. The descrambling can be disabled through the DESCRM_DIS bit in the LTE receive channel provisioning register for each channel.

Table 103. Descrambler Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Descrambling Control	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_DESCR_DIS	4	0×1115
Descrambling Mode	SONFEC_RX_MODE (R/W)	RX_DESCR_MODE	1	0×1110

26 Transpose Demultiplexer

26.1 Functional Description of the Transpose Demultiplexer (TDMX)

The TDMX macro receives the STS-192 stream in 16-byte blocks. Each set of 16 bytes belongs to one of the four possible STS-48 output channels. The macro then outputs bytes for each of the STS-48 channels every clock period.

For STS-192 data, the input stream must be demultiplexed to create four STS-48 data streams for further processing. The transpose demultiplexer reorders the data so that the STS-192 is divided into its four constituent STS-48 data streams.

The byte ordering of the individual STS-1s, or STS-1 components of an STS-Nc that comprise the STS-192 as it enters the TDMX and after the TDMX (STS-48 byte ordering), and the details of the STS-192 to STS-48 demultiplexing, can be found in *GR-253-CORE* Section 5-1, *Network Element Architectural Features (Multiplexing Procedure*) page 5-1. If the device is in STS-48 mode, the data is received on all four channels and the TDMX should be bypassed.

Table 104. Transpose Demultiplexer Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Transpose Demultiplexer Disable Control	SONFEC_RX_TP_BYPASS (R/W)	RX_TDMX_DIS	1	0×1112

27 RDI/AIS Detection

27.1 Functional Description of RDI/AIS Detection

The RDI/AIS detector in the receive direction detects AIS frames prior to BCH decoding. If AIS is detected, then BCH decoding is disabled. In the transmit direction, it detects AIS before overhead processing and, if detected, disables BCH encoding. RDI in the receive direction is done during overhead processing.

Table 105. RDI/AIS Detector Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
AIS Detection Disable Control	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_AISD_DIS	4	0×1115
AIS Detection Mode Control	SONFEC_RX_MODE (R/W)	RX_AISD_MODE	1	0×1110
AIS State	OHP_RX_SA_STATE_S0 (RO)	RX_AIS_L	4	0×10E8
AIS Alarm	OHP_RX_SA_ALARM_S0 (W1C)	RX_AIS_L_A	4	0×1024
AIS Alarm Mask	OHP_RX_SA_MASK_S0 (R/W)	RX_AIS_L_M	4	0×1070
AIS Persistency	OHP_RX_SA_PERSIST_S0 (RO)	RX_AIS_L_P	4	0×10B8
AIS PM	OHP_RX_PM_S0 (RO)	RX_LINE_AIS_PM	4	0×132C
RDI State (Tx Only)	OHP_TX_NSA_STATE_S0 (RO)	TX_LINE_RDI	4	0×10F4
RDI Alarm (Tx Only)	OHP_TX_NSA_ALARM_S0 (W1C)	TX_LINE_RDI_A	4	0×1034
RDI Alarm Mask (Tx Only)	OHP_TX_NSA_MASK_S0 (R/W)	TX_LINE_RDI_M	4	0×1080
RDI Persistency (Tx Only)	OHP_TX_NSA_PERSIST_S0 (RO)	TX_LINE_RDI_P	4	0×10C4
RDI PM (Tx Only)	OHP_TX_PM_S0 (RO)	TX_LINE_RDI_PM	4	0×1394

Note: In 10 Gbits/s mode, the master slice (that processes the STS-48 #1 in a STS-192) is slice 3. Therefore, though all the rest of the 10 Gbits/s alarms are reported in slice 0, in the RDI/AIS detector, the alarms in 10 Gbits/s are reported at slice 3 registers. Following the same reason, regardless of 10 Gbits/s or 2.5 Gbits/s mode of operation, all the slices are to be programmed.

28 B2 Monitoring

28.1 Functional Description of B2 Monitoring

The line BIP-8 is located in each STS-1 of the STS-48, or STS-192, and carries the even parity for the line overhead and SPE data within the previous STS-1 frame. The N-line BIP-8 bytes in an STS-N are intended to provide a single error monitoring facility for the entire STS-N signal. Thus, each B2 monitor block is used to check the 48 line BIP-8 codes, whether in STS-48 or STS-192 mode. Each BIP-8 bit found to be in error causes an internal 22-bit counter to increment.

The value in the counter is transferred to the line coding violation (CV-L) registers on the positive edge of the performance monitoring clock, at which point the counter is cleared. The counter will stop at the maximum value and will not roll over. When in STS-192 mode, a read of the STS-48 slice 0 CV-L registers returns the 24-bit sum of the four constituent STS-48 channel CV-L counts. Therefore, though the registers are 24-bit, in 2.5 Gbits/s mode, only the lower 22 bits are valid. In 10 Gbits/s mode, only slice 0's 24 bits are valid, though the maximum count is 0×FFFFFC.

During AIS insertion due to LOS, LOF, SEF, or line AIS, processing of the B2 byte is inhibited. It takes five frames of line AIS before the actual line AIS alarm is declared. Once AIS insertion is removed, processing of the B2 byte is delayed for two frames.

A single B2 controller block collects all the B2 errors and sums up to a single register for 10 Gbits/s mode of operation. Both transmit and receive B2 monitors are identical. In the receive direction, two B2 monitors are implemented before and after BCH decoding. These two B2 monitors can be used to compute the coding gain of the decoder.

Table 106. B2 Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
B2 Monitoring Disable (Rx Only)	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_PRE_B2MON_DIS	4	0×1115
B2 Monitoring Mode (Rx Only)	SONFEC_RX_MODE (R/W)	RX_PRE_B2MON_MODE	1	0×1110
Coding Violations Count (Rx Only)	OHP_RX_PRE_CVL_L_PM_S0/ OHP_RX_PRE_CVL_U_PM_S0 (RO)	RX_PRE_CVL_L/ RX_PRE_CVL_U	4	0×134B/ 0×134A
B2 Monitoring Disable (Rx Only)	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_POST_B2MON_DIS	4	0×1115
B2 Monitoring Mode (Rx Only)	SONFEC_RX_MODE (R/W)	RX_POST_B2MON_MODE	1	0×1110
Coding Violations Count (Rx Only)	OHP_RX_POST_CVL_L_PM_S0/ OHP_RX_POST_CVL_U_PM_S0 (RO)	RX_POST_CVL_L/ RX_POST_CVL_U	4	0×1342/ 0×1341
B2 Monitoring Disable (Tx Only)	SONFEC_TX_BYPASS_S0 (R/W)	OHP_TX_B2MON_DIS	4	0×1119
B2 Monitoring Mode (Tx Only)	SONFEC_TX_MODE (R/W)	TX_B2MON_MODE	1	0×1111
Coding Violations Count (Tx Only)	OHP_TX_CVL_L_PM_S0/ OHP_TX_CVL_L_PM_S0 (RO)	TX_CVL_L/ TX_CVL_U	4	0×139D/ 0×139C

29 BER—SD/SF Detection

29.1 Functional Description of BER—SD/SF Detection

The line/section BIP-8 errors can also be tracked in 16-bit signal fail (SF) and signal degrade (SD) counters. These counters are used to detect SF (signal fail) and SD (signal degrade) conditions for protection switching. The BER threshold for each defect is separately provisionable for each channel over a range of 1×10^{-N} values, where N = 3 to 5 for SF and N = 5 to 9 for SD. The detection times and error limits used to detect and clear both defects are dependent on the provisioned BER threshold, as shown in Table 107. The STS-192 values shown in the table are the powerup defaults. These values can be changed through the corresponding registers and are common to all channels.

The clearing BER threshold for each defect is always 1/10th of the detection threshold. As can be seen in Table 107, the range of possible detect thresholds is 1×10^{-3} to 1×10^{-9}, which results in clear thresholds of 1×10^{-4} to 1×10^{-10}. For example, to detect SD at 1×10^{-5} BER in an STS-192, the detection time is 4 ms and the detect error limit is 358. The clearing would take place at 1×10^{-6} BER, with a clearing time of 6.5 ms and a clearing error limit of 77. Figure 53 on page 137 illustrates SD detection and clearing using the default STS-192 values specified in Table 107. SD thresholds of 1×10^{-10} to 1×10^{-15} are supported through software.

Table 107. BER Threshold Time and Error Limits for Line SD and SF Detection

BER Threshold	Detection Time		Detect Error Limit		Clear Error Limit	
	STS-48	STS-192	STS-48	STS-192	STS-48	STS-192
1×10^{-3}	4 ms	4 ms	4818	19453	—	—
1×10^{-4}	4 ms	4 ms	862	3543	957	3734
1×10^{-5}	4 ms	4 ms	81	358	114	423
1×10^{-6}	31 ms	6.5 ms	62	51	91	77
1×10^{-7}	312.5 ms	65 ms	62	51	91	77
1×10^{-8}	2600 ms	650 ms	51	51	77	77
1×10^{-9}	21 s	5250 ms	40	40	63	63
1×10^{-10}	170 s	41 s	—	—	52	51

In STS-192 mode, the thresholds are compared against the sum of the four STS-48 channel SF and SD counts. A detected SF or SD defect causes a corresponding maskable interrupt status bit to be set in the LTE receive slice N service-affecting alarm register.

The SD/SF BER control bits in the LTE receive channel N maintenance register select the bit error rate for a particular channel. These control bits then select the detection time, detect error limit, and clear error limits for each channel from the LTE receive SD/SF registers. The detect error limit and the clear error limit registers contain 16-bit values, while the detection time registers use the lower 15 bits for a value and the upper 1 bit for a time unit specifier. For the detection time register, the value contained in the lower 15 bits is either specified in 0.5 ms units (upper bit = 0) or in seconds (upper bit = 1). Note that the performance monitoring clock input to the device is used as the timing reference when the detection time is expressed in seconds. The SD/SF BER select control bits are described in Table 108 and Table 109 on page 138.

A fixed windowing scheme is used for SD/SF detection. The window size is determined by the value in the detection time register for the specified bit error rate. An SD or SF alarm is declared immediately when the accumulated error count exceeds the value specified in the detect error limit register. In the detection process, when the error count equals the threshold, the window is prematurely ended and clearing process starts immediately. If this error limit is not reached by the end of the window, then the accumulated error count is reset to zero. When an SD or SF alarm is declared, the accumulated error count resets and clearing begins using the bit error rate threshold that is 1/10th of the specified value along with the corresponding detection time registers. Clearing of the SD or SF alarm only occurs at the end of the window when the accumulated error count is less than the value specified in the clear error limit register.

29 BER—SD/SF Detection (continued)

29.1 Functional Description of BER—SD/SF Detection (continued)

The SONFEC incorporates two SD/SF detectors in the receive direction. These two monitors can be used as a measurement for the coding gain. The pre-SD/SF detector monitors the B1 or B2 errors for SD/SF detection before BCH decoding. The post-SD/SF detector monitors the B2 errors after BCH decoding.

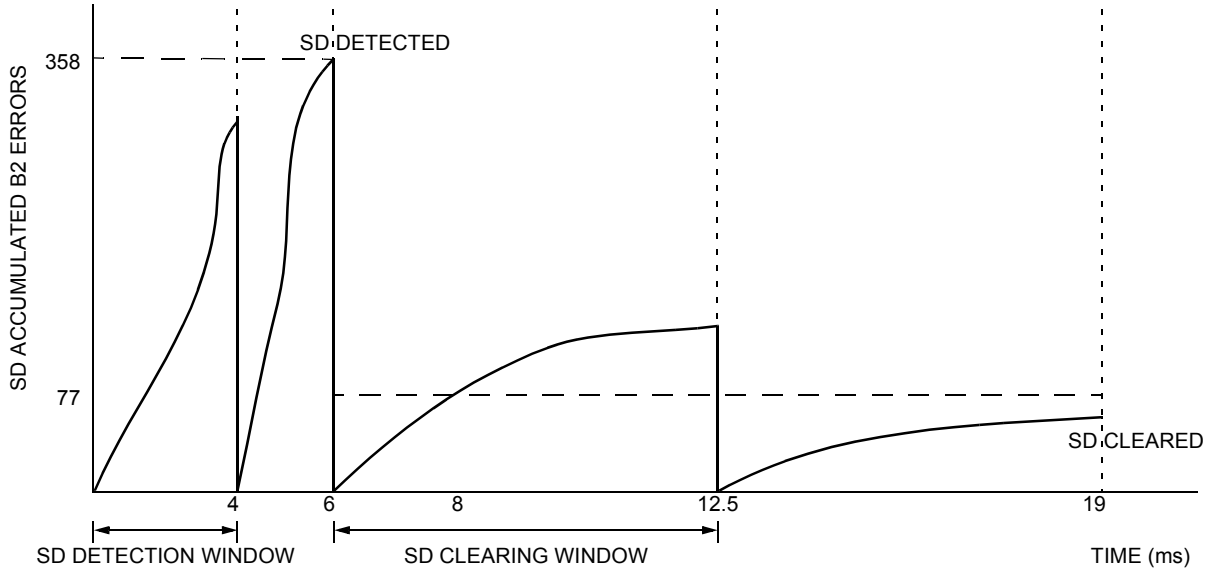


Figure 53. Example of STS-192 SD Detection (10^{-5} BER) and Clearing (10^{-6} BER)

During AIS, insertion due to LOS, LOF, SEF, or line AIS, processing of the B2 byte is inhibited and the internal SF/SD counters are reset back to zero. It takes 5 frames of line AIS before the actual line AIS alarm is declared; it is likely that the signal degrade alarm will also be triggered. Due to this fact, once AIS insertion is removed, processing of the SD/SF is delayed for 2 frames.

Table 108. SD BER Select Control

Register Bits	Value	Description
RX_PRE_SD_BER_SEL/ RX_POST_SD_BER_SEL	000	Select BER 1 x 10^{-5}.
	001	Select BER 1 x 10^{-6}.
	010	Select BER 1 x 10^{-7}.
	011	Select BER 1 x 10^{-8}.
	100	Select BER 1 x 10^{-9}.
	Others	Select BER 1 x 10^{-5}.

Note: See Table 110, B2 Register Summary, on page 138 for RX_PRE_SD_BER_SEL and for RX_POST_SD_BER_SEL descriptions.

29 BER—SD/SF Detection (continued)

29.1 Functional Description of BER—SD/SF Detection (continued)

Table 109. SF BER Select Control

Register Bits	Value	Description
RX_PRE_SF_BER_SEL/ RX_POST_SF_BER_SEL	00	Select BER 1 x 10^{-3}.
	01	Select BER 1 x 10^{-4}.
	10	Select BER 1 x 10^{-5}.
	Others	Select BER 1 x 10^{-3}.

Note: See Table 110 for RX_PRE_SF_BER_SEL and for RX_POST_SF_BER_SEL descriptions.

Table 110. B2 Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
SD/SF Detection Time (1 x 10^{-3})[1]	OHP_RX_SDSF_DT3 (R/W)	RX_SDSF_DT_UNIT_3 RX_SDSF_DT_VAL_3	8	0×1220
SD/SF Detect Error Limit (1 x 10^{-3})[1]	OHP_RX_SDSF_SET3 (R/W)	RX_SDSF_SET_LIMIT_3	7	0×1250
SD/SF Clear Error Limit (1 x 10^{-4})[1]	OHP_RX_SDSF_CLR4 (R/W)	RX_SDSF_CLR_LIMIT_4	7	0×1280
PRE SD/SF BIP Select	OHP_RX_MAINT_S0 (R/W)	RX_PRE_SD_SF_BIPSEL	4	0×1318
SD/SF Threshold Selection	OHP_RX_MAINT_S0 (R/W)	RX_PRE_SD_BER_SEL RX_PRE_SF_BER_SEL	4	0×1318
SD/SF Interrupt Alarms	OHP_RX_SA_ALARM_S0 (W1C)	RX_PRE_SD_A RX_PRE_SF_A	4	0×1024
SD/SF Interrupt Masks	OHP_RX_SA_MASK_S0 (R/W)	RX_PRE_SD_M RX_PRE_SF_M	4	0×1070
SD/SF State	OHP_RX_SA_STATE_S0 (RO)	RX_PRE_SD RX_PRE_SF	4	0×10E8
SD/SF Persistency	OHP_RX_SA_PERSIST_S0 (RO)	RX_PRE_SD_P RX_PRE_SF_P	4	0×10B8

1. These registers are the highest BER. Lower ber configuration registers directly follow these, in secession.

30 Receive Transport Overhead Processing

30.1 Functional Description of the Receive Transport Overhead Processing

This block terminates the transport overhead and incorporates four identical STS-48 overhead processing blocks. Each block accepts the frame and byte-aligned data for one STS-48 channel and extracts the transport section and line overhead. The extracted overhead is then either stored internally or provided externally on a serial output, and may also be further processed for alarm or performance monitoring purposes. The received overhead bytes can also be allowed to pass through unchanged. The definition and associated storage or processing of each byte is detailed in the following subsections.

All processing of overhead bytes is inhibited under AIS conditions. An AIS frame can be generated either by hardware or software.

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

Table 111. Hardware AIS Generation Summary (Receive)

AIS Generation Alarms	AIS Generation Disables	Description
RX_LOC_A	—	Loss of clock.
RX_LOS_A	—	Loss of signal.
RX_SEF_A	RX_SEF_AIS_DIS	Detected severely errored frame.
RX_LOF_A	RX_LOF_AIS_DIS	Detected loss of frame.
RX_AIS_L_A	RX_LINE_AIS_DIS	Detected line AIS frame.
RX_J0_MISMATCH_A	RX_TIM_L_AIS_DIS	Detected J0 mismatch.
RX_POST_SF_A	RX_SF_AIS_DIS	Detected signal fail.

In addition to the individual storage or external availability of the overhead bytes described below, the transport overhead bytes for each STS-48 (individual or part of STS-192) are serialized and output on the TOAC pins of the device. There are four sets of TOAC data pins available for each STS-48 channel. This TOAC interface can operate in two modes[1]. In full TOAC drop mode, the full set of transport overhead bytes for each STS-48 channel (1296 bytes) is output on the TOAC pins. In partial TOAC drop mode, only the transport overhead bytes of the first STS-1 of each STS-48 channel (27 bytes) are output on the TOAC pins. The bytes are output, MSN (most significant nibble) first (4 bits on 4 pins), with each bit output on the positive edge of the TOAC clock (20.736 MHz (full)/ 1.728 MHz (partial)). The location of the MSN of the first A1 byte is identified by the TOAC sync output going high.

In STS-48 mode, each of the TOAC data pins transmits the transport overhead for an STS-48 channel. In STS-192 (full TOAC) mode, the four pairs of the TOAC data pins transmit the STS-192 overhead (5184 bytes), where the TOAC data #1 pins transmit STS channels 1 through 48, and the TOAC data #2, TOAC data #3, and TOAC data #4 pins transmit STS channels 49 through 96, 97 through 144, and 145 through 192, respectively. The receive TOAC drop is described in detail in Section 32.1 on page 160.

Note: In SONFEC, four overhead processors capable of processing an entire STS-48 are implemented. In 2.5 Gbits/s mode, each functions independently. However, in 10 Gbits/s mode, only one slice (that process the STS-48 #1 in a STS-192) functions as master slice and the others function very minimally. In OHP, this master slice is slice 3. Therefore, though all the rest of the 10 Gbits/s alarms are reported in slice 0, in OHP, the alarms in 10 Gbits/s are reported in the slice 3 registers. Following the same reason, regardless of 10 Gbits/s or 2.5 Gbits/s mode of operation, all the overhead processing slices are to be programmed.

30.1.1 Global Overhead Byte Processing

Insertion of AIS on the receive side can be either due to hardware or software. If hardware AIS is detected, then the overhead bytes, except A1 and A2, are set to 0xFF. A1 bytes and A2 bytes will have the inserted framing pattern. In the following sections, the term rx_hw_insert_ais is used to indicate a hardware controlled AIS condition.

The register bit receive SDH mode controls the default values of overhead bytes. If set to 1, the default overhead values are set to 0×FF (SDH mode); otherwise, it is set to 0×00 (SONET mode).

Table 112. Receive Overhead Processor General Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
SONET/SDH Mode	OHP_RX_PROV_S0 (R/W)	RX_SDH_MODE	4	0×1310
OHP Mode Control	SONFEC_RX_MODE (R/W)	RX_OHP_MODE	1	0×1110
AIS-L Insert Control	OHP_RX_MAINT_S0 (R/W)	RX_LINE_AIS_INS	4	0×1314

1. For more information on the two TOAC modes, see Section 2.4, TOAC Insert/Drop Channel Overview, on page 10.

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.1 Default All Undefined Bytes in Section Overhead

For all the bytes that are not specified in the following sections, and default bytes in other STS-1(s) in a STS-48 or STS-192, processing is done as follows:

```
if NOT (rx_hw_insert_ais)
    Section_Undefined_Byte = Received_Line_Data;
else
    Section_Undefined_Byte = Default_SONET_SDH;
end
```

30.1.1.2 Default All Undefined Bytes in Line Overhead

For all the bytes that are not specified in the following sections, and default bytes in other STS-1(s) in a STS-48 or STS-192, processing is done as follows:

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    Line_Undefined_Byte = 0xFF;
else
    Line_Undefined_Byte = Received_Line_Data;
end
```

30.1.1.3 Framing Byte (A1)

The framing byte A1 is overwritten if not inhibited by software. If normal framing is selected, the A1 bytes are set to 0xF6, while the A2 bytes are set to 0x28. If enhanced framing is selected, using the framing mode control bit, the A1 bytes and A2 bytes contain normal framing (0xF6 and 0x28) in odd STS-1 time slots and the inverse value (0x09 and 0xD7) in even STS-1 time slots.

```
if (RX_A1A2_INH) and NOT (rx_hw_insert_ais)
    A1 = Received_Line_Data;
else if (RX_ENH_FRMG_INS)
    A1 = Enhanced_Framing_A1;
else
    A1 = Normal_Framing_A1;
end
```

Table 113. A1 Register Summary (Receive)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
A1 Insertion Enable	OHP_RX_PROV_S0 (R/W)	RX_A1A2_INH	4	0×1310
Enhanced Framing		RX_ENH_FRMG_INS	4	0×1310

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.4 Framing Byte (A2)

The framing byte A2 is overwritten if not inhibited by software. If normal framing is selected, the A1 bytes are set to 0xF6, while the A2 bytes are set to 0x28. If enhanced framing is selected using the framing mode control bit, the A1 bytes and A2 bytes contain normal framing (0xF6 and 0x28) in odd STS-1 time slots and the inverse value (0x09 and 0xD7) in even STS-1 time slots.

```
if (RX_A1A2_INH) and NOT (rx_hw_insert_ais)
    A2 = Received_Line_Data;
else if (RX_ENH_FRMG_INS)
    A2 = Enhanced_Framing_A2;
else
    A2 = Normal_Framing_A2;
end
```

Table 114. A2 Register Summary (Receive)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
A2 Insertion Enable	OHP_RX_PROV_S0 (R/W)	RX_A1A2_INH	4	0×1310
Enhanced Framing		RX_ENH_FRMG_INS	4	0×1310

30.1.1.5 Section Trace (J0)

The section trace byte is present in the first STS-1 of the STS-48 or STS-192 only. Specified by the J0 message type control bit, the TOH processor supports extraction of either SONET 64-byte (ASCII, <CR><LF> terminated) or SDH 16-byte (E.164) section trace messages which are stored in internal memory. Processing of the received message then depends on the J0 message mode control bit. The content of the message is either monitored for a mismatch from a provisioned expected message, or monitored for a sustained change (validation) in the received message.

Table 115. J0 Message Control Register Bits (Receive)

Register Bits	Value	Description
RX_J0_TYPE	0	SONET format (64 byte).
	1	SDH format (16 byte).
RX_J0_MODE	01	Provisioned (expected value).
	10	Validated (sustaining value).
	11/00	Undefined.

Note: See Table 116 for RX_J0_TYPE and RX_J0_MODE descriptions.

If the J0 message mode control bit is set to the provisioned mode, then the incoming message is compared against the software programmed expected message. The expected message is stored in the internal memory for each STS-48 channel. A mismatch is declared if a consistent received message differs from the expected message for ten consecutive messages. The mismatch clears when four out of five received messages match the expected message (fixed windowing is used for clearing). This mismatch state is reflected in the J0 message mismatch alarm bit.

If J0 mismatch is detected, it can optionally generate AIS frames if software enabled.

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

When the J0 message mode control bit is set to the validated mode, the incoming message is monitored for a sustained change. A sustained change is detected when the received message differs from the last stable message for ten consecutive messages. The new message then becomes the stable message, is stored in internal memory, and the processor starts checking for a sustained change from this new stable message (i.e., there is no clearing criteria for a sustained change). The J0 new message alarm bit is set when a sustained change is detected.

Selection of the message type, SONET or SDH format, and the content monitoring mode (provisioned or validated), are provisionable on a per STS-48 channel basis through a corresponding LTE receive channel maintenance register. The associated alarms for the two modes are reported in the corresponding LTE receive channel nonservice affecting interrupt alarm register.

The expected messages for all channels are provisioned through the microprocessor interface using the 64-byte J0 access expected message buffer. The sustained or captured messages for all channels are available through the microprocessor interface, using the 64-byte J0 access received message buffer.

```
if NOT (rx_hw_insert_ais)
    J0 = Received_Line_Data;
else
    J0 = 0×FF;
end
```

Table 116. J0 Register Summary (Receive)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Message Type Control	OHP_RX_MAINT_S0 (R/W)	RX_J0_TYPE RX_J0_MODE	4	1318
Message Mismatch Alarm	OHP_RX_NSA_0_ALARM_S0 (W1C)	RX_J0_MISMATCH_A	4	0×102C
New Message Alarm	OHP_RX_NSA_1_ALARM_S0 (W1C)	RX_J0_NEW_A	4	0×1028
Message Mismatch Alarm Mask	OHP_RX_NSA_0_MASK_S0 (R/W)	RX_J0_MISMATCH_M	4	0×1078
New Message Alarm Mask	OHP_RX_NSA_1_MASK_S0 (R/W)	RX_J0_NEW_M	4	0×1074
Message Mismatch State	OHP_RX_NSA_0_STATE_S0 (RO)	RX_J0_MISMATCH	4	0×10EC
Message Mismatch Persistency	OHP_RX_NSA_0_PERSIST_S0 (RO)	RX_J0_MISMATCH_P	4	0×10BC
J0 Access Expected Message Buffer	OHP_RX_J0EXP0_S0 OHP_RX_J0EXP31_S0 (R/W)	RX_J0_EXP_0 RX_J0_EXP_31 [32]	4	0×1800 0×181F
J0 Access Sustained Message Buffer	OHP_RX_J0SUS0_S0 OHP_RX_J0SUS31_S0 (RO)	RX_J0_SUS_0 RX_J0_SUS_31 [32]	4	0×1880 0×189F

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.6 Section Growth (Z0)

No receive function has been defined for the section growth byte present in the remaining STS-1 locations of the STS-48 or STS-192 J0 byte. In the receive direction, these bytes are transferred to the system interface or TOAC drop without modification.

```
if NOT (rx_hw_insert_ais)
    Z0 = Received_Line_Data;
else
    Z0 = 0×FF;
end
```

30.1.1.7 Section BIP-8 (B1)

The section BIP-8 B1 byte is located in the first STS-1 of the STS-48 or STS-192 only. The computed B1 is inserted on the first STS-1 B1 byte location. The other STS-1 B1 bytes are transferred to the system interface or TOAC drop without modification. Optionally, B1 can be corrupted by enabling the B1 corrupt enable bit. B1 insertion is controlled by B1 compute block.

The overhead processor bypasses the received B1.

30.1.1.8 Local Orderwire (E1)

The local orderwire byte is located in the first STS-1 of the STS-48 or STS-192 only and provides a 64 kHz channel for voice communications between regenerators, hubs, and remote terminals. These bytes are transferred to the system interface or TOAC drop without modification.

```
if NOT (rx_hw_insert_ais)
    E1 = Received_Line_Data;
else
    E1 = 0×FF;
end
```

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.9 Section User Channel (F1)

The section user channel byte is located in the first STS-1 of the STS-48 or STS-192 only and provides a 64 kHz channel for use by the network provider. The byte is extracted from each frame. A new value is only validated and stored in the F1 byte after it has been received for the programmed N consecutive times. Detection of a new validated byte is indicated by the F1 new byte alarm bit. The alarm is only generated when the value of the new validated byte is different from the value of the last validated byte. The other STS-1 F1 bytes are transferred to the system interface or TOAC drop without modification.

```
if NOT (rx_hw_insert_ais)
    F1 = Received_Line_Data;
else
    F1 = 0×FF;
end
```

Table 117. Section User Channel (F1) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
New Validated F1 Alarm	OHP_RX_NSA_1_ALARM_S0 (W1C)	RX_F1_NEW_A	4	0×1028
New Validated F1 Alarm Mask	OHP_RX_NSA_1_MASK_S0 (R/W)	RX_F1_NEW_M	4	0×1074
New Validated F1 Value	OHP_RX_F1S1BYTE_S0 (RO)	RX_F1_BYTE	4	0×1334
Validated F1 N-Time Detect	OHP_RX_F1S1DET_S0 (R/W)	RX_F1_NDET	4	0×1328

30.1.1.10 Section Data Communications Channel (D1, D2, and D3)

The section data communications channel bytes are located in the first STS-1 of the STS-48 or STS-192 only and are used as one 192 kHz message-based channel for operations, administration, and maintenance (OA&M) communication. These bytes are transferred to the system interface or TOAC drop without modification.

```
if NOT (rx_hw_insert_ais)
    D1_To_D3 = Received_Line_Data;
else
    D1_To_D3 = 0×FF;
end
```

30.1.1.11 Line BIP-8 (B2)

The line BIP-8 B2 byte is provided in all the STS-1s of the STS-48 or STS-192. The computed B2 is inserted in these locations. Optionally, B2 can be corrupted by enabling the B2 corrupt enable bit.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    B2 = 0xFF;
else
    B2 = Computed_B2;
end
```

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.12 STS Payload Pointer (H1, H2, and H3)

The STS pointers are passed through unchanged. If PRBS payload monitoring is enabled, these pointer values are set to 522[1]. These bytes are transferred to the system interface or TOAC drop without modification.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    H1_To_H3 = 0xFF;
else
    H1_To_H3 = Received_Line_Data;
end
```

30.1.1.13 Receive APS Channel (K1 and K2)

The APS channels' bytes are located in the first STS-1 of the STS-48 or STS-192 only, and are used for automatic protection switching (APS) signaling to coordinate line-level protection switching. In addition, the K2 byte is also used to carry line AIS (AIS-L) and line RDI (RDI-L) signals. The other STS-1 K1/K2 bytes are transferred to the system interface or TOAC drop without modification.

A new value in either byte is only validated after it has been received N times consecutively, where N is provisionable to 3 or 5 using the K1K2 validate select control bit. When a K1 or K2 byte is validated, the value is stored in the K byte status register and the K1K2 new byte alarm bit is set. These two alarms are only generated when the value of the new validated K1 or K2 byte is different from the value of the last validated byte. Validation of the K1 and K2 bytes, and the generation of the alarms, is not affected by the line AIS status.

The validated K1 and K2 bytes are further processed for the following defects:

- Protection switching byte. This defect occurs when either an inconsistent APS byte or an invalid code is detected. An inconsistent APS byte occurs when no N consecutive K1 bytes of the last twelve successive frames are identical, starting with the last frame containing a previously consistent byte. An invalid code occurs when the incoming K1 byte contains an unused code or a code irrelevant for the specific switching operation in three consecutive frames. An invalid code also occurs when the incoming K1 byte contains an invalid channel number in three consecutive frames. Because invalid code detection requires information not readily available to hardware, it must be detected by software polling of the validated K1 byte value. An inconsistent APS byte defect is detected by hardware and will cause an alarm status bit to be set in the corresponding LTE receive channel nonservice-affecting interrupt alarm register. It is cleared when a K1 byte is received and validated. An inconsistent APS byte defect is neither detected nor terminated during an AIS-L defect. Processing of the inconsistent APS byte defect is also inhibited when the validated K1 byte has a value of 0xFF and bits 2—0 of the validated K2 byte have a value of 111 (line AIS). This additional feature prevents a change in the inconsistent APS defect state just before line AIS is declared.
- Channel mismatch. This defect occurs when the channel numbers in the transmitted K1 byte (bits 3—0) and the validated received K2 byte (bits 7—4) are not identical. Detection of a channel mismatch defect causes a latched alarm status bit to be set in the corresponding LTE receive channel nonservice-affecting interrupt alarm register. A channel mismatch defect is neither detected nor terminated during an AIS-L defect. Processing of the channel mismatch defect is also inhibited when the validated K2 byte has a value of 1111x111 binary. This additional feature prevents a change in the channel mismatch defect state just before line AIS is declared.

1. The pointer is set by the incoming signal. Only when PRBS data is injected into the SONET frame is the pointer set, by the device, to 522.

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

In addition, the currently received K2 byte is processed for the following defects:

- Line AIS (AIS-L). Declared when bits 2—0 of K2 contain 111 for five consecutive frames. Cleared when any other pattern is received for five consecutive frames. Detection of a line AIS defect is indicated by an alarm status bit, a persistency bit, and a 1 s PM bit being set in the registers for the affected channel.
- Line RDI (RDI-L). Declared when bits 2—0 of K2 contain 110 (binary) for five consecutive frames. Cleared when any other pattern is received for five consecutive frames. Detection of a line RDI defect is indicated by a latched alarm status bit and a 1 s PM bit being set in the registers for the affected channel.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    K1_To_K2 = 0xFF;
else
    K1_To_K2 = Received_Line_Data;
end
```

Table 118. APS Channel (K1 and K2) Register Summary (Receive)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
K1K2 Validation Length Select (3 or 5)	OHP_RX_PROV_S0 (R/W)	RX_K_VAL_LIMIT_SEL	4	0×1310
Validated K1K2 Storage	OHP_RX_K1K2BYTE_S0 (RO)	RX_K1_BYTE RX_K2_BYTE	4	0×1330
New Validated K1K2 Alarm	OHP_RX_NSA_1_ALARM_S0 (W1C)	RX_K1_NEW_A RX_K2_NEW_A	4	0×1028
Inconsistent APS Alarm	OHP_RX_NSA_0_ALARM_S0 (W1C)	RX_INCONSISTENT_APS_A	4	0×102C
Channel Mismatch Alarm	OHP_RX_NSA_0_ALARM_S0 (W1C)	RX_K1K2CH_MISMATCH_A	4	0×102C
New Validated K1K2 Alarm Mask	OHP_RX_NSA_1_MASK_S0 (W1C)	RX_K1_NEW_M RX_K2_NEW_M	4	0×1074
Inconsistent APS Alarm Mask	OHP_RX_NSA_0_MASK_S0 (R/W)	RX_INCONSISTENT_APS_M	4	0×1078
Channel Mismatch Alarm Mask	OHP_RX_NSA_0_MASK_S0 (R/W)	RX_K1K2CH_MISMATCH_M	4	0×1078
RDI-L Alarm	OHP_RX_NSA_0_ALARM_S0 (W1C)	RX_LINE_RDI_A	4	0×102C
RDI-L Alarm Mask	OHP_RX_NSA_0_MASK_S0 (R/W)	RX_LINE_RDI_M	4	0×1078
Last Second RDI-L PM	OHP_RX_PM_S0 (RO)	RX_LINE_RDI_PM	4	0×132C
Inconsistent APS State	OHP_RX_NSA_0_STATE_S0 (RO)	RX_INCONSISTENT_APS	4	0×10EC
Channel Mismatch State	OHP_RX_NSA_0_STATE_S0 (RO)	RX_K1K2CH_MISMATCH	4	0×10EC
Inconsistent APS Persistency	OHP_RX_NSA_0_PERSIST_S0 (RO)	RX_INCONSISTENT_APS_P	4	0×10EC
Channel Mismatch Persistency	OHP_RX_NSA_0_PERSIST_S0 (RO)	RX_K1K2CH_MISMATCH_P	4	0×10BC
RDI-L State	OHP_RX_NSA_0_STATE_S0 (RO)	RX_LINE_RDI	4	0×10EC
RDI-L Persistency	OHP_RX_NSA_0_PERSIST_S0 (RO)	RX_LINE_RDI_P	4	0×10BC

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.14 Line Data Communication Channel (D4—D12)

The line data communication channel bytes are located in the first STS-1 of the STS-48 or STS-192 only and are used as one 576 kHz message-based channel for operations, administration, and maintenance communication (OA & M). These bytes are transferred to the system interface or TOAC drop without modification.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    D4_To_D12 = 0xFF;
else
    D4_To_D12 = Received_Line_Data;
end
```

30.1.1.15 Synchronization Status (S1)

The synchronization status byte is located in the first STS-1 of the STS-48 or STS-192 only and is used to convey the synchronization status of a network element. The byte is extracted from each frame. A new value is only validated and stored in the S1 byte after it has been received for the programmed N consecutive times. Detection of a new validated byte is indicated by the S1 new byte alarm bit. The alarm is only generated when the value of the new validated byte is different from the value of the last validated byte. The other STS-1 S1 bytes are transferred to the system interface or TOAC drop without modification.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    S1 = 0xFF;
else
    S1 = Received_Line_Data;
end
```

Table 119. Receive Synchronization Status (S1) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
New Validated S1 Alarm	OHP_RX_NSA_1_ALARM_S0 (W1C)	RX_S1_NEW_A	4	0×1028
New Validated S1 Alarm Mask	OHP_RX_NSA_1_MASK_S0 (R/W)	RX_S1_NEW_M	4	0×1074
New Validated S1 Value	OHP_RX_F1S1BYTE_S0 (RO)	RX_S1_BYTE	4	0×1334
Validated S1 N-Time Detect	OHP_RX_F1S1DET_S0 (R/W)	RX_S1_NDET	4	0×1328

30 Receive Transport Overhead Processing (continued)

30.1 Functional Description of the Receive Transport Overhead Processing (continued)

30.1.1.16 Line Remote Error Indication (M1)

The line remote error indication (REI-L) byte is located in the third STS-1 of the STS-48 or STS-192 only (in order of appearance in the STS-192 signal) and is used to convey to the far end the number of errors detected using the line BIP-8 bytes (truncated at 255). The byte is extracted from each frame and the value added to an internal 21-bit counter. The value in the counter is transferred to the REI-L registers on the positive edge of the performance monitoring (PM) clock input, at which point the counter is cleared. The counter will stop at the maximum value and will not roll over. The other STS-1 M1 bytes are transferred to the system interface or TOAC drop without modification.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    M1 = 0xFF;
else
    M1 = Received_Line_Data;
end
```

Table 120. Line REI (M1) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Last Second REI-L Count	OHP_RX_REI_L_PM_S0 OHP_RX_REI_U_PM_S0 (RO)	RX_REIL_U RX_REIL_L	4 4	0×1338 0×1339

30.1.1.17 Express Orderwire (E2)

The express orderwire byte is located in the first STS-1 of the STS-48 or STS-192 only and provides a 64 kHz channel for voice communications between line entities. The other STS-1 E2 bytes are transferred to the system interface or TOAC drop without modification.

```
if (RX_LINE_AIS_INS) or (rx_hw_insert_ais)
    E2 = 0xFF;
else
    E2 = Received_Line_Data;
end
```

31 Transmit Transport Overhead (TOH) Processor

31.1 Functional Description of TOH Processor

This block inserts the transport overhead and incorporates four identical STS-48 overhead processing blocks. Each block accepts the data for one STS-48 channel from the transmit payload add interface and inserts the transport section and line overhead. The inserted overhead is either sourced internally or provided externally on serial inputs. If sourced internally, the overhead may be from registers in the microprocessor interface, or derived. The received overhead bytes can also be allowed to pass through unchanged.

In STS-48 mode, each channel carries complete transport overhead. In STS-192 mode, only the first STS-48 channel carries complete transport overhead, while the other channels only carry framing (A1, A2), Z0, and line BIP-8. In addition, the line overhead bytes can all be overwritten with all ones (along with all of the payload SPE bytes) by enabling line AIS insertion. If software is disabled, the transmit overhead processing is disabled. Software can disable either the line overhead bytes processing, section overhead bytes processing, or both.

All processing of overhead bytes is inhibited under AIS conditions. An AIS frame can be generated either by hardware or software.

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

Table 121. Hardware AIS Generation Summary (Transmit)

AIS Generation Alarms	AIS Generation Disables	Description
TX_LOC_A	—	Loss of clock.
TX_LOS_A	—	Loss of signal.
TX_SEF_A	TX_SEF_AIS_DIS	Detected severely errored frame.
TX_LOF_A	TX_LOF_AIS_DIS	Detected loss of frame.
TX_AIS_L_A	TX_LINE_AIS_DIS	Detected line AIS frame.

In addition to the individual storage or external availability of the overhead bytes described, the transport overhead bytes for each STS-48 (individual or part of STS-192) can be sourced serially using the TOAC data pins. This TOAC interface can operate in two modes[1]. In full TOAC drop mode, the full set of transport overhead bytes for each STS-48 channel (1296 bytes) can be sourced on the TOAC pins. In partial TOAC drop mode, only the transport overhead bytes of the first STS-1 of each STS-48 channel (27 bytes) can be sourced on the TOAC pins. Insertion must be globally enabled through software using the TOH data insert control bit, and then enabled on a per-byte basis by strobing the TOAC enable pin high during the LSB of the byte to insert (the state of the TOAC enable is ignored during the other bits). The bytes are received, MSN (most significant nibble) first (4 bits on 4 pins), with each bit output on the positive edge of the TOAC clock (20.736 MHz (full)/1.728 MHz (partial)). The location of the MSN (most significant nibble) bit of the first A1 byte is identified by the TOAC sync output going high. For B2, the value received is actually used as an XOR corruption mask for the internally calculated values.

In STS-48 mode, the individual TOAC data pins, along with the TOAC enable pin, capture the transport overhead for that STS-48 channel. In STS-192 mode, the four pairs of TOAC data pins, along with their respective TOAC enable pins, capture the entire STS-192 overhead (5184 bytes), where the TOAC data #1 pins capture STS channels 1 through 48, and the TOAC data #2, TOAC data #3, and TOAC data #4 pins capture STS channels 49 through 96, 97 through 144, and 145 through 192, respectively. The TOAC insert functionality is described in detail later in this section.

Note: In SONFEC, four overhead processors capable of processing an entire STS-48 are implemented. In 2.5 Gbits/s mode, each functions independently. However, in 10 Gbits/s mode, only one slice (that process the STS-48 #1 in an STS-192) functions as a master slice and all others functions are very minimal. In OHP, the master slice is slice 3. Therefore, though all the rest of the 10 Gbits/s alarms are reported in slice 0, in overhead processor, the alarms in 10 Gbits/s are reported at slice 3 registers. Following the same reason, regardless of 10 Gbits/s or 2.5 Gbits/s mode of operation, all the overhead processing slices are to be programmed.

1. For more information on the two TOAC modes, see Section 2.4 on page 10.

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1 Global Overhead Byte Insertion

If TOAC insertion is enabled, the first 2 bits (MSB and MSB – 1 positions of the data) of the TOAC data enable input control the overhead byte insertion.

Table 122. TOAC Byte Insertion Control

TOAC Enable Data	Value	Description
TX_TOAC_ENB (Pin) Sampled at [MSB], [MSB – 1] Positions Only	11	Insert data from the serial TOAC input.
	00	Default data.
	01	Bypass data.
	10	Software controlled data.

In the following sections, the term TOAC_Controlled_Data is used to indicate the data inserted in the overhead byte position, depending on the TOAC enable pin.

If AIS is detected, then all the line overhead bytes are set to 0xFF. Insertion of AIS can be either due to hardware or software. In the following sections, the term tx_hw_insert_ais is used to indicate a hardware-controlled AIS condition.

The register bit transmit SDH mode controls the default values of overhead bytes. If set to 1, the default value is set to either 0xFF (SDH mode) or 0x00 (SONET mode).

Table 123. Transmit Overhead Processor General Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
OHP (SOH) Disable Control	SONFEC_TX_BYPASS_S0 (R/W)	OHP_TX_SOH_PROC_DIS	4	0×1119
OHP (LOH) Disable Control	SONFEC_TX_BYPASS_S0 (R/W)	OHP_TX_LOH_PROC_DIS	4	0×1119
Global TOAC Byte Insert Control	OHP_TX_PROV_S0 (R/W)	TX_TOAC_ENB	4	0×1370
SONET/SDH Mode	OHP_TX_PROV_S0 (R/W)	TX_SDH_MODE	4	0×1370
OHP Mode Control	SONFEC_TX_MODE (R/W)	TX_OHP_MODE	1	0×1111
AIS-L Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_LINE_AIS_INS	4	0×1374

31.1.1.1 Default All Undefined Bytes in Section Overhead

For all the bytes that are not specified in the following sections and default bytes in other STS-1(s) in an STS-48 or STS-192, processing is done as follows:

```
if (TX_TOAC_ENB)
        Section_Undefined_Byte = TOAC_Controlled_Data;
else if (OHP_TX_SOH_PROC_DIS) and NOT (tx_hw_insert_ais)
    Section_Undefined_Byte = Received_System_Data;
else
    Section_Undefined_Byte = Default_SONET_SDH;
end
```

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1.2 Default All Undefined Bytes in Line Overhead

For all the bytes that are not specified in the following sections and default bytes in other STS-1(s) in an STS-48 or STS-192, processing is done as follows:

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    Line_Undefined_Byte = 0xFF;
else if (TX_TOAC_ENB)
    Line_Undefined_Byte = TOAC_Controlled_Data;
else if (OHP_TX_LOH_PROC_DIS)
    Line_Undefined_Byte = Received_System_Data;
else
    Line_Undefined_Byte = Default_SONET_SDH;
end
```

31.1.1.3 Framing Byte (A1)

The framing byte A1 is overwritten if not inhibited by software. If normal framing is selected, the A1 bytes are set to 0xF6, while the A2 bytes are set to 0x28. If enhanced framing is selected using the framing mode control bit, the A1 bytes and A2 bytes contain normal framing (0xF6 and 0x28) in odd STS-1 time slots and the inverse value (0x09 and 0xD7) in even STS-1 time slots.

```
if (TX_TOAC_ENB)
        A1 = TOAC_Controlled_Data;
else if (TX_A1A2_INH) and NOT (tx_hw_insert_ais)
    A1 = Received_System_Data;
else if (TX_ENH_FRMG_INS)
    A1 = Enhanced_Framing_A1;
else
    A1 = Normal_Framing_A1;
end
```

Table 124. A1 Register Summary (Transmit)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
A1 Insertion Enable	OHP_TX_PROV_S0 (R/W)	TX_A1A2_INH	4	0×1370
Enhanced Framing		TX_ENH_FRMG_INS	4	0×1370

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1.4 Framing Byte (A2)

The framing byte A2 is overwritten if not inhibited by software. If normal framing is selected, the A1 bytes are set to 0xF6, while the A2 bytes are set to 0x28. If enhanced framing is selected using the framing mode control bit, the A1 bytes and A2 bytes contain normal framing (0xF6 and 0x28) in odd STS-1 time slots and the inverse value (0x09 and 0xD7) in even STS-1 time slots. Alternatively, errors can be inserted in A2 bytes by setting the corresponding TX_A2_ERR_INS bit for each slice. The errors are inserted by inverting every fourth A2 byte out of the 192 A2 bytes starting with the first byte. Also, during A2 error insertion, normal framing is always used even if TX_ENH_FRMG_INS is set to 1.

```
if (TX_TOAC_ENB)
        A2 = TOAC_Controlled_Data;
else if (TX_A2_ERR_INS)
    A2 = Errored_A2;
else if (TX_A1A2_INH) and NOT (tx_hw_insert_ais)
    A2 = Received_System_Data;
else if (TX_ENH_FRMG_INS)
    A2 = Enhanced_Framing_A2;
else
    A2 = Normal_Framing_A2;
end
```

Table 125. A2 Register Summary (Transmit)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
A2 Insertion Enable	OHP_TX_PROV_S0 (R/W)	TX_A1A2_INH	4	0×1370
Enhanced Framing	OHP_TX_PROV_S0 (R/W)	TX_ENH_FRMG_INS	4	0×1370
A2 Error Control	OHP_TX_MAINT_S0 (R/W)	TX_A2_ERR_INS	4	0×1378

31.1.1.5 Section Trace (J0)

The section trace byte is present in the first STS-1 of the STS-48 or STS-192 only. The TOH processor supports insertion of either SONET 64-byte (ASCII, <CR><LF> terminated) or SDH 16-byte (E.164) section trace messages. The message is stored in internal memory and should be repeated four times if a 16-byte SDH message is to be sent. The message is provisioned by software using the section trace access registers. After the message is provisioned, insertion of the message must be enabled through the J0 message insert control bit. If insertion is not enabled, the J0 byte is instead sent as 0x01 for STS-48/STS-192 mode.

```
if (TX_TOAC_ENB)
        J0 = TOAC_Controlled_Data;
else if (TX_J0_INS)
    J0 = MPU_Programmed_J0;
else if (OHP_TX_SOH_PROC_DIS) and NOT (tx_hw_insert_ais)
    J0 = Received_System_Data;
else
    J0 = 0×01;
end
```

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

Table 126. J0 Register Summary (Transmit)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Message Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_J0_INS	4	0×1378
J0 Provisioned Message Buffer	OHP_TX_J0BYTE0_S0 OHP_TX_J0BYTE31_S0 (R/W)	TX_J0_EXP_0 TX_J0_EXP_31	4	0×1900 0×191F

31.1.1.6 Section Growth (Z0)

The section growth bytes are present in the STS-1 locations, excluding the first STS-1 of the STS-48 or STS-192. They are set to the fixed pattern 0xCC in STS-192 mode, or to an increasing binary count (2 to 48, corresponding to order of appearance) in STS-48 mode.

```
if (TX_TOAC_ENB)
        Z0 = TOAC_Controlled_Data;
else if (OHP_TX_SOH_PROC_DIS and NOT (tx_hw_insert_ais)
    Z0 = Received_System_Data;
else if (TX_OHP_MODE equals 2G5)
    Z0 = 0×02_to_0×48;
else
    Z0 = 0×CC;
end
```

31.1.1.7 Section BIP-8 (B1)

The section BIP-8 B1 byte is located only in the first STS-1 of the STS-48 or STS-192. The computed B1 is inserted on the first STS-1 B1 byte location. Optionally, B1 can be corrupted by enabling the B1 corrupt enable bit.

```
if (TX_TOAC_ENB)
        B1 = TOAC_Controlled_Data;
else if (OHP_TX_SOH_PROC_DIS) and NOT (tx_hw_insert_ais)
    B1 = Received_System_Data;
else
    B1 = Default_SONET_SDH;
end
```

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1.8 Local Orderwire (E1)

The local orderwire byte is located only in the first STS-1 of the STS-48 or STS-192, and provides a 64 kHz channel for voice communications between regenerators, hubs, and remote terminals.

```
if (TX_TOAC_ENB)
        E1 = TOAC_Controlled_Data;
else if (OHP_TX_SOH_PROC_DIS) and NOT (tx_hw_insert_ais)
    E1 = Received_System_Data;
else
    E1 = Default_SONET_SDH;
end
```

31.1.1.9 Section User Channel (F1)

The section user channel byte is located only in the first STS-1 of the STS-48 or STS-192 and provides a 64 kHz channel for use by the network provider. The byte is inserted in each frame using either a value provisioned in the F1 byte control register or from a value received on the TOAC data input.

```
if (TX_TOAC_ENB)
        F1 = TOAC_Controlled_Data;
else if (TX_F1_INS)
    F1 = MPU_Programmed_F1;
else if (OHP_TX_SOH_PROC_DIS) and NOT (tx_hw_insert_ais)
    F1 = Received_System_Data;
else
    F1 = Default_SONET_SDH;
end
```

Table 127. Transmit F1 Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Byte Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_F1_INS	4	0×1378
Provisioned F1 Byte	OHP_TX_F1S1BYTE_S0 (R/W)	TX_F1_BYTE	4	0×1388

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1.10 Section Data Communications Channel (D1, D2, and D3)

The section data communications channel bytes are located only in the first STS-1 of the STS-48 or STS-192, and are used as one 192 kHz message-based channel for operations, administration, and maintenance (OA & M) communication.

```
if (TX_TOAC_ENB)
        D1_To_D3 = TOAC_Controlled_Data;
else if (OHP_TX_SOH_PROC_DIS) and NOT (tx_hw_insert_ais)
    D1_To_D3 = Received_System_Data;
else
    D1_To_D3 = Default_SONET_SDH;
end
```

31.1.1.11 Line BIP-8 (B2)

The line BIP-8 B2 byte is provided in all the STS-1s of the STS-48 or STS-192. The computed B2 is inserted in these locations. If B2 calculation and TOAC insertion are enabled, the computed B2 value is XORed with the received TOAC B2 byte value (if TOAC data enable is asserted on the MSB of B2 byte). Optionally, B2 can be corrupted by enabling the B2 corrupt enable bit.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    B2 = 0xFF;
else if (TOAC Mode)
    if (TOAC Enable Mode is 11)
        B2 = Computed_B2 xor TOAC_Data;
    else
        B2 = bypass, default, or software controlled depending on TOAC enable mode 01, 00, or 10;
    end if
else if (OHP_TX_B2_BYPASS)
    B2 = Received_System_Data;
else
    B2 = Computed_B2;
end
```

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1.12 STS Payload Pointer (H1/H2/H3)

The STS payload pointer bytes are normally set to the values received at the system interface. These values are overwritten under the following conditions (in order of precedence from highest to lowest):

If the H1, H2, or H3 pointers are changed, then **no other** overhead processing is done. TOAC or software controls are ignored.

- Software/hardware AIS insertion: if enabled, overwrites the pointer bytes for the channel with 0xFFFFFF.
- Unequipped signal insertion: if enabled, overwrites the pointer bytes for the channel with 0x600000.
- PRBS payload insertion: if enabled, overwrites the pointer bytes for the channel with 0x620A00.
- Invalid pointer insertion: if enabled, overwrites the pointer bytes for the channel with 0x633300.
- NDF pointer insertion: if enabled, overwrites the pointer bytes for the channel with 0x920A00.
- TOAC data insertion: controlled by TOAC.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    H1 = 0xFF;
    H2 = 0xFF;
    H3 = 0xFF;
else if (TX_LINE_UNEQ_INS)
    H1 = 0x60;
    H2 = 0x00;
    H3 = 0x00;
else if (TX_PRBS_ENB)
    H1 = 0x62;
    H2 = 0x0A;
    H3 = 0x00;
else if (TX_INV_PTR_INS)
    H1 = 0x63;
    H2 = 0x33;
    H3 = 0x00;
else if (TX_NDF_INS)
    H1 = 0x92;
    H2 = 0x0A;
    H3 = 0x00;
else if (TX_TOAC_ENB)
    if (TX_LINE_AIS_INS OR tx_hw_insert_ais)
        H1 = Non TOAC Functionality
        H2 = Non TOAC Functionality
        H3 = Non TOAC Functionality
    else
        H1 = TOAC_Controlled_Data;
        H2 = TOAC_Controlled_Data;
        H3 = TOAC_Controlled_Data;
else
    H1 = Received_System_Data;
    H2 = Received_System_Data;
    H3 = Received_System_Data;
end
```

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

Table 128. Transmit STS Payload Pointer Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
NDF Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_NDF_INS	4	0×1378
Invalid Pointer Insert Control		TX_INV_PTR_INS	4	0×1378
UNEQ-L Insert Control		TX_LINE_UNEQ_INS	4	0×1378

31.1.1.13 APS Channel (K1 and K2)

The APS channel bytes are located only in the first STS-1 of the STS-48 or STS-192 and are used for automatic protection switching (APS) signaling to coordinate line level protection switching. In addition, the K2 byte is also used to carry line AIS and line RDI signals. Both bytes are inserted during each frame, normally using values stored in the K-byte register. In addition, the value of bits 2—0 in K2 can optionally be automatically overwritten by 110 (RDI-L) when AIS-L, LOS, SEF, or LOF (SEF and LOF only if AIS insertion is enabled) are detected for the receive STS-48 or STS-192. This insertion is controlled by the RDI-L select bit in the LTE transmit channel maintenance register. When RDI-L is triggered, it will be inserted for a minimum of 20 consecutive frames, if not software disabled.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    K1 = 0xFF;
    K2 = 0xFF;
else if (TX_TOAC_ENB)
    K1 = TOAC_Controlled_Data;
    if (TX_RDI_L_SEL) and (tx_hw_insert_rdi)
        K2 = K2[7:3] & “110“;
    else if (TX_RDI_L_SEL)
        K2 = TOAC_Controlled_Data;
    end
else if (APS_BYPASS)
    K1 = By Pass Data;
    K2 = By Pass Data;
else
    K1 = MPU_Programmed_K1;
    if (TX_RDI_L_SEL) and (tx_hw_insert_rdi)
        K2 = K2[7:3] & “110“;
    else if (TX_RDI_L_SEL)
        K2 = TOAC_Controlled_Data;
    end
end
```

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

Table 129. Transmit APS Channel (K1K2) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
K1K2 Software Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_K1K2_BYPASS	4	0×1378
K1K2 Software Insert Value	OHP_TX_K1K2BYTE_S0 (R/W)	TX_K1_BYTE TX_K2_BYTE	4	0×138C
RDI-L Duration Control	OHP_TX_AIS_RDI_S0 (R/W)	TX_20FRM_RDI_DIS	4	0×1374
RDI-L Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_RDI_L_SEL	4	0×1378

31.1.1.14 Line Data Communication Channel (D4—D12)

The line data communications channel bytes are located only in the first STS-1 of the STS-48 or STS-192, and are used as one 576 kHz message-based channel for operations, administration, and maintenance communication.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    D4_To_D12 = 0xFF;
else if (TX_TOAC_ENB)
    D4_To_D12 = TOAC_Controlled_Data;
else if (OHP_TX_LOH_PROC_DIS)
    D4_To_D12 = Received_System_Data;
else
    D4_To_D12 = Default_SONET_SDH;
end
```

31.1.1.15 Synchronization Status (S1)

The synchronization status byte is located only in the first STS-1 of the STS-48 or STS-192 and is used to convey the synchronization status of a network element. The byte is inserted in each frame using either a value provisioned in the S1 byte control register or from a value received on the TOAC data input.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    S1 = 0xFF;
else if (TX_TOAC_ENB)
    S1 = TOAC_Controlled_Data;
else if (TX_S1_INS)
    S1 = MPU_Programmed_S1;
else if (OHP_TX_LOH_PROC_DIS)
    S1 = Received_System_Data;
else
    S1 = Default_SONET_SDH;
end
```

Table 130. Transmit Synchronization Status (S1) Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Byte Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_S1_INS	4	0×1378
Provisioned S1 Byte	OHP_TX_F1S1BYTE_S0 (R/W)	TX_S1_BYTE	4	0×1388

31 Transmit Transport Overhead (TOH) Processor (continued)

31.1 Functional Description of TOH Processor (continued)

31.1.1.16 STS-192 Line Remote Error Indication (M1)

The line remote error indication (REI-L) byte is located only in the third STS-1 of the STS-48 or STS-192 (in order of appearance in the STS-192 signal) and is used to convey to the far end the number of errors detected in the receive direction using the line BIP-8 bytes. The byte is inserted each frame with a binary value indicating the number of line BIP-8 errors (truncated at 255) detected in the previous receive frame for the entire STS-48 or STS-192. The value of the byte can be fully corrupted (by setting all bits) on a per STS-48 channel basis using the M1 corrupt enable control bit. The duration of the corruption is defined in frames per second, up to a maximum of 8000 frames (1 second), and corruption starts with the next frame after the rising edge of performance monitoring clock. The M1 corrupt frame count register specifies this duration.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    M1 = 0xFF;
else if (TX_TOAC_ENB)
    M1 = TOAC_Controlled_Data;
else if (TX_M1CORRUPT_EN)
    M1 = 0xFF;
else if (TX_M1_INS)
    M1 = Monitored_B2_Error_Count;
else if (OHP_TX_LOH_PROC_DIS)
    M1 = Received_System_Data;
else
    M1 = 0x00;
end
```

Table 131. Transmit M1 Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Byte Insert Control	OHP_TX_MAINT_S0 (R/W)	TX_M1_INS	4	0×1378
M1 Corrupt Enable	OHP_TX_PROV_S0 (R/W)	TX_M1CORRUPT_ENB	4	0×1370
M1 Corrupt Duration Control	OHP_TX_M1CORRUPT_S0 (R/W)	TX_M1CORRUPT_FRM_CNT	4	0×1384

31.1.1.17 Express Orderwire (E2)

The express orderwire byte is located only in the first STS-1 of the STS-48 or STS-192 and provides a 64 kHz channel for voice communications between line entities.

```
if (TX_LINE_AIS_INS) or (tx_hw_insert_ais)
    E2 = 0xFF;
else if (TX_TOAC_ENB)
    E2 = TOAC_Controlled_Data;
else if (OHP_TX_LOH_PROC_DIS)
    E2 = Received_System_Data;
else
    E2 = Default_SONET_SDH;
end
```

32 Receive TOAC Drop/Transmit TOAC Insert

Four TOAC insert/drop functions are provided in quad STS-48/STM-16 mode and one in STS-192/STM-64 mode.

32.1 Receive TOAC Drop

In the receive direction (TOAC drop), each transport overhead byte is extracted in each frame, buffered, and output MSN (most significant nibble) first (4 bits on 4 pins), with each bit output on the positive edge of the TOAC clock (20.736 MHz (full)/1.728 MHz (partial)). During AIS insertion, due to LOS, LOF, or SEF (provisionable), 0xFF is constantly output. The location of the MSN of the first A1 byte is identified by the TOAC sync output going high.

In STS-48 mode, each of the four TOAC data pins per STS-48 frame transmits the transport overhead for an STS-48 channel. In STS-192 mode, four sets of four TOAC data pins transmit the entire STS-192 overhead (5184 bytes), where the fourth set of four TOAC data pins transmit STS channels 1 through 48, the third set of four TOAC data pins transmit STS channels 49 through 96, the second set of four TOAC data pins transmit channels 97 through 144, and the first set of four TOAC data pins transmit channels 145 through 192.

Internally, a memory is used for each channel in order to buffer the data and transfer it between the internal processing rate and the external data rate. This allows for the data to be transmitted in a nongapped manner. The operation of the memory is monitored using parity and any errors are reported using the TOAC data parity error alarm bit. This alarm bit is present in the corresponding LTE receive channel nonservice-affecting interrupt alarm register and is valid regardless of the mode (STS-48/STM-16 or STS-192/STM-48) of the device.

32.2 Transmit TOAC Insert

In the transmit direction (TOAC insert), each transport overhead byte for each STS-48 (individual or part of an STS-192) can be sourced serially using the four TOAC data pins allocated per STS-48 channel. Insertion of these received bytes is controlled through a global TOAC insert enable bit in the transmit provisioning register. The insertion is then enabled on a per-byte basis by strobing the TOAC data enable pin high during the entire period of the byte to insert. The bytes are received MSN (most significant nibble) first (4 bits on 4 pins), with each bit output on the positive edge of the TOAC clock (20.736 MHz (full)/1.728 MHz (partial)). The location of the MSN (most significant nibble) bit of the first A1 byte is identified by the TOAC sync output going high. For B2, the value received is actually used as an XOR corruption mask for the internally calculated values.

In STS-48 mode, the individual TOAC data pins, along with the TOAC enable pin, capture the transport overhead for that STS-48 channel. In STS-192 mode, the four sets of four TOAC data pins, along with their respective TOAC enable pins, capture the entire STS-192 overhead (5184 bytes), where the fourth set of four TOAC data pins capture STS channels 1 through 48, the third set of four TOAC data pins capture STS channels 49 through 96, the second set of four TOAC data pins capture channels 97 through 144, and the first set of four TOAC data pins capture channels 145 through 192.

Internally, a memory is used for each channel to buffer the data and transfer it between the external data rate and the internal data rate. The operation of the memory is monitored using parity and any errors are reported using the TOAC data parity error alarm bit. This alarm bit is present in the LTE transmit interrupt alarm register and is valid regardless of the mode (STS-48 or STS-192) in which the device is operating.

When enabled, the overhead serial link takes precedence over all other overhead sources, with the exception of bytes that are software enabled.

32 Transmit Transport Overhead (TOH) Processor (continued)

32.3 TOAC Modes

Both the receive TOAC drop and transmit TOAC insert interfaces can operate in two modes: full TOAC insert/drop mode and partial insert/drop mode (see Section 32.3.1 and Section 32.3.2 on page 161).

32.3.1 Full TOAC Insert/Drop Mode

- TOAC clock output at 20.736 MHz.
- TOAC sync output 8 kHz coincide with the MSN (most significant nibble) of the first A1 nibble.
- TOAC data enable input (Tx only) active during the MSN (most significant nibble) of each byte to be inserted into the output stream.
- TOAC data bus (transmit insert input/receive drop output):
  — In STS-48 mode, four bits/stream at 20.736 Mbits/s that transition at the rising edge of the clock (10,368 bits per STS-48/STM-16 SONET/SDH frame).
  — In STS-192 mode, sixteen bits at 20.736 Mbits/s that transition at the rising edge of the clock ([10368 $\times$ 4] = 41472 bits per STS-192/STM-64 SONET/SDH frame).

The byte ordering of the individual STS-1s or STS-1 components of an STS-Nc that comprise the STS-192 and the details of the STS-192 to STS-48 demultiplexing can be found in *GR-253-CORE* Section 5-1, *Network Element Architectural Features (Multiplexing Procedure)*, page 5-1. The TOAC channels output/accept the nibble data in STS-48/STM-16 byte ordering independent of the full drop/insert mode. Therefore, in STS-192/STM-64 mode, four TOAC channels are needed to drop/insert the entire transport overhead bytes. A byte is inserted into the transmit data stream through an external input that is sampled per clock cycle. If the signal is active (high) during the MSB/MSN (most significant bit/nibble), the byte is inserted into the transmitted overhead stream.

32.3.2 Partial TOAC Insert/Drop Mode

First STS-1/STM-0 (J0, E1, D1—D3, D4—D12, S1, E2, including the M1 byte accessible):

- TOAC clock output at 1.728 MHz (in 10 Gbits/s mode, only RTOAC_CLKO_4, RTOAC_SYNCO_4, and RTOAC_DATAO_4 are used).
- TOAC sync output at 8 kHz coincide with the MSN (most significant nibble) of the first A1 nibble.
- TOAC data enable input (Tx only) active during the MSN (most significant nibble) of each byte to be inserted into the output stream.
- TOAC data bus (transmit insert input/receive drop output):
  — One bit/stream at 1.728 Mbits/s that transitions at the rising edge of the clock (216 bits per STS-192/STM-64 or STS-48/STM-16 frame).

32 Receive TOAC Drop/Transmit TOAC Insert (continued)

32.3 TOAC Modes (continued)

Table 132 summarizes the frame format in the STS-1/STM-0 mode. Data is transmitted from left to right, then top to bottom with A1 bit 7 being the first bit to be transmitted/received.

Table 132. TOAC Insert/Drop Frame Format—STS-1/STM-0 Mode

Row		Column Numbers		
		1	2	3
Section/RS	1	A1	A2	J0
	2	B1	E1	F1
	3	D1	D2	D3
Line/MS	4	H1	H2	H3
	5	B2	K1	K2
	6	D4	D5	D6
	7	D7	D8	D9
	8	D10	D11	D12
	9	S1	M1[1]	E2

1. The Z2 byte is overwritten by the M1 value.

Table 133. Receive Overhead Serial Links Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
TOAC Byte Drop Control	OHP_RX_PROV_S0 (R/W)	RX_TOAC_MODE	4	0×1310

Table 134. Transmit Overhead Serial Links Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Global TOAC Byte Insert Control	OHP_TX_PROV_S0 (R/W)	TX_TOAC_ENB TX_TOAC_MODE	4	0×1370

33 Receive/Transmit Payload Processing

33.1 Receive Payload Processing

In the receive direction, optionally, the payload data of an STS-192c/STS-48c can be monitored with a PRBS analyzer. This PRBS monitor is provided per STS-48 for continuity checking. The pointer value of the receive STS-48c signal must be 522[1]. This allows monitoring without the need for a pointer interpreter. Three different PRBS monitoring sequences are supported: PRBS15, PRBS20, and PRBS23. Additionally, each of the PRBS data received can be programmed to be inverted before monitoring. Monitoring can be done in two modes. In full SPE monitoring, the complete payload as well as POH bytes contains PRBS data. In normal SPE monitoring, only the payload bytes contain the PRBS data; POH bytes and stuff bytes are ignored.

1. The pointer is set by the incoming signal. Only when PRBS data is injected into the SONET frame is the pointer set, by the device, to 522.

33 Receive/Transmit Payload Processing (continued)

33.1 Receive Payload Processing (continued)

Table 135. Receive PRBS Payload Type

Register Bits	Value	Description
RX_PRBS_TYPE	01	PRBS15
	10	PRBS20
	00, 11	PRBS23

Table 136. Receive PRBS Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
PRBS Out-of-Sync Alarm	OHP_RX_NSA_0_ALARM_S0 (W1C)	RX_PRBS_OOS_A	4	0×102C
PRBS Out-of-Sync Alarm Mask	OHP_RX_NSA_0_MASK_S0 (R/W)	RX_PRBS_OOS_M	4	0×1078
PRBS Out-of-Sync State	OHP_RX_NSA_0_STATE_S0 (RO)	RX_PRBS_OOS	4	0×10EC
PRBS Out-of-Sync Persistency	OHP_RX_NSA_0_PERSIST_S0 (RO)	RX_PRBS_OOS_P	4	0×10BC
PRBS Data Inversion Enable	OHP_RX_PROV_S0 (R/W)	RX_PRBS_INV	4	0×1310
PRBS Data Type	OHP_RX_PROV_S0 (R/W)	RX_PRBS_TYPE	4	0×1310
PRBS Mode	OHP_RX_PROV_S0 (R/W)	RX_PRBS_MODE	4	0×1310
PRBS Data Monitoring Enable	OHP_RX_PROV_S0 (R/W)	RX_PRBS_ENB	4	0×1310
PRBS BER Count	OHP_RX_PRBS_BER_S0 (COR)	RX_PRBS_BER_CNT0	4	0×1600

33.2 Transmit Payload Processing

In the transmit direction, optionally, internally generated PRBS data can be inserted as the STS-192c/STS-48c payload. This PRBS generator is provided per STS-48 for continuity checking. Four STS-48 PRBS signals are inserted in an STS-192 signal for 10 Gbits/s mode.

The PRBS generated signal is placed in the STS-192c/STS-48c payload with a fixed pointer value of 522[1]. Three different PRBS generation sequences are supported: PRBS15, PRBS20, and PRBS23. Additionally, each of the PRBS data transmitted can be programmed to be inverted before monitoring. Insertion can be done in two modes. In full SPE insertion, the complete payload as well as POH bytes contains PRBS data. In normal SPE insertion, only the payload bytes contain the PRBS data; POH bytes and the STS-48c/STS-192c stuff bytes are ignored.

Table 137. Transmit PRBS Payload Type

Register Bits	Value	Description
TX_PRBS_TYPE	01	PRBS15
	10	PRBS20
	00, 11	PRBS23

1. The pointer is set by the incoming signal. Only when PRBS data is injected into the SONET frame is the pointer set, by the device, to 522.

33 Receive/Transmit Payload Processing (continued)

33.2 Transmit Payload Processing (continued)

Table 138. Transmit PRBS Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
PRBS Data Inversion Enable	OHP_TX_PROV_S0 (R/W)	TX_PRBS_INV	4	0×1370
PRBS Data Type		TX_PRBS_TYPE	4	0×1370
PRBS Mode		TX_PRBS_MODE	4	0×1370
PRBS Data Insertion Enable		TX_PRBS_ENB	4	0×1370

34 B2 Computing

34.1 Functional Description of B2 Computing

The line BIP-8 is located in each STS-1 of the STS-48 or STS-192 and carries the even parity for the line overhead and SPE data in the previous STS-1 frame. Since the B2 byte is calculated for each STS-1 independent of the other STS-1s, the device mode (STS-48 or STS-192) does not affect the operation of this block. The B2 values in all STS-1s in an STS-48 channel can be fully corrupted (by inverting all the bits) on a per STS-48 basis, using the B2 corrupt enable control bit. The duration of the corruption is defined in frames per second, up to a maximum of 8000 frames (1 second) between rising edges of the performance monitoring clock. The B2 corrupt frame count register specifies this duration.

Table 139. B2 Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
B2 Calculation Disable	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_B2CAL_DIS	4	0×1115
B2 Corrupt Enable	OHP_RX_PROV_S0 (R/W)	RX_B2CORRUPT_ENB	4	0×1310
B2 Corrupt Duration Control	OHP_RX_B2CORRUPT_S0 (R/W)	RX_B2CORRUPT_FRM_CNT	4	0×1320

35 Transpose Multiplexer (TMX)

35.1 Functional Description of the TMX

In STS-192 mode, the bytes in the four STS-48 channels need to be combined and reordered to create an STS-192 data stream. This is performed by the transpose multiplexer (TMX). The byte ordering of the individual STS-1s, or STS-1 components of an STS-Nc, that comprise the STS-48 as it enters the TDMX and after the TDMX (STS-192 byte ordering) and the details of the STS-48 to STS-192 multiplexing can be found in *GR-253-CORE* Section 5-1, *Network Element Architectural Features (Multiplexing Procedure)*, page 5-1. If the device is in STS-48 mode, the data is received on all four channels and the TMX is bypassed.

The module receives individual STS-48 bytes every clock period from each STS-48 and will output 16 bytes on the STS-192. Because SONET interleaving causes each STS-48 bandwidth to be multiplexed into an STS-192 16 bytes at a time, each STS-48 must have 16 bytes stored and then output every fourth clock on the 16-byte wide STS-192 output. That is, each STS-48 must source all 16 bytes in the STS-192 word once every four clocks.

Table 140. Transpose Multiplexer Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Transpose Multiplexer Disable Control	SONFEC_RX_TP_BYPASS (R/W)	RX_TMX_DIS	1	0×1112

36 Scrambler

36.1 Functional Description of the Scrambler in the Transpose Multiplexer

The data stream is optionally scrambled using the standard generator polynomial $1 + x^6 + x^7$. The scrambling can be disabled by the corresponding scrambler disable bit of the LTE channel N provisioning register.

Table 141. Scrambler Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Scrambler Disable Control	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_SCRM_DIS	4	0×1115
Scrambler Mode Control	SONFEC_RX_MODE (R/W)	RX_SCR_MODE	1	0×1110

37 B1 Computing

37.1 Functional Description of B1 Computing

The section BIP-8 byte is located only in the first STS-1 of the STS-48 or STS-192 and carries the even parity of the scrambled data in the previous STS-192 frame. In every frame, the calculated BIP-8 for the previous frame is inserted in the B1 byte of the current frame prior to scrambling. The B1 value can be fully corrupted (by inverting all bits) on a per-channel basis using the B1 corrupt enable control bit. The duration of the corruption is defined in frames per second, up to a maximum of 8000 frames (1 second) between rising edges of performance monitoring clock. The B1 corrupt frame count register specifies this duration.

Table 142. B1 Computing Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
B1 Calculation Disable	SONFEC_RX_BYPASS_S0 (R/W)	OHP_RX_B1CAL_DIS	4	0×1115
B1 Calculation Mode	SONFEC_RX_MODE (R/W)	RX_B1CALC_MODE	1	0×1110
B1 Corrupt Enable	OHP_RX_PROV_S0 (R/W)	RX_B1CORRUPT_ENB	4	0×1310
B1 Corrupt Duration Control	OHP_RX_B1CORRUPT_S0 (R/W)	RX_B1CORRUPT_FRM_CNT	4	0×131C

38 Microprocessor Interface

38.1 Microprocessor Interface Overview

The TFEC0410G microprocessor interface architecture is configured for glueless interface to the *Motorola* MPC860 and MC68360 microprocessors. The *Intel* microcontrollers 8XC251 and 80C196 and the i960 microprocessor may also be utilized to interface to the TFEC0410G. However, provisions on the board need to be made to (de)multiplex the address and data bus. The state of the MPTYPE_IM input signal indicates to the device whether it interfaces to a *Motorola* microprocessor or an *Intel* microcontroller. Other microprocessors may be used if their timing requirements fit to one of the modes described.

The TFEC0410G has separate 16-bit wide address and data buses. The MPDB_8_16 input distinguishes between an 8-bit or 16-bit wide microprocessor data bus being used. In case of an 8-bit wide microprocessor data bus interface, the eight upper bits of the device data bus ports are not being used and are held 3-state.

The microprocessor interface operates at the frequency of the microprocessor clock (PCLK) input, which should be in the range of 10 MHz to 100 MHz.

Depending on the state of the MPMODE_AS input signal, the interface to the 80960SX microprocessor is synchronous, while the interface to the 8XC251 and 80C196 microcontrollers is asynchronous.

Similarly, with the MPC860 or MC68360 microprocessors being used, the state of the MPMODE_AS input signal determines whether bus transfers are synchronous or asynchronous, respectively. In this case, the microprocessor interface also generates an external processor bus error if an internal data acknowledgment is not received in a predetermined period of time, or on parity errors if the MPPAREN input is enabled.

All internal counters are latched using an external or internal performance monitor (PM) latch pulse that must occur once per second to ensure all internal counters do not saturate.

Persistency alarm registers are used in conjunction with the interrupt alarm registers to indicate whether alarms are persistent.

The TFEC0410G contains 48 general purpose inputs/outputs (GPIOs), which can be used to monitor signals on the board.

38.2 Subblock Address Space Assignment

The 16-bit address space is assigned to the subblocks of the device, as shown in Table 143.

Table 143. Subblock Address Space Assignment

Base Address	Block	Block Name
0x0000	Microprocessor interface/top level.	MPU
0x1000	DWFEC macro.	DWFEC
0x2000	SONFEC macro.	SONFEC
0x3000	Unused.	—

38 Microprocessor Interface (continued)

38.2 Microprocessor Interface Overview (continued)

Table 144. MPU General Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
Version Control	DEV_VER (RO)	DEV_VER	1	0×0
Device Identification 0	DEV_ID0 (RO)	DEV_ID0	1	0×1
Device Identification 1	DEV_ID1 (RO)	DEV_ID1	1	0×2
Device Identification 2	DEV_ID2 (RO)	DEV_ID2	1	0×3
Device Identification 3	DEV_ID3 (RO)	DEV_ID3	1	0×4
Device Identification 4	DEV_ID4 (RO)	DEV_ID4	1	0×5
Scratch	DEV_SCRATCH (R/W)	DEV_SCRATCH	1	0×200

38.3 Microprocessor Interface Modes

Table 145 highlights the four microprocessor modes controlled by the MPTYPE_IM and MPMODE_AS inputs.

Table 145. Microprocessor Configuration Modes

Mode	MPTYPE_IM	MPMODE_AS	Description	Typical Application
MODE 1	1	1	Synchronous interface; handshake using data acknowledge.	MPC860
MODE 2	1	0	Asynchronous interface; handshake using data acknowledge.	MC68360, MC68HC16X
MODE 3	0	1	Synchronous interface; handshake through inserted wait states; asynchronous address latching.	i960 (80960SX)
MODE 4	0	0	Asynchronous interface; handshake through inserted wait states; asynchronous address latching.	80c196, 8XC251

38.4 Microprocessor Interface Pinout Descriptions

The MODE[1—4] specific pin definitions are given in Table 146. Note that the microprocessor interface uses the same set of pins in all modes.

38 Microprocessor Interface (continued)

38.4 Microprocessor Interface Pinout Descriptions (continued)

Table 146. MODE[1—4] Microprocessor Pin Definitions

Configuration	Device Pin Name	Microprocessor Pin Name	Pin Type	Assertion Sense	Function
MODE 1	CS_N	CS	Input	Active-low	Chip select.
	TS_N	TS	Input	Active-low	Transfer start.
	RW_N	R/$\overline{W}$	Input	—	Read/write: RW_N = 1 for read. RW_N = 0 for write.
	ADDRESS	A	Input	—	Address bus.
	DATA	D	I/O	—	Data bus.
	PARITY	DP	I/O	—	Parity bus (odd parity supported only).
	TA_N	TA	Output	Active-low	Transfer acknowledge.
	TEA_N	TEA	Output	Active-low	Transfer error acknowledge.
	INTH_N/ INTL_N	IRQ*	Output	Active-low	Interrupt.
MODE 2	CS_N	CS	Input	Active-low	Chip select.
	TS_N	TS	Input	Active-low	Transfer start.
	RW_N	R/$\overline{W}$	Input	—	Read/write: RW_N = 1 for read. RW_N = 0 for write.
	DS_N	DS	+Input	Active-low	Data strobe.
	ADDRESS	A	Input	—	Address bus.
	DATA	D	I/O	—	Data bus.
	PARITY	PRTY	I/O	—	Parity bus.
	TA_N	DSACK*	Output	Active-low	Transfer acknowledge.
	TEA_N	BERR	Output	Active-low	Bus error.
	INTH_N/ INTL_N	IRQ*	Output	Active-low	Interrupt.
MODE 3	CS_N	—	Input	Active-low	Chip select.
	TS_N	ALE	Input	Active-high	Address latch enable.
	RW_N	W/$\overline{R}$	Input	—	Write/read: RW_N = 0 for read. RW_N = 1 for write.
	DS_N	AS	Input	Active-low	Address strobe.
	ADDRESS	AD	Input	—	Address bus.
	DATA	AD	I/O	—	Data bus.
	TA_N	READY	Output	Active-low	Ready signal.
	INTH_N/ INTL_N	INT*	Output	Active-low	Interrupt.

38 Microprocessor Interface (continued)

38.4 Microprocessor Interface Pinout Descriptions (continued)

Table 146. MODE[1—4] Microprocessor Pin Definitions (continued)

Configuration	Device Pin Name	Microprocessor Pin Name	Pin Type	Assertion Sense	Function
MODE 4	CS_N	CSx	Input	Active-low	Chip select.
	TS_N	ALE	Input	Active-high	Address latch enable.
	RW_N	RD	Input	Active-low	Read enable.
	DS_N	WR	Input	Active-low	Write enable.
	ADDRESS	AD	Input	—	Address bus.
	DATA	AD, D	I/O	—	Data bus.
	TA_N	$\overline{\text{READY}}$, $\overline{\text{WAIT}}$	Output	Active-low	Ready, wait signal.
	INTH_N/ INTL_N	INT*	Output	Active-low	Interrupt.

38.5 Reset Behavior

The microprocessor interface can be reset by driving the pin RST_N active-low. It will take about 5 clock cycles of PCLK after the reset gets negated until the microprocessor interface is fully functional.

The software reset registers (0×300—0×304) can be used to reset parts of the device. Those registers themselves can only be reset by the hardware reset, i.e., by pulling RST_N active low.

After a reset of the MPU macro, the MPU registers within the SONFEC and DWFEC macro are powered down and held in reset. They can be put back to function by enabling the bits DEV_SONFEC_PCLK_PDN and DEV_DWFEC_PCLK_PDN in the DEV_PDN_ICLK register. Note that all previously programmed values in the MPU registers of SONFEC and DWFEC will be lost during powerdown.

Similarly, the clock MUXing control register DEV_CTL_CLKMUX[0:4]_S[0:3] will disable the internal functional clocks upon a reset of the MPU macro. All registers that rely on a functional clock to write or return data will not be accessible before those clocks are enabled. This affects the PRBS counter registers OHP_RX_PRBS_BER_S[0:3] in the SONFEC macro and DW_RX_CNT_PRBS_S[0:3] in the DWFEC macro. An attempt to access those registers in this case will cause the microprocessor interface to get stuck waiting for an internal acknowledge. In mode 1 and mode 2, the interface will time-out itself and generate a processor bus error (see Section 38.7, Transfer Error Acknowledge (Mode 1 and Mode 2 Only), on page 171). In mode 3 and mode 4, the microprocessor interface can be reset from this state by negating and asserting CS_N.

In general, the microprocessor interface will terminate any access after detecting CS_N being negated.

38 Microprocessor Interface (continued)

38.6 Microprocessor Data Bus Width

The microprocessor allows the connection of either an 8-bit or 16-bit wide data bus. The MPDB_8_16 input signal indicates which data bus width is being used. MPDB_8_16 = 0 assumes 8-bit data bus transfers, while MPDB_8_16 = 1 assumes 16-bit data bus transfers. The MPDB_8_16 input is supposed to be a static input.

Since all internal registers of the TFEC0410G are 16 bits wide, an additional holding register is needed to facilitate an 8-bit data transfer. This implies that on an 8-bit data bus, two accesses are necessary to read or write the complete contents of an internal register.

The internal holding register is 8 bits wide and resides at the address location 0x500. It is connected to the upper byte of the internal data bus that connects to the registers.

To write an internal register, a first access needs to write the upper byte of the 16-bit data to the holding register. During a second write, the lower byte of the data together with the contents of the holding register gets written to the address location specified.

Similarly, in read mode, the upper byte of the register that was specified by the address gets loaded in the holding register, while the lower byte is visible on the external data bus. During a second read access, the upper byte can be made available on the data bus by reading the holding register.

Table 147. Hold Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
8-Bit Mode Hold Register	DEV_HOLD (R/W)	DEV_HOLD	1	0×500

38.7 Transfer Error Acknowledge (Mode 1 and Mode 2 Only)

The TFEC0410G contains a bus time-out counter. It will terminate the device access if an internal data acknowledgment is not received within 32 PCLK periods, in case of an access to an undefined address region. This interval is used since all valid internal accesses to the device will be completed in significantly less than 32 PCLK periods. The transfer error acknowledge output TEA_N will be driven low in the event of a bus time-out. This feature must be considered with respect to the external processor’s ability to generate its own bus time-out.

The output pin TEA_N is asserted in conjunction with TA_N, if the calculated parity value does not match the parity generated by the external microprocessor on a data transfer and the input MPPAREN is driven high. The device only supports odd parity.

38 Microprocessor Interface (continued)

38.8 Interrupt Structure

The interrupt structure of the TFEC0410G is designed to minimize the effort for software/firmware to isolate the interrupt source. The interrupt structure is comprised of different registers, depending on the consolidation level. At the lowest level (source level), there are the three following registers:

- Alarm register (AR), typically of the write-1-clear (W1C) type.
- Interrupt mask (IM) register of the read/write (R/W) type.
- Persistency alarm (PA) register of the read-only (RO) type.

An alarm register latches a raw status alarm. This latched alarm may contribute to an interrupt if its corresponding interrupt mask bit is enabled. Individual latched alarms are consolidated into an interrupt status register (ISR). If any of the latched alarms that are consolidated into a bit of an ISR are set and unmasked, the ISR bit is set. The ISR bit may contribute to an interrupt if its corresponding interrupt mask bit is disabled. ISRs may be consolidated into a higher-level ISR in a similar fashion until all alarms are consolidated into the chip-level ISR. The alarm register that causes an interrupt can be determined by traversing the tree of ISRs, starting at the chip-level ISR, until the source alarm is found. The raw nonregistered interrupt source can also be accessed through an address in the address map where applicable.

At the chip level, all high-priority interrupts, e.g., LOC, are grouped together into one ISR and all lower-level interrupts, e.g., bit error, etc., are grouped into another ISR. There will be two dedicated device outputs, one for high-priority interrupts and one for low-priority interrupts. In the case that the microprocessor supports only one interrupt input, the low-priority ISR can be mapped into one maskable bit of the high-priority ISR and will be observable on that output pin.

Note: Interrupts are masked when the corresponding bit in the mask register is 0. If the mask register bit is 1, the interrupt is enabled.

38.9 Interrupt Alarm and Interrupt Persistency Registers

An alarm is persistent if it has been asserted continuously (i.e., the alarm has not been negated from the time it was asserted to the time it was read by software). An alarm is not persistent if it is negated one or more times from the point at which it was asserted to the point at which it was read by software.

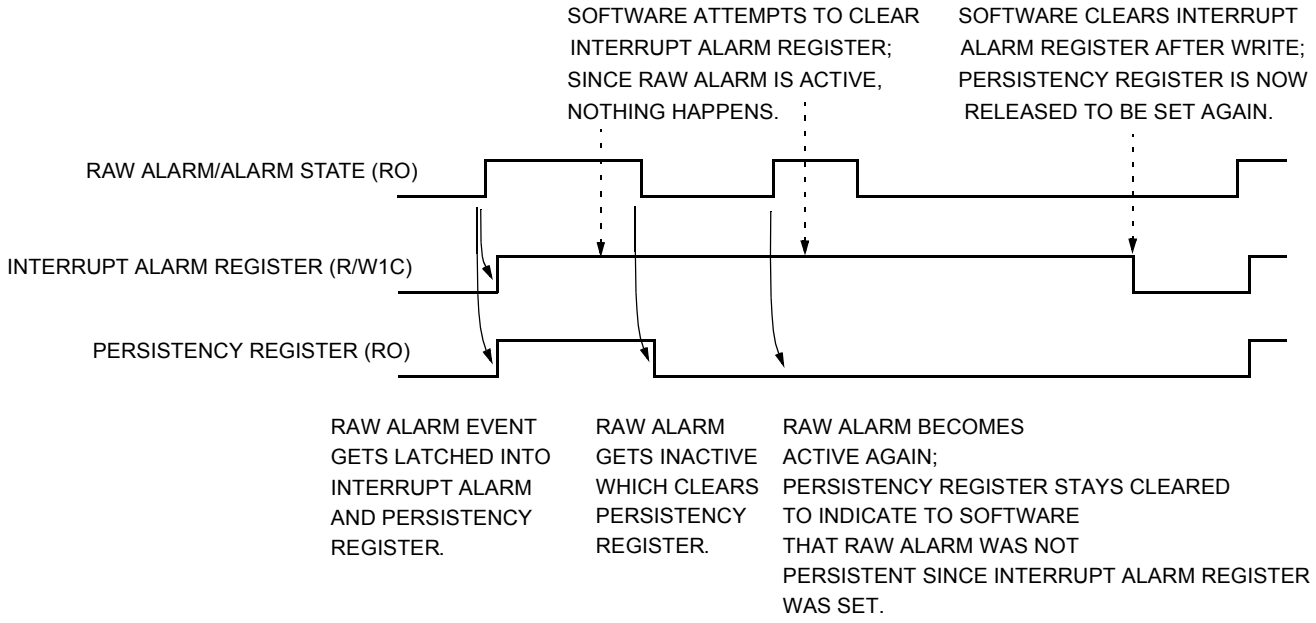
The persistency register monitors the state of an alarm point, and indicates to software whether the alarm is persistent. The following timing diagram (Figure 54) indicates the operation of the persistency register relative to the raw status alarm, and its corresponding interrupt alarm register. It also describes the software interaction with respect to its attempt to clear the alarm and its interpretation.

At the rising edge of the raw alarm point, the corresponding interrupt alarm and persistency alarm register are set. The falling edge of the raw alarm causes the persistency alarm register to be reset (cleared). Any subsequent assertion of the raw alarm does not cause the persistency alarm register to be asserted. It remains reset until the interrupt alarm register is cleared (after the raw alarm is negated and the interrupt alarm register is cleared). Once the interrupt alarm register is cleared, its corresponding persistency alarm register reset is released. The persistency register is now able to be set on the next assertion of the raw alarm point.

Note: For the raw alarm to be reliably latched by PCLK, it needs to be stable for at least 10 clock cycles of a 78 MHz/83 MHz internal clock.

38 Microprocessor Interface (continued)

38.9 Interrupt Alarm and Interrupt Persistency Registers (continued)



Note: All above registers can be read at any time by software to have the interrupt status evaluated without any impact to their state.

Figure 54. Persistency Register Operation

38.10 Performance Monitor (PM) Clock

The PM_CLK signal is sent to all blocks for performance monitoring (collecting statistics). PM_CLK can come from an external pin, an internal 1 s timer, or be controlled by software, depending on the PM mode DEV_PMMODE[1:0] bits.

The external PM_CLK pin is a bidirectional signal controlled by the DEV_PMCLK_IOCTL bit. This bit defaults to 0, making the pin an input.

Table 148. PMCLK Configuration and Interrupt Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
PMCLK Configuration	DEV_PMCLK_CFG (R/W)	DEV_PMMODE	1	0×100
PMCLK Configuration	DEV_PMCLK_CFG (R/W)	DEV_PMCLK_IOCTL	1	0×100
PM Counter Preload Value	DEV_PMCLK_PRELD (R/W)	DEV_PMCLK_PRELD	1	0×101
Software Reset for MPU Registers	DEV_MPUREG_SWRST (R/W)	DEV_PM_TRIG_SWRST	1	0×300
PMCLK Interrupt Alarm	DEV_PMCLK_ALARM (W1C)	DEV_PMCLK_A	1	0×1B
PMCLK Interrupt Alarm Mask	DEV_PMCLK_MASK (R/W)	DEV_PMCLK_M	1	0×4A

38 Microprocessor Interface (continued)

38.10 Performance Monitor (PM) Clock (continued)

Table 149. PMCLK Counter Register Summary

Function	Register Name	Qty.	1st Addr (hex)
Receive Performance Monitoring Register [4:0]	OHP_RX_PM	4	0×132C
Receive REI-L Performance Monitoring [20:16]	OHP_RX_REI_U_PM	4	0×1338
Receive REI-L Performance Monitoring [15:0]	OHP_RX_REI_L_PM	4	0×1339
Receive CV-L Performance Monitoring [23:16]	OHP_RX_POST_CVL_U_PM	4	0×1341
Receive CV-L Performance Monitoring [15:0]	OHP_RX_POST_CVL_L_PM	4	0×1342
Receive CV-L Performance Monitoring [23:16]	OHP_RX_PRE_CVL_U_PM	4	0×134A
Receive CV-L Performance Monitoring [15:0]	OHP_RX_PRE_CVL_L_PM	4	0×134B
Receive CV-S Performance Monitoring [15:0]	OHP_RX_CVS_PM	4	0×1353
Transmit PM Register [4:0]	OHP_TX_PM	4	0×1394
Transmit CV-L Performance Monitoring [23:16]	OHP_TX_CVL_U_PM	4	0×139C
Transmit CV-L Performance Monitoring [15:0]	OHP_TX_CVL_L_PM	4	0×139D
Transmit CV-S Performance Monitoring [15:0]	OHP_TX_CVS_PM	4	0×13A5
DW BIP-0 Counter [26:16]	DW_RX_CNT_BIP00	4	0×2328
DW BIP-0 Counter [15:0]	DW_RX_CNT_BIP01	4	0×2329
DW BIP-1 Counter [26:16]	DW_RX_CNT_BIP10	4	0×2331
DW BIP-1 Counter [15:0]	DW_RX_CNT_BIP11	4	0×2332
DW BEI-0 Counter [26:16]	DW_RX_CNT_BEI00	4	0×233A
DW BEI-0 Counter [15:0]	DW_RX_CNT_BEI01	4	0×233B
DW BEI-1 Counter [26:16]	DW_RX_CNT_BEI10	4	0×2343
DW BEI-1 Counter [15:0]	DW_RX_CNT_BEI11	4	0×2344

38.11 General Purpose Input/Output (GPIO)

The programmable I/O general purpose input/output (GPIO) consists of 48 device pins that can be used for internal or external signal observation. These pins can be configured to be either inputs or outputs, depending on the DEV_GPIO_CFG[47:0] bits. These pins are useful for board designers who need the ability to monitor or control signals on their boards.

If a GPIO pin is configured for input, it can be programmed to generate either a level-sensitive interrupt, a positive edge detect interrupt, a negative edge detect interrupt, or both edges detect interrupt contributing to the composite external interrupt. The raw value on this pin can be read from the DEV_GPI_STATE[47:0] bits. The interrupt alarm register is DEV_GPI_ALARM and the corresponding mask and persistency registers are DEV_GPI_MASK and DEV_GPI_PERSIST, respectively.

If a GPIO pin is configured for output, different internal signals can be monitored depending on the four select bits for that pin in the DEV_GPO_SEL[0—3] registers. Note that only the lower 16 GPIO pins can be used to monitor internal signals, while the other GPIO pins are connected to an internal register permanently.

Select Bits = 0000: The value provisioned in the DEV_GPO_VAL[47:0] bits will appear on the device pin immediately.

38 Microprocessor Interface (continued)

38.11 General Purpose Input/Output (GPIO) (continued)

Select Bits = 0001: The value of an alarm status signal will be visible at the pin according to the assignment in Table 150. Note that pins 16—47 are undefined in this case.

Table 150. GPIO Pin Assignment when Select Bits = 0001

GPIO Pin	Internal Signal
15	Slice 3, SONFEC Tx composite alarm.
14	Slice 2, SONFEC Tx composite alarm.
13	Slice 1, SONFEC Tx composite alarm.
12	Slice 0, SONFEC Tx composite alarm.
11	Slice 3, DWFEC Tx composite alarm.
10	Slice 2, DWFEC Tx composite alarm.
9	Slice 1, DWFEC Tx composite alarm.
8	Slice 0, DWFEC Tx composite alarms.
7	Slice 3, SONFEC Rx composite alarm.
6	Slice 2, SONFEC Rx composite alarm.
5	Slice 1, SONFEC Rx composite alarm.
4	Slice 0, SONFEC Rx composite alarm.
3	Slice 3, DWFEC Rx composite alarm.
2	Slice 2, DWFEC Rx composite alarm.
1	Slice 1, DWFEC Rx composite alarm.
0	Slice 0, DWFEC Rx composite alarms.

Select Bits = 0010: The value of the transmit and receive phase detector reference and variable signals will be visible at the pin according to the assignment in Table 151. Note that pins 16—47 are undefined in this case.

Table 151. GPIO Pin Assignment when Select Bits = 0010

GPIO Pin	Internal Signal
15	Slice 3—Phase detector Tx variable signal (44.434 MHz).
14	Slice 2—Phase detector Tx variable signal (44.434 MHz).
13	Slice 1—Phase detector Tx variable signal (44.434 MHz).
12	Slice 0—Phase detector Tx variable signal (44.434 MHz).
11	Slice 3—Phase detector Tx reference signal (44.434 MHz).
10	Slice 2—Phase detector Tx reference signal (44.434 MHz).
9	Slice 1—Phase detector Tx reference signal (44.434 MHz).
8	Slice 0—Phase detector Tx reference signal (44.434 MHz).
7	Slice 3—Phase detector Rx variable signal (44.434 MHz).
6	Slice 2—Phase detector Rx variable signal (44.434 MHz).
5	Slice 1—Phase detector Rx variable signal (44.434 MHz).
4	Slice 0—Phase detector Rx variable signal (44.434 MHz).
3	Slice 3—Phase detector Rx reference signal (44.434 MHz).
2	Slice 2—Phase detector Rx reference signal (44.434 MHz).
1	Slice 1—Phase detector Rx reference signal (44.434 MHz).
0	Slice 0—Phase detector Rx reference signal (44.434 MHz).

38 Microprocessor Interface (continued)

38.11 General Purpose Input/Output (GPIO) (continued)

Select Bits = 0011: The value of an alarm status signal will be visible at the pin according to the assignment in Table 152. Note that pins 16—47 are undefined in this case.

Table 152. GPIO Pin Assignment when Select Bits = 0011

GPIO Pin	Internal Signal
15	Logic 0.
14	Logic 0.
13	Logic 0.
12	Logic 0.
11	Logic 0.
10	Logic 0.
9	Logic 0.
8	Logic 0.
7	Slice 3—SONFEC Tx free-running 8 kHz signal.
6	Slice 2—SONFEC Tx free-running 8 kHz signal.
5	Slice 1—SONFEC Tx free-running 8 kHz signal.
4	Slice 0—SONFEC Tx free-running 8 kHz signal.
3	Slice 3—DWFEC Tx free-running 8 kHz signal.
2	Slice 2—DWFEC Tx free-running 8 kHz signal.
1	Slice 1—DWFEC Tx free-running 8 kHz signal.
0	Slice 0—DWFEC Tx free-running 8 kHz signal.

Select Bits = Others: Logic 0.

38 Microprocessor Interface (continued)

38.11 General Purpose Input/Output (GPIO) (continued)

Table 153. GPIO Register Summary

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
GPIO Configuration 0 (for GPI pins 47:32)	DEV_GPI_CFG0 (R/W)	DEV_GPIO_DIR0	1	0×120
GPIO Configuration 1 (for GPI pins 31:16)	DEV_GPI_CFG1 (R/W)	DEV_GPIO_DIR1	1	0×121
GPIO Configuration 2 (for GPI pins 15:0)	DEV_GPI_CFG2 (R/W)	DEV_GPIO_DIR2	1	0×122
GPI Interrupt Polarity Configuration 0 (for GPI pins 47:32)	DEV_GPI_INT_POL0 (R/W)	DEV_GPI_INT_POL0	1	0×123
GPI Interrupt Polarity Configuration 1 (for GPI pins 31:16)	DEV_GPI_INT_POL1 (R/W)	DEV_GPI_INT_POL1	1	0×124
GPI Interrupt Polarity Configuration 2 (for GPI pins 15:0)	DEV_GPI_INT_POL2 (R/W)	DEV_GPI_INT_POL2	1	0×125
GPI Interrupt Type Configuration 0 (for GPI pins 7:0)	DEV_GPI_INT_TYP0 (R/W)	DEV_GPI[7:0]_INT_TYP[1:0]	1	0×126
GPI Interrupt Type Configuration 1 (for GPI pins 15:8)	DEV_GPI_INT_TYP1 (R/W)	DEV_GPI[15:8]_INT_TYP[1:0]	1	0×127
GPI Interrupt Type Configuration 2 (for GPI pins 23:16)	DEV_GPI_INT_TYP2 (R/W)	DEV_GPI[23:16]_INT_TYP[1:0]	1	0×128
GPI Interrupt Type Configuration 3 (for GPI pins 31:24)	DEV_GPI_INT_TYP3 (R/W)	DEV_GPI[31:24]_INT_TYP[1:0]	1	0×129
GPI Interrupt Type Configuration 4 (for GPI pins 39:32)	DEV_GPI_INT_TYP4 (R/W)	DEV_GPI[39:32]_INT_TYP[1:0]	1	0×12A
GPI Interrupt Type Configuration 5 (for GPI pins 47:40)	DEV_GPI_INT_TYP5 (R/W)	DEV_GPI[47:40]_INT_TYP[1:0]	1	0×12B
GPO Output Value 0 (for GPO pins 47:32)	DEV_GPO_VAL0 (R/W)	DEV_GPO_VAL0	1	0×12C
GPO Output Value 1 (for GPO pins 31:16)	DEV_GPO_VAL1 (R/W)	DEV_GPO_VAL1	1	0×12D
GPO Output Value 2 (for GPO pins 15:0)	DEV_GPO_VAL2 (R/W)	DEV_GPO_VAL2	1	0×12E
GPO Selection 0 (for GPO pins 3:0)	DEV_GPO_SEL0 (R/W)	DEV_GPO[3:0]_SEL[3:0]	1	0×12F
GPO Selection 1 (for GPO pins 7:4)	DEV_GPO_SEL1 (R/W)	DEV_GPO[7:4]_SEL[3:0]	1	0×130

38 Microprocessor Interface (continued)

38.11 General Purpose Input/Output (GPIO) (continued)

Table 153. GPIO Register Summary (continued)

Function	Register Name (First Occurrence)	Register Bits	Qty.	1st Addr (hex)
GPO Selection 2 (for GPO pins 11:8)	DEV_GPO_SEL2 (R/W)	DEV_GPO[11:8]_SEL[3:0]	1	0×131
GPO Selection 3 (for GPO pins 15:12)	DEV_GPO_SEL3 (R/W)	DEV_GPO[15:12]_SEL[3:0]	1	0×132
GPI Interrupt Alarm 0 (for GPI pins 47:32)	DEV_GPI_ALARM0 (W1C)	DEV_GPI_A0	1	0×18
GPI Interrupt Alarm 1 (for GPI pins 31:16)	DEV_GPI_ALARM1 (W1C)	DEV_GPI_A1	1	0×19
GPI Interrupt Alarm 2 (for GPI pins 15:0)	DEV_GPI_ALARM2 (W1C)	DEV_GPI_A2	1	0×1A
GPI Interrupt Mask 0 (for GPI pins 47:32)	DEV_GPI_MASK0 (R/W)	DEV_GPI_M0	1	0×47
GPI Interrupt Mask 1 (for GPI pins 31:16)	DEV_GPI_MASK1 (R/W)	DEV_GPI_M1	1	0×48
GPI Interrupt Mask 2 (for GPI pins 15:0)	DEV_GPI_MASK2 (R/W)	DEV_GPI_M2	1	0×49
GPI Interrupt Persistency 0 (for GPI pins 47:32)	DEV_GPI_PERSIST0 (RO)	DEV_GPI_P0	1	0×74
GPI Interrupt Persistency 1 (for GPI pins 31:16)	DEV_GPI_PERSIST1 (RO)	DEV_GPI_P1	1	0×75
GPI Interrupt Persistency 2 (for GPI pins 15:0)	DEV_GPI_PERSIST2 (RO)	DEV_GPI_P2	1	0×76
GPI Interrupt Raw State 0 (for GPI pins 47:32)	DEV_GPI_STATE0 (RO)	DEV_GPI0	1	0×94
GPI Interrupt Raw State 1 (for GPI pins 31:16)	DEV_GPI_STATE1 (RO)	DEV_GPI1	1	0×95
GPI Interrupt Raw State 2 (for GPI pins 15:0)	DEV_GPI_STATE2 (RO)	DEV_GPI2	1	0×96

39 TFEC Primary Clock Inputs

The following table lists the possible TFEC modes and the clocks (primary inputs) needed for each mode. The first column (Mode) lists all the commonly used modes of the device. For each of these modes there is a reference (hyperlink) to the figures in the data sheet listed in the second column (Figure Number), if one exists. The receive line clock primary input (RCLKLI 3-2-1-0), as well as the total receive line rate (Rx-Line Bandwidth), are listed in columns 3 and 4, respectively. The same listing is repeated for receive system, transmit line, and transmit system in subsequent columns. In regenerator mode, loopback is on the system side; for weak FEC, this loopback could be before or after the elastic store on the system side. Only commonly used modes are listed below. The bidirectional mode does **not** use the elastic store in DWFEC. Abbreviations used are listed below:

Strong: Strong FEC **only**, can be FEC or digital wrapper mode.
Weak: Weak FEC **only**.
x: Clock input need **not** be present.
p: Clock input needs to be present.

Table 154. TFEC Clock Setup

Mode	Figure Number	RCLKLI 3-2-1-0	Rx-Line Bandwidth	RCLKSI 3-2-1-0	Rx-System Bandwidth	TCLKLI 3-2-1-0	Tx-Line Bandwidth	TCLKSI 3-2-1-0	Tx-System Bandwidth
Terminal [Rx/Tx Symmetric; 16 Bits at 622 MHz/666 MHz]									
Strong 10 Gbits/s	**12/14**	x-x-x-p	1 x 10.666	x-x-x-p	1 x 09.953	x-x-x-p	1 x 10.666	x-x-x-p	1 x 9.953
Strong 2.5 Gbits/s	**12/14**	p-p-p-p	4 x 2.666	p-p-p-p	4 x 2.488	p-p-p-p	4 x 2.666	p-p-p-p	4 x 2.488
Strong Bidirectional 10 Gbits/s	**16**	x-x-x-p	1 x 10.666	—	1 x 10.666	—	1 x 10.666	x-x-x-p	1 x 10.666
Strong Bidirectional 2.5 Gbits/s	**16**	p-p-p-p	4 x 2.666	—	4 x 2.666	—	4 x 2.666	p-p-p-p	4 x 2.666
Weak 10 Gbits/s	**17**	x-x-x-p	1 x 9.953	—	1 x 9.953	—	1 x 9.953	x-x-x-p	1 x 9.953
Weak 2.5 Gbits/s	**17**	p-p-p-p	4 x 2.488	—	4 x 2.488	—	4 x 2.488	p-p-p-p	4 x 2.488
Strong and Weak 10 Gbits/s	**19/21**	x-x-x-p	1 x 10.666	x-x-x-p	1 x 9.953	x-x-x-p	1 x 10.666	x-x-x-p	1 x 9.953
Strong and Weak 2.5 Gbits/s	**19/21**	p-p-p-p	4 x 2.666	p-p-p-p	4 x 2.488	p-p-p-p	4 x 2.666	p-p-p-p	4 x 2.488
Regenerator [Rx/Tx Symmetric, Internal Loopback on the System; 16 Bits at 622 MHz/666 MHz]									
Strong 10 Gbits/s	**13/15**	x-x-x-p	1 x 10.666	x-x-x-p	—	—	1 x 10.666	—	—
Strong 2.5 Gbits/s	**13/15**	p-p-p-p	4 x 2.666	p-p-p-p	—	—	4 x 2.666	—	—
Strong Bidirectional 10 Gbits/s	**—**	x-x-x-p	1 x 10.666	—	—	—	1 x 10.666	—	—
Strong Bidirectional 2.5 Gbits/s	**—**	p-p-p-p	4 x 2.666	—	—	—	4 x 2.666	—	—
Weak 10 Gbits/s before LB ES	**18**	x-x-x-p	1 x 9.953	—	—	—	1 x 9.953	—	—
Weak 2.5 Gbits/s before LB ES	**18**	p-p-p-p	4 x 2.488	—	—	—	4 x 2.488	—	—
Strong and Weak 10 Gbits/s	**20**	x-x-x-p	1 x 10.666	x-x-x-p	—	—	1 x 9.953	—	—
Strong and Weak 2.5 Gbits/s	**20**	p-p-p-p	4 x 2.666	p-p-p-p	—	—	4 x 2.488	—	—
Multiplex Mode Terminal [Weak FEC Only, 2.5 Gbits/s to 10 Gbits/s/10 Gbits/s to 2.5 Gbits/s; 16 Bits at 622 MHz/666 MHz]									
10GLine_2G5System	**22**	x-x-x-p	1 x 9.953	—	4 x 2.488	—	1 x 9.953	x-x-x-p	4 x 2.488
Strong 10GLine_2G5System	**22**	x-x-x-p	1 x 10.666	x-x-x-p	4 x 2.488	x-x-x-p	1 x 10.666	x-x-x-p	4 x 2.488
Single 2.5 Gbits/s Terminal [16 Bits at 155 MHz/166 MHz]									
Strong 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.666	x-x-x-p	1 x 2.488	x-x-x-p	1 x 2.666	x-x-x-p	1 x 2.488
Strong Bidirectional 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.666	—	1 x 2.666	—	1 x 2.666	x-x-x-p	1 x 2.666
Weak 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.488	—	1 x 2.488	—	1 x 2.488	x-x-x-p	1 x 2.488
Strong and Weak 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.666	x-x-x-p	1 x 2.488	x-x-x-p	1 x 2.666	x-x-x-p	1 x 2.488
Single 2.5 Gbits/s Regenerator [16 Bits at 155 MHz/166 MHz]									
Strong 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.666	x-x-x-p	—	—	1 x 2.666	—	—
Strong Bidirectional 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.666	—	—	—	1 x 2.666	—	—
Weak 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.488	—	—	—	1 x 2.488	—	—
Strong and Weak 2.5 Gbits/s	**23**	x-x-x-p	1 x 2.666	x-x-x-p	—	—	1 x 2.666	—	—

40 TFEC Clock Multiplexers

The clock multiplexers listed below refer to Figure 24 on page 30. The values shown below are those for DEV_CTL_CLKMUXn_Sm. When programming the clock multiplexer registers, the clock inversion control bit should be set to 0x0 (no inversion) under all conditions.

40.1 Clock Multiplexers and Register Bits Selection

- Clock MUX A: DEV_CTL_CLKMUX0_Sn [10:8]
- Clock MUX B: DEV_CTL_CLKMUX4_Sn [02:0]
- Clock MUX C: DEV_CTL_CLKMUX0_Sn [02:0]
- Clock MUX D: DEV_CTL_CLKMUX1_Sn [10:8]
- Clock MUX E: DEV_CTL_CLKMUX1_Sn [02:0]
- Clock MUX F: DEV_CTL_CLKMUX2_Sn [10:8]
- Clock MUX G: DEV_CTL_CLKMUX2_Sn [02:0]
- Clock MUX H: DEV_CTL_CLKMUX3_Sn [10:8]
- Clock MUX I: DEV_CTL_CLKMUX4_Sn [10:8]
- Clock MUX J: DEV_CTL_CLKMUX3_Sn [02:0]

40.2 Clock Selection

- 0x00: Ground
- 0x01: Transmit System Clock
- 0x02: Receive System Clock
- 0x03: Transmit Line Clock
- 0x04: Receive Line Clock

40 TFEC Clock Multiplexers (continued)

40.2 Clock Selection (continued)

Table 155. TFEC Clock Multiplexers Programming

Mode	Figure Number	A[1]	B	C	D	E	F	G	H	I	J[1]
Terminal [Rx/Tx Symmetric; 16 Bits at 622 MHz/666 MHz]											
Strong 10 Gbits/s	12/14	0x03	0x03	0x03	0x01	0x00	0x04	0x02	0x00	0x02	0x02
Strong 2.5 Gbits/s	12/14	0x03	0x03	0x03	0x01	0x00	0x04	0x02	0x00	0x02	0x02
Strong Bidirectional 10 Gbits/s	16	0x01	0x01	0x01	0x01	0x00	0x04	0x00	0x00	0x04	0x04
Strong Bidirectional 2.5 Gbits/s	16	0x01	0x01	0x01	0x01	0x00	0x04	0x00	0x00	0x04	0x04
Weak 10 Gbits/s	17	0x01	0x01	0x00	0x00	0x01	0x00	0x00	0x04	0x04	0x04
Weak 2.5 Gbits/s	17	0x01	0x01	0x00	0x00	0x01	0x00	0x00	0x04	0x04	0x04
Strong and Weak 10 Gbits/s	19/21	0x03	0x03	0x03	0x01	0x01	0x04	0x02	0x02	0x02	0x02
Strong and Weak 2.5 Gbits/s	19/21	0x03	0x03	0x03	0x01	0x01	0x04	0x02	0x02	0x02	0x02
Regenerator [Rx/Tx Symmetric, Internal Loopback on the System; 16 Bits at 622 MHz/666 MHz]											
Strong 10 Gbits/s	13/15	0x04	0x04	0x04	0x02	0x00	0x04	0x02	0x00	0x00	0x00
Strong 2.5 Gbits/s	13/15	0x04	0x04	0x04	0x02	0x00	0x04	0x02	0x00	0x00	0x00
Strong Bidirectional 10 Gbits/s	—	0x04	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x00	0x00
Strong Bidirectional 2.5 Gbits/s	—	0x04	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x00	0x00
Weak 10 Gbits/s	18	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x04	0x00	0x00
Weak 2.5 Gbits/s	18	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x04	0x00	0x00
Strong and Weak 10 Gbits/s before LB ES	20	0x04	0x04	0x04	0x02	0x02	0x04	0x02	0x02	0x00	0x00
Strong and Weak 2.5 Gbits/s before LB ES	20	0x04	0x04	0x04	0x02	0x02	0x04	0x02	0x02	0x00	0x00
Multiplex Mode Terminal [Weak FEC Only, 2.5 Gbits/s To 10 Gbits/s/10 Gbits/s To 2.5 Gbits/s; 16 Bits at 622 MHz/666 MHz]											
10GLine_2G5System	22	0x01	0x01	0x00	0x00	0x01	0x00	0x00	0x04	0x04	0x04
Strong 10GLine_2G5System	22	0x03	0x03	0x03	0x01	0x01	0x04	0x02	0x02	0x02	0x02
Single 2.5 Gbits/s Terminal [16 Bits at 155 MHz/166 MHz]											
Strong 2.5 Gbits/s	23	0x03	0x03	0x03	0x01	0x00	0x04	0x02	0x00	0x02	0x02
Strong Bidirectional 2.5 Gbits/s	23	0x01	0x01	0x01	0x01	0x00	0x04	0x00	0x00	0x04	0x04
Weak 2.5 Gbits/s	23	0x01	0x01	0x00	0x00	0x01	0x00	0x00	0x04	0x04	0x04
Strong and Weak 2.5 Gbits/s	23	0x03	0x03	0x03	0x01	0x01	0x04	0x02	0x02	0x02	0x02
Single 2.5 Gbits/s Regenerator [16 Bits at 155 MHz/166 MHz]											
Strong 2.5 Gbits/s	23	0x04	0x04	0x04	0x02	0x00	0x04	0x02	0x00	0x00	0x00
Strong Bidirectional 2.5 Gbits/s	23	0x04	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x00	0x00
Weak 2.5 Gbits/s	23	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x04	0x00	0x00
Strong and Weak 2.5 Gbits/s	23	0x04	0x04	0x04	0x02	0x02	0x04	0x02	0x02	0x00	0x00

1. For clock multiplexers A and J, in 10 Gbits/s mode, only slice 0 needs to be programmed.

41 TFEC Data Multiplexers

The data multiplexers listed below refers to Figure 24 on page 30. The values shown below are those for DEV_CTL_DMUX_Sm.

41.1 Data Multiplexers and Register Bits Selection

- Data MUX K: DEV_CTL_DMUX_Sn [5:4]
- Data MUX L: DEV_CTL_DMUX_Sn [7:6]
- Data MUX M: DEV_CTL_DMUX_Sn [8]
- Data MUX N: DEV_CTL_DMUX_Sn [3]
- Data MUX O: DEV_CTL_DMUX_Sn [2]
- Data MUX P: DEV_CTL_DMUX_Sn [1:0]

Table 156. TFEC Data Multiplexer Programming

A value of 0xXX indicates a do not care condition. It could be set to 0x00.

Mode	Figure Number	K	L	M	N	O	P
Terminal [Rx/Tx Symmetric, 16 Bits at 622 MHz/666 MHz]							
Strong 10 Gbits/s	12/14	0x00	0x01	0xXX	0xXX	0x00	0x01
Strong 2.5 Gbits/s	12/14	0x00	0x01	0xXX	0xXX	0x00	0x01
Strong Bidirectional 10 Gbits/s	16	0x00	0x01	0xXX	0xXX	0x01	0x01
Strong Bidirectional 2.5 Gbits/s	16	0x00	0x01	0xXX	0xXX	0x01	0x01
Weak 10 Gbits/s	17	0x01	0xXX	0x00	0x01	0xXX	0x00
Weak 2.5 Gbits/s	17	0x01	0xXX	0x00	0x01	0xXX	0x00
Strong and Weak 10 Gbits/s	19/21	0x00	0x00	0x00	0x00	0xXX	0x00
Strong and Weak 2.5 Gbits/s	19/21	0x00	0x00	0x00	0x00	0xXX	0x00
Regenerator [Rx/Tx Symmetric, Internal Loopback on the System; 16 Bits at 622 MHz/666 MHz]							
Strong 10 Gbits/s[1]	13/15	0x00	0x02	0xXX	0xXX	0xXX	0xXX
Strong 2.5 Gbits/s[1]	13/15	0x00	0x02	0xXX	0xXX	0xXX	0xXX
Strong Bidirectional 10 Gbits/s[2]	—	0x00	0xXX	0xXX	0xXX	0xXX	0xXX
Strong Bidirectional 2.5 Gbits/s[2]	—	0x00	0xXX	0xXX	0xXX	0xXX	0xXX
Weak 10 Gbits/s[3]	18	0x01	0xXX	0xXX	0x01	0xXX	0xXX
Weak 2.5 Gbits/s[3]	18	0x01	0xXX	0xXX	0x01	0xXX	0xXX
Strong and Weak 10 Gbits/s[3]	20	0x00	0x00	0xXX	0x00	0xXX	0xXX
Strong and Weak 2.5 Gbits/s[3]	20	0x00	0x00	0xXX	0x00	0xXX	0xXX

Notes:

1. Loopback assumes at data MUX L.
2. Loopback assumes after DW inside DWFEC.
3. Loopback assumes inside SONFEC.

41 TFEC Data Multiplexers (continued)

Table 156. TFEC Data Multiplexer Programming (continued)

A value of 0xXX indicates a do not care condition. It could be set to 0x00.

Mode	Figure Number	K	L	M	N	O	P
Multiplex Mode Terminal [Weak FEC Only, 2.5 Gbits/s to 10 Gbits/s/10 Gbits/s to 2.5 Gbits/s; 16 Bits at 622 MHz/666 MHz]							
10GLine_2G5System	22	0x01	0xXX	0x00	0x01	0xXX	0x00
Strong 10GLine_2G5System	22	0x00	0x00	0x00	0x00	0xXX	0x00
Single 2.5 Gbits/s Terminal [16 Bits at 155 MHz/166 MHz]							
Strong 2.5 Gbits/s	23	0x00	0x01	0xXX	0xXX	0x00	0x01
Strong Bidirectional 2.5 Gbits/s	23	0x00	0x01	0xXX	0xXX	0x01	0x01
Weak 2.5 Gbits/s	23	0x01	0xXX	0x00	0x01	0xXX	0x00
Strong and Weak 2.5 Gbits/s	23	0x00	0x00	0x00	0x00	0xXX	0x00
Single 2.5 Gbits/s Regenerator [16 Bits at 155 MHz/166 MHz]							
Strong 2.5 Gbits/s[1]	23	0x00	0x02	0xXX	0xXX	0xXX	0xXX
Strong Bidirectional 2.5 Gbits/s[2]	23	0x00	0xXX	0xXX	0xXX	0xXX	0xXX
Weak 2.5 Gbits/s[3]	23	0x01	0xXX	0xXX	0x01	0xXX	0xXX
Strong and Weak 2.5 Gbits/s[3]	23	0x00	0x00	0xXX	0x00	0xXX	0xXX

1. Loopback assumes at data MUX L.
2. Loopback assumes after DW inside DWFEC.
3. Loopback assumes before data MUX M, inside SONFEC.

42 TFEC Phase Detectors

42.1 Clock Division Select

- 0x0: 622 MHz clock, division by 14 or 79.
- 0x1: 666 MHz clock, division by 15 or 85.

42.2 Clock Selection

- 0x00: Ground
- 0x01: Transmit System Clock
- 0x02: Transmit Line Clock
- 0x03: Receive System Clock
- 0x04: Receive Line Clock

42 TFEC Phase Detectors (continued)

42.2 Clock Selection (continued)

Table 157. TFEC Phase Detectors Programming

The polarity of the phase detectors is programmed to no inversion by default.

Mode	Figure Number	RCLKLI	RCLKSI	Receive PD Controls				TCLKLI	TCLKSI	Transmit PD Controls			
				Variable		Reference				Variable		Reference	
				Div	Sel	Div	Sel			Div	Sel	Div	Sel
Terminal [Rx/Tx Symmetric; 16 Bits at 622 MHz/666 MHz]													
Strong 10 Gbits/s	12/14	666 MHz	622 MHz	0x0	0x03	0x1	0x04	666 MHz	622 MHz	0x1	0x02	0x0	0x01
Strong 2.5 Gbits/s	12/14	666 MHz	622 MHz	0x0	0x03	0x1	0x04	666 MHz	622 MHz	0x1	0x02	0x0	0x01
Strong Bidirectional 10 Gbits/s	16	666 MHz	—	—	—	—	—	—	666 MHz	—	—	—	—
Strong Bidirectional 2.5 Gbits/s	16	666 MHz	—	—	—	—	—	—	666 MHz	—	—	—	—
Weak 10 Gbits/s	17	622 MHz	—	—	—	—	—	—	622 MHz	—	—	—	—
Weak 2.5 Gbits/s	17	622 MHz	—	—	—	—	—	—	622 MHz	—	—	—	—
Strong and Weak 10 Gbits/s	19/21	666 MHz	622 MHz	0x0	0x03	0x1	0x04	666 MHz	622 MHz	0x1	0x02	0x0	0x01
Strong and Weak 2.5 Gbits/s	19/21	666 MHz	622 MHz	0x0	0x03	0x1	0x04	666 MHz	622 MHz	0x1	0x02	0x0	0x01
Regenerator [Rx/Tx Symmetric, Internal Loopback on the System; 16 Bits at 622 MHz/666 MHz]													
Strong 10 Gbits/s	13/15	666 MHz	622 MHz	0x0	0x03	0x1	0x04	—	—	—	—	—	—
Strong 2.5 Gbits/s	13/15	666 MHz	622 MHz	0x0	0x03	0x1	0x04	—	—	—	—	—	—
Strong Bidirectional 10 Gbits/s	—	666 MHz	—	—	—	—	—	—	—	—	—	—	—
Strong Bidirectional 2.5 Gbits/s	—	666 MHz	—	—	—	—	—	—	—	—	—	—	—
Weak 10 Gbits/s before LB ES	18	622 MHz	—	—	—	—	—	—	—	—	—	—	—
Weak 2.5 Gbits/s before LB ES	18	622 MHz	—	—	—	—	—	—	—	—	—	—	—
Weak 10 Gbits/s through LB ES	18	622 MHz	—	—	—	—	—	622 MHz	—	0x0	0x02	0x0	0x04
Weak 2.5 Gbits/s through LB ES	18	622 MHz	—	—	—	—	—	622 MHz	—	0x0	0x02	0x0	0x04
Strong and Weak 10 Gbits/s before LB ES	20	666 MHz	622 MHz	0x0	0x03	0x1	0x04	—	—	—	—	—	—
Strong and Weak 2.5 Gbits/s before LB ES	20	666 MHz	622 MHz	0x0	0x03	0x1	0x04	—	—	—	—	—	—
Strong and Weak 10 Gbits/s through LB ES	20	666 MHz	622 MHz	0x0	0x03	0x1	0x04	622 MHz	—	0x0	0x02	0x1	0x04
Strong and Weak 2.5 Gbits/s through LB ES	20	666 MHz	622 MHz	0x0	0x03	0x1	0x04	622 MHz	—	0x0	0x02	0x1	0x04
Multiplex Mode Terminal [Weak FEC Only, 2.5 Gbits/s To 10 Gbits/s/10 Gbits/s To 2.5 Gbits/s; 16 Bits at 622 MHz/666 MHz]													
10GLine_2G5System	22	622 MHz	—	—	—	—	—	—	622 MHz	—	—	—	—
Strong 10GLine_2G5System	22	666 MHz	622 MHz	0x0	0x03	0x1	0x04	666 MHz	622 MHz	0x1	0x02	0x0	0x01
Single 2.5 Gbits/s Terminal [16 Bits at 155 MHz/166 MHz]													
Strong 2.5 Gbits/s	23	166 MHz	155 MHz	0x0	0x03	0x1	0x04	166 MHz	155 MHz	0x1	0x02	0x0	0x01
Strong Bidirectional 2.5 Gbits/s	23	166 MHz	—	—	—	—	—	—	166 MHz	—	—	—	—
Weak 2.5 Gbits/s	23	155 MHz	—	—	—	—	—	—	155 MHz	—	—	—	—
Strong and Weak 2.5 Gbits/s	23	166 MHz	155 MHz	0x0	0x03	0x1	0x04	166 MHz	155 MHz	0x1	0x02	0x0	0x01
Single 2.5 Gbits/s Regenerator [16 Bits at 155 MHz/166 MHz]													
Strong 2.5 Gbits/s	23	166 MHz	155 MHz	0x0	0x03	0x1	0x04	—	—	—	—	—	—
Strong Bidirectional 2.5 Gbits/s	23	166 MHz	—	—	—	—	—	—	—	—	—	—	—
Weak 2.5 Gbits/s before LB ES	23	155 MHz	—	—	—	—	—	—	—	—	—	—	—
Weak 2.5 Gbits/s through LB ES	23	155 MHz	—	—	—	—	—	155 MHz	—	0x0	0x02	0x0	0x04
Strong and Weak 2.5 Gbits/s before LB ES	23	166 MHz	155 MHz	0x0	0x03	0x1	0x04	—	—	—	—	—	—
Strong and Weak 2.5 Gbits/s through LB ES	23	166 MHz	155 MHz	0x0	0x03	0x1	0x04	155 MHz	—	0x0	0x02	0x1	0x04

43 TFEC Loopbacks

The valid loopback configurations of TFEC are listed below. Refer to Figure 24 on page 30. The high-speed interface loopbacks are at 78 MHz or 83 MHz. These loopbacks are essentially loops through the high-speed multiplexer and demultiplexer blocks which could be operated at either of these clock frequencies. In all these modes, if an elastic store is present, any other clock could be used as long as its frequency matches that of the clock on the other side of the elastic store. The settings shown below are to be considered as guidelines only. As an example, it is possible to initiate two loopbacks inside the device, one within DWFEC (RDW2TDW_LB) and another within SONFEC (TLINE2RLINE_LB), simultaneously. Such combinations are not listed in Table 158.

The primary input TFRMLI can only be used if the TCLKLI is present. However, TCLKLI could be used directly or as a substitute for any other clock via RCLKSI if the use of TFRMLI is desired. In 10 Gbits/s mode, only slice 0 of clock multiplexers A and J needs to be programmed.

Table 158. TFEC Loopback Programming

Loopback (Active Signal)	Primary Clocks	Clock Multiplexers								Data Multiplexers					
		A/B	C	D	E	F	G	H	I/J	K	L	M	N	O	P
Receive High-Speed Interface [at 78 MHz/83 MHz] Loopbacks (DWFEC and SONFEC are disabled)															
R2TF_LB	RCLKLI	0x04	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x02	0xXX	0xXX	0xXX	0xXX	0xXX
Receive DWFEC Only Loopbacks (SONFEC is Disabled)															
RDW2TDW_LB	RCLKLI	0x04	0x04	0x00	0x00	0x04	0x00	0x00	0x00	0x00	0xXX	0xXX	0xXX	0xXX	0xXX
RES2TES_LB	RCLKLI RCLKSI	0x04	0x04	0x02	0x00	0x04	0x02	0x00	0x00	0x00	0x02	0xXX	0xXX	0xXX	0xXX
Receive SONFEC Only Loopbacks (DWFEC Disabled)															
RSYS2TSYS_LB	RCLKLI	0x04	0x00	0x00	0x04	0x00	0x00	0x04	0x00	0x01	0xXX	0xXX	0x01	0xXX	0xXX
Receive DWFEC and SONFEC Loopbacks															
RSYS2TSYS_LB	RCLKLI RCLKSI TCLKLI	0x03	0x03	0x02	0x02	0x04	0x02	0x02	0x00	0x00	0x00	0xXX	0x00	0xXX	0xXX
Transmit High-Speed Interface [at 78 MHz/83 MHz] Loopbacks (DWFEC and SONFEC are Disabled)															
T2RF_LB	TCLKSI	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x01	0xXX	0xXX	0xXX	0xXX	0xXX	0x02
Transmit SONFEC Only Loopbacks (DWFEC is Disabled)															
TLINE2RLINE_LB	TCLKSI	0x00	0x00	0x00	0x01	0x00	0x00	0x01	0x01	0xXX	0xXX	0x00	0xXX	0xXX	0x00
Transmit DWFEC Only Loopbacks (SONFEC is Disabled)															
TDW2RDW_LB[1]	TCLKSI	0x00	0x01	0x00	0x00	0x01	0x00	0x00	0x01	0xXX	0x01	0xXX	0xXX	0x01	0x01
TDW2RDW_LB[2]	TCLKSI TCLKLI RCLKSI	0x00	0x03	0x01	0x00	0x03	0x02	0x00	0x02	0xXX	0x01	0xXX	0xXX	0x00	0x01
TRSEN2RRSDE_LB[1]	TCLKSI	0x00	0x01	0x00	0x00	0x01	0x00	0x00	0x01	0xXX	0x01	0xXX	0xXX	0x01	0x01
TRSEN2RRSDE_LB[2]	TCLKSI TCLKLI RCLKSI	0x00	0x03	0x01	0x00	0x03	0x02	0x00	0x02	0xXX	0x01	0xXX	0xXX	0x00	0x01
Transmit DWFEC and SONFEC Loopbacks															
TDW2RDW_LB	TCLKSI TCLKLI RCLKSI	0x00	0x03	0x01	0x01	0x03	0x02	0x02	0x02	0xXX	0x00	0x00	0x00	0xXX	0x00
TRSEN2RRSDE_LB	TCLKSI TCLKLI RCLKSI	0x00	0x03	0x01	0x01	0x03	0x02	0x02	0x02	0xXX	0x00	0x00	0x00	0xXX	0x00

1. This loopback assumes DWES is bypassed (bidirectional mode); TFRMLI cannot be used to generate FEC/DW frames.
2. This loopback assumes DWES is present; TFRMLI could be used to generate FEC/DW frames.

44 TFEC Valid Modes

The following truth table illustrates possible Rx/Tx modes in the TFEC0410G. Any combinations of these modes could be used. However care must be taken to set up the clocks in these modes. Refer to the Section 40, TFEC Clock Multiplexers, on page 180 to see the following settings:

- DWFEC: Strong FEC (FEC/DW Mode)
- SONFEC: Weak FEC
- DWES: DWFEC Elastic Store

44.1 General Conditions on Primary Clock Inputs

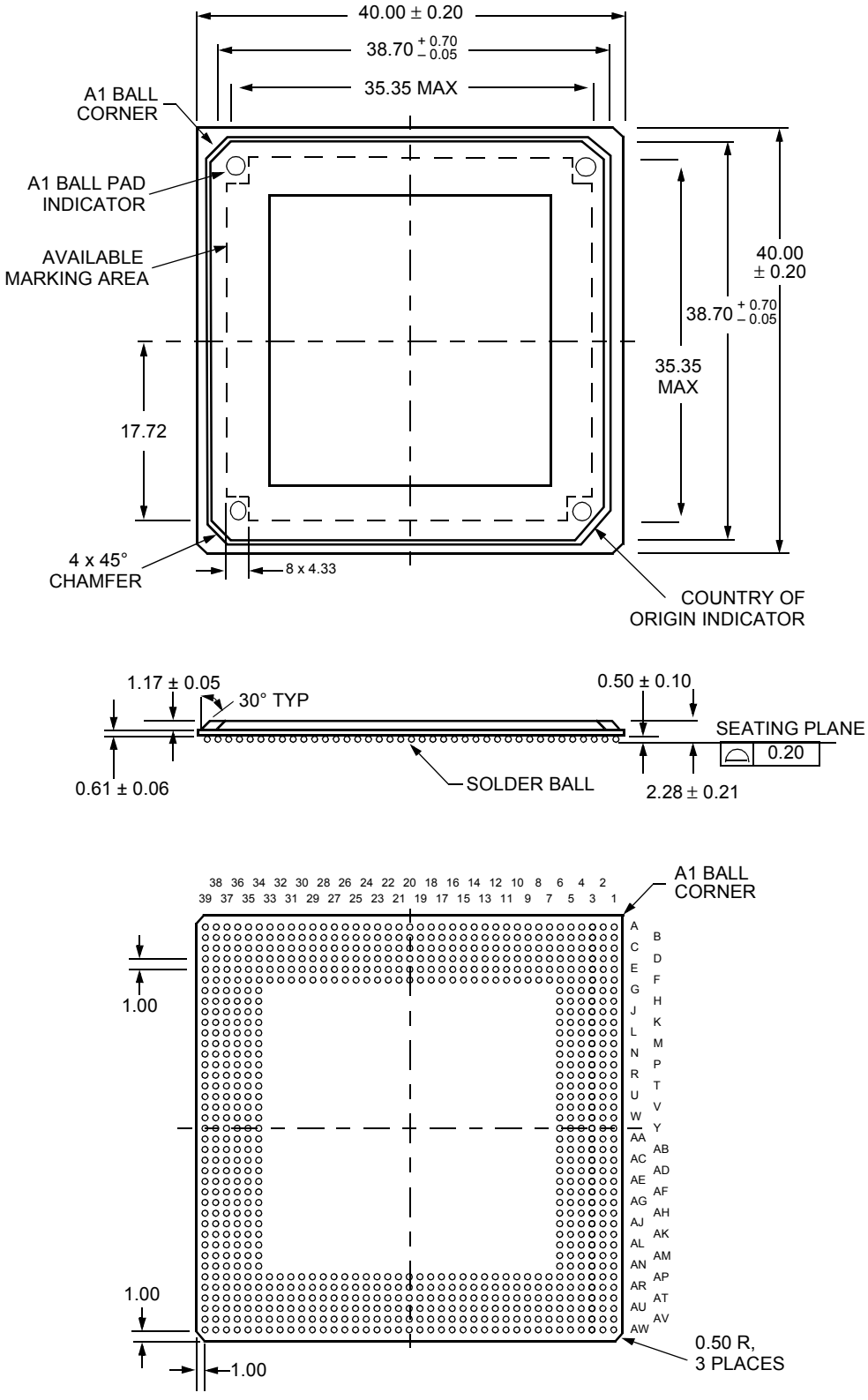
- Both RCLKLI and TCLKSI need to be present in all modes, except loopback/regenerator modes.
- If DWFEC is used along with SONFEC and/or DWES, then both TCLKLI and RCLKSI need to be present.
- If DWFEC is used with no DWES or SONFEC, then no other clocks need be present.
- In case of multiplexing (10 Gbits/s ↔ 2.5 Gbits/s), all four 2.5 Gbits/s signals are to be bit synchronous to the same clock via TCLKSI[0].

LINE \ SYSTEM	1 x 10.666	1 x 09.953	4 x 02.666	4 x 02.488
1 x 10.666	DWFEC—NO DWES	DWFEC + DWES DWFEC + SONFEC	INVALID	DWFEC + SONFEC
1 x 09.953	INVALID	SONFEC	INVALID	SONFEC
4 x 02.666	INVALID	INVALID	DWFEC—NO DWES	DWFEC + DWES DWFEC + SONFEC
4 x 02.488	INVALID	SONFEC [Tx ONLY]	INVALID	SONFEC

Figure 55. TFEC Rx/Tx Possible Modes

45 Outline Diagram

45.1 792-Pin PBGAM1TH



46 List of Acronyms

A

ADM	Add/Drop Multiplexer
AIS	Alarm Indication Signal
AIS-L	Line Alarm Indication Signal
API	Application Program Interface
APLL	Analog Phase Locked Loop
AR	Alarm Register
AU	Administrative Unit (SDH naming for frames)

B

B1, B2, B3	Error Count Bits
BAR	Base Address Register
BCH	Bose-Chaudhuri-Hocquenguem (weak FEC cyclic code)
BDI	Backward Defect Indication
BDI-O	Backward Defect Indication Overhead
BDI-P	Backward Defect Indication Payload
BEI	Backward Error Indication
BER	Bit Error Rate
BI	Backward Indication
BIM	Byte Interleaved Multiplexer
BIP	Bit Interleaved Parity
BIP-8	Bit Interleaved Parity Level 8
BIST	Built-In Self-Test
bit	Binary Digit
BLI	Backward Line Indication
BLSR	Bidirectional Line Switch Ring
Bits/s	Bits Per Second
BS	Boundary Scan

C

C2	Expected Payload Label Bit
CBR	Constant Bit Rate
CDR	Clock Data Recovery
CM	Common Mode or Configuration Management or Connection Monitoring
CMEP	Connection Monitoring End Point
CMF	Common-Mode Failure
CML	Current-Mode Logic
CMOH	Connection Monitoring Overhead
CMR	Common Mode Rejection
CMS	Current-Mode Switching
CMV	Common-Mode Voltage
CNTD	Continuous N-Times Detect
COR	Clear on Read
CORBA	Common Object Request Broker Architecture
COW	Clear on Write
CPT	Cell Pointer Table
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check or Cyclic Redundancy Code
CV	Coding Violation
CV-L	Line Coding Violation
CV-P	Path Coding Violation
CV-S	Section Coding Violation

D

DCC	Data Communications Channel
DLL	Delay-Locked Loop
DPLL	Dedicated Phase-Locked Loop
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
DW	Digital Wrapper
DWAC	Digital Wrapper Access Channel
DWDM	Dense Wavelength Division Multiplexing
DWSFEC	Digital Wrapper Enhanced Forward Error Correction

E

EFEC	Enhanced Forward Error Correction
ES	Errored Second or Elastic Store
ESD	Electrostatic Discharge
ESF	Extended Superframe
ESI	End System Identifier
EVT	Egress VC Table
EXTEST	External Test
ExTI	Expected Trace Identifier

F

FAE	Field Application Engineer
FAS	Frame Alignment Signal
FCBGA	Flip-Chip Ball-Grid Array
FCS	Frame Check Sequence
FDI	Forward Defect Indication
FDI-O	Forward Defect Indication Overhead
FDI-P	Forward Defect Indication Payload
FE	Framing (bit) Error
FEBE	Far-End Block Error
FEC	Forward Error Correction
FIFO	First In, First Out
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
FS	Fixed Stuff
FSI	FEC Status Indicator
FSM	Finite State Machine
FTFL	Fault Type and Fault Location

46 List of Acronyms (continued)

G

GbE	Gigabit Ethernet
GND	Ground
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
GRST	Global Reset
GSR	Global Set/Reset

H

H1, H2	SONET Signal Payload Pointer Bits
HDLC	High-Level Data Link Control
HEC	Header Error Correction or Header Error Control
HSI	High-Speed Interface
HW	Hardware

I

I/O	Input/Output
IaDI	Intra-Domain Interface
IAE	Incoming Alignment Error
IDI	Initial Domain Identifier
IrDI	Inter-Domain Interface
IRQ	Interrupt Request
ISR	Interrupt Status Register
ITU	International Telecommunications Union

J

J1	Trace Byte
JEDEC	Joint Electronic Devices Engineering Council
JC	Stuff Control Byte
JTAG	Joint Test Access Group

K

K1, K2	APS Bits of SONET Signal

L

laDI	Intradomain Interface
LAN	Local Area Network
LAPI	Low-Level Application Programming Interface
LB	Loopback
LCK	Locked
LED	Light Emitting Diode
LOC	Loss of Clock
LOF	Loss of Frame
LOFA	Loss of Frame Alignment
LOH	Line Overhead
LOL	Loss of Lock
LOM	Loss of Multiframe Alignment
LOP	Loss of Pointer
LOS	Loss of Signal
LOTC	Loss of Transmit Clock
lrDI	Interdomain Interface
LSB	Least Significant Bit/Byte
LSN	Least Significant Nibble
LTE	Line Terminating Equipment
LV	Low Voltage
LVDS	Low-Voltage Differential Signal

M

MFAS	Multiframe Alignment Signal
MPI	Microprocessor Interface
MPIF	Master Processor Interface
MS	Multiplex Section
MSB	Most Significant Bit/Byte
MSI	Multiplex Structure Identifier
MSN	Most Significant Nibble
MUTEX	Mutual Exclusion
MUX	Multiplex or Multiplexor

N

NJO	Negative Justification Offset (Negative Justification Byte)
NRZ	Nonreturn to Zero
NSA	Non-Service Affecting
N-Time Detect	A received value remains the same for N consecutive frames.

46 List of Acronyms (continued)

O

OA&M	Operations Administration and Maintenance
OCh	Optical Channel (single)
OCI	Open Connection Indication
ODUk	Optical Channel Data Unit
OH	Overhead
OHP	Overhead Processor
OHPI	Overhead Processor Insertion
OHPM	Overhead Processor Monitoring
OMSn	Optical Multiplex Section Overhead
OMS	Optical Multiplexing Section
OMU	Optical Multiplexing Unit
ONNI	Optical Transport Network Node Interface
OOA	Out of Alignment
OOF	Out of Frame
OOM	Out of Multiframe Alignment
OOS	Optical Transport Module Overhead Signal
OPU	Optical Channel Payload Unit
OSC	Optical Supervisory Channel
OSI	Open System Interconnect
OTH	Optical Transport Hierarchy
OTM	Optical Transport Module
OTM-0	Optical Transport Module of Order 0
OTN	Optical Transport Network
OTS	Optical Transmission Section
OTSn	Optical Transmission Section Overhead
OTUk	Optical Channel Transport Unit

P

PA	Persistency Alarm
PBGA	Plastic Ball Grid Array
PBGAM	Plastic Ball Grid Array Multilayer
PCLK	Microprocessor Clock
PD	Phase Detector
PDI	Payload Defect Indication
PHY	Physical Layer
PJO	Positive Justification Offset Byte
PLL	Phase-Locked Loop
PM	Performance Monitoring
PMCLK	Performance Monitoring Clock
PMOH	Path Monitoring Overhead
PN	Pseudo-Random Noise Sequence or Pseudo-Random Number (i.e., PN29)
PNZ	Positive/Negative/Zero
POAC	Path Overhead Access Channel
POH	Path Overhead
POS	Packet-Over-SONET/SDH
P-P	Peak to Peak
PP	Pointer Processor
PPLL	Programmable Phase-Locked Loop
PRAM	Pointer Random Access Memory
PRBS	Pseudo-Random Bit Sequence
PSI	Payload Structure Identifier

Q

QoS	Quality of Service

R

R/W	Read/Write
RAI	Remote Alarm Indication
RDI	Remote Defect Indicator
RDI-L	Line Remote Defect Indication
REI	Remote Error Indication
REI-L	Line Remote Error Indication
RES	Reserved
RN	Random Number
RO	Read Only
RS	Reed Solomon (strong FEC)
RW	Read/Write
Rx	Receive
RZ	Return to Zero

46 List of Acronyms (continued)

S

SA	Service Affecting
SCLK	System Clock
SD	Signal Degrade
SDH	Synchronous Digital Hierarchy
SEF	Severely Errored Frame
SERDES	Serializer/Deserializer
SF	Signal Fail
SFI	SERDES Framer Interface
SFI-4	SERDES Framer Interface Level 4
SM	Section Monitoring
SNMP	Simple Network Management Protocol
SNR	Signal-to-Noise Ratio
SOH	Section Overhead
SONET	Synchronous Optical Network
SONFEC	SONET Forward Error Correction
SPA	Selected Packet Available
SPE	SONET Payload Envelope
SPIF	Slave Processor Interface
STAT	Status Indication
STE	Section Terminating Equipment
SWI	Software Interrupt

T

TA	Transfer Acknowledge
T_A	Ambient Temperature
TBD	To Be Determined
TC	Temperature Coefficient or Time Constant or Tandem Connection
T_C	Case Temperature
TCK	Test Clock
TCM	Tandem Connection Monitoring
TCMOH	Tandem Connection Monitoring Overhead
TDI	Test Data In
TDM	Time Division Multiplexer
TDMX	Transpose DeMultiplexer
TDO	Test Data Out
TEA	Transfer Error Acknowledge
TFEC	Transmission Forward Error Correcting
TIM	Trace Identifier Mismatch
T_J	Junction Temperature
TMS	Test Mode Select
TOAC	Transport Overhead Access Channel
TOH	Transport Overhead
T_{prop}	Propagation Time
TRSTN	Test Reset (Active Low)
TS	Time Slot or Tributary Slot
TSI	Time-Slot Interchange
TSM	Tributary Slot Multiplexing
TTI	Trail Trace Identifier
Tx	Transmit

U

UNEQ	Unequipped
UNI	User-Network Interface
UPSR	Unidirectional Path Switch Ring
UTOPIA	Universal Test and Operations Physical Interface for ATM

V

VBR	Variable Bit Rate
VC	Virtual Channel
VCI	Virtual Connection Indicator
VCO	Voltage-Controlled Oscillator
VP	Virtual Path
VPI	Virtual Path Indicator
VT	Virtual Tributary
VTG	Virtual Tributary Group

W

W1C	Write One Clear
WDM	Wavelength Division Multiplexing
WRR	Weighted Round Robin

X

XPIF	External Processor Interface

Z

Z0	Section Overhead Bit

List of Objects

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

List of Objects (continued)

S

List of Objects (continued)

47 Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TFEC0410G-3PBGA2	792-Pin PBGAM1TH	–40 °C to 85 °C	700012029

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July 2002
DS02-232SONT

TFEC0410G 2.5/10 Gbits/s Optical Networking Interface with Strong/Weak FEC and Digital Wrapper

1 Document Organization

This document is primarily intended for designers and engineers whom require I/O characteristics for board design of the TFEC0410G optical networking interface. This is a companion document to the TFEC0410G document group, which consists of the following:

- TFEC0410G Product Description
- TFEC0410G Operational Description
- TFEC0410G Hardware Register Map
- TFEC0410G Hardware Design Guide
- TFEC0410G System Design Guide

This document contains the following information, and where it can be found in this document, on the TFEC0410G device:

Table of Contents

Contents Page

2 Pin Information

2.1 Pin Maps

The following tables list the pins of the TFEC0410G for both 2.5 Gbits/s mode and 10 Gbits/s mode (see Table 1 and Table 2 on page 11). The 2.5 Gbits/s mode pins are the first listed, in the full-size font. The second name, if present, is the pin name in 10 Gbits/s mode. This 10 Gbits/s pin name is in a smaller font, when appropriate.

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VDD	B1	VDD	C1	No Connect	D1	No Connect
A2	VDD	B2	VDD	C2	No Connect	D2	No Connect
A3	No Connect	B3	No Connect	C3	VSS	D3	VSS
A4	No Connect	B4	No Connect	C4	VSS	D4	VSS
A5	RPHASE_DW_3	B5	RPHASE_UP_3	C5	No Connect	D5	No Connect
A6	TTOAC_DENI_1	B6	No Connect	C6	RPHASE_DW_1	D6	RPHASE_UP_1
A7	TTOAC_DATAI_1_2	B7	TTOAC_DATAI_1_3	C7	RPHASE_DW_4	D7	RPHASE_UP_4
A8	TTOAC_DENI_2	B8	No Connect	C8	VSS	D8	VDD
A9	TTOAC_CLKO_3	B9	No Connect	C9	TTOAC_SYNCO_2	D9	TTOAC_CLKO_2
A10	TTOAC_DENI_3	B10	TTOAC_SYNCO_3	C10	TTOAC_DATAI_2_0	D10	TTOAC_DATAI_2_1
A11	No Connect	B11	No Connect	C11	VDD	D11	VSS
A12	TTOAC_CLKO_4	B12	No Connect	C12	TTOAC_DATAI_3_2	D12	TTOAC_DATAI_3_3
A13	TTOAC_DATAI_4_0	B13	TTOAC_DATAI_4_1	C13	TTOAC_DENI_4	D13	TTOAC_SYNCO_4
A14	No Connect	B14	No Connect	C14	VSS	D14	VDD
A15	ADDRESS_14	B15	ADDRESS_15	C15	MPPAREN	D15	MPDB_8_16
A16	ADDRESS_10	B16	ADDRESS_11	C16	ADDRESS_12	D16	ADDRESS_13
A17	ADDRESS_6	B17	ADDRESS_7	C17	VDD	D17	VSS
A18	ADDRESS_0	B18	ADDRESS_1	C18	ADDRESS_2	D18	ADDRESS_3
A19	VSS	B19	VSS	C19	TS_N	D19	DS_N
A20	VDD	B20	VDD	C20	VDD	D20	VDD
A21	VSS	B21	VSS	C21	CS_N	D21	RW_N
A22	PCLK	B22	INTH_N	C22	MPMODE_AS	D22	TA_N
A23	DATA_0	B23	DATA_1	C23	VDD	D23	VSS
A24	DATA_4	B24	DATA_5	C24	DATA_6	D24	DATA_7
A25	DATA_8	B25	DATA_9	C25	DATA_12	D25	DATA_13
A26	DATA_14	B26	DATA_15	C26	VSS	D26	VDD
A27	TDW_CLKO_1	B27	TDW_SYNCO_1	C27	TDW_DENI_1	D27	TDW_DATAI_1
A28	No Connect	B28	No Connect	C28	TDW_SYNCO_2	D28	TDW_DENI_2
A29	TDW_DATAI_2	B29	No Connect	C29	VDD	D29	VSS
A30	TDW_CLKO_3	B30	TDW_SYNCO_3	C30	TDW_DENI_4	D30	TDW_DATAI_4
A31	TDW_CLKO_4	B31	TDW_SYNCO_4	C31	GPIO_15	D31	GPIO_14
A32	GPIO_17	B32	GPIO_16	C32	VSS	D32	VDD
A33	GPIO_11	B33	GPIO_10	C33	GPIO_7	D33	GPIO_6
A34	No Connect	B34	No Connect	C34	No Connect	D34	No Connect
A35	GPIO_5	B35	GPIO_4	C35	No Connect	D35	No Connect
A36	No Connect	B36	No Connect	C36	VSS	D36	VSS
A37	No Connect	B37	No Connect	C37	VSS	D37	VSS
A38	VDD	B38	VDD	C38	No Connect	D38	No Connect
A39	VDD	B39	VDD	C39	No Connect	D39	No Connect

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
E1	No Connect	E21	VDD15	F1	TPHASE_UP_2	F21	VDD15
E2	No Connect	E22	TEA_N	F2	TPHASE_DW_2	F22	INTL_N
E3	No Connect	E23	DATA_2	F3	No Connect	F23	DATA_3
E4	No Connect	E24	DATA_10	F4	No Connect	F24	DATA_11
E5	VDD15	E25	PARITY_1	F5	VDD15	F25	PARITY_0
E6	VDD15	E26	No Connect	F6	VDD15	F26	No Connect
E7	No Connect	E27	TDW_CLKO_2	F7	No Connect	F27	No Connect
E8	RPHASE_DW_2	E28	TDW_DENI_3	F8	RPHASE_UP_2	F28	TDW_DATAI_3
E9	TTOAC_SYNCO_1	E29	TESTMODE	F9	TTOAC_CLKO_1	F29	No Connect
E10	TTOAC_DATAI_1_0	E30	GPIO_13	F10	TTOAC_DATAI_1_1	F30	GPIO_12
E11	TTOAC_DATAI_2_2	E31	GPIO_9	F11	TTOAC_DATAI_2_3	F31	GPIO_8
E12	No Connect	E32	No Connect	F12	No Connect	F32	No Connect
E13	TTOAC_DATAI_3_0	E33	No Connect	F13	TTOAC_DATAI_3_1	F33	No Connect
E14	TTOAC_DATAI_4_2	E34	VDD15	F14	TTOAC_DATAI_4_3	F34	VDD15
E15	MPTYPE_IM	E35	VDD15	F15	PM_CLK	F35	VDD15
E16	No Connect	E36	No Connect	F16	No Connect	F36	No Connect
E17	ADDRESS_8	E37	No Connect	F17	ADDRESS_9	F37	No Connect
E18	ADDRESS_4	E38	No Connect	F18	ADDRESS_5	F38	TDLO_4_2N/ TDLO_14N
E19	VDD15	E39	No Connect	F19	VDD15	F39	TDLO_4_2P/ TDLO_14P
E20	VDD15	—	—	F20	VDD15	—	—

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
G1	TPHASE_UP_1	J1	TDSI_4_1N/ TDSI_13N	L1	TCLKSI_4N	N1	TCLKSI_3N
G2	TPHASE_DW_1	J2	TDSI_4_1P/ TDSI_13P	L2	TCLKSI_4P	N2	TCLKSI_3P
G3	TPHASE_UP_4	J3	GPIO_3	L3	VSS	N3	TDSI_3_1N/TDSI_9N
G4	TPHASE_DW_4	J4	GPIO_2	L4	VDD	N4	TDSI_3_1P/TDSI_9P
G5	No Connect	J5	TPHASE_UP_3	L5	TDSI_4_3N/ TDSI_15N	N5	TDSI_3_3N/ TDSI_11N
G6	No Connect	J6	TPHASE_DW_3	L6	TDSI_4_3P/ TDSI_15P	N6	TDSI_3_3P/ TDSI_11P
G34	No Connect	J34	No Connect	L34	VSS	N34	TDLO_3_1P/ TDLO_9P
G35	No Connect	J35	No Connect	L35	VDD	N35	TDLO_3_1N/ TDLO_9N
G36	No Connect	J36	TDLO_3_3N/ TDLO_11N	L36	VSS	N36	TCLKLO_2N
G37	No Connect	J37	TDLO_3_3P/ TDLO_11P	L37	VDD	N37	TCLKLO_2P
G38	TDLO_4_1N/ TDLO_13N	J38	TDLO_2_3N/ TDLO_7N	L38	TDLO_2_1N/ TDLO_5N	N38	TDLO_1_2N/ TDLO_2N
G39	TDLO_4_1P/ TDLO_13P	J39	TDLO_2_3P/ TDLO_7P	L39	TDLO_2_1P/ TDLO_5P	N39	TDLO_1_2P/ TDLO_2P
H1	No Connect	K1	TDSI_4_0N/ TDSI_12N	M1	TDSI_3_2N/ TDSI_10N	P1	TDSI_2_3N/TDSI_7N
H2	No Connect	K2	TDSI_4_0P/ TDSI_12P	M2	TDSI_3_2P/ TDSI_10P	P2	TDSI_2_3P/TDSI_7P
H3	VSS	K3	TDSI_4_2N/ TDSI_14N	M3	CTAP_TDSI_3	P3	VSS
H4	VDD	K4	TDSI_4_2P/ TDSI_14P	M4	CTAP_TCLKSI_4	P4	VDD
H5	No Connect	K5	No Connect	M5	No Connect	P5	TDSI_3_0N/TDSI_8N
H6	No Connect	K6	GPIO_1	M6	CTAP_TDSI_4	P6	TDSI_3_0P/TDSI_8P
H34	No Connect	K34	TDLO_4_3N/ TDLO_15N	M34	TDLO_4_0P/ TDLO_12P	P34	TDLO_3_0P/ TDLO_8P
H35	No Connect	K35	TDLO_4_3P/ TDLO_15P	M35	TDLO_4_0N/ TDLO_12N	P35	TDLO_3_0N/ TDLO_8N
H36	VDD	K36	TDLO_3_2N/ TDLO_10N	M36	TDLO_2_2N/ TDLO_6N	P36	VDD
H37	VSS	K37	TDLO_3_2P/ TDLO_10P	M37	TDLO_2_2P/ TDLO_6P	P37	VSS
H38	TCLKLO_4N	K38	TCLKLO_3N	M38	TDLO_1_3N/ TDLO_3N	P38	TDLO_1_0N/ TDLO_0N
H39	TCLKLO_4P	K39	TCLKLO_3P	M39	TDLO_1_3P/ TDLO_3P	P39	TDLO_1_0P/ TDLO_0P

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
R1	TDSI_2_1N/ TDSI_5N	U1	TDSI_1_3N/ TDSI_3N	W1	VSS	AA1	VSS
R2	TDSI_2_1P/ TDSI_5P	U2	TDSI_1_3P/ TDSI_3P	W2	VSS	AA2	VSS
R3	No Connect	U3	VSS	W3	No Connect	AA3	TCLKSI_1P
R4	CTAP_TDSI_2	U4	VDD	W34	VDD15	AA4	TCLKSI_1N
R5	No Connect	U5	TCLKSI_2N	W35	VDD15	AA5	VDD15
R6	CTAP_TCLKSI_3	U6	TCLKSI_2P	W36	TCLKLI_3N	AA6	VDD15
R34	TDLO_2_0P/ TDLO_4P	U34	TCLKLI_2N	W37	TCLKLI_3P	AA34	VDD15
R35	TDLO_2_0N/ TDLO_4N	U35	TCLKLI_2P	W38	VSS	AA35	VDD15
R36	TCLKLO_1N	U36	TFRMLI_1N	W39	VSS	AA36	CTAP_TCLKLI_4
R37	TCLKLO_1P	U37	TFRMLI_1P	W4	CTAP_TDSI_1	AA37	No Connect
R38	CTAP_TCLKLI_1	U38	TFRMLI_2N	W5	VDD15	AA38	VSS
R39	CTAP_TFRMLI_1	U39	TFRMLI_2P	W6	VDD15	AA39	VSS
T1	No Connect	V1	TDSI_1_0N/ TDSI_0N	Y1	VDD	AB1	CTAP_TCLKSI_1
T2	CTAP_TCLKSI_2	V2	TDSI_1_0P/ TDSI_0P	Y2	VDD	AB2	CTAP_RCLKSI_1
T3	TDSI_2_0N/ TDSI_4N	V3	TDSI_1_1N/ TDSI_1N	Y3	VDD	AB3	RCLKSI_1P
T4	TDSI_2_0P/ TDSI_4P	V4	TDSI_1_1P/ TDSI_1P	Y4	VDD	AB4	RCLKSI_1N
T5	TDSI_2_2N/ TDSI_6N	V5	TDSI_1_2N/ TDSI_2N	Y5	VDD15	AB5	CTAP_RCLKSI_2
T6	TDSI_2_2P/ TDSI_6P	V6	TDSI_1_2P/ TDSI_2P	Y6	VDD15	AB6	No Connect
T34	TDLO_1_1N/ TDLO_1N	V34	CTAP_TFRMLI_2	Y34	VDD15	AB34	No Connect
T35	TDLO_1_1P/ TDLO_1P	V35	No Connect	Y35	VDD15	AB35	CTAP_TFRMLI_4
T36	TCLKLI_1N	V36	TFRMLI_3N	Y36	VDD	AB36	TFRMLI_4P
T37	TCLKLI_1P	V37	TFRMLI_3P	Y37	VDD	AB37	TFRMLI_4N
T38	No Connect	V38	CTAP_TFRMLI_3	Y38	VDD	AB38	TCLKLI_4P
T39	CTAP_TCLKLI_2	V39	CTAP_TCLKLI_3	Y39	VDD	AB39	TCLKLI_4N

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AC1	RCLKSI_2P	AE1	CTAP_RCLKSI_4	AG1	RCLKSO_4P	AJ1	RDSO_3_1P/ RDSO_9P
AC2	RCLKSI_2N	AE2	RDSO_4_2P/ RDSO_14P	AG2	RCLKSO_4N	AJ2	RDSO_3_1N/ RDSO_9N
AC3	RCLKSI_3P	AE3	RDSO_4_2N/ RDSO_14N	AG3	RDSO_3_3P/ RDSO_11P	AJ3	VDD
AC4	RCLKSI_3N	AE4	RDSO_4_0P/ RDSO_12P	AG4	RDSO_3_3N/ RDSO_11N	AJ4	VSS
AC5	VDD	AE5	RDSO_4_0N/ RDSO_12N	AG5	LVDS_SRESHI	AJ5	No Connect
AC6	VSS	AE6	No Connect	AG6	LVDS_SRESLO	AJ6	No Connect
AC34	RDLI_4_2P/RDLI_14P	AE34	RDLI_3_2P/ RDLI_10P	AG34	CTAP_RDLI_2	AJ34	RDLI_1_3P/ RDLI_3P
AC35	RDLI_4_2N/RDLI_14N	AE35	RDLI_3_2N/ RDLI_10N	AG35	No Connect	AJ35	RDLI_1_3N/ RDLI_3N
AC36	VSS	AE36	CTAP_RDLI_3	AG36	CTAP_RCLKLI_3	AJ36	VSS
AC37	VDD	AE37	CTAP_RCLKLI_4	AG37	No Connect	AJ37	VDD
AC38	RDLI_4_3P/RDLI_15P	AE38	CTAP_RDLI_4	AG38	RDLI_3_1P/RDLI_9P	AJ38	RDLI_2_2P/ RDLI_6P
AC39	RDLI_4_3N/RDLI_15N	AE39	No Connect	AG39	RDLI_3_1N/RDLI_9N	AJ39	RDLI_2_2N/ RDLI_6N
AD1	CTAP_RCLKSI_3	AF1	RDSO_4_1P/ RDSO_13P	AH1	RDSO_3_2P/ RDSO_10P	AK1	RDSO_3_0P/ RDSO_8P
AD2	RCLKSI_4P	AF2	RDSO_4_1N/ RDSO_13N	AH2	RDSO_3_2N/ RDSO_10N	AK2	RDSO_3_0N/ RDSO_8N
AD3	RCLKSI_4N	AF3	VSS	AH3	RCLKSO_3P	AK3	RDSO_2_2P/ RDSO_6P
AD4	RDSO_4_3P/ RDSO_15P	AF4	VDD	AH4	RCLKSO_3N	AK4	RDSO_2_2N/ RDSO_6N
AD5	RDSO_4_3N/ RDSO_15N	AF5	LVDS_SREF10	AH5	RDSO_2_1P/ RDSO_5P	AK5	RDSO_1_3P/ RDSO_3P
AD6	No Connect	AF6	LVDS_SREF14	AH6	RDSO_2_1N/ RDSO_5N	AK6	RDSO_1_3N/ RDSO_3N
AD34	RCLKLI_4P	AF34	RDLI_3_0P/RDLI_8P	AH34	RDLI_2_0P/RDLI_4P	AK34	RDLI_1_0P/ RDLI_0P
AD35	RCLKLI_4N	AF35	RDLI_3_0N/RDLI_8N	AH35	RDLI_2_0N/RDLI_4N	AK35	RDLI_1_0N/ RDLI_0N
AD36	RDLI_4_0P/RDLI_12P	AF36	VDD	AH36	RDLI_2_3P/RDLI_7P	AK36	No Connect
AD37	RDLI_4_0N/RDLI_12N	AF37	VSS	AH37	RDLI_2_3N/RDLI_7N	AK37	CTAP_RCLKLI_2
AD38	RDLI_4_1P/RDLI_13P	AF38	RDLI_3_3P/RDLI_11P	AH38	RCLKLI_3P	AK38	RDLI_2_1P/ RDLI_5P
AD39	RDLI_4_1N/RDLI_13N	AF39	RDLI_3_3N/ RDLI_11N	AH39	RCLKLI_3N	AK39	RDLI_2_1N/ RDLI_5N

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AL1	RDSO_2_3P/ RDSO_7P	AM34	No Connect	AP1	RDSO_1_1P/ RDSO_1P	AP20	VDD15
AL2	RDSO_2_3N/ RDSO_7N	AM35	No Connect	AP2	RDSO_1_1N/ RDSO_1N	AP21	VDD15
AL3	RCLKSO_2P	AM36	VDD	AP3	No Connect	AP22	No Connect
AL4	RCLKSO_2N	AM37	VSS	AP4	No Connect	AP23	No Connect
AL5	RDSO_1_0P/ RDSO_0P	AM38	RDLI_1_2P/ RDLI_2P	AP5	VDD15	AP24	No Connect
AL6	RDSO_1_0N/ RDSO_0N	AM39	RDLI_1_2N/ RDLI_2N	AP6	VDD15	AP25	RDW_SYNCO_1
AL34	No Connect	AN1	RDSO_1_2P/ RDSO_2P	AP7	No Connect	AP26	No Connect
AL35	CTAP_RCLKLI_1	AN2	RDSO_1_2N/ RDSO_2N	AP8	GPIO_18	AP27	No Connect
AL36	RDLI_1_1P/ RDLI_1P	AN3	RCLKSO_1P	AP9	GPIO_22	AP28	No Connect
AL37	RDLI_1_1N/ RDLI_1N	AN4	RCLKSO_1N	AP10	TDI	AP29	No Connect
AL38	RCLKLI_2P	AN5	No Connect	AP11	RTOAC_DATO_1_2	AP30	No Connect
AL39	RCLKLI_2N	AN6	No Connect	AP12	RTOAC_DATO_2_2	AP31	LVDS_LREF14
AM1	RDSO_2_0P/ RDSO_4P	AN34	No Connect	AP13	RTOAC_DATO_3_2	AP32	LVDS_LRESLO
AM2	RDSO_2_0N/ RDSO_4N	AN35	No Connect	AP14	RTOAC_DATO_4_2	AP33	RXREFO_2N
AM3	VSS	AN36	RXREFO_1P	AP15	GPIO_25	AP34	VDD15
AM4	VDD	AN37	RXREFO_1N	AP16	GPIO_31	AP35	VDD15
AM5	No Connect	AN38	No Connect	AP17	GPIO_37	AP36	No Connect
AM6	No Connect	AN39	CTAP_RDLI_1	AP18	GPIO_41	AP37	No Connect
—	—	—	—	AP19	VDD15	AP38	RCLKLI_1P
—	—	—	—	—	—	AP39	RCLKLI_1N

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AR1	No Connect	AT1	No Connect	AU1	No Connect	AV1	VDD
AR2	No Connect	AT2	No Connect	AU2	No Connect	AV2	VDD
AR3	No Connect	AT3	VSS	AU3	VSS	AV3	No Connect
AR4	No Connect	AT4	VSS	AU4	VSS	AV4	No Connect
AR5	VDD15	AT5	No Connect	AU5	No Connect	AV5	GPIO_20
AR6	VDD15	AT6	No Connect	AU6	No Connect	AV6	GPIO_24
AR7	No Connect	AT7	No Connect	AU7	No Connect	AV7	TMS
AR8	GPIO_19	AT8	VDD	AU8	VSS	AV8	RTOAC_DATO_1_0
AR9	GPIO_23	AT9	RTOAC_SYNCO_1	AU9	RTOAC_CLKO_1	AV9	RTOAC_DATO_2_0
AR10	TCK	AT10	RTOAC_SYNCO_2	AU10	RTOAC_CLKO_2	AV10	RTOAC_SYNCO_3
AR11	RTOAC_DATO_1_3	AT11	VSS	AU11	VDD	AV11	No Connect
AR12	RTOAC_DATO_2_3	AT12	RTOAC_DATO_3_0	AU12	RTOAC_DATO_3_1	AV12	RTOAC_SYNCO_4
AR13	RTOAC_DATO_3_3	AT13	RTOAC_DATO_4_0	AU13	RTOAC_DATO_4_1	AV13	No Connect
AR14	RTOAC_DATO_4_3	AT14	VDD	AU14	VSS	AV14	GPIO_27
AR15	GPIO_26	AT15	GPIO_29	AU15	GPIO_30	AV15	GPIO_33
AR16	GPIO_32	AT16	No Connect	AU16	No Connect	AV16	GPIO_35
AR17	GPIO_38	AT17	VSS	AU17	VDD	AV17	GPIO_39
AR18	GPIO_42	AT18	GPIO_43	AU18	GPIO_44	AV18	No Connect
AR19	VDD15	AT19	GPIO_45	AU19	GPIO_46	AV19	VSS
AR20	VDD15	AT20	VDD	AU20	VDD	AV20	VDD
AR21	VDD15	AT21	No Connect	AU21	No Connect	AV21	VSS
AR22	No Connect	AT22	RST_N	AU22	IDDQ_N	AV22	GPIO_48
AR23	No Connect	AT23	VSS	AU23	VDD	AV23	No Connect
AR24	No Connect	AT24	No Connect	AU24	No Connect	AV24	No Connect
AR25	RDW_CLKO_1	AT25	No Connect	AU25	No Connect	AV25	No Connect
AR26	RDW_DATAO_1	AT26	VDD	AU26	VSS	AV26	No Connect
AR27	No Connect	AT27	No Connect	AU27	RDW_CLKO_2	AV27	No Connect
AR28	No Connect	AT28	No Connect	AU28	RDW_CLKO_3	AV28	RDW_DATAO_2
AR29	No Connect	AT29	VSS	AU29	VDD	AV29	No Connect
AR30	No Connect	AT30	No Connect	AU30	No Connect	AV30	RDW_CLKO_4
AR31	LVDS_LREF10	AT31	No Connect	AU31	No Connect	AV31	RDW_DATAO_4
AR32	LVDS_LRESHI	AT32	VDD	AU32	VSS	AV32	No Connect
AR33	RXREFO_2P	AT33	No Connect	AU33	No Connect	AV33	No Connect
AR34	VDD15	AT34	RXREFO_4N	AU34	RXREFO_4P	AV34	SCANCLK1
AR35	VDD15	AT35	No Connect	AU35	No Connect	AV35	No Connect
AR36	No Connect	AT36	VSS	AU36	VSS	AV36	RXREFO_3N
AR37	No Connect	AT37	VSS	AU37	VSS	AV37	No Connect
AR38	No Connect	AT38	No Connect	AU38	No Connect	AV38	VDD
AR39	No Connect	AT39	No Connect	AU39	No Connect	AV39	VDD

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 1. Pin Assignments for 792-Pin PBGAM1TH by Pin Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AW1	VDD	AW11	No Connect	AW21	VSS	AW31	RDW_SYNCO_4
AW2	VDD	AW12	RTOAC_CLKO_4	AW22	GPIO_47	AW32	No Connect
AW3	No Connect	AW13	No Connect	AW23	No Connect	AW33	No Connect
AW4	No Connect	AW14	GPIO_28	AW24	No Connect	AW34	SCANCLK2
AW5	GPIO_21	AW15	GPIO_34	AW25	No Connect	AW35	No Connect
AW6	TDO	AW16	GPIO_36	AW26	No Connect	AW36	RXREFO_3P
AW7	TRST_N	AW17	GPIO_40	AW27	No Connect	AW37	No Connect
AW8	RTOAC_DATO_1_1	AW18	No Connect	AW28	RDW_SYNCO_2	AW38	VDD
AW9	RTOAC_DATO_2_1	AW19	VSS	AW29	RDW_SYNCO_3	AW39	VDD
AW10	RTOAC_CLKO_3	AW20	VDD	AW30	RDW_DATAO_3	—	—

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A18	ADDRESS_0	R39	CTAP_TFRMLI_1	AW5	GPIO_21	C15	MPPAREN
B18	ADDRESS_1	V34	CTAP_TFRMLI_2	AP9	GPIO_22	E15	MPTYPE_IM
C18	ADDRESS_2	V38	CTAP_TFRMLI_3	AR9	GPIO_23	B11	No Connect
D18	ADDRESS_3	AB35	CTAP_TFRMLI_4	AV6	GPIO_24	B12	No Connect
E18	ADDRESS_4	A23	DATA_0	AP15	GPIO_25	B14	No Connect
F18	ADDRESS_5	B23	DATA_1	AR15	GPIO_26	B28	No Connect
A17	ADDRESS_6	E23	DATA_2	AV14	GPIO_27	B29	No Connect
B17	ADDRESS_7	F23	DATA_3	AW14	GPIO_28	B3	No Connect
E17	ADDRESS_8	A24	DATA_4	AT15	GPIO_29	B34	No Connect
F17	ADDRESS_9	B24	DATA_5	AU15	GPIO_30	B36	No Connect
A16	ADDRESS_10	C24	DATA_6	AP16	GPIO_31	B37	No Connect
B16	ADDRESS_11	D24	DATA_7	AR16	GPIO_32	B4	No Connect
C16	ADDRESS_12	A25	DATA_8	AV15	GPIO_33	B6	No Connect
D16	ADDRESS_13	B25	DATA_9	AW15	GPIO_34	B8	No Connect
A15	ADDRESS_14	E24	DATA_10	AV16	GPIO_35	B9	No Connect
B15	ADDRESS_15	F24	DATA_11	AW16	GPIO_36	A11	No Connect
C21	CS_N	C25	DATA_12	AP17	GPIO_37	A14	No Connect
AL35	CTAP_RCLKLI_1	D25	DATA_13	AR17	GPIO_38	A28	No Connect
AK37	CTAP_RCLKLI_2	A26	DATA_14	AV17	GPIO_39	A3	No Connect
AG36	CTAP_RCLKLI_3	B26	DATA_15	AW17	GPIO_40	A34	No Connect
AE37	CTAP_RCLKLI_4	D19	DS_N	AP18	GPIO_41	A36	No Connect
AB2	CTAP_RCLKSI_1	K6	GPIO_1	AR18	GPIO_42	A37	No Connect
AB5	CTAP_RCLKSI_2	J4	GPIO_2	AT18	GPIO_43	A4	No Connect
AD1	CTAP_RCLKSI_3	J3	GPIO_3	AU18	GPIO_44	AA37	No Connect
AE1	CTAP_RCLKSI_4	B35	GPIO_4	AT19	GPIO_45	AB34	No Connect
AN39	CTAP_RDLI_1	A35	GPIO_5	AU19	GPIO_46	AB6	No Connect
AG34	CTAP_RDLI_2	D33	GPIO_6	AW22	GPIO_47	AD6	No Connect
AE36	CTAP_RDLI_3	C33	GPIO_7	AV22	GPIO_48	AE39	No Connect
AE38	CTAP_RDLI_4	F31	GPIO_8	AU22	IDDQ_N	AE6	No Connect
R38	CTAP_TCLKLI_1	E31	GPIO_9	B22	INTH_N	AG35	No Connect
T39	CTAP_TCLKLI_2	B33	GPIO_10	F22	INTL_N	AG37	No Connect
V39	CTAP_TCLKLI_3	A33	GPIO_11	AR31	LVDS_LREF10	AJ5	No Connect
AA36	CTAP_TCLKLI_4	F30	GPIO_12	AP31	LVDS_LREF14	AJ6	No Connect
AB1	CTAP_TCLKSI_1	E30	GPIO_13	AR32	LVDS_LRESHI	AK36	No Connect
T2	CTAP_TCLKSI_2	D31	GPIO_14	AP32	LVDS_LRESLO	AL34	No Connect
R6	CTAP_TCLKSI_3	C31	GPIO_15	AF5	LVDS_SREF10	AM34	No Connect
M4	CTAP_TCLKSI_4	B32	GPIO_16	AF6	LVDS_SREF14	AM35	No Connect
W4	CTAP_TDSI_1	A32	GPIO_17	AG5	LVDS_SRESHI	AM5	No Connect
R4	CTAP_TDSI_2	AP8	GPIO_18	AG6	LVDS_SRESLO	AM6	No Connect
M3	CTAP_TDSI_3	AR8	GPIO_19	D15	MPDB_8_16	AN34	No Connect
M6	CTAP_TDSI_4	AV5	GPIO_20	C22	MPMODE_AS	AN35	No Connect

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AN38	No Connect	AT28	No Connect	AV4	No Connect	E38	No Connect
AN5	No Connect	AT30	No Connect	AW11	No Connect	E39	No Connect
AN6	No Connect	AT31	No Connect	AW13	No Connect	E4	No Connect
AP22	No Connect	AT33	No Connect	AW18	No Connect	E7	No Connect
AP23	No Connect	AT35	No Connect	AW23	No Connect	F12	No Connect
AP24	No Connect	AT38	No Connect	AW24	No Connect	F16	No Connect
AP26	No Connect	AT39	No Connect	AW25	No Connect	F26	No Connect
AP27	No Connect	AT5	No Connect	AW26	No Connect	F27	No Connect
AP28	No Connect	AT6	No Connect	AW27	No Connect	F29	No Connect
AP29	No Connect	AT7	No Connect	AW3	No Connect	F3	No Connect
AP3	No Connect	AU1	No Connect	AW32	No Connect	F32	No Connect
AP30	No Connect	AU16	No Connect	AW33	No Connect	F33	No Connect
AP36	No Connect	AU2	No Connect	AW35	No Connect	F36	No Connect
AP37	No Connect	AU21	No Connect	AW37	No Connect	F37	No Connect
AP4	No Connect	AU24	No Connect	AW4	No Connect	F4	No Connect
AP7	No Connect	AU25	No Connect	C1	No Connect	F7	No Connect
AR1	No Connect	AU30	No Connect	C2	No Connect	G34	No Connect
AR2	No Connect	AU31	No Connect	C34	No Connect	G35	No Connect
AR22	No Connect	AU33	No Connect	C35	No Connect	G36	No Connect
AR23	No Connect	AU35	No Connect	C38	No Connect	G37	No Connect
AR24	No Connect	AU38	No Connect	C39	No Connect	G5	No Connect
AR27	No Connect	AU39	No Connect	C5	No Connect	G6	No Connect
AR28	No Connect	AU5	No Connect	D1	No Connect	H1	No Connect
AR29	No Connect	AU6	No Connect	D2	No Connect	H2	No Connect
AR3	No Connect	AU7	No Connect	D34	No Connect	H34	No Connect
AR30	No Connect	AV11	No Connect	D35	No Connect	H35	No Connect
AR36	No Connect	AV13	No Connect	D38	No Connect	H5	No Connect
AR37	No Connect	AV18	No Connect	D39	No Connect	H6	No Connect
AR38	No Connect	AV23	No Connect	D5	No Connect	J34	No Connect
AR39	No Connect	AV24	No Connect	E1	No Connect	J35	No Connect
AR4	No Connect	AV25	No Connect	E12	No Connect	K5	No Connect
AR7	No Connect	AV26	No Connect	E16	No Connect	M5	No Connect
AT1	No Connect	AV27	No Connect	E2	No Connect	R3	No Connect
AT16	No Connect	AV29	No Connect	E26	No Connect	R5	No Connect
AT2	No Connect	AV3	No Connect	E3	No Connect	T1	No Connect
AT21	No Connect	AV32	No Connect	E32	No Connect	T38	No Connect
AT24	No Connect	AV33	No Connect	E33	No Connect	V35	No Connect
AT25	No Connect	AV35	No Connect	E36	No Connect	W3	No Connect
AT27	No Connect	AV37	No Connect	E37	No Connect	—	—

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
F25	PARITY_0	AN4	RCLKSO_1N	AH34	RDLI_2_0P/ RDLI_4P	AL6	RDSO_1_0N/ RDSO_0N
E25	PARITY_1	AN3	RCLKSO_1P	AK38	RDLI_2_1P/ RDLI_5P	AP2	RDSO_1_1N/ RDSO_1N
A22	PCLK	AL4	RCLKSO_2N	AJ38	RDLI_2_2P/ RDLI_6P	AN2	RDSO_1_2N/ RDSO_2N
F15	PM_CLK	AL3	RCLKSO_2P	AH36	RDLI_2_3P/ RDLI_7P	AK6	RDSO_1_3N/ RDSO_3N
AP39	RCLKLI_1N	AH4	RCLKSO_3N	AF35	RDLI_3_0N/ RDLI_8N	AL5	RDSO_1_0P/ RDSO_0P
AP38	RCLKLI_1P	AH3	RCLKSO_3P	AG39	RDLI_3_1N/ RDLI_9N	AP1	RDSO_1_1P/ RDSO_1P
AL39	RCLKLI_2N	AG2	RCLKSO_4N	AE35	RDLI_3_2N/ RDLI_10N	AN1	RDSO_1_2P/ RDSO_2P
AL38	RCLKLI_2P	AG1	RCLKSO_4P	AF39	RDLI_3_3N/ RDLI_11N	AK5	RDSO_1_3P/ RDSO_3P
AH39	RCLKLI_3N	AK35	RDLI_1_0N/ RDLI_0N	AF34	RDLI_3_0P/ RDLI_8P	AM2	RDSO_2_0N/ RDSO_4N
AH38	RCLKLI_3P	AL37	RDLI_1_1N/ RDLI_1N	AG38	RDLI_3_1P/ RDLI_9P	AH6	RDSO_2_1N/ RDSO_5N
AD35	RCLKLI_4N	AM39	RDLI_1_2N/ RDLI_2N	AE34	RDLI_3_2P/ RDLI_10P	AK4	RDSO_2_2N/ RDSO_6N
AD34	RCLKLI_4P	AJ35	RDLI_1_3N/ RDLI_3N	AF38	RDLI_3_3P/ RDLI_11P	AL2	RDSO_2_3N/ RDSO_7N
AB4	RCLKSI_1N	AK34	RDLI_1_0P/ RDLI_0P	AD37	RDLI_4_0N/ RDLI_12N	AM1	RDSO_2_0P/ RDSO_4P
AB3	RCLKSI_1P	AL36	RDLI_1_1P/ RDLI_1P	AD39	RDLI_4_1N/ RDLI_13N	AH5	RDSO_2_1P/ RDSO_5P
AC2	RCLKSI_2N	AM38	RDLI_1_2P/ RDLI_2P	AC35	RDLI_4_2N/ RDLI_14N	AK3	RDSO_2_2P/ RDSO_6P
AC1	RCLKSI_2P	AJ34	RDLI_1_3P/ RDLI_3P	AC39	RDLI_4_3N/ RDLI_15N	AL1	RDSO_2_3P/ RDSO_7P
AC4	RCLKSI_3N	AH35	RDLI_2_0N/ RDLI_4N	AD36	RDLI_4_0P/ RDLI_12P	AK2	RDSO_3_0N/ RDSO_8N
AC3	RCLKSI_3P	AK39	RDLI_2_1N/ RDLI_5N	AD38	RDLI_4_1P/ RDLI_13P	AJ2	RDSO_3_1N/ RDSO_9N
AD3	RCLKSI_4N	AJ39	RDLI_2_2N/ RDLI_6N	AC34	RDLI_4_2P/ RDLI_14P	AH2	RDSO_3_2N/ RDSO_10N
AD2	RCLKSI_4P	AH37	RDLI_2_3N/ RDLI_7N	AC38	RDLI_4_3P/ RDLI_15P	AG4	RDSO_3_3N/ RDSO_11N

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AK1	RDSO_3_0P/ RDSO_8P	AW29	RDW_SYNCO_3	AR12	RTOAC_DATAO_2_3	AV34	SCANCLK1
AJ1	RDSO_3_1P/ RDSO_9P	AW31	RDW_SYNCO_4	AT12	RTOAC_DATAO_3_0	AW34	SCANCLK2
AH1	RDSO_3_2P/ RDSO_10P	C6	RPHASE_DW_1	AU12	RTOAC_DATAO_3_1	D22	TA_N
AG3	RDSO_3_3P/ RDSO_11P	E8	RPHASE_DW_2	AP13	RTOAC_DATAO_3_2	AR10	TCK
AE5	RDSO_4_0N/ RDSO_12N	A5	RPHASE_DW_3	AR13	RTOAC_DATAO_3_3	T36	TCLKLI_1N
AF2	RDSO_4_1N/ RDSO_13N	C7	RPHASE_DW_4	AT13	RTOAC_DATAO_4_0	T37	TCLKLI_1P
AE3	RDSO_4_2N/ RDSO_14N	D6	RPHASE_UP_1	AU13	RTOAC_DATAO_4_1	U34	TCLKLI_2N
AD5	RDSO_4_3N/ RDSO_15N	F8	RPHASE_UP_2	AP14	RTOAC_DATAO_4_2	U35	TCLKLI_2P
AE4	RDSO_4_0P/ RDSO_12P	B5	RPHASE_UP_3	AR14	RTOAC_DATAO_4_3	W36	TCLKLI_3N
AF1	RDSO_4_1P/ RDSO_13P	D7	RPHASE_UP_4	AT9	RTOAC_SYNCO_1	W37	TCLKLI_3P
AE2	RDSO_4_2P/ RDSO_14P	AT22	RST_N	AT10	RTOAC_SYNCO_2	AB39	TCLKLI_4N
AD4	RDSO_4_3P/ RDSO_15P	AU9	RTOAC_CLKO_1	AV10	RTOAC_SYNCO_3	AB38	TCLKLI_4P
AR25	RDW_CLKO_1	AU10	RTOAC_CLKO_2	AV12	RTOAC_SYNCO_4	R36	TCLKLO_1N
AU27	RDW_CLKO_2	AW10	RTOAC_CLKO_3	D21	RW_N	R37	TCLKLO_1P
AU28	RDW_CLKO_3	AW12	RTOAC_CLKO_4	AN37	RXREFO_1N	N36	TCLKLO_2N
AV30	RDW_CLKO_4	AV8	RTOAC_DATAO_1_0	AN36	RXREFO_1P	N37	TCLKLO_2P
AR26	RDW_DATAO_1	AW8	RTOAC_DATAO_1_1	AP33	RXREFO_2N	K38	TCLKLO_3N
AV28	RDW_DATAO_2	AP11	RTOAC_DATAO_1_2	AR33	RXREFO_2P	K39	TCLKLO_3P
AW30	RDW_DATAO_3	AR11	RTOAC_DATAO_1_3	AV36	RXREFO_3N	H38	TCLKLO_4N
AV31	RDW_DATAO_4	AV9	RTOAC_DATAO_2_0	AW36	RXREFO_3P	H39	TCLKLO_4P
AP25	RDW_SYNCO_1	AW9	RTOAC_DATAO_2_1	AT34	RXREFO_4N	AA4	TCLKSI_1N
AW28	RDW_SYNCO_2	AP12	RTOAC_DATAO_2_2	AU34	RXREFO_4P	AA3	TCLKSI_1P

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
U5	TCLKSI_2N	L39	TDLO_2_1P/ TDLO_5P	V1	TDSI_1_0N/ TDSI_0N	P6	TDSI_3_0P/ TDSI_8P
U6	TCLKSI_2P	M37	TDLO_2_2P/ TDLO_6P	V3	TDSI_1_1N/ TDSI_1N	N4	TDSI_3_1P/ TDSI_9P
N1	TCLKSI_3N	J39	TDLO_2_3P/ TDLO_7P	V5	TDSI_1_2N/ TDSI_2N	M2	TDSI_3_2P/ TDSI_10P
N2	TCLKSI_3P	P35	TDLO_3_0N/ TDLO_8N	U1	TDSI_1_3N/ TDSI_3N	N6	TDSI_3_3P/ TDSI_11P
L1	TCLKSI_4N	N35	TDLO_3_1N/ TDLO_9N	V2	TDSI_1_0P/ TDSI_0P	K1	TDSI_4_0N/ TDSI_12N
L2	TCLKSI_4P	K36	TDLO_3_2N/ TDLO_10N	V4	TDSI_1_1P/ TDSI_1P	J1	TDSI_4_1N/ TDSI_13N
AP10	TDI	J36	TDLO_3_3N/ TDLO_11N	V6	TDSI_1_2P/ TDSI_2P	K3	TDSI_4_2N/ TDSI_14N
P38	TDLO_1_0N/ TDLO_0N	P34	TDLO_3_0P/ TDLO_8P	U2	TDSI_1_3P/ TDSI_3P	L5	TDSI_4_3N/ TDSI_15N
T34	TDLO_1_1N/ TDLO_1N	N34	TDLO_3_1P/ TDLO_9P	T3	TDSI_2_0N/ TDSI_4N	K2	TDSI_4_0P/ TDSI_12P
N38	TDLO_1_2N/ TDLO_2N	K37	TDLO_3_2P/ TDLO_10P	R1	TDSI_2_1N/ TDSI_5N	J2	TDSI_4_1P/ TDSI_13P
M38	TDLO_1_3N/ TDLO_3N	J37	TDLO_3_3P/ TDLO_11P	T5	TDSI_2_2N/ TDSI_6N	K4	TDSI_4_2P/ TDSI_14P
P39	TDLO_1_0P/ TDLO_0P	M35	TDLO_4_0N/ TDLO_12N	P1	TDSI_2_3N/ TDSI_7N	L6	TDSI_4_3P/ TDSI_15P
T35	TDLO_1_1P/ TDLO_1P	G38	TDLO_4_1N/ TDLO_13N	T4	TDSI_2_0P/ TDSI_4P	A27	TDW_CLKO_1
N39	TDLO_1_2P/ TDLO_2P	F38	TDLO_4_2N/ TDLO_14N	R2	TDSI_2_1P/ TDSI_5P	E27	TDW_CLKO_2
M39	TDLO_1_3P/ TDLO_3P	K34	TDLO_4_3N/ TDLO_15N	T6	TDSI_2_2P/ TDSI_6P	A30	TDW_CLKO_3
R35	TDLO_2_0N/ TDLO_4N	M34	TDLO_4_0P/ TDLO_12P	P2	TDSI_2_3P/ TDSI_7P	A31	TDW_CLKO_4
L38	TDLO_2_1N/ TDLO_5N	G39	TDLO_4_1P/ TDLO_13P	P5	TDSI_3_0N/ TDSI_8N	D27	TDW_DATAI_1
M36	TDLO_2_2N/ TDLO_6N	F39	TDLO_4_2P/ TDLO_14P	N3	TDSI_3_1N/ TDSI_9N	A29	TDW_DATAI_2
J38	TDLO_2_3N/ TDLO_7N	K35	TDLO_4_3P/ TDLO_15P	M1	TDSI_3_2N/ TDSI_10N	F28	TDW_DATAI_3
R34	TDLO_2_0P/ TDLO_4P	AW6	TDO	N5	TDSI_3_3N/ TDSI_11N	D30	TDW_DATAI_4

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
C27	TDW_DENI_1	E10	TTOAC_DATAI_1_0	B39	VDD	AM36	VDD
D28	TDW_DENI_2	F10	TTOAC_DATAI_1_1	C11	VDD	AM4	VDD
E28	TDW_DENI_3	A7	TTOAC_DATAI_1_2	C17	VDD	AT14	VDD
C30	TDW_DENI_4	B7	TTOAC_DATAI_1_3	C20	VDD	AT20	VDD
B27	TDW_SYNCO_1	C10	TTOAC_DATAI_2_0	C23	VDD	AT26	VDD
C28	TDW_SYNCO_2	D10	TTOAC_DATAI_2_1	C29	VDD	AT32	VDD
B30	TDW_SYNCO_3	E11	TTOAC_DATAI_2_2	D14	VDD	AT8	VDD
B31	TDW_SYNCO_4	F11	TTOAC_DATAI_2_3	D20	VDD	AU11	VDD
E22	TEA_N	E13	TTOAC_DATAI_3_0	D26	VDD	AU17	VDD
E29	TESTMODE	F13	TTOAC_DATAI_3_1	D32	VDD	AU20	VDD
U36	TFRMLI_1N	C12	TTOAC_DATAI_3_2	D8	VDD	AU23	VDD
U37	TFRMLI_1P	D12	TTOAC_DATAI_3_3	H36	VDD	AU29	VDD
U38	TFRMLI_2N	A13	TTOAC_DATAI_4_0	H4	VDD	AV1	VDD
U39	TFRMLI_2P	B13	TTOAC_DATAI_4_1	L35	VDD	AV2	VDD
V36	TFRMLI_3N	E14	TTOAC_DATAI_4_2	L37	VDD	AV20	VDD
V37	TFRMLI_3P	F14	TTOAC_DATAI_4_3	L4	VDD	AV38	VDD
AB37	TFRMLI_4N	A6	TTOAC_DENI_1	P36	VDD	AV39	VDD
AB36	TFRMLI_4P	A8	TTOAC_DENI_2	P4	VDD	AW1	VDD
AV7	TMS	A10	TTOAC_DENI_3	U4	VDD	AW2	VDD
G2	TPHASE_DW_1	C13	TTOAC_DENI_4	Y1	VDD	AW20	VDD
F2	TPHASE_DW_2	E9	TTOAC_SYNCO_1	Y2	VDD	AW38	VDD
J6	TPHASE_DW_3	C9	TTOAC_SYNCO_2	Y3	VDD	AW39	VDD
G4	TPHASE_DW_4	B10	TTOAC_SYNCO_3	Y4	VDD	AA5	VDD15
G1	TPHASE_UP_1	D13	TTOAC_SYNCO_4	Y36	VDD	AA6	VDD15
F1	TPHASE_UP_2	A1	VDD	Y37	VDD	AA34	VDD15
J5	TPHASE_UP_3	A2	VDD	Y38	VDD	AA35	VDD15
G3	TPHASE_UP_4	A20	VDD	Y39	VDD	AP19	VDD15
AW7	TRST_N	A38	VDD	AC37	VDD	AP20	VDD15
C19	TS_N	A39	VDD	AC5	VDD	AP21	VDD15
F9	TTOAC_CLKO_1	B1	VDD	AF36	VDD	AP34	VDD15
D9	TTOAC_CLKO_2	B2	VDD	AF4	VDD	AP35	VDD15
A9	TTOAC_CLKO_3	B20	VDD	AJ3	VDD	AP5	VDD15
A12	TTOAC_CLKO_4	B38	VDD	AJ37	VDD	AP6	VDD15

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.1 Pin Maps (continued)

Table 2. Pin Assignments for 792-Pin PBGAM1TH by Signal Name Order (continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
AR19	VDD15	W5	VDD15	AT17	VSS	C36	VSS
AR20	VDD15	W6	VDD15	AT23	VSS	C37	VSS
AR21	VDD15	Y34	VDD15	AT29	VSS	C4	VSS
AR34	VDD15	Y35	VDD15	AT3	VSS	C8	VSS
AR35	VDD15	Y5	VDD15	AT36	VSS	D11	VSS
AR5	VDD15	Y6	VDD15	AT37	VSS	D17	VSS
AR6	VDD15	B19	VSS	AT4	VSS	D23	VSS
E19	VDD15	B21	VSS	AU14	VSS	D29	VSS
E20	VDD15	A19	VSS	AU26	VSS	D3	VSS
E21	VDD15	A21	VSS	AU3	VSS	D36	VSS
E34	VDD15	AA1	VSS	AU32	VSS	D37	VSS
E35	VDD15	AA2	VSS	AU36	VSS	D4	VSS
E5	VDD15	AA38	VSS	AU37	VSS	H3	VSS
E6	VDD15	AA39	VSS	AU4	VSS	H37	VSS
F19	VDD15	AC36	VSS	AU8	VSS	L3	VSS
F20	VDD15	AC6	VSS	AV19	VSS	L34	VSS
F21	VDD15	AF3	VSS	AV21	VSS	L36	VSS
F34	VDD15	AF37	VSS	AW19	VSS	P3	VSS
F35	VDD15	AJ36	VSS	AW21	VSS	P37	VSS
F5	VDD15	AJ4	VSS	C14	VSS	U3	VSS
F6	VDD15	AM3	VSS	C26	VSS	W1	VSS
W34	VDD15	AM37	VSS	C3	VSS	W2	VSS
W35	VDD15	AT11	VSS	C32	VSS	W38	VSS
—	—	—	—	—	—	W39	VSS

Notes: No Connect refers to no connect pins. Do not connect pins so designated.

The second pin name (smaller font) is the pin in 10 Gbits/s mode.

2 Pin Information (continued)

2.2 Pin Descriptions

The following tables outline the individual pin descriptions grouped by functionality.

Table 3. Pin Descriptions—System Control

Pin	Symbol	Type*	Name/Description
AU22	IDDQ_N	I^u	**Global Pin 3-State Control (Active-Low).** This input incorporates hysteresis. 0 = All outputs assume a high-impedance state (except for JTAG test data output (TDO)). 1 = Normal operation.
AT22	RST_N	I^u	**Asynchronous Chip Reset (Active-Low).** This input incorporates hysteresis. To ensure proper reset, this input should be held low for a minimum of 26 ns. The device will not come out of reset until a clock is provided. 0 = Causes an asynchronous reset of the device. 1 = Normal operation.
C22	MPMODE_AS	I†	**Microprocessor Mode.** 1 = Synchronous mode. 0 = Asynchronous mode.
E15	MPTYPE_IM	I†	**Microprocessor *Intel*®/*Motorola*® Mode.** 1 = *Motorola* interface. 0 = *Intel* interface.
D15	MPDB_8_16	I†	**Microprocessor Data Bus Size.** 1 = 16-bit data bus. 0 = 8-bit data bus.
C15	MPPAREN	I†	**Microprocessor Parity Ignore Control.** 1 = Check parity during read/write operations. 0 = Ignore parity failures during read/write operations.
F15	PM_CLK	I^u/O	**One Second Performance Monitoring Clock.** The performance monitoring registers are updated on the rising edge of this signal. The internal PM anomaly counters are cleared at the same time. PM_CLK must be high for at least 250 ns, and low for at least 250 ns. The period of the performance monitoring clock will normally be 1 s, but the minimum period required for proper operation is 500 ns (during testing and development, for example).

* O = output, I^u = input with internal pull-up resistor. I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of all internal pull-up resistors is 100 kΩ.

† Input with 50 kΩ pull-up resistor.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 4. Pin Descriptions—Transmit Phase Detectors

Pin	Symbol	Type*	Name/Description
G2	TPHASE_DW_1	O	**Transmit Phase Detector Output Channel 1.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—used.
G1	TPHASE_UP_1	O	
F2	TPHASE_DW_2	O	**Transmit Phase Detector Output Channel 2.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—not used.
F1	TPHASE_UP_2	O	
J6	TPHASE_DW_3	O	**Transmit Phase Detector Output Channel 3.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—not used.
J5	TPHASE_UP_3	O	
G4	TPHASE_DW_4	O	**Transmit Phase Detector Output Channel 4.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—not used.
G3	TPHASE_UP_4	O	

* O = output. I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.

Table 5. Pin Descriptions—Receive Phase Detectors

Pin	Symbol	Type*	Name/Description
C6	RPHASE_DW_1	O	**Receive Phase Detector Output Channel 1.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—used.
D6	RPHASE_UP_1	O	
E8	RPHASE_DW_2	O	**Receive Phase Detector Output Channel 2.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—not used.
F8	RPHASE_UP_2	O	
A5	RPHASE_DW_3	O	**Receive Phase Detector Output Channel 3.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—not used.
B5	RPHASE_UP_3	O	
C7	RPHASE_DW_4	O	**Receive Phase Detector Output Channel 4.** — Quad 2.5 Gbits/s mode—used. — 10 Gbits/s mode—not used.
D7	RPHASE_UP_4	O	

* O = output. I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 6. Pin Descriptions—Receive Line Interface

Pin	10 G Mode Symbol	2.5 G Mode Symbol	Type*	Name/Description
AP38 AP39	RCLKLI_1P RCLKLI_1N	RCLKLI_1P RCLKLI_1N	I LVDS	**Receive Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—clock (666/622 MHz). — 10 Gbits/s mode–clock (669/622 MHz).
AN36 AN37	RXREFO_1P RXREFO_1N	RXREFO_1P RXREFO_1N	O LVDS	**Receive Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—line timing reference (8 kHz). — 10 Gbits/s mode—line timing reference (8 kHz).
AK34 AK35	RDLI_0P RDLI_0N	RDLI_1_0P RDLI_1_0N	I LVDS	**Receive Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 0 (LSB).
AL36 AL37	RDLI_1P RDLI_1N	RDLI_1_1P RDLI_1_1N	I LVDS	**Receive Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 1.
AM38 AM39	RDLI_2P RDLI_2N	RDLI_1_2P RDLI_1_2N	I LVDS	**Receive Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 2.
AJ34 AJ35	RDLI_3P RDLI_3N	RDLI_1_3P RDLI_1_3N	I LVDS	**Receive Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 3.
AL38 AL39	—	RCLKLI_2P RCLKLI_2N	I LVDS	**Receive Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—clock (666/622 MHz). — 10 Gbits/s mode—not used.
AR33 AP33	—	RXREFO_2P RXREFO_2N	O LVDS	**Receive Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—line timing reference (8 kHz). — 10 Gbits/s mode—not used.
AH34 AH35	RDLI_4P RDLI_4N	RDLI_2_0P RDLI_2_0N	I LVDS	**Receive Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 4.
AK38 AK39	RDLI_5P RDLI_5N	RDLI_2_1P RDLI_2_1N	I LVDS	**Receive Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 5.
AJ38 AJ39	RDLI_6P RDLI_6N	RDLI_2_2P RDLI_2_2N	I LVDS	**Receive Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 6.
AH36 AH37	RDLI_7P RDLI_7N	RDLI_2_3P RDLI_2_3N	I LVDS	**Receive Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 7.

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 6. Pin Descriptions—Receive Line Interface (continued)

Pin	10 G Mode Symbol	2.5 G Mode Symbol	Type*	Name/Description
AH38 AH39	—	RCLKLI_3P RCLKLI_3N	I LVDS	**Receive Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—clock (666/622 MHz). — 10 Gbits/s mode—not used.
AW36 AV36	—	RXREFO_3P RXREFO_3N	O LVDS	**Receive Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—line timing reference (8 kHz). — 10 Gbits/s mode—not used.
AF34 AF35	RDLI_8P RDLI_8N	RDLI_3_0P RDLI_3_0N	I LVDS	**Receive Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 8.
AG38 AG39	RDLI_9P RDLI_9N	RDLI_3_1P RDLI_3_1N	I LVDS	**Receive Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 9.
AE34 AE35	RDLI_10P RDLI_10N	RDLI_3_2P RDLI_3_2N	I LVDS	**Receive Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 10.
AF38 AF39	RDLI_11P RDLI_11N	RDLI_3_3P RDLI_3_3N	I LVDS	**Receive Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 11.
AD34 AD35	—	RCLKLI_4P RCLKLI_4N	I LVDS	**Receive Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—clock (666/622 MHz). — 10 Gbits/s mode—not used.
AU34 AT34	—	RXREFO_4P RXREFO_4N	O LVDS	**Receive Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—line timing reference (8 kHz). — 10 Gbits/s mode—not used.
AD36 AD37	RDLI_12P RDLI_12N	RDLI_4_0P RDLI_4_0N	I LVDS	**Receive Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 12.
AD38 AD39	RDLI_13P RDLI_13N	RDLI_4_1P RDLI_4_1N	I LVDS	**Receive Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 13.
AC34 AC35	RDLI_14P RDLI_14N	RDLI_4_2P RDLI_4_2N	I LVDS	**Receive Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 14.
AC38 AC39	RDLI_15P RDLI_15N	RDLI_4_3P RDLI_4_3N	I LVDS	**Receive Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 15 (MSB).

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 7. Pin Descriptions—LVDS Reference, Line Interface

Pin	Symbol	Type*	Name/Description
AN39	CTAP_RDLI1	I	**Center Tap for RDLI_1 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RDLI_[0:3]/RDLI_1_[0:3], Table 6 on page 20).
AG34	CTAP_RDLI2	I	**Center Tap for RDLI_2 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RDLI_[4:7]/RDLI_2_[4:7], Table 6 on page 20).
AE36	CTAP_RDLI3	I	**Center Tap for RDLI_3 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RDLI_[8:11]/RDLI_3_[8:11], Table 6 on page 21).
AE38	CTAP_RDLI4	I	**Center Tap for RDLI_4 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RDLI_[12:15]/RDLI_4_[12:15], Table 6 on page 21).
AL35	CTAP_RCLKLI1	I	**Center Tap for RCLKLI_1 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKLI_1, Table 6 on page 20).
AK37	CTAP_RCLKLI2	I	**Center Tap for RCLKLI_2 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKLI_2, Table 6 on page 20).
AG36	CTAP_RCLKLI3	I	**Center Tap for RCLKLI_3 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKLI_3, Table 6 on page 21).
AE37	CTAP_RCLKLI4	I	**Center Tap for RCLKLI_4 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKLI_4, Table 6 on page 21).
AB2	CTAP_RCLKSI1	I	**Center Tap for RCLKSI_1 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKSI_1, Table 8 on page 23).
AB5	CTAP_RCLKSI2	I	**Center Tap for RCLKSI_2 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKSI_2, Table 8 on page 23).
AD1	CTAP_RCLKSI3	I	**Center Tap for RCLKSI_3 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKSI_3, Table 8 on page 24).
AE1	CTAP_RCLKSI4	I	**Center Tap for RCLKSI_4 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see RCLKSI_4, Table 8 on page 24).
AR31	LVDS_LREF10	I	**1.0 V ± 3% Reference Voltage for Line-Side LVDS Interface I/Os.** **Note:** A suggested schematic diagram is given in Figure 1 on page 28.
AP31	LVDS_LREF14	I	**1.4 V ± 3% Reference Voltage for Line-Side LVDS Interface I/Os.** **Note:** A suggested schematic diagram is given in Figure 1 on page 28.
AR32	LVDS_LRESHI	I	**Connect a 100 Ω ± 1% resistor between these pins.**
AP32	LVDS_LRESLO	I	

* I = input.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 8. Pin Descriptions—Receive System Interface

Pin	10 G Mode Symbol	2.5 G Mode Symbol	Type*	Name/Description
AB3 AB4	RCLKSI_1P RCLKSI_1N	RCLKSI_1P RCLKSI_1N	I LVDS	**Receive System Interface Channel 1.** — Quad 2.5 Gbits/s mode—input clock (622 MHz). — 10 Gbits/s mode—input clock (622 MHz).
AN3 AN4	RCLKSO_1P RCLKSO_1N	RCLKSO_1P RCLKSO_1N	O LVDS	**Receive System Interface Channel 1.** — Quad 2.5 Gbits/s mode—output clock (622 MHz). — 10 Gbits/s mode—output clock (622 MHz).
AL5 AL6	RDSO_0P RDSO_0N	RDSO_1_0P RDSO_1_0N	O LVDS	**Receive System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 0 (LSB).
AP1 AP2	RDSO_1P RDSO_1N	RDSO_1_1P RDSO_1_1N	O LVDS	**Receive System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 1.
AN1 AN2	RDSO_2P RDSO_2N	RDSO_1_2P RDSO_1_2N	O LVDS	**Receive System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 2.
AK5 AK6	RDSO_3P RDSO_3N	RDSO_1_3P RDSO_1_3N	O LVDS	**Receive System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 3.
AC1 AC2	—	RCLKSI_2P RCLKSI_2N	I LVDS	**Receive System Interface Channel 2.** — Quad 2.5 Gbits/s mode—input clock (622 MHz). — 10 Gbits/s mode—not used.
AL3 AL4	—	RCLKSO_2P RCLKSO_2N	O LVDS	**Receive System Interface Channel 2.** — Quad 2.5 Gbits/s mode—output clock (622 MHz). — 10 Gbits/s mode—not used.
AM1 AM2	RDSO_4P RDSO_4N	RDSO_2_0P RDSO_2_0N	O LVDS	**Receive System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 4.
AH5 AH6	RDSO_5P RDSO_5N	RDSO_2_1P RDSO_2_1N	O LVDS	**Receive System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 5.
AK3 AK4	RDSO_6P RDSO_6N	RDSO_2_2P RDSO_2_2N	O LVDS	**Receive System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 6.
AL1 AL2	RDSO_7P RDSO_7N	RDSO_2_3P RDSO_2_3N	O LVDS	**Receive System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 7.

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 8. Pin Descriptions—Receive System Interface (continued)

Pin	10 G Mode Symbol	2.5 G Mode Symbol	Type*	Name/Description
AC3 AC4	—	RCLKSI_3P RCLKSI_3N	I LVDS	**Receive System Interface Channel 3.** — Quad 2.5 Gbits/s mode—input clock (622 MHz). — 10 Gbits/s mode—not used.
AH3 AH4	—	RCLKSO_3P RCLKSO_3N	O LVDS	**Receive System Interface Channel 3.** — Quad 2.5 Gbits/s mode—output clock (622 MHz). — 10 Gbits/s mode—not used.
AK1 AK2	RDSO_8P RDSO_8N	RDSO_3_0P RDSO_3_0N	O LVDS	**Receive System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 8.
AJ1 AJ2	RDSO_9P RDSO_9N	RDSO_3_1P RDSO_3_1N	O LVDS	**Receive System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 9.
AH1 AH2	RDSO_10P RDSO_10N	RDSO_3_2P RDSO_3_2N	O LVDS	**Receive System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 10.
AG3 AG4	RDSO_11P RDSO_11N	RDSO_3_3P RDSO_3_3N	O LVDS	**Receive System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 11.
AD2 AD3	—	RCLKSI_4P RCLKSI_4N	I LVDS	**Receive System Interface Channel 4.** — Quad 2.5 Gbits/s mode—input clock (622 MHz). — 10 Gbits/s mode—not used.
AG1 AG2	—	RCLKSO_4P RCLKSO_4N	O LVDS	**Receive System Interface Channel 4.** — Quad 2.5 Gbits/s mode—output clock (622 MHz). — 10 Gbits/s mode—not used.
AE4 AE5	RDSO_12P RDSO_12N	RDSO_4_0P RDSO_4_0N	O LVDS	**Receive System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 12.
AF1 AF2	RDSO_13P RDSO_13N	RDSO_4_1P RDSO_4_1N	O LVDS	**Receive System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 13.
AE2 AE3	RDSO_14P RDSO_14N	RDSO_4_2P RDSO_4_2N	O LVDS	**Receive System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 14.
AD4 AD5	RDSO_15P RDSO_15N	RDSO_4_3P RDSO_4_3N	O LVDS	**Receive System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 15 (MSB).

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 9. Pin Descriptions—Transmit System Interface

Pin	10 G Mode Symbol	2.5 G Mode Symbol	Type*	Name/Description
AA3 AA4	TCLKSI_1P TCLKSI_1N	TCLKSI_1P TCLKSI_1N	I LVDS	**Transmit System Interface Channel 1.** — Quad 2.5 Gbits/s mode—clock (622 MHz). — 10 Gbits/s mode—clock (622 MHz).
V2 V1	TDSI_0P TDSI_0N	TDSI_1_0P TDSI_1_0N	I LVDS	**Transmit System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 0 (LSB).
V4 V3	TDSI_1P TDSI_1N	TDSI_1_1P TDSI_1_1N	I LVDS	**Transmit System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 1.
V6 V5	TDSI_2P TDSI_2N	TDSI_1_2P TDSI_1_2N	I LVDS	**Transmit System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 2.
U2 U1	TDSI_3P TDSI_3N	TDSI_1_3P TDSI_1_3N	I LVDS	**Transmit System Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 3.
U6 U5	—	TCLKSI_2P TCLKSI_2N	I LVDS	**Transmit System Interface Channel 2.** — Quad 2.5 Gbits/s mod—clock (622 MHz). — 10 Gbits/s mode—not used.
T4 T3	TDSI_4P TDSI_4N	TDSI_2_0P TDSI_2_0N	I LVDS	**Transmit System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 4.
R2 R1	TDSI_5P TDSI_5N	TDSI_2_1P TDSI_2_1N	I LVDS	**Transmit System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 5.
T6 T5	TDSI_6P TDSI_6N	TDSI_2_2P TDSI_2_2N	I LVDS	**Transmit System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 6.
P2 P1	TDSI_7P TDSI_7N	TDSI_2_3P TDSI_2_3N	I LVDS	**Transmit System Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 7.

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 9. Pin Descriptions—Transmit System Interface (continued)

Pin	10 G Mode Symbol	2.5 G Mode Symbol	Type*	Name/Description
N2 N1	—	TCLKSI_3P TCLKSI_3N	I LVDS	**Transmit System Interface Channel 3.** — Quad 2.5 Gbits/s mode—clock (622 MHz). — 10 Gbits/s mode—not used.
P6 P5	TDSI_8P TDSI_8N	TDSI_3_0P TDSI_3_0N	I LVDS	**Transmit System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 8.
N4 N3	TDSI_9P TDSI_9N	TDSI_3_1P TDSI_3_1N	I LVDS	**Transmit System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 9.
M2 M1	TDSI_10P TDSI_10N	TDSI_3_2P TDSI_3_2N	I LVDS	**Transmit System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 10.
N6 N5	TDSI_11P TDSI_11N	TDSI_3_3P TDSI_3_3N	I LVDS	**Transmit System Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 11.
L2 L1	—	TCLKSI_4P TCLKSI_4N	I LVDS	**Transmit System Interface Channel 4.** — Quad 2.5 Gbits/s mode—clock (622 MHz). — 10 Gbits/s mode—not used.
K2 K1	TDSI_12P TDSI_12N	TDSI_4_0P TDSI_4_0N	I LVDS	**Transmit System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 12.
J2 J1	TDSI_13P TDSI_13N	TDSI_4_1P TDSI_4_1N	I LVDS	**Transmit System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 13.
K4 K3	TDSI_14P TDSI_14N	TDSI_4_2P TDSI_4_2N	I LVDS	**Transmit System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 14.
L6 L5	TDSI_15P TDSI_15N	TDSI_4_3P TDSI_4_3N	I LVDS	**Transmit System Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 15 (MSB).

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 10. Pin Descriptions—LVDS Reference, Transmit System/Line Interface

Pin	Symbol	Type*	Name/Description
W4	CTAP_TDSI_1	I	**Center Tap for TDSI_1 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TDSI_[0:3]/TDSI_1_[3:0], Table 9 on page 25).
R4	CTAP_TDSI_2	I	**Center Tap for TDSI_2 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TDSI_[4:7]/TDSI_2_[3:0], Table 9 on page 25).
M3	CTAP_TDSI_3	I	**Center Tap for TDSI_3 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TDSI_[8:11]/TDSI_3_[3:0], Table 9 on page 26).
M6	CTAP_TDSI_4	I	**Center Tap for TDSI_4 Inputs.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TDSI_[12:15]/TDSI_4_[3:0], Table 9 on page 26).
AB1	CTAP_TCLKSI_1	I	**Center Tap for TCLKSI_1 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKSI_1, Table 9 on page 25).
T2	CTAP_TCLKSI_2	I	**Center Tap for TCLKSI_2 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKSI_2, Table 9 on page 25).
R6	CTAP_TCLKSI_3	I	**Center Tap for TCLKSI_3 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKSI_3, Table 9 on page 26).
M4	CTAP_TCLKSI_4	I	**Center Tap for TCLKSI_4 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKSI_4, Table 9 on page 26).
R38	CTAP_TCLKLI_1	I	**Center Tap for TCLKLI_1 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKLI_1, Table 11 on page 29).
T39	CTAP_TCLKLI_2	I	**Center Tap for TCLKLI_2 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKLI_2, Table 11 on page 29).
V39	CTAP_TCLKLI_3	I	**Center Tap for TCLKLI_3 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKLI_3, Table 11 on page 30).
AA36	CTAP_TCLKLI_4	I	**Center Tap for TCLKLI_4 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TCLKLI_4, Table 11 on page 30).
R39	CTAP_TFRMLI_1	I	**Center Tap for TFRMLI_1 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TFRMLI_1, Table 11 on page 29).
V34	CTAP_TFRMLI_2	I	**Center Tap for TFRMLI_2 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TFRMLI_2, Table 11 on page 29).
V38	CTAP_TFRMLI_3	I	**Center Tap for TFRMLI_3 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TFRMLI_3, Table 11 on page 30).

* I = input.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 10. Pin Descriptions—LVDS Reference, Transmit System/Line Interface (continued)

Pin	Symbol	Type*	Name/Description
AB35	CTAP_TFRMLI_4	I	**Center Tap for TFRMLI_4 Input.** Provides center-tapped common-mode termination. This input should be terminated through an external 0.01 µF capacitor to ground (see TFRMLI_4, Table 11 on page 30).
AF5	LVDS_SREF10	I	1.0 V ± 3% reference voltage for system-side LVDS interface I/Os. **Note:** A suggested schematic diagram is given in Figure 1.
AF6	LVDS_SREF14	I	1.4 V ± 3% reference voltage for system-side LVDS interface I/Os. **Note:** A suggested schematic diagram is given in Figure 1.
AG5	LVDS_SRESHI	I	Connect a 100 Ω ± 1% resistor between these pins.
AG6	LVDS_SRESLO	I	

* I = input.

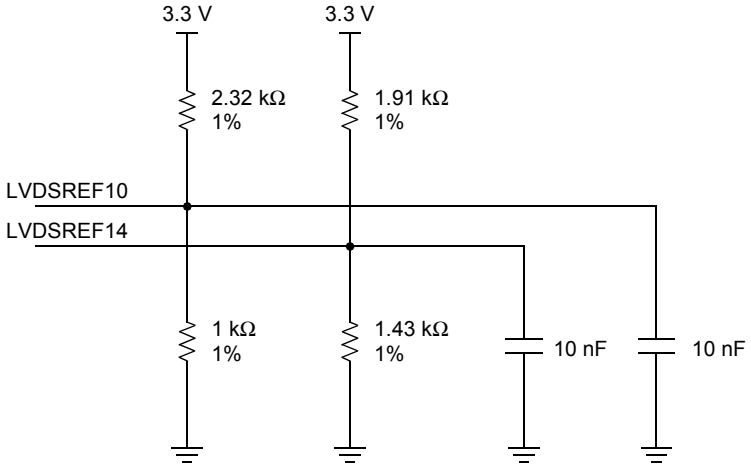


Figure 1. Suggested Schematic for 1.0 V and 1.4 V Reference Voltages

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 11. Pin Descriptions—Transmit Line Interface

Pin	10 Gbits/s Mode Symbol	2.5 Gbits/s Mode Symbol	Type*	Name/Description
T37 T36	TCLKLI_1P TCLKLI_1N	TCLKLI_1P TCLKLI_1N	I LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—input clock (666/669/622 MHz). — 10 Gbits/s mode—input clock (669/622 MHz).
U37 U36	TFRMLI_1P TFRMLI_1N	TFRMLI_1P TFRMLI_1N	I LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—DW frame alignment frame sync. — 10 Gbits/s mode—DW frame alignment frame sync (any multiple of the DW frame rate).
R37 R36	TCLKLO_1P TCLKLO_1N	TCLKLO_1P TCLKLO_1N	O LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—output clock (666/669/622 MHz). — 10 Gbits/s mode—output clock (669/622 MHz)
P39 P38	TDLO_0P TDLO_0N	TDLO_1_0P TDLO_1_0N	O LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 0 (LSB).
T35 T34	TDLO_1P TDLO_1N	TDLO_1_1P TDLO_1_1N	O LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 1.
N39 N38	TDLO_2P TDLO_2N	TDLO_1_2P TDLO_1_2N	O LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 2.
M39 M38	TDLO_3P TDLO_3N	TDLO_1_3P TDLO_1_3N	O LVDS	**Transmit Line Interface Channel 1.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 3.
U35 U34	—	TCLKLI_2P TCLKLI_2N	I LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—clock (666/622 MHz). — 10 Gbits/s mode—not used.
U39 U38	—	TFRMLI_2P TFRMLI_2N	I LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—DW frame alignment frame sync. — 10 Gbits/s mode—not used.
N37 N36	—	TCLKO_2P TCLKO_2N	O LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—output clock (666/622 MHz). — 10 Gbits/s mode—not used.
R34 R35	TDLO_4P TDLO_4N	TDLO_2_0P TDLO_2_0N	O LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 4.
L39 L38	TDLO_5P TDLO_5N	TDLO_2_1P TDLO_2_1N	O LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 5.
M37 M36	TDLO_6P TDLO_6N	TDLO_2_2P TDLO_2_2N	O LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 6.
J39 J38	TDLO_7P TDLO_7N	TDLO_2_3P TDLO_2_3N	O LVDS	**Transmit Line Interface Channel 2.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 7.

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 11. Pin Descriptions—Transmit Line Interface (continued)

Pin	10 Gbits/s Mode Symbol	2.5 Gbits/s Mode Symbol	Type*	Name/Description
W37 W36	—	TCLKLI_3P TCLKLI_3N	I LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—input clock (666/622 MHz). — 10 Gbits/s mode—not used.
V37 V36	—	TFRMLI_3P TFRMLI_3N	I LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—DW frame alignment frame sync. — 10 Gbits/s mode—not used.
K39 K38	—	TCLKLO_3P TCLKLO_3N	O LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—output clock (666/622 MHz). — 10 Gbits/s mode—not used.
P34 P35	TDLO_8P TDLO_8N	TDLO_3_0P TDLO_3_0N	O LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 8.
N34 N35	TDLO_9P TDLO_9N	TDLO_3_1P TDLO_3_1N	O LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 9.
K37 K36	TDLO_10P TDLO_10N	TDLO_3_2P TDLO_3_2N	O LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 10.
J37 J36	TDLO_11P TDLO_11N	TDLO_3_3P TDLO_3_3N	O LVDS	**Transmit Line Interface Channel 3.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 11.
AB38 AB39	—	TCLKLI_4P TCLKLI_4N	I LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—clock (666/622 MHz). — 10 Gbits/s mode—not used.
AB36 AB37	—	TFRMLI_4P TFRMLI_4N	I LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—DW frame alignment frame sync. — 10 Gbits/s mode—not used.
H39 H38	—	TCLKLO_4P TCLKLO_4N	O LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—output clock (666/622 MHz). — 10 Gbits/s mode—not used.
M34 M35	TDLO_12P TDLO_12N	TDLO_4_0P TDLO_4_0N	O LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 0 (LSB). — 10 Gbits/s mode—bit 12.
G39 G38	TDLO_13P TDLO_13N	TDLO_4_1P TDLO_4_1N	O LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 1. — 10 Gbits/s mode—bit 13.
F39 F38	TDLO_14P TDLO_14N	TDLO_4_2P TDLO_4_2N	O LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 2. — 10 Gbits/s mode—bit 14.
K35 K34	TDLO_15P TDLO_15N	TDLO_4_3P TDLO_4_3N	O LVDS	**Transmit Line Interface Channel 4.** — Quad 2.5 Gbits/s mode—bit 3 (MSB). — 10 Gbits/s mode—bit 15 (MSB).

* I = input, O = output, LVDS = low-voltage differential signal.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 12. Pin Descriptions—Receive Section/Line Overhead Interface (Drop)

Pin	Symbol	Type*	Name/Description
AU9	RTOAC_CLKO_1	O	**Receive Channel 1 TOAC Drop Clock.** — Quad 2.5 Gbits/s mode—TOAC drop clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC drop clock (20.736 MHz/not used)†.
AT9	RTOAC_SYNCO_1	O	**Receive Channel 1 TOAC Drop Sync.** — Quad 2.5 Gbits/s mode—TOAC drop sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC drop sync (8 kHz/not used)†.
AV8	RTOAC_DATAO_1_0	O	**Receive Channel 1 TOAC Drop Data.** — Quad 2.5 Gbits/s mode—TOAC drop data (20.736/1.728[0] Mbits/s)† (in partial TOAC mode, only bit 0 is valid). — 10 Gbits/s mode—TOAC drop data (20.736 Mbits/s/not used)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #145—192] modes.
AW8	RTOAC_DATAO_1_1	O	
AP11	RTOAC_DATAO_1_2	O	
AR11	RTOAC_DATAO_1_3	O	
AU10	RTOAC_CLKO_2	O	**Receive Channel 2 TOAC Drop Clock.** — Quad 2.5 Gbits/s mode—TOAC drop clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC drop clock (20.736 MHz/not used)†.
AT10	RTOAC_SYNCO_2	O	**Receive Channel 2 TOAC Drop Sync.** — Quad 2.5 Gbits/s mode—TOAC drop sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC drop sync (8 kHz/not used)†.
AV9	RTOAC_DATAO_2_0	O	**Receive Channel 2 TOAC Drop Data.** — Quad 2.5 Gbits/s mode—TOAC drop data (20.736/1.728[0] Mbits/s)† (in partial TOAC mode, only bit 0 is valid). — 10 Gbits/s mode—TOAC drop data (20.736 Mbits/s/not used)†. **Note:** MSB= bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #97—144] modes.
AW9	RTOAC_DATAO_2_1	O	
AP12	RTOAC_DATAO_2_2	O	
AR12	RTOAC_DATAO_2_3	O	

* O = output. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.
† The frequencies in the parenthesis are for full mode and partial mode, respectively.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 12. Pin Descriptions—Receive Section/Line Overhead Interface (Drop) (continued)

Pin	Symbol	Type*	Name/Description
AW10	RTOAC_CLKO_3	O	**Receive Channel 3 TOAC Drop Clock.** — Quad 2.5 Gbits/s mode—TOAC drop clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC drop clock (20.736 MHz/not used)†.
AV10	RTOAC_SYNCO_3	O	**Receive Channel 3 TOAC Drop Sync.** — Quad 2.5 Gbits/s mode—TOAC drop sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC drop sync (8 kHz/not used)†.
AT12	RTOAC_DATAO_3_0	O	**Receive Channel 3 TOAC Drop Data.** — Quad 2.5 Gbits/s mode—TOAC serial drop data (20.736/1.728[0] Mbits/s†; in partial TOAC mode, only bit 0 is valid). — 10 Gbits/s mode—TOAC serial drop data (20.736 Mbits/s/not used)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #49—96] modes.
AU12	RTOAC_DATAO_3_1	O	
AP13	RTOAC_DATAO_3_2	O	
AR13	RTOAC_DATAO_3_3	O	
AW12	RTOAC_CLKO_4	O	**Receive Channel 4 TOAC Drop Clock.** — Quad 2.5 Gbits/s mode—TOAC drop clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC drop clock (20.736/1.728 MHz)†.
AV12	RTOAC_SYNCO_4	O	**Receive Channel 4 TOAC Drop Sync.** — Quad 2.5 Gbits/s mode—TOAC drop sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC drop sync (8/8 kHz)†.
AT13	RTOAC_DATAO_4_0	O	**Receive Channel 4 TOAC Drop Data.** — Quad 2.5 Gbits/s mode—TOAC serial drop data (20.736/1.728[0] Mbits/s)† (in partial TOAC mode, only bit 0 is valid). — 10 Gbits/s mode—TOAC serial drop data (20.736/1.728 Mbits/s)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #1—48] modes.
AU13	RTOAC_DATAO_4_1	O	
AP14	RTOAC_DATAO_4_2	O	
AR14	RTOAC_DATAO_4_3	O	

* O = output. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.
† The frequencies in the parenthesis are for full mode and partial mode, respectively.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 13. Pin Descriptions—Transmit Section/Line Overhead Interface (Insert)

Pin	Symbol	Type*	Name/Description
F9	TTOAC_CLKO_1	O	**Transmit Channel 1 TOAC Insert Clock.** — Quad 2.5 Gbits/s mode—TOAC insert clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC insert clock (20.736 MHz/not used)†.
E9	TTOAC_SYNCO_1	O	**Transmit Channel 1 TOAC Insert Sync.** — Quad 2.5 Gbits/s mode—TOAC insert sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC insert sync (8 kHz/not used)†.
A6	TTOAC_DENI_1	Id	**Transmit Channel 1 TOAC Insert Enable.** — Quad 2.5 Gbits/s mode—TOAC insert enable. — 10 Gbits/s mode—TOAC insert enable.
E10	TTOAC_DATAI_1_0	Id	**Transmit Channel 1 TOAC Data.** — Quad 2.5 Gbits/s mode—TOAC data (20.736/1.728 [0] Mbits/s)†. — 10 Gbits/s mode—TOAC data (20.736 Mbits/s/not used)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #145—192] modes.
F10	TTOAC_DATAI_1_1	Id	
A7	TTOAC_DATAI_1_2	Id	
B7	TTOAC_DATAI_1_3	Id	
D9	TTOAC_CLKO_2	O	**Transmit Channel 2 TOAC Insert Clock.** — Quad 2.5 Gbits/s mode—TOAC insert clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC insert clock (20.736 MHz/not used)†.
C9	TTOAC_SYNCO_2	O	**Transmit Channel 2 TOAC Insert Sync.** — Quad 2.5 Gbits/s mode—TOAC insert sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC insert sync (8 kHz/not used)†.
A8	TTOAC_DENI_2	Id	**Transmit Channel 2 TOAC Insert Enable.** — Quad 2.5 Gbits/s mode—TOAC insert enable. — 10 Gbits/s mode—TOAC insert enable.
C10	TTOAC_DATAI_2_0	Id	**Transmit Channel 2 TOAC Data.** — Quad 2.5 Gbits/s mode—TOAC data (20.736/1.728 [0] Mbits/s)†. — 10 Gbits/s mode—TOAC data (20.736 Mbits/s/not used)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #97—144] modes.
D10	TTOAC_DATAI_2_1	Id	
E11	TTOAC_DATAI_2_2	Id	
F11	TTOAC_DATAI_2_3	Id	

* O = output, Id = input with internal pull-down resistor. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of all internal pull-down resistors is 50 kΩ.

† The frequencies in the parenthesis are for full mode and partial mode, respectively.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 13. Pin Descriptions—Transmit Section/Line Overhead Interface (Insert) (continued)

Pin	Symbol	Type*	Name/Description
A9	TTOAC_CLKO_3	O	**Transmit Channel 3 TOAC Insert Clock.** — Quad 2.5 Gbits/s mode—TOAC insert clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC insert clock (20.736 MHz/not used)†.
B10	TTOAC_SYNCO_3	O	**Transmit Channel 3 TOAC Insert Sync.** — Quad 2.5 Gbits/s mode—TOAC insert sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC insert sync (8 kHz/not used)†.
A10	TTOAC_DENI_3	Id	**Transmit Channel 3 TOAC Insert Enable.** — Quad 2.5 Gbits/s mode—TOAC insert enable. — 10 Gbits/s mode—TOAC insert enable.
E13	TTOAC_DATAI_3_0	Id	**Transmit Channel 3 TOAC Data.** — Quad 2.5 Gbits/s mode—TOAC data (20.736/1.728[0] Mbits/s)†. — 10 Gbits/s mode—TOAC data (20.736 Mbits/s/not used)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #49—96] modes.
F13	TTOAC_DATAI_3_1	Id	
C12	TTOAC_DATAI_3_2	Id	
D12	TTOAC_DATAI_3_3	Id	
A12	TTOAC_CLKO_4	O	**Transmit Channel 4 TOAC Insert Clock.** — Quad 2.5 Gbits/s mode—TOAC insert clock (20.736/1.728 MHz)†. — 10 Gbits/s mode—TOAC insert clock (20.736/1.728 MHz)†.
D13	TTOAC_SYNCO_4	O	**Transmit Channel 4 TOAC Insert Sync.** — Quad 2.5 Gbits/s mode—TOAC insert sync (8/8 kHz)†. — 10 Gbits/s mode—TOAC insert sync (8/8 kHz)†.
C13	TTOAC_DENI_4	Id	**Transmit Channel 4 TOAC Insert Enable.** — Quad 2.5 Gbits/s mode—TOAC insert enable. — 10 Gbits/s mode— TOAC insert enable.
A13	TTOAC_DATAI_4_0	Id	**Transmit Channel 4 TOAC Data.** — Quad 2.5 Gbits/s mode—TOAC data (20.736/1.728[0] Mbits/s)†. — 10 Gbits/s mode—TOAC data (20.736/1.728 Mbits/s)†. **Note:** MSB = bit 3, LSB = bit 0, valid in both quad 2.5 Gbits/s/10 Gbits/s [STS-1s, #1—48] modes.
B13	TTOAC_DATAI_4_1	Id	
E14	TTOAC_DATAI_4_2	Id	
F14	TTOAC_DATAI_4_3	Id	

* O = output, Id = input with internal pull-down resistor. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of all internal pull-down resistors is 50 kΩ.

† The frequencies in the parenthesis are for full mode and partial mode, respectively.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 14. Pin Descriptions—Receive FEC/Digital Wrapper Overhead Drop (FEC/DW) Interface

Pin	Symbol	Type*	Name/Description
AR25	RDW_CLKO_1	O	**Receive DWAC Channel 1 Drop Clock.** — Quad 2.5 Gbits/s mode—FEC/DW drop clock (~10.455/~10.455 MHz)†. — 10 Gbits/s mode—FEC/DW drop clock (~10.455/~10.455 MHz)†.
AP25	RDW_SYNCO_1	O	**Receive DWAC Channel 1 Drop Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW drop superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—FEC/DW drop superframe sync (~326.7/~81.68 kHz)†.
AR26	RDW_DATAO_1	O	**Receive DWAC Channel 1 Drop Data.** — Quad 2.5 Gbits/s mode—FEC/DW drop data (~10.455 Mbits/s)†. — 10 Gbits/s mode—FEC/DW drop data bit 1 of 4 (LSB) (~10.455 Mbits/s)†.
AU27	RDW_CLKO_2	O	**Receive DWAC Channel 2 Drop Clock.** — Quad 2.5 Gbits/s mode—FEC/DW drop clock (~10.455 MHz)†. — 10 Gbits/s mode—not used.
AW28	RDW_SYNCO_2	O	**Receive DWAC Channel 2 Drop Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW drop superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—not used.
AV28	RDW_DATAO_2	O	**Receive DWAC Channel 2 Drop Data.** — Quad 2.5 Gbits/s mode—FEC/DW drop data (~10.455 MHz)†. — 10 Gbits/s mode—FEC/DW drop data bit 2 of 4 (~10.455 Mbits/s)†.
AU28	RDW_CLKO_3	O	**Receive DWAC Channel 3 Drop Clock.** — Quad 2.5 Gbits/s mode—FEC/DW drop clock (~10.455 MHz)†. — 10 Gbits/s mode—not used.
AW29	RDW_SYNCO_3	O	**Receive DWAC Channel 3 Drop Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW drop superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—not used.
AW30	RDW_DATAO_3	O	**Receive DWAC Channel 3 Drop Data.** — Quad 2.5 Gbits/s mode—FEC/DW drop data (~10.455 Mbits/s)†. — 10 Gbits/s mode—FEC/DW drop data bit 3 of 4 (~10.455 Mbits/s)†.
AV30	RDW_CLKO_4	O	**Receive DWAC Channel 4 Drop Clock.** — Quad 2.5 Gbits/s mode—FEC/DW drop clock (~10.455 MHz)†. — 10 Gbits/s mode—FEC/DW not used.
AW31	RDW_SYNCO_4	O	**Receive DWAC Channel 3 Drop Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW drop superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—not used.
AV31	RDW_DATAO_4	O	**Receive DWAC Channel 4 Drop Data.** — Quad 2.5 Gbits/s mode—FEC/DW drop data (~10.455 Mbits/s)†. — 10 Gbits/s mode—FEC/DW drop data bit 4 of 4 MSB (~10.455 Mbits/s)†.

* O = output. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.
† The frequencies in the parenthesis are the FEC rate and DW rate, respectively.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 15. Pin Descriptions—Transmit Digital Wrapper Overhead Insert Interface

Pin	Symbol	Type*	Name/Description
A27	TDW_CLKO_1	O	**Transmit DWAC (FEC/DW) Channel 1 Insert Clock.** — Quad 2.5 Gbits/s mode—FEC/DW insert clock (~10.455/~10.455 MHz)†. — 10 Gbits/s mode—FEC/DW insert clock (~10.455/~10.455 MHz)†.
B27	TDW_SYNCO_1	O	**Transmit DWAC (FEC/DW) Channel 1 Insert Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW insert superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—FEC/DW insert superframe sync (~326.7/~81.68 kHz)†.
C27	TDW_DENI_1	Id	**Transmit DWAC (FEC/DW) Channel 1 Insert Enable.** — Quad 2.5 Gbits/s mode—FEC/DW insert enable. — 10 Gbits/s mode—FEC/DW insert enable.
D27	TDW_DATAI_1	Id	**Transmit DWAC (FEC/DW) Channel 1 Insert Data.** — Quad 2.5 Gbits/s mode—FEC/DW insert data (~10.455 Mbits/s). — 10 Gbits/s mode—FEC/DW insert data bit 1 of 4 (LSB) (~10.455 Mbits/s).
E27	TDW_CLKO_2	O	**Transmit DWAC (FEC/DW) Channel 2 Insert Clock.** — Quad 2.5 Gbits/s mode—FEC/DW insert clock (~10.455 MHz). — 10 Gbits/s mode—not used.
C28	TDW_SYNCO_2	O	**Transmit DWAC (FEC/DW) Channel 2 Insert Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW insert superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—not used.
D28	TDW_DENI_2	Id	**Transmit DWAC (FEC/DW) Channel 2 Insert Enable.** — Quad 2.5 Gbits/s mode—FEC/DW insert enable. — 10 Gbits/s mode—not used.
A29	TDW_DATAI_2	Id	**Transmit DWAC (FEC/DW) Channel 2 Insert Data.** — Quad 2.5 Gbits/s mode—FEC/DW insert data (~10.455 MHz). — 10 Gbits/s mode—FEC/DW insert data bit 2 of 4 (~10.455 Mbits/s).
A30	TDW_CLKO_3	O	**Transmit DWAC (FEC/DW) Channel 3 Insert Clock.** — Quad 2.5 Gbits/s mode—FEC/DW insert clock (~10.455 MHz). — 10 Gbits/s mode—not used.
B30	TDW_SYNCO_3	O	**Transmit DWAC (FEC/DW) Channel 3 Insert Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW insert superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—not used.
E28	TDW_DENI_3	Id	**Transmit DWAC (FEC/DW) Channel 3 Insert Enable.** — Quad 2.5 Gbits/s mode—FEC/DW insert enable. — 10 Gbits/s mode—not used.
F28	TDW_DATAI_3	Id	**Transmit DWAC (FEC/DW) Channel 3 Insert Data.** — Quad 2.5 Gbits/s mode—FEC/DW insert data (~10.455 Mbits/s). — 10 Gbits/s mode—FEC/DW insert data bit 3 of 4 (~10.455 Mbits/s).
A31	TDW_CLKO_4	O	**Transmit DWAC (FEC/DW) Channel 4 Insert Clock.** — Quad 2.5 Gbits/s mode—FEC/DW insert clock (~10.455 MHz). — 10 Gbits/s mode—not used.
B31	TDW_SYNCO_4	O	**Transmit DWAC (FEC/DW) Channel 4 Insert Superframe Sync.** — Quad 2.5 Gbits/s mode—FEC/DW insert superframe sync (~81.68/~20.42 kHz)†. — 10 Gbits/s mode—not used.
C30	TDW_DENI_4	Id	**Transmit DWAC (FEC/DW) Channel 4 Insert Enable.** — Quad 2.5 Gbits/s mode—FEC/DW insert enable. — 10 Gbits/s mode—not used.
D30	TDW_DATAI_4	Id	**Transmit DWAC (FEC/DW) Channel 4 Insert Data.** — Quad 2.5 Gbits/s mode—FEC/DW insert data (~10.455 Mbits/s). — 10 Gbits/s mode—FEC/DW insert data bit 4 of 4 MSB (~10.455 Mbits/s).

* O = output, Id = input with internal pull-down resistor. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of all internal pull-down resistors is 50 kΩ.

† The frequencies in the parenthesis are the FEC rate and DW rate, respectively.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 16. Pin Descriptions—Microprocessor Interface

Pin	Symbol	Type*	Name/Description
A22	PCLK	I	**Microprocessor Clock.** This clock can operate from 10 MHz to 78 MHz in asynchronous mode and 10 MHz to 50 MHz in synchronous mode.
C21	CS_N	I	**Chip Select (Active-Low).** This signal must be low during register access.
C19	TS_N	I	**Transfer Start or Address Strobe (Active-Low).** Transfer start when MPMODE = 1 (synchronous). Address strobe when MPMODE = 0 (asynchronous).
D19	DS_N	I†	**Data Strobe (Active-Low).** This signal, when used in the asynchronous mode (MPMODE = 0), indicates that the data is valid for MPU writes.
D21	RW_N	I†	**Read/Write.** This signal is low to indicate a write operation and is high to indicate a read operation.
D22	TA_N	O	**Data Transfer Acknowledge (Active-Low).** This signal acknowledges the data transfer cycle.
E22	TEA_N	O	**Transfer Error Acknowledge (Active-Low).** This signal goes low to indicate an internal error related to the data transfer cycle.
F22	INTL_N	O	**Interrupt Low (Active-Low).** This signal goes low when the device generates an unmasked low-priority interrupt. The interrupt signal is cleared when the unmasked raw alarm that generated the interrupt is cleared.
B22	INTH_N	O	**Interrupt High (Active-Low).** This signal goes low when the device generates an unmasked high-priority interrupt. The interrupt signal is cleared when the unmasked raw alarm that generated the interrupt is cleared.
B15	ADDRESS_15	I†	**Address Bus [15:0].** This bus is used to address registers. **Note:** ADDRESS_15 is the MSB, ADDRESS_0 is the LSB.
A15	ADDRESS_14	I†	
D16	ADDRESS_13	I†	
C16	ADDRESS_12	I†	
B16	ADDRESS_11	I†	
A16	ADDRESS_10	I†	
F17	ADDRESS_9	I†	
E17	ADDRESS_8	I†	
B17	ADDRESS_7	I†	
A17	ADDRESS_6	I†	
F18	ADDRESS_5	I†	
E18	ADDRESS_4	I†	
D18	ADDRESS_3	I†	
C18	ADDRESS_2	I†	
B18	ADDRESS_1	I†	
A18	ADDRESS_0	I†	

* I = input, O = output. All I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.
† Input with 50 kΩ pull-up resistor.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 16. Pin Descriptions—Microprocessor Interface (continued)

Pin	Symbol	Type*	Name/Description
B26	DATA_15	I†/O	**Data Bus [15:0].** This bus is a bidirectional data bus for writing and reading software registers. **Note:** DATA_15 is the MSB, DATA_0 is the LSB.
A26	DATA_14	I†/O	
D25	DATA_13	I†/O	
C25	DATA_12	I†/O	
F24	DATA_11	I†/O	
E24	DATA_10	I†/O	
B25	DATA_9	I†/O	
A25	DATA_8	I†/O	
D24	DATA_7	I†/O	
C24	DATA_6	I†/O	
B24	DATA_5	I†/O	
A24	DATA_4	I†/O	
F23	DATA_3	I†/O	
E23	DATA_2	I†/O	
B23	DATA_1	I†/O	
A23	DATA_0	I†/O	
F25	PARITY_0	I†/O	**Data Bus Parity—Lower Byte.** Odd parity for lower byte [7:0].
E25	PARITY_1	I†/O	**Data Bus Parity—Upper Byte.** Odd parity for upper byte [15:8].

* I = input, O = output, I^u = input with internal pull-up resistor. I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of all internal pull-up resistors is 100 kΩ.
† Input with 50 kΩ pull-up resistor.

Table 17. Data Bus and Parity Bit Usage—8-Bit and 16-Bit Modes

MPDB_8_16 (Pin D22)	Data Bus Size	MSB (Bit)	LSB (Bit)	Parity Bus
1	16 bits	DATA_15	DATA_0	PARITY_1 and PARITY_0.
0	8 bits	DATA_7	DATA_0	PARITY_0 only.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 18. Pin Descriptions—JTAG Interface/Scan Signals

Pin	Symbol	Type*	Name/Description
AR10	TCK	I_d	**Test Clock.** This signal provides timing for test operations.
AV7	TMS	I^u	**Test Mode Select.** Controls test operations. TMS is sampled on the rising edge of TCK.
AP10	TDI	I^u	**Test Data In.** TDI is sampled on the rising edge of TCK.
AW6	TDO	O	**Test Data Out.** This output is updated on the falling edge of TCK. The TDO output is 3-stated except when scanning out test data.
AW7	TRST_N	I^u	**Test Reset (Active-Low).** This signal provides an asynchronous reset for the TAP. This input should be tied low (to V_{SS}) for normal device operation. If TRST_N is high, a TCK must be present to ensure that the correct test mode is clocked in on the TMS input.
Factory Test			
E29	TESTMODE	I_d	**Scan Testmode.** Active-high. No connect on operating designs.
AV34	SCANCLK1	I_d	**Scan Clock 1.** No connect on operating designs.
AW34	SCANCLK2	I_d	**Scan Clock 2.** No connect on operating designs.

* I = input, O = output, I_d = input with internal pull-down resistor (50 kΩ), I^u = input with internal pull-up resistor (100 kΩ). I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 19. Pin Descriptions—GPIO

Pin	Symbol	Type*	Name/Description	Usage
K6	GPIO_1	I^U/O	GPIO—general purpose I/O.	Available for internal uses. See the operational description for details.
J4	GPIO_2	I^U/O	GPIO—general purpose I/O.	
J3	GPIO_3	I^U/O	GPIO—general purpose I/O.	
B35	GPIO_4	I^U/O	GPIO—general purpose I/O.	
A35	GPIO_5	I^U/O	GPIO—general purpose I/O.	
D33	GPIO_6	I^U/O	GPIO—general purpose I/O.	
C33	GPIO_7	I^U/O	GPIO—general purpose I/O.	
F31	GPIO_8	I^U/O	GPIO—general purpose I/O.	
E31	GPIO_9	I^U/O	GPIO—general purpose I/O.	
B33	GPIO_10	I^U/O	GPIO—general purpose I/O.	
A33	GPIO_11	I^U/O	GPIO—general purpose I/O.	
F30	GPIO_12	I^U/O	GPIO—general purpose I/O.	
E30	GPIO_13	I^U/O	GPIO—general purpose I/O.	
D31	GPIO_14	I^U/O	GPIO—general purpose I/O.	
C31	GPIO_15	I^U/O	GPIO—general purpose I/O.	
B32	GPIO_16	I^U/O	GPIO—general purpose I/O.	
A32	GPIO_17	I^U/O	GPIO—general purpose I/O.	
AP8	GPIO_18	I^U/O	GPIO—general purpose I/O.	
AR8	GPIO_19	I^U/O	GPIO—general purpose I/O.	
AV5	GPIO_20	I^U/O	GPIO—general purpose I/O.	
AW5	GPIO_21	I^U/O	GPIO—general purpose I/O.	
AP9	GPIO_22	I^U/O	GPIO—general purpose I/O.	
AR9	GPIO_23	I^U/O	GPIO—general purpose I/O.	
AV6	GPIO_24	I^U/O	GPIO—general purpose I/O.	
AP15	GPIO_25	I^U/O	GPIO—general purpose I/O.	
AR15	GPIO_26	I^U/O	GPIO—general purpose I/O.	
AV14	GPIO_27	I^U/O	GPIO—general purpose I/O.	
AW14	GPIO_28	I^U/O	GPIO—general purpose I/O.	
AT15	GPIO_29	I^U/O	GPIO—general purpose I/O.	

1. I/O = bidirectional pin, I^U = input with internal pull-up resistor. I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of the internal pull-up resistors is 100 kΩ.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 19. Pin Descriptions—GPIO (continued)

Pin	Symbol	Type*	Name/Description	Usage
AU15	GPIO_30	I^U/O	GPIO—general purpose I/O.	Available for generic use. See the operational description for details.
AP16	GPIO_31	I^U/O	GPIO—general purpose I/O.	
AR16	GPIO_32	I^U/O	GPIO—general purpose I/O.	
AV15	GPIO_33	I^U/O	GPIO—general purpose I/O.	
AW15	GPIO_34	I^U/O	GPIO—general purpose I/O.	
AV16	GPIO_35	I^U/O	GPIO—general purpose I/O.	
AW16	GPIO_36	I^U/O	GPIO—general purpose I/O.	
AP17	GPIO_37	I^U/O	GPIO—general purpose I/O.	
AR17	GPIO_38	I^U/O	GPIO—general purpose I/O.	
AV17	GPIO_39	I^U/O	GPIO—general purpose I/O.	
AW17	GPIO_40	I^U/O	GPIO—general purpose I/O.	
AP18	GPIO_41	I^U/O	GPIO—general purpose I/O.	
AR18	GPIO_42	I^U/O	GPIO—general purpose I/O.	
AT18	GPIO_43	I^U/O	GPIO—general purpose I/O.	
AU18	GPIO_44	I^U/O	GPIO—general purpose I/O.	
AT19	GPIO_45	I^U/O	GPIO—general purpose I/O.	
AU19	GPIO_46	I^U/O	GPIO—general purpose I/O.	
AW22	GPIO_47	I^U/O	GPIO—general purpose I/O.	
AV22	GPIO_48	I^U/O	GPIO—general purpose I/O.	

* I/O = bidirectional pin, I^U = input with internal pull-up resistor. I/O are 5 V compatible, 3.3 V TTL. They will tolerate 5 V at their inputs or outputs. The value of the internal pull-up resistors is 100 kΩ.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 20. Pin Descriptions—Power and Ground

Pin	Symbol	Type*	Name/Description
A1, A2, A20, A38, A39, AC5, AC37, AF4, AF36, AJ3, AJ37, AM4, AM36, AT8, AT14, AT20, AT26, AT32, AU11, AU17, AU20, AU23, AU29, AV1, AV2, AV20, AV38, AV39, AW1, AW2, AW20, AW38, AW39, B1, B2, B20, B38, B39, C11, C17, C20, C23, C29, D8, D14, D20, D26, D32, H4, H36, L4, L35, L37, P4, P36, U4, Y1, Y2, Y3, Y4, Y36, Y37, Y38, Y39	VDD	P	3.3 V positive supply voltage (~3.15 W worst case).
E5, E6, E19, E20, E21, E34, E35, F5, F6, F19, F20, F21, F34, F35, W5, W6, W34, W35, Y5, Y6, Y34, Y35, AA5, AA6, AA34, AA35, AP5, AP6, AP19, AP20, AP21, AP34, AP35, AR5, AR6, AR19, AR20, AR21, AR34, AR35	VDD15	P	1.5 V positive supply voltage (~3.15 W worst case).
A19, A21, AA1, AA2, AA38, AA39, AC36, AC6, AF3, AF37, AJ4, AJ36, AM3, AM37, AT3, AT4, AT11, AT17, AT23, AT29, AT36, AT37, AU3, AU4, AU8, AU14, AU26, AU32, AU36, AU37, AV19, AV21, AW19, AW21, B19, B21, C3, C4, C8, C14, C26, C32, C36, C37, D3, D4, D11, D17, D23, D29, D36, D37, H3, H37, L3, L34, L36, P3, P37, U3, W1, W2, W38, W39	VSS	G	Ground.

1. P = power, G = ground.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 20. Pin Descriptions—Power and Ground (continued)

Pin	Symbol	Type*	Name/Description
W3, V35, T38, T1, R5, R3, M5, K5, J35, J34, H6, H5, H35, H34, H2, H1, G6, G5, G37, G36, G35, G34, F7, F4, F37, F36, F33, F32, F3, F29, F27, F26, F16, F12, E7, E4, E39, E38, E37, E36, E33, E32, E3, E26, E2, E16, E12, E1, D5, D39, D38, D35, D34, D2, D1, C5, C39, C38, C35, C34, C2, C1, AW4, AW37, AW35, AW33, AW32, AW3, AW27, AW26, AW25, AW24, AW23, AW18, AW13, AW11, AV4, AV37, AV35, AV33, AV32, AV3, AV29, AV27, AV26, AV25, AV24, AV23, AV18, AV13, AV11, AU7, AU6, AU5, AU39, AU38, AU35, AU33, AU31, AU30, AU25, AU24, AU21, AU2, AU16, AU1, AT7, AT6, AT5, AT39, AT38, AT35, AT33, AT31, AT30, AT28, AT27, AT25, AT24, AT21, AT2, AT16, AT1, AR7, AR4, AR39, AR38, AR37, AR36, AR30, AR3, AR29, AR28, AR27, AR24, AR23, AR22, AR2, AR1, AP7, AP4, AP37, AP36, AP30, AP3, AP29, AP28, AP27, AP26, AP24, AP23, AP22, AN6, AN5, AN38, AN35, AN34, AM6, AM5, AM35, AM34, AL34, AK36, AJ6, AJ5, AG37, AG35, AE6, AE39, AD6, AB6, AB34, AA37, A4, A37, A36, A34, A3, A28, A14, A11, B3, B4, B6, B8, B9, B11, B12, B14, B28, B29, B34, B36, B37	NC	—	No connect. Do not connect these pins.

* P = power, G = ground.

2 Pin Information (continued)

2.2 Pin Descriptions (continued)

Table 21. Pin Count Summary

Interface	Pin Count
System Control Pins	7
Transmit Phase Detectors	8
Receive Phase Detectors	8
Receive Line Interface	48
Receive Line Interface LVDS Reference	16
Receive System Interface	48
Transmit System Interface	40
Transmit System/Line LVDS Reference	16
LVDS Reference	4
Transmit Line Interface	56
Receive Section/Line OH (Drop)	24
Transmit Section/Line OH (Insert)	28
Receive FEC/DW OH Drop	12
Transmit DW OH Insert	16
Microprocessor Interface	43
JTAG/Scan	8
GPIO	48
Interface Pins	**430**
Power (3.3 V Supply)	64
Power (1.5 V Supply)	40
Ground	64
No Connect	194
Total	**792**

Note: CMOS inputs are 5 V tolerant. Logic inputs can be driven from standard TTL levels, and logic outputs can drive standard TTL inputs. 3.3 V TTL is preferred.

3 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. Component case temperature shall not exceed 220 °C during solder reflow attachment.

Table 22. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	125	°C
Voltage on Any Pin with Respect to Ground	V_{SS}	GND – 0.5	V_{DD} + 0.5*	V
Power Dissipation	P_D	—	6.3	W

* This maximum rating only applies when the device is powered up with V_{DD}.

4 Typical Operating Conditions

Table 23. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply—3.3 V I/O	V_{DD}	3.135	3.3	3.465	V
Power Supply—1.5 V	V_{DD}	1.425	1.5	1.575	V
Low-Level Input Voltage	V_{IL}	See Table 27, Logic Interface Characteristics, on page 46.			V
High-Level Input Voltage	V_{IH}				V
Ambient Operating Temperature Range	T_A	–40	—	85	°C

5 Thermal Characteristics

Table 24. 792-Pin PBGAM Thermal Resistance

Power (W)	Thermal Budget (°C/W)	(Theta-jc) (°C/W)	Heat Sink Speck (°C/W)	Theta-ja (°C/W)	Theta-ja with Airflow (200 Linear Feet per Minute) (°C/W)
6	6.7	2.2	4.5	14.5	11.5

Note: Any heat sink that has a lower thermal specification than those specified in Table 24 is adequate for use with the device.

Table 25. Package Temperature Coefficients (without Heat Sink)

Parameter	Symbol	Value	Airflow
Junction to Ambient	θja	10.5 °C/W	0 linear meters/second
Junction to Ambient	θja	8.5 °C/W	100 linear meters/second
Junction to Ambient	θja	7.5 °C/W	250 linear meters/second

6 Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 26. HBM ESD Minimum Threshold

Device	Model	Voltage
TFEC0410G	Minimum HBM Threshold	2000 V
	Minimum CDM	500 V

7 Electrical Characteristics

Table 27. Logic Interface Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage: Low High	 V_{IL} V_{IH}	—	 GND V_{DD} – 1.0	 1.0 V_{DD}	 V V
Input Leakage	I_L	—	—	1.0	µA
Output Voltage: Low High	 V_{OL} V_{OH}	 –5.0 mA 5.0 mA	 GND V_{DD} – 1.0	 0.5 V_{DD}	 V V
Input Capacitance	C_I	—	—	—	pF
Load Capacitance	C_L	—	—	—	pF

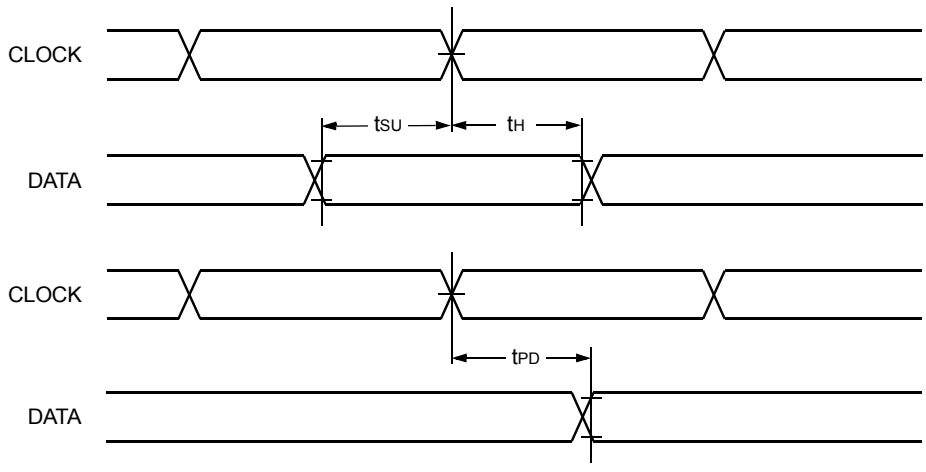


Figure 2. Generic Interface Data Timing

7 Electrical Characteristics (continued)

7.1 Low-Voltage Differential Signal (LVDS) Buffers

The LVDS buffers are compliant with the *EIA*®-644 standard. The only exception to compliance with this standard is associated with the input leakage current. The LVDS input buffers have a maximum input leakage current of 300 μA.

The LVDS buffers are also compliant to the *IEEE*® 1596.3 standard. The only exception to compliance with this standard is the input termination resistance. The LVDS input buffers have an input termination resistance of 100 Ω ± 20%.

The LVDS outputs are hot-swap compatible, and can be connected to other vendor's LVDS I/O buffers. The maximum input current for the Agere Systems Inc. LVDS input buffers is 9 mA. Prolonged exposure to higher current levels will have an impact on long-term reliability.

The LVDS buffers support point-to-point connections. They are not intended for, and are not recommended for, bussed implementations.

Unused LVDS inputs may be left unconnected. They have circuitry that forces them to remain in a defined state if left open. Open inputs will not oscillate for this reason.

Unused LVDS inputs may be left unconnected. They have 14 kΩ ± 40% pull-up resistors that forces them to remain in a defined state if left open. Open inputs will not oscillate for this reason.

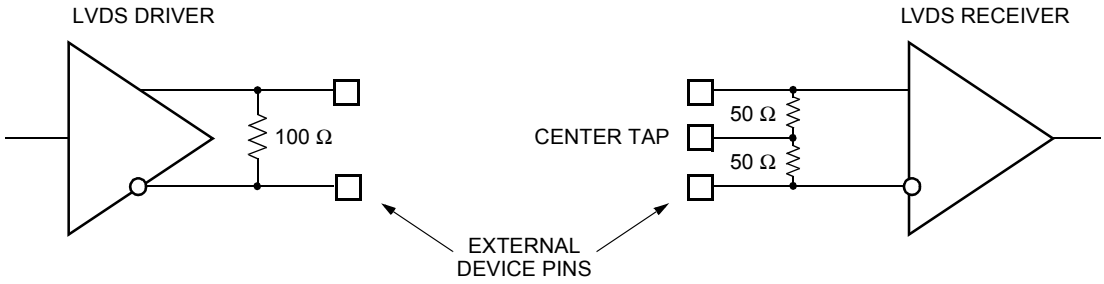


Figure 3. LVDS Driver and Receiver and Associated Internal Components

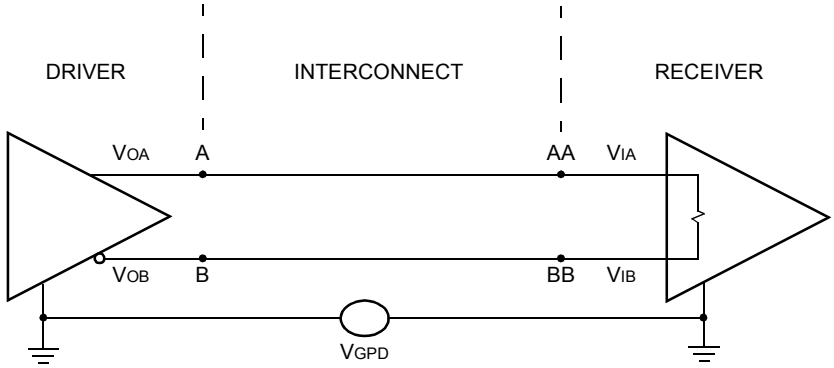


Figure 4. LVDS Driver and Receiver

7 Electrical Characteristics (continued)

7.1 Low-Voltage Differential Signal (LVDS) Buffers (continued)

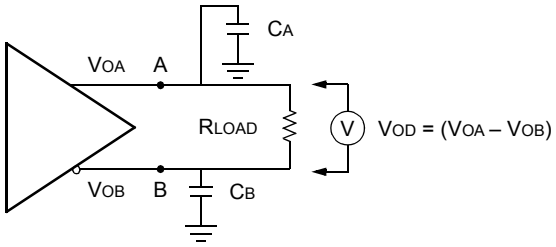


Figure 5. LVDS Driver

7.1.1 LVDS Receiver Buffer Capabilities

A disabled or unpowered LVDS receiver can withstand a driving LVDS transmitter over the full range of driver operating range, for an unlimited period of time, without being damaged. Table 28 illustrates LVDS driver dc data, Table 29 the ac data, and Table 31 on page 49 the LVDS receiver data.

Note: V_{DD} = 3.1 V—3.5 V, 0 °C—125 °C, slow-fast process.

Table 28. LVDS Driver dc Data

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Driver Output Voltage High, V_{OA} or V_{OB}	V_{OH}	R_{LOAD} = 100 Ω ± 1% Refer to Figure 5 on page 48.	—	—	1.475*	V
Driver Output Voltage Low, V_{OA} or V_{OB}	V_{OL}	R_{LOAD} = 100 Ω ± 1%.	0.925*	—	—	V
Driver Output Differential Voltage V_{OD} = (V_{OA} – V_{OB}) (with external reference resistor)	$\lvert V_{OD} \rvert$	R_{LOAD} = 100 Ω ± 1%.	0.25	—	0.45*	V
Driver Output Offset Voltage V_{OS} = (V_{OA} + V_{OB})/2	V_{OS}	R_{LOAD} = 100 Ω ± 1% Refer to Figure 5 on page 48.	1.125*	—	1.275*	V
Output Impedance, Single-Ended	R_O	V_{CM} = 1.0 V and 1.4 V.	40	50	60	W
R_O Mismatch Between A and B	ΔR_O	V_{CM} = 1.0 V and 1.4 V.	—	—	10	%
Change in $\lvert \Delta V_{OD} \rvert$ Between 0 and 1	$\lvert \Delta V_{OD} \rvert$	R_{LOAD} = 100 Ω ± 1%.	—	—	25	mV
Change in $\lvert \Delta V_{OS} \rvert$ Between 0 and 1	$\lvert \Delta V_{OS} \rvert$	R_{LOAD} = 100 Ω ± 1%.	—	—	25	mV
Output Current	I_{SA}, I_{SB}	Driver shorted to ground.	—	—	24	mA
Output Current	I_{SAB}	Driver shorted together.	—	—	12	mA
Power-Off Output Leakage	$\lvert I_{XA} \rvert$, $\lvert I_{XB} \rvert$	V_{DD} = 0 V. V_{PAD}, V_{PADN} = 0 V—3 V.	—	—	30	µA

* External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%. See Figure 1 on page 27 for a schematic.

7 Electrical Characteristics (continued)

7.1 Low-Voltage Differential Signal (LVDS) Buffers (continued)

Table 29. LVDS Driver ac Data

Parameter	Symbol	Conditions	Min	Max	Unit
V_{OD} Fall Time, 80% to 20%	tFALL	Z_{LOAD} = 100 Ω ± 1%. C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF.	100	210	ps
V_{OD} Rise Time, 20% to 80%	tRISE	Z_{LOAD} = 100 Ω ± 1%. C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF.	100	210	ps
Differential Skew $\lvert tp_{HLA} - tp_{LHB} \rvert$ or $\lvert tp_{HLB} - tp_{LHA} \rvert$	tSKEW1	Any differential pair on package at 50% point of the transition.	—	50	ps

Table 30. LVDS Driver Reference Data

Parameter	Conditions	Min	Typ	Max	Unit
REF10E, REF10L Voltage Range	—	0.95	1.0	1.05	V
REF14E, REF14L Voltage Range	—	1.35	1.4	1.45	V
Nominal Input Current—REF10 and REF14 Reference Inputs	—	—	10	—	µA

Table 31. LVDS Receiver dc Data

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Receiver input Voltage Range, V_{IA} or V_{IB}	V_I	$\lvert V_{GPD} \rvert$ < 925 mV dc—1MHz.	0	1.2	2.4	V
Receiver Input Differential Threshold	$\lvert V_{IDTH} \rvert$	$\lvert V_{GPD} \rvert$ < 925 mV—400 MHz.	–100	—	100	mV
Receiver Input Differential Hysteresis	V_{HYST}	$V_{IDTHH} - V_{IDTHL}$.	—	—	—*	mV
Receiver Differential Input Impedance	R_{IN}	With built-in termination, center tapped.	80	100	120	W

* Buffer will not produce transition when input is open-circuited.

Table 32. LVDS Receiver ac Data

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Rise Time (20%—80%)	tR	CL = 0.5 pF.	150	—	350	ps
Output Fall Time (80%—20%)	tF	CL = 0.5 pF.	150	—	350	ps

8 Power

8.1 Power Sequencing

The device power should be applied concurrently to both voltage level inputs. The 3.3 V supply powers the I/O buffers, and the 1.5 V supply powers the core logic of the device. In the event that either supply is powered individually, even for a reasonably long period of time (such as a few seconds), the device will not be damaged. In the event both voltages are not applied concurrently, a device reset is recommended before normal operation.

8.2 Power Consumption

The following table (Table 26) lists the maximum power consumption (by mode) of the TFEC0410G device.

Table 33. TFEC0410G Power Consumption

Mode		Power Consumption
Strong FEC/Digital Wrapper—Terminal	10 Gbits/s	TBD
	Quad 2.5 Gbits/s	TBD
	Dual 2.5 Gbits/s	TBD
	Single 2.5 Gbits/s	TBD
Strong FEC/Digital Wrapper—Regenerator	10 Gbits/s	TBD
	Quad 2.5 Gbits/s	TBD
Strong FEC/Digital Wrapper—Bidirectional Mode	10 Gbits/s	TBD
	Quad 2.5 Gbits/s	TBD
Weak FEC—Terminal	10 Gbits/s	TBD
	Quad 2.5 Gbits/s	TBD
Weak FEC—Regenerator	10 Gbits/s	TBD
	Quad 2.5 Gbits/s	TBD
Strong (Digital Wrapper) FEC/Weak FEC—Terminal	10 Gbits/s	TBD
	Quad 2.5 Gbits/s	TBD

9 Timing Characteristics

9.1 Receive/Transmit Input Data/Sync Interface

9.1.1 Receive (Line)/Transmit (System) Quad 2.5 Gbits/s Mode/10 Gbits/s Mode Data and Sync Inputs

Figure 6 illustrates the timing for the receive (line) and transmit (system) quad 2.5 Gbits/s/10 Gbits/s data stream. Both the clock and data pins are low-voltage differential signal (LVDS) input buffers. The expected clock rate is 622.08 MHz—692.64 MHz and the receive/transmit data is clocked on the rising edge of the clock. In quad 2.5 Gbits/s mode, each channel uses one set of RCLKLI_[15—0]/TCLKSI_[15—0] and RDLI_[4—1]_[3:0]/ TDSI_[4—1]_[3:0] data pins. In 10 Gbits/s mode, or virtual 10 Gbits/s mode (data is arranged as four 2.5 Gbits/s signals), only RCLKLI_1/TCLKSI_1 are used, along with the 16 RDLI/TDSI pins, respectively.

Both the clock and frame sync are low-voltage differential signal (LVDS) input buffers. The expected clock is 666.51 MHz—692.64 MHz and the sync is clocked on the rising edge of the clock. In quad 2.5 Gbits/s mode, each channel uses one set of TCLKLI_[4—1] and TFRMLI_[4—1] sync pins. In 10 Gbits/s mode, only TCLKLI_1 is used, along with the TFRMLI_1 sync input. The timing values for the diagram are given in Table 34.

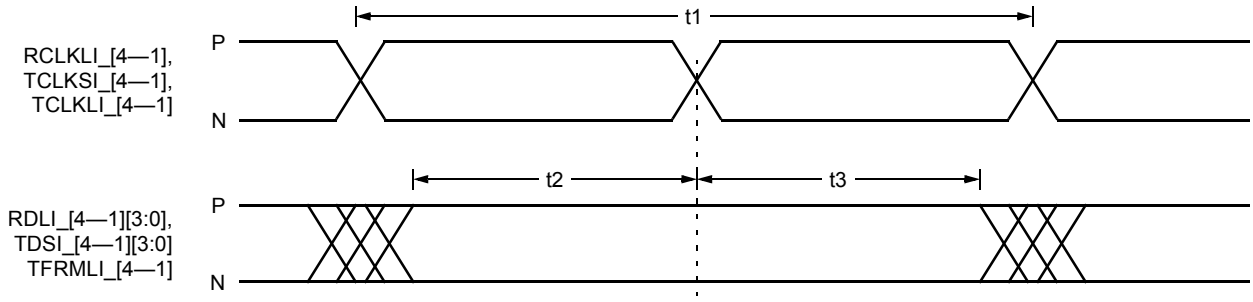


Figure 6. Receive/Transmit Data Timing

Table 34. Receive (Line)/Transmit (System) Data Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Clock Period	—	1608/1443	—	ps
t2	Data Setup Time Required	220	—	—	ps
t3	Data Hold Time Required	220	—	—	ps

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

9.1.2 Transmit (Line)/Receive (System) Quad 2.5 Gbits/s/10 Gbits/s Data Outputs

Figure 7 illustrates the timing for the transmit (line)/receive (system) quad 2.5 Gbits/s/10 Gbits/s output data streams. Both the clock and data pins are driven with low-voltage differential signal buffers. The expected clock rate is 622.08 MHz—692.64 MHz and the receive/transmit data is clocked out on the rising edge of the clock. In quad 2.5 Gbits/s mode, each channel uses one set of RCLKSO_[4—1]/TCLKLO_[4—1] and RDSO_[4—1]_[3:0]/ TDLO_[4—1]_[3:0] data pins. In 10 Gbits/s mode, or virtual 10 Gbits/s mode (data is arranged as four 2.5 Gbits/s signals), only RCLKSO_1/TCLKLO_1 are used, along with the 16 RDSO/TDLO pins respectively. The timing values for the diagram are given in Table 35.

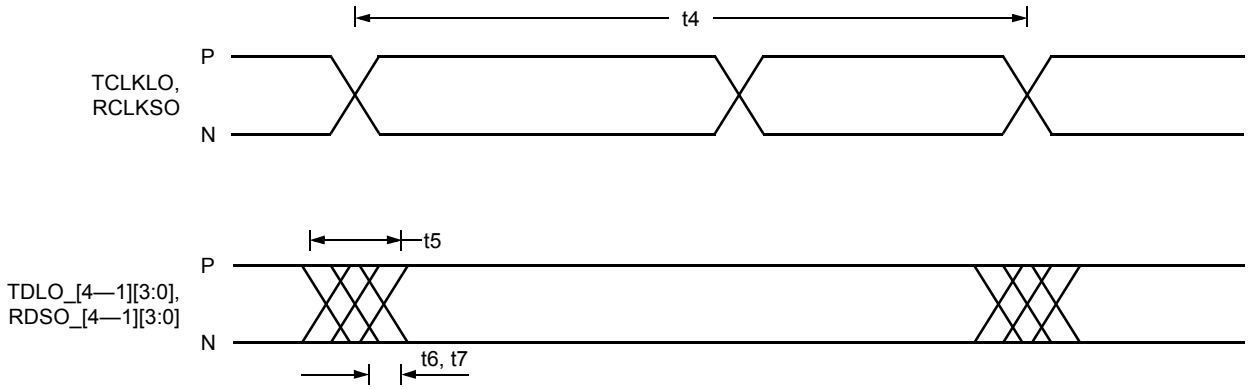


Figure 7. Transmit (Line)/Receive (System) Data Timing

Table 35. Transmit (Line)/Receive (System) Data Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t4	Clock Period	—	1608/1443	—	ps
—	Duty Cycle*	45	50	55	%
t5	Data Delay from Clock Edge	–220	—	220	ps
t6	Data Rise Time: 20%—80%	100	—	200	ps
t7	Data Fall Time: 80%—20%	100	—	200	ps
—	Clock Output Variation	—	3 bit periods at 622.08 MHz	—	—

* This requirement is for all sources of the output clocks (e.g., RCLKSI, etc.).

9.1.3 Receive Transport Overhead Access Channel (RTOAC)

9.1.3.1 Full TOAC Drop Mode (Rx)

- The RTOAC_DATA_[4—1]_[3:0] pins transmit the complete transport overhead data for every received frame. The RTOAC_DATA_[4—1]_ [3:0] pins are timed using the rising edge of the TTOAC_CLKO_[4—1] signal. Sampling of the RTOAC_DATAO_[4—1]_[3:0] pins is intended to occur at the positive edge of the RTOAC_CLKO_[4—1] signals.
- 1296 overhead bytes are transmitted in 125 μs using a 4-bit interface, making the average frequency of RTOAC_CLK 20.736 MHz.
- The RTOAC_SYNCO_[4—1] pins indicate the frame position by toggling high during the most significant nibble of the first A1 byte in the data stream, as illustrated in Figure 8 on page 53.

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

9.1.3.2 Partial (First STS-1) TOAC Drop Mode (Rx)

- The RTOAC_DATAO_[4—1]_0 pin transmits the first STS-1 transport overhead data for every received frame. The RTOAC_DATAO_[4—1]_ 0 pin is timed using the rising edge of the RTOAC_CLKO_[4—1] signal. Sampling of the RTOAC_DATAO_[4—1]_0 pin is intended to occur at the positive edge of the RTOAC_CLK_[4—1] signals.
- 27 overhead bytes are transmitted in 125 μs using a 1-bit interface, making the average frequency of RTOAC_CLK 1.728 MHz.
- The RTOAC_SYNCO_[4—1] pin indicates the frame position by toggling high during the most significant bit of the first A1 byte in the data stream, as illustrated in Figure 8.

The timing characteristics for the receive overhead serial pins are given in Figure 8 and Table 36.

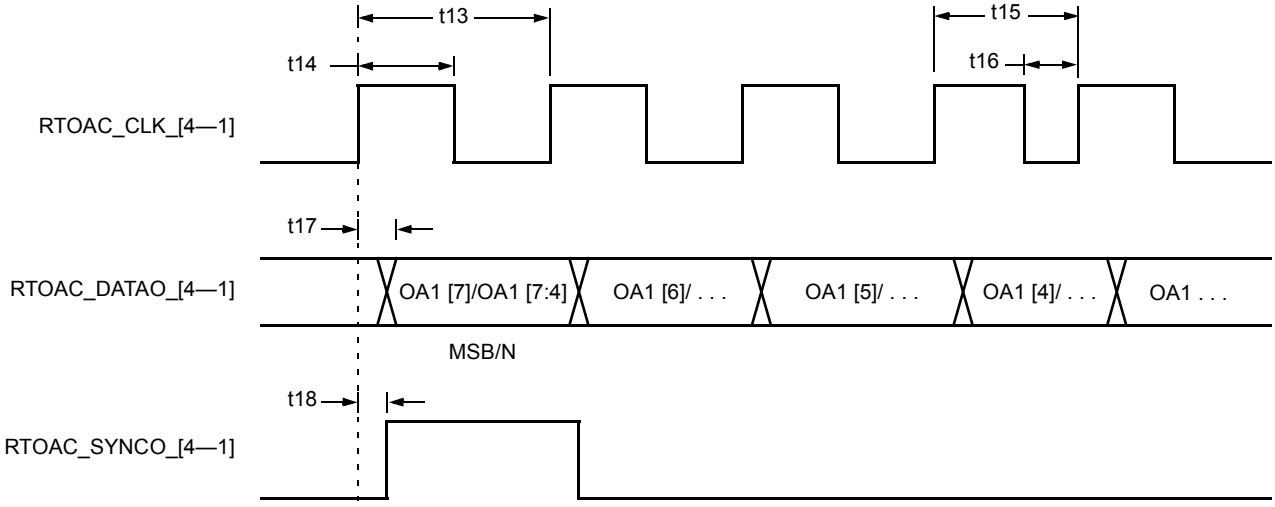


Figure 8. Receive Overhead Serial Timing (Drop)

Table 36. Receive Transport Overhead Access Channel Timing (Full TOAC Drop Mode—20.736 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
t13	Clock Period (long clock)	—	51.44	—	ns
t14	Clock High Width	—	25.72	—	ns
t15	Clock Period (short clock)	—	38.58	—	ns
t16	Clock Low Width	—	12.86	—	ns
t17	Clock to Data Delay	0.6	—	8	ns
t18	Clock to Frame Pulse Delay	0.6	—	8	ns

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

Table 37. Receive Transport Overhead Access Channel Timing (STS-1 TOAC Drop Mode—1.728 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
t13	Clock Period (long clock)	—	617.28	—	ns
t14	Clock High Width	—	308.64	—	ns
t15	Clock Period (short clock)	—	462.96	—	ns
t16	Clock Low Width	—	154.32	—	ns
t17	Clock to Data Delay	0.6	—	8	ns
t18	Clock to Frame Pulse Delay	0.6	—	8	ns

Table 38. Receive Transport Overhead Access Channel Timing—Load/Rise and Fall Times

Signal	Test Load	Max—tR/tF	Unit
RTOAC_CLKO_[4—1]	C_L = 15 pF	3.5/3.5	ns
RTOAC_DATAO_[4—1]_[3:0]	C_L = 15 pF	3.5/3.5	ns
RTOAC_SYNCO_[4—1]	C_L = 15 pF	3.5/3.5	ns

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

9.1.4 Transmit Transport Overhead Access Channel

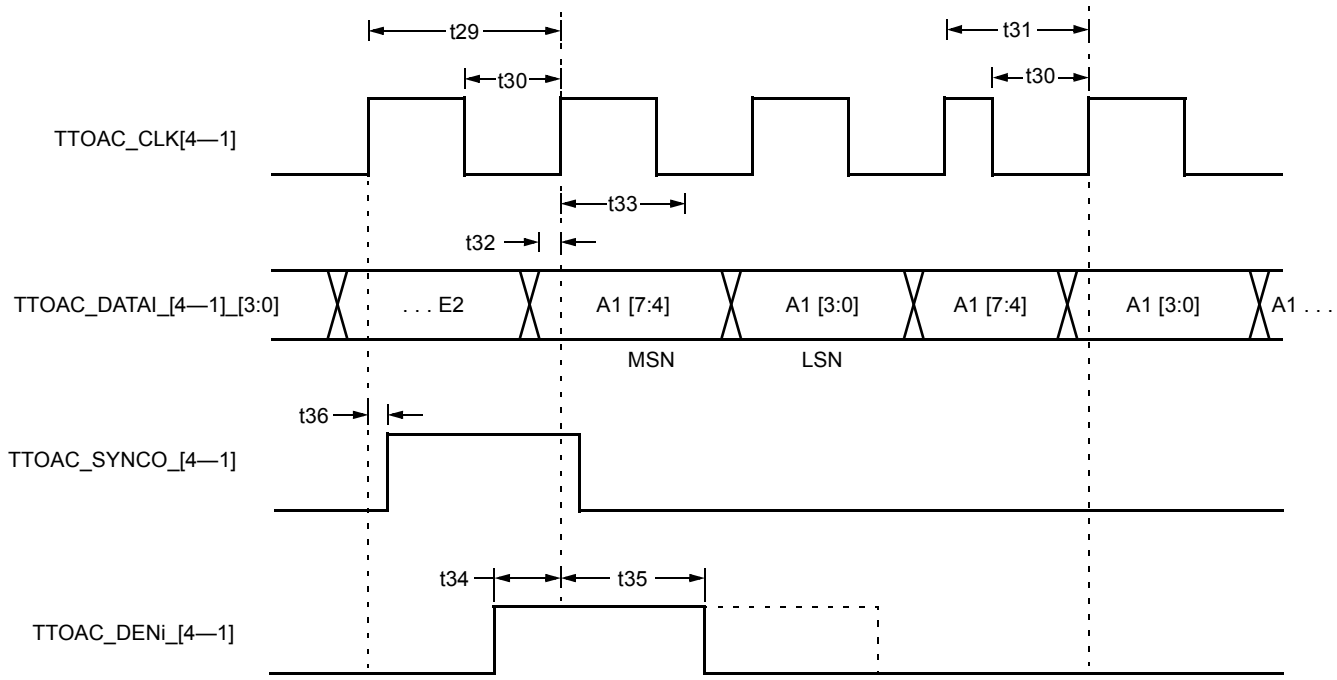


Figure 9. Transmit Overhead Serial Timing

9.1.4.1 Full TOAC Drop Mode (Tx)

- The TTOAC_DATAI_[4—1]_[3:0] pins are optionally used to insert transport overhead bytes into the transmit data stream. The TTOAC_DATAI_[4—1]_[3:0] pins are sampled internally using the rising edge of the TTOAC_CLKO_[4—1] signal. Generation of the TTOAC_DATAI signal is intended to occur at the positive edge of the TTOAC_CLKO signal. This is possible since there is zero hold time required on the TTOAC_DATAI_[4—1]_[3:0] inputs.
- 1296 overhead bytes are received in 125 μs using a 4-bit interface, which makes the average frequency of TTOAC_CLKO 20.736 MHz.
- The TTOAC_SYNCO_[4—1] pin indicates the frame position by toggling high during the most significant nibble of the first A1 byte in the data stream, as illustrated in Figure 9.
- The timing characteristics for the transmit overhead serial pins are given in Table 39 on page 56.
- TTOAC_DENI_[4—1] is only sampled on the rising edge of the clock during the most significant nibble and least significant nibble of the byte (see Figure 9).

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

9.1.4.2 Partial (First STS-1) TOAC Drop Mode (Tx)

- The TTOAC_DATAI_[4—1]_0 pin is optionally used to insert transport overhead bytes into the transmit data stream. The TTOAC_DATAI_[4—1]_0 pin is sampled internally using the rising edge of the TTOAC_CLKO_[4—1] signal. Generation of the TTOAC_DATAI signal is intended to occur at the positive edge of the TTOAC_CLK signal. This is possible since there is zero hold time required on the TTOAC_DATAI_[4—1]_[3:0] inputs.
- 27 overhead bytes are received in 125 μs using a 1-bit interface, which makes the average frequency of TTOAC_CLK 1.728 MHz.
- The TTOAC_SYNCO_[4—1] pin indicates the frame position by toggling high during the most significant bit of the first A1 byte in the data stream, as illustrated in Figure 9 on page 55.
- The timing characteristics for the transmit overhead serial pins are given in Table 40 on page 57.
- TTOAC_DENI_[4—1] is sampled on the rising edge of the clock during the most significant bit [7] and bit [6] of the byte (see Figure 9 on page 55).

Table 39. Transmit Transport Overhead Access Channel Timing (Full TOAC Mode—20.736 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
t29	Clock Period (long clock)	—	51.44	—	ns
t30	Clock Low Width	—	25.72	—	ns
t31	Clock Period (short clock)	—	38.58	—	ns
t32	Data Setup Time Required	8	—	—	ns
t33	Data Hold Time Required	0	—	—	ns
t34	TTOAC_DENI_[4—1] Setup Time Required	8	—	—	ns
t35	TTOAC_DENI_[4—1] Hold Time Required	0	—	—	ns
t36	Clock to Frame Pulse Delay*	0.6	—	8	ns

* The frame pulse may occur after either a long clock or a short clock.

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

Table 40. Transmit Transport Overhead Access Channel Timing (Partial (STS-1) TOAC Mode—1.728 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
t29	Clock Period (long clock)	—	617.28	—	ns
t30	Clock Low Width	—	308.64	—	ns
t31	Clock Period (short clock)	—	462.96	—	ns
t32	Data Setup Time Required	8	—	—	ns
t33	Data Hold Time Required	0	—	—	ns
t34	TTOAC_DENI_[4—1] Setup Time Required	8	—	—	ns
t35	TTOAC_DENI_[4—1] Hold Time Required	0	—	—	ns
t36	Clock to Frame Pulse Delay*	0.6	—	8	ns

* The frame pulse may occur after either a long clock or a short clock.

Table 41. Transmit Transport Overhead Access Channel—Load/Rise and Fall Times

Signal	Test Load	Max—tR/tF	Unit
TTOAC_CLK_[4—1]	C_L = 15 pF	3.5/3.5	ns
TTOAC_SYNCO_[4—1]	C_L = 15 pF	3.5/3.5	ns
TTOAC_DATAI_[4—1]	NA*	3.5/3.5	ns
TTOAC_DENI_[4—1]	NA*	3.5/3.5	ns

* Not applicable. No test load.

9.1.5 Receive FEC/Digital Wrapper Receive Overhead Drop Interface

The RDW_DATAO_[4—1] pin transmits the complete FEC/DW overhead every received FEC frame. The RDW_DATAO_[4—1] pins are timed using the rising edge of the RDW_CLKO_[4—1] signal. Sampling of the RDW_DATAO_[4—1] pins is intended to occur at the positive edge of the RDW_CLKO_[4—1] signals.

Since 16 overhead bytes are transmitted per FEC frame using a 1/4-bit interface, the average frequency of RDW_CLKO_[4—1] is 10.455 MHz in both 2.5 Gbits/s and 10 Gbits/s mode.

The RDW_SYNCO_[4—1] pin indicates the frame position by toggling high during the most significant bit/nibble of the first overhead byte in the data stream, as illustrated in Figure 10 on page 58.

The timing characteristics for the receive overhead serial pins are given in Table 42 on page 58.

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

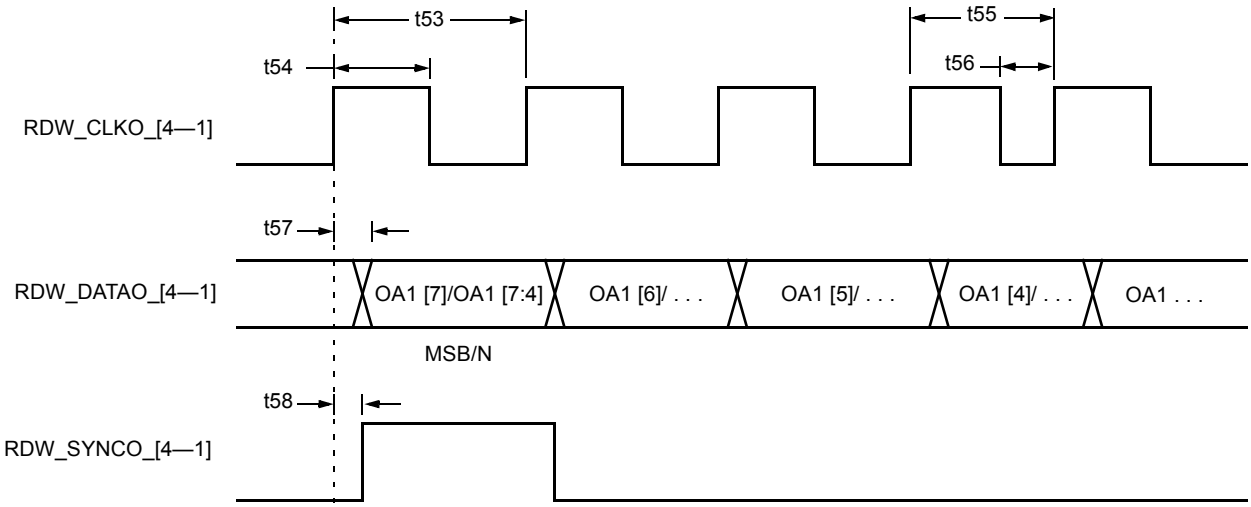


Figure 10. Receive DW Data Communication Channels Timing

Table 42. Receive DW Data Communication Channels Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t53	Clock Period (long clock)	—	96.02	—	ns
t54	Clock High Width	—	48.01	—	ns
t55	Clock Period (short clock)	—	84.02	—	ns
t56	Clock Low Width	—	36.01	—	ns
t57	Clock to Data Delay	0.6	—	8	ns
t58	Clock to Frame Pulse Delay	0.6	—	8	ns

Table 43. Receive DW Data Communication Channels—Load/Rise and Fall Times

Signal	Test Load	Max—tR/tF	Unit
RDW_CLKO_[4—1]	C_L = 15 pF	3.5/3.5	ns
RDW_DATAO_[4—1]	C_L = 15 pF	3.5/3.5	ns
RDW_SYNCO_[4—1]	C_L = 15 pF	3.5/3.5	ns

9.1.6 Transmit FEC/Digital Wrapper Insert Overhead Channel

The TDW_DATAI_[4—1] pins are optionally used to insert FEC/digital wrapper (OCh) overhead bytes into the transmit data stream. The TDW_DATAI_[4—1] pins are sampled internally using the rising edge of the TDW_CLKO_[4—1] signal. Generation of the TDW_DATAO_[4—1] signals are intended to occur at the positive edge of the TDW_CLKO signal. This is possible since there is zero hold time required on the TDW_DATAI_[4—1] inputs.

16 overhead bytes are received in one FEC/DW frame period using a 1-bit interface, which makes the average frequency of TDW_CLKO_[4—1] 10.455 MHz.

The TDW_SYNCO_[4—1] pin indicates the frame position by toggling high during the most significant bit of the first overhead byte in the data stream, as illustrated in Figure 11 on page 59.

9 Timing Characteristics (continued)

9.1 Receive/Transmit Input Data/Sync Interface (continued)

The TDW_DENI_[4—1] is an encoded signal sampled on the rising edge of the DWAC clock which identifies three possible actions: the DWAC data overwrites the selected overhead byte, a default value is inserted, or the incoming value is passed unchanged.

The timing characteristics for the transmit overhead serial pins are given in Figure 11 and Table 44.

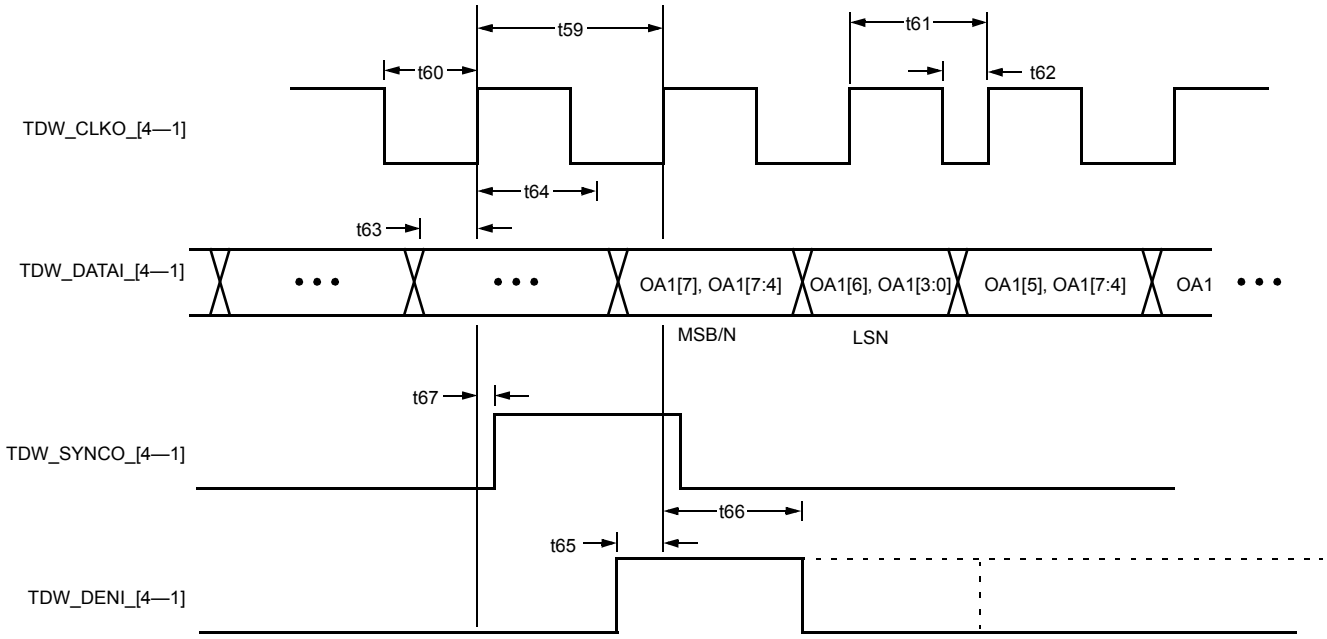


Figure 11. Transmit FEC/Digital Wrapper Overhead Serial Timing

Table 44. Transmit FEC/Digital Wrapper Overhead Channel

Symbol	Parameter	Min	Typ	Max	Unit
t59	Clock Period (long clock)	—	96.02	—	ns
t60	Clock High Width	—	48.01	—	ns
t61	Clock Period (short clock)	—	84.02	—	ns
t62	Clock Low Width	—	36.01	—	ns
t63	Data Setup Time Required	8	—	—	ns
t64	Data Hold Time Required	0	—	—	ns
t65	TDW_DENI_[4—1] Setup Time Required	8	—	—	ns
t66	TDW_DENI_[4—1] Hold Time Required	0	—	—	ns
t67	Clock to Frame Pulse Delay	0.6	—	8	ns

Table 45. Transmit FEC/Digital Wrapper Overhead Channel—Load/Rise and Fall Times

Signal	Test Load	Max—tR/tF	Unit
TDW_CLKO_[4—1]	C_L = 15 pF	3.5/3.5	ns
TDW_SYNCO_[4—1]	C_L = 15 pF	3.5/3.5	ns
TDW_DATAI_[4—1]	NA	3.5/3.5	ns
TDW_DENI_[4—1]	NA	3.5/3.5	ns

10 Test

10.1 Scan

This device supports the *IEEE* 1149.1 JTAG interface for memory BIST, boundary scan, and 32-bit ID register instructions.

10.2 Boundary Scan

Full boundary scan is supported on this device. Boundary scan is activated from the JTAG port.

10.3 RAM BIST

Embedded memories support BIST. The BIST algorithm is activated from the JTAG port.

11 Microprocessor Interface

11.1 Microprocessor Interface Overview

The TFEC0410G microprocessor interface architecture is configured for glueless interface to the *Motorola* MPC860 and MC68360 microprocessors. The *Intel* microcontrollers 8XC251 and 80C196 and the *i960* microprocessor may also be utilized to interface to the TFEC0410G. However, provisions on the board need to be made to (de)multiplex the address and data bus. The state of the MPTYPE_IM input signal indicates to the device whether it interfaces to a *Motorola* microprocessor or an *Intel* microcontroller. Other microprocessors may be used if their timing requirements fit to one of the modes described.

The TFEC0410G has separate 16-bit wide address and data busses. The MPDB_8_16 input distinguishes between an 8-bit or 16-bit wide microprocessor data bus being used. In case of an 8-bit wide microprocessor data bus interface, the eight upper bits of the device data bus ports are not being used and are held 3-state.

The microprocessor interface operates at the frequency of the microprocessor clock (PCLK) input which should be in the range of 10 MHz to 100 MHz.

Depending on the state of the MPMODE_AS input signal, the interface to the 80960SX microprocessor is synchronous, while the interface to the 8XC251 and 80C196 microcontrollers is asynchronous.

Similarly, with the MPC860 or MC68360 microprocessors being used, the state of the MPMODE_AS input signal determines whether bus transfers are synchronous or asynchronous, respectively. In this case, the microprocessor interface also generates an external processor bus error if an internal data acknowledgment is not received in a predetermined period of time, or on parity errors if the MPPAREN input is enabled.

All internal counters are latched using an external or internal performance monitor (PM) latch pulse that must occur once per second to ensure all internal counters do not saturate.

Persistency alarm registers are used in conjunction with the interrupt alarm registers to indicate whether alarms are persistent.

The TFEC0410G contains 48 general purpose inputs/outputs (GPIOs), which can be used to monitor signals on the board.

11.2 Microprocessor Interface Modes

Table 46 highlights the four microprocessor modes controlled by the MPTYPE_IM and MPMODE_AS inputs.

Table 46. Microprocessor Configuration Modes

Mode	MPTYPE_IM	MPMODE_AS	Description	Typical Application
Mode 1	1	1	Synchronous interface; handshake using data acknowledge.	MPC860
Mode 2	1	0	Asynchronous interface; handshake using data acknowledge.	MC68360, MC68HC16X
Mode 3	0	1	Synchronous interface; handshake through inserted wait states; asynchronous address latching.	*i960* (80960SX)
Mode 4	0	0	Asynchronous interface; handshake through inserted wait states; asynchronous address latching.	80C196, 8XC251

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing

The following sections show the timing specification of the external microprocessor interface in the four different modes. Note that all output timings assume a 70 pF external load.

11.3.1 Mode 1 (MPC860)

The synchronous microprocessor interface mode for the MPC860 is selected when MPTYPE_IM = 1 and MPMODE_AS = 1. Interface timing for the synchronous mode write cycle is given in Figure 12 and in Table 47. Interface timing for the read cycle is given in Figure 13 and Table 49 on page 63.

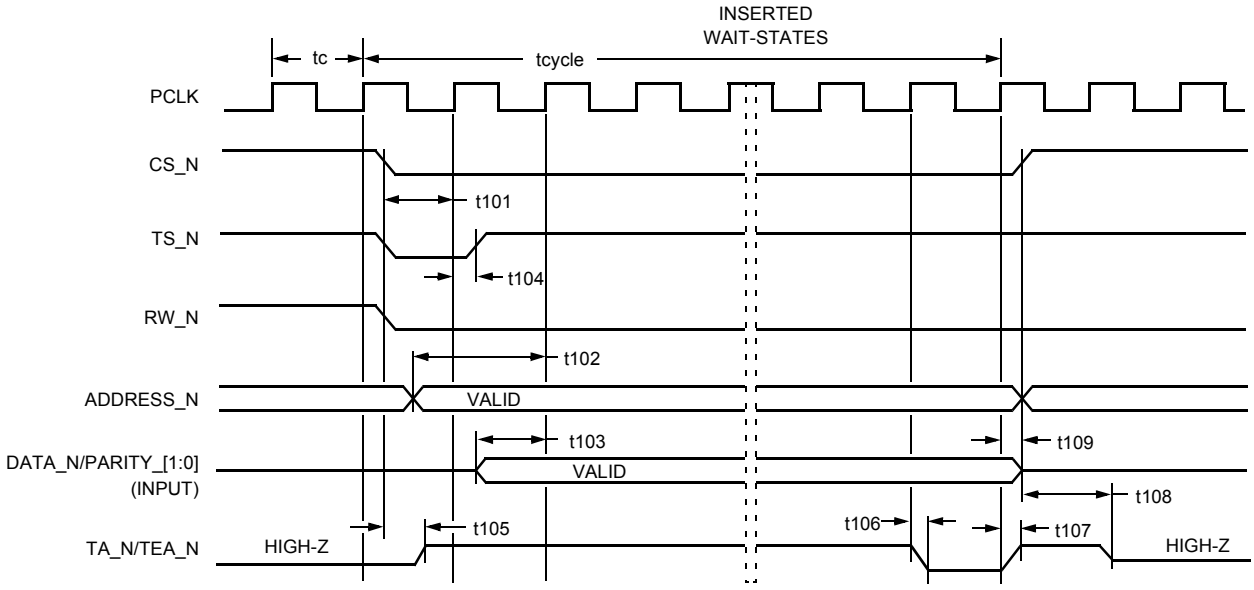


Figure 12. Microprocessor Interface Mode 1—Write Cycle Timings

Table 47. Microprocessor Interface Mode 1—Write Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
tc	PCLK Period	20	100	ns
tcycle	Bus Transfer Cycle Time	5*		tc
t101	CS_N, TS_N, RW_N Asserted Low Setup to PCLK Rise	5	—	ns
t102	ADDRESS_N Valid Setup to PCLK Rise	tc + 5	—	ns
t103	DATA_N Valid Setup to PCLK Rise	7	—	ns
t104	TS_N Asserted Low Hold after PCLK Rise	0	—	ns
t105	CS_N Asserted Low to TA_N/TEA_N High Delay	—	10	ns
t106	PCLK Rise to TA_N/TEA_N Asserted Low Delay	2	10	ns
t107	PCLK Rise to TA_N/TEA_N Negated High Delay	2	10	ns
t108	CS_N Negated to TA_N/TEA_N 3-state Delay	—	10	ns
t109	CS_N, RW_N Asserted Low Hold/ADDRESS_N, DATA_N Valid Hold after PCLK Rise	0	—	ns

* This value would be 35 tc in case of a transfer error (TA_N = 1, TEA_N = 0).

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

Table 48. TA_N/TEA_N Cycle Termination for Mode 1—Write Cycle

TA_N	TEA_N	Encoding Description
0	0	Write data parity error.
0	1	Normal cycle termination.
1	0	Access to undefined address region and bus time-out—transfer error.
1	1	No cycle termination—external processor generated time-out.

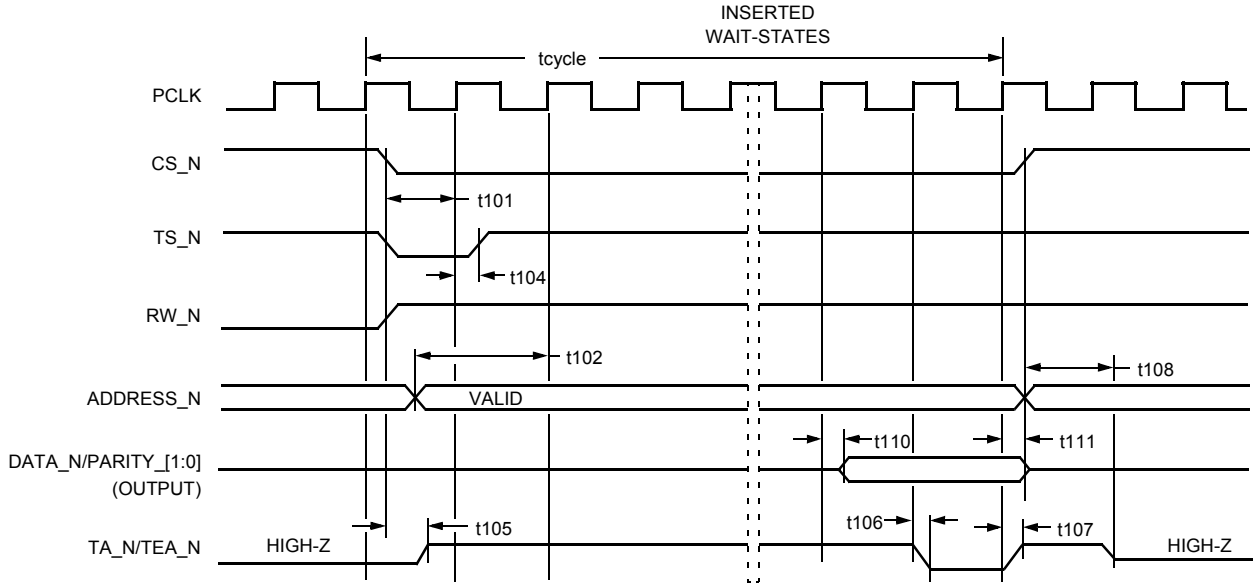


Figure 13. Microprocessor Interface Mode 1—Read Cycle Timings

Table 49. Microprocessor Interface Mode 1—Read Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
tcycle	Bus Transfer Cycle Time	7	16*	tc
t110	PCLK Rise to DATA_N Valid Delay	2	16	ns
t111	PCLK Rise to DATA_N 3-state Delay	2	16	ns

* This value would be 35 tc in case of a transfer error (TA_N = 1, TEA_N = 0). The typical value for most of the register accesses is 8 tc.

Table 50. TA_N/TEA_N Cycle Termination for Mode 1—Read Cycle

TA_N	TEA_N	Encoding Description
0	0	Not possible during read cycle.
0	1	Normal cycle termination.
1	0	Access to undefined address region and bus time-out—transfer error.
1	1	No cycle termination—external processor generated time-out.

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

11.3.2 Mode 2 (MC68360)

The asynchronous microprocessor interface mode for the MC68360 is selected when MPTYPE_IM = 1 and MPMODE_AS = 0. Interface timing for the asynchronous mode write cycle is given in Figure 14 and in Table 51. Interface timing for the read cycle is given in Figure 15 and in Table 53.

All microprocessor signals to the device should be stable for at least the time of one cycle of PCLK plus additional setup time to be safely detected by the device. For this reason, the PCLK should be connected to the CLKO2 output of the MC68360 or a faster clock.

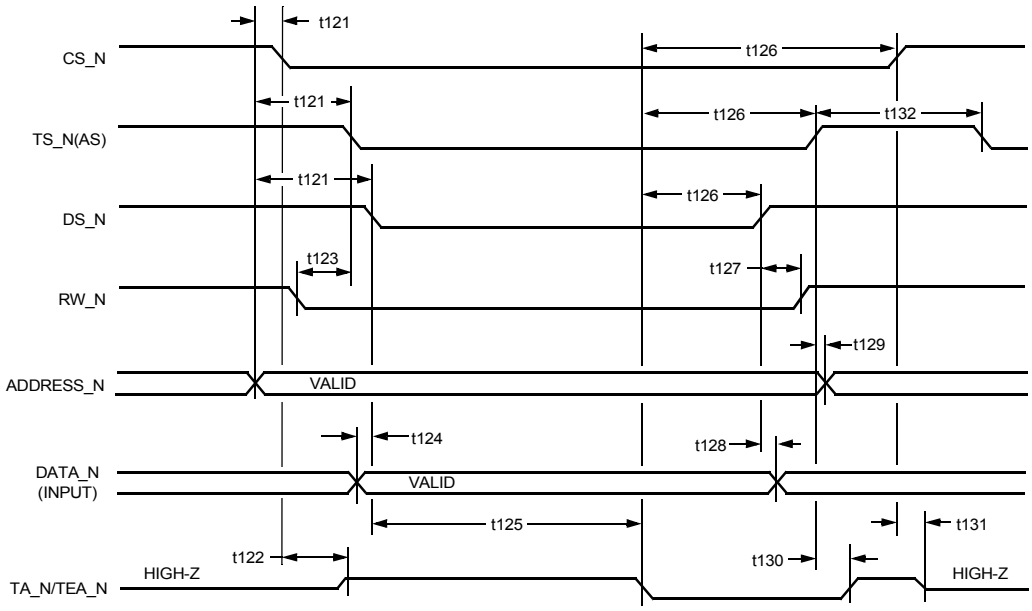


Figure 14. Microprocessor Interface Mode 2—Write Cycle Timings

Table 51. Microprocessor Interface Mode 2—Write Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
tc	PCLK Period	10	100	ns
t121	ADDRESS_N Valid Setup to CS_N, DS_N, TS_N Asserted Low	0	—	ns
t122	CS_N Asserted Low to TA_N/TEA_N High Delay	—	10	ns
t123	RW_N Asserted Low Setup to TS_N Asserted Low	0	—	ns
t124	DATA_N Valid Setup to DS_N Asserted Low	0	—	ns
t125	DS_N Asserted Low to TA_N/TEA_N Asserted Low Delay	5	6*	tc
t126	CS_N, DS_N, TS_N Asserted Low Hold after TA_N Asserted Low	1	—	tc
t127	RW_N Asserted Low Hold after DS_N Negated	0	—	ns
t128	DATA_N Valid Hold after DS_N Negated	0	—	ns
t129	ADDRESS_N Valid Hold after TS_N Negated	0	—	ns
t130	TS_N Negated to TA_N/TEA_N Asserted High Delay	0	10	ns
t131	CS_N Negated to TA_N/TEA_N 3-state Delay	—	10	ns
t132	TS_N Negated Hold after TS_N Asserted	tc + 5	—	ns

* This value would be 36 tc in case of a transfer error (TA_N = 1, TEA_N = 0).

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

Table 52. TA_N/TEA_N Cycle Termination for Mode 2—Write Cycle

TA_N	TEA_N	Encoding Description
0	0	Write data parity error.
0	1	Normal cycle termination.
1	0	Access to undefined address region and bus time-out—transfer error.
1	1	No cycle termination—external processor generated time-out.

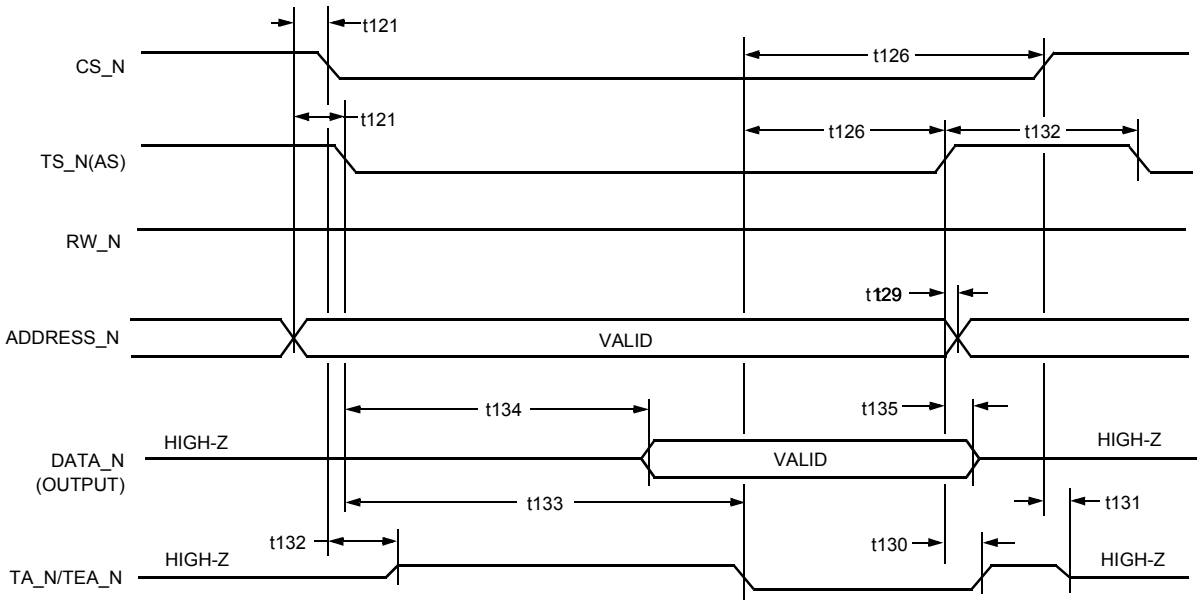


Figure 15. Microprocessor Interface Mode 2—Read Cycle Timings

Table 53. Microprocessor Interface Mode 2—Read Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
t133	TS_N (AS) Asserted Low to TA_N/TEA_N Asserted Low Delay	7	22*	tc
t134	TS_N (AS) Asserted Low to DATA_N Valid Delay	6	21	tc
t135	TS_N Negated to DATA_N 3-state Delay	0	16	ns

* This value would be 36 tc in case of a transfer error (TA_N = 1, TEA_N = 0). The typical value for most of the register accesses is 8 tc.

Table 54. TA_N/TEA_N Cycle Termination for Mode 2—Read Cycle Mode 3 (*i960*)

TA_N	TEA_N	Encoding Description
0	0	Not possible during read cycle.
0	1	Normal cycle termination.
1	0	Access to undefined address region and bus time-out—transfer error.
1	1	No cycle termination—external processor generated time-out.

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

11.3.3 Mode 3 (*i960* (80960SX))

The synchronous microprocessor interface mode for the *i960* (80960SX) is selected when MPTYPE_IM = 0 and MPMODE_AS = 1. Interface timing for the synchronous mode write cycle is given in Figure 16 and in Table 55. Interface timing for the read cycle is given in Figure 17 and Table 56 on page 67.

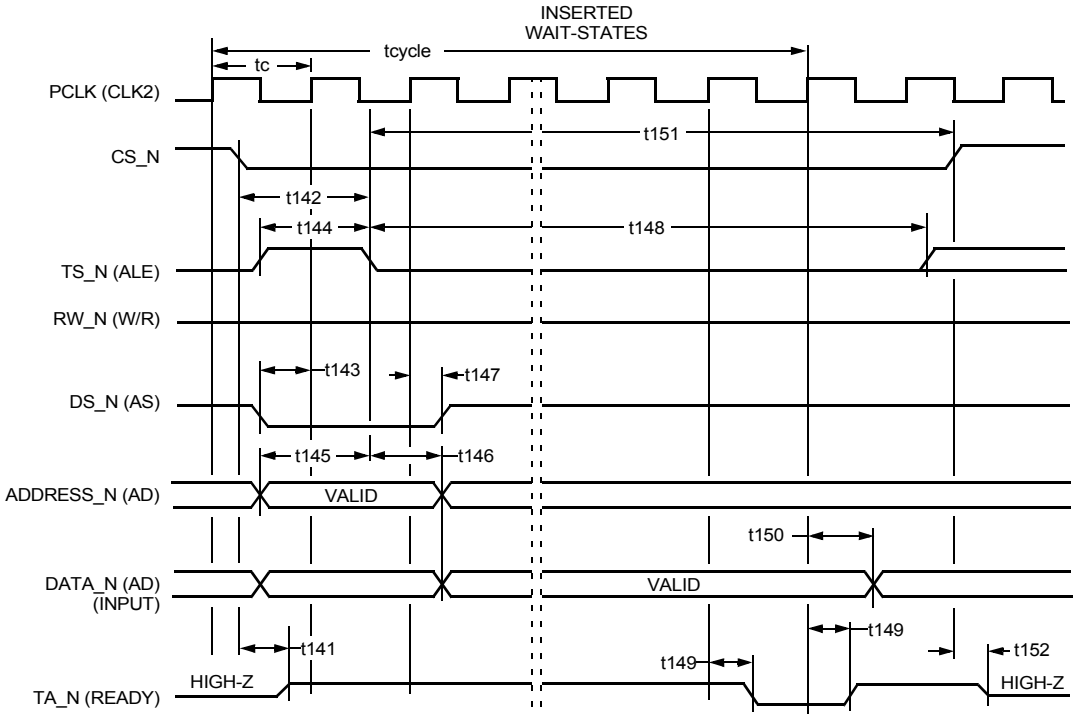


Figure 16. Microprocessor Interface Mode 3—Write Cycle Timings

Table 55. Microprocessor Interface Mode 3—Write Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
tc	PCLK Period	25	100	ns
tcycle	Bus Transfer Cycle Time	6		tc
t141	CS_N Asserted Low to TA_N (READY) High Delay	—	10	ns
t142	CS_N Asserted Low Setup to TS_N (ALE) Fall	10	—	ns
t143	DS_N (AS)/RW_N (W/R) Asserted Low Setup to PCLK Rise	5	—	ns
t144	TS_N (ALE) High to Fall Setup	10	—	ns
t145	ADDRESS_N Valid Setup to TS_N (ALE) Fall	10	—	ns
t146	ADDRESS_N Valid Hold/DATA Valid Delay after TS_N (ALE) Fall	5	—	ns
t147	DS_N (AS) Asserted Low Hold after PCLK Rise	0	—	ns
t148	TS_N (ALE) Asserted Low Hold	5	—	tc
t149	PCLK Rise to TA_N (READY) Delay	2	10	ns
t150	DATA_N Valid Hold after PCLK Rise	0	—	ns
t151	CS_N Asserted Low Hold after TS_N (ALE) Fall	6	—	tc
t152	CS_N Negated to TA_N (READY) 3-state Delay	—	10	ns

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

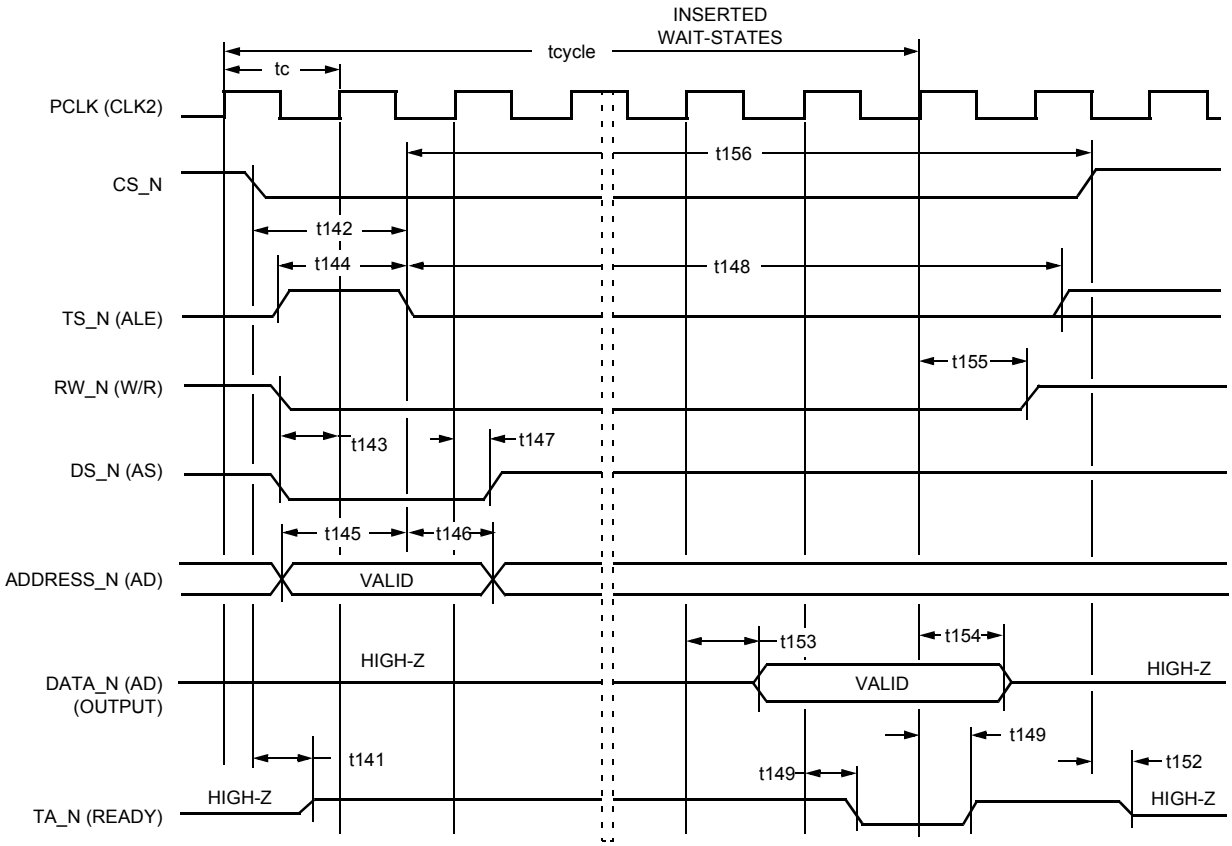


Figure 17. Microprocessor Interface Mode 3—Read Cycle Timings

Table 56. Microprocessor Interface Mode 3—Read Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
tcycle	Bus Transfer Cycle Time	8	16*	tc
t153	PCLK Rise to DATA_N Valid Delay	2	16	ns
t154	PCLK Rise to DATA_N 3-state Delay	2	16	ns
t155	RW_N (W/R) Asserted Low Hold after PCLK Rise	0	—	ns
t156	CS_N Asserted Low Hold after TS_N (ALE) Fall	8	—	tc

* The typical value for most register accesses is 8 tc.

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

11.3.4 Mode 4 (80C196, 8XC251)

The asynchronous microprocessor interface mode for the 80C196 and 8XC251 is selected when MPTYPE_IM = 0 and MPMODE_AS = 0. Interface timing for the asynchronous mode write cycle is given in Figure 18 and in Table 57. Interface timing for the read cycle is given in Figure 19 and Table 58 on page 69. All microprocessor signals to the device should be stable for at least the time of one cycle of PCLK (tc) plus additional setup time to be safely detected by the device. In the case that the 80C196 is being used, one programmed wait state may be needed to ensure that the falling edge of TA_N (READY) gets captured early enough by the microprocessor.

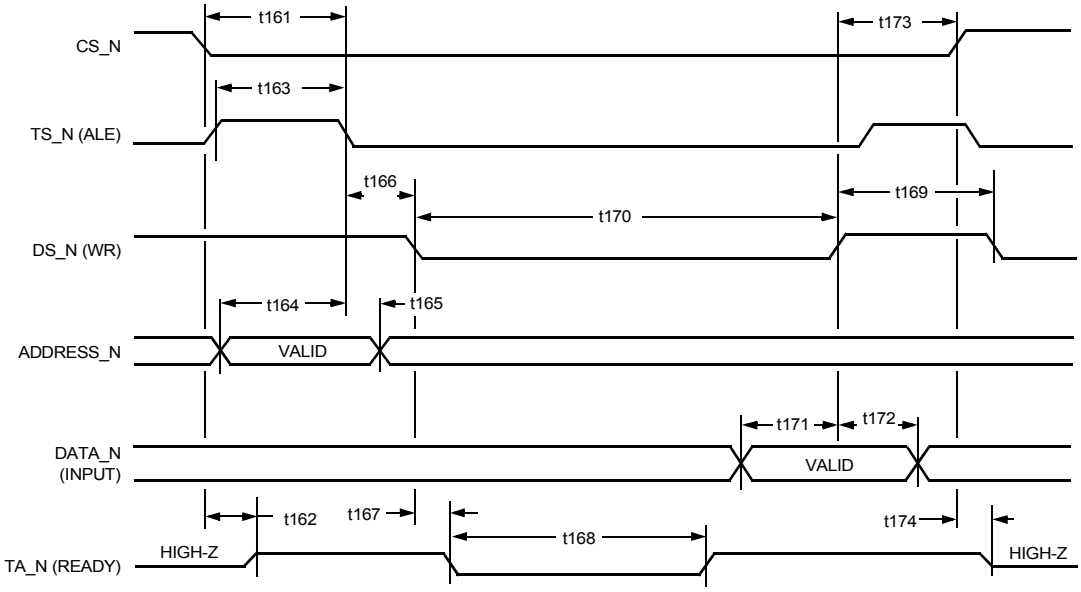


Figure 18. Microprocessor Interface Mode 4—Write Cycle Timings

Table 57. Microprocessor Interface Mode 4—Write Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
tc	PCLK Period	10	100	ns
t161	CS_N Asserted Low Setup to TS_N (ALE) Fall	10	—	ns
t162	CS_N Asserted Low to TA_N (READY) High Delay	—	10	ns
t163	TS_N (ALE) High to Fall Setup	10	—	ns
t164	ADDRESS_N Valid Setup to TS_N (ALE) Fall	10	—	ns
t165	ADDRESS_N Valid Hold after TS_N (ALE) Fall	10	—	ns
t166	TS_N (ALE) Fall Setup to DS_N (WR) Asserted Low	0	—	ns
t167	DS_N (WR) Asserted Low to TA_N (READY) Asserted Low Delay	0	10	ns
t168	TA_N (READY) Asserted Low to Negated Delay	6	8	tc
t169	DS_N (WR) /RW_N (RD) Negated Hold	tc + 5	—	ns
t170	DS_N (WR) Asserted Low Hold*	7	—	tc
t171	DATA_N Valid Setup to DS_N (WR) Negated	10	—	ns
t172	DATA_N Valid Hold after DS_N (WR) Negated	5	—	ns
t173	CS_N Asserted Low Hold after DS_N (WR) Negated	0	—	ns
t174	CS_N Negated to TA_N (READY) 3-state Delay	—	10	ns

* The rising edge of DS_N (WR) is expected to come after the rising edge of TA_N (READY).

11 Microprocessor Interface (continued)

11.3 Microprocessor Interface Timing (continued)

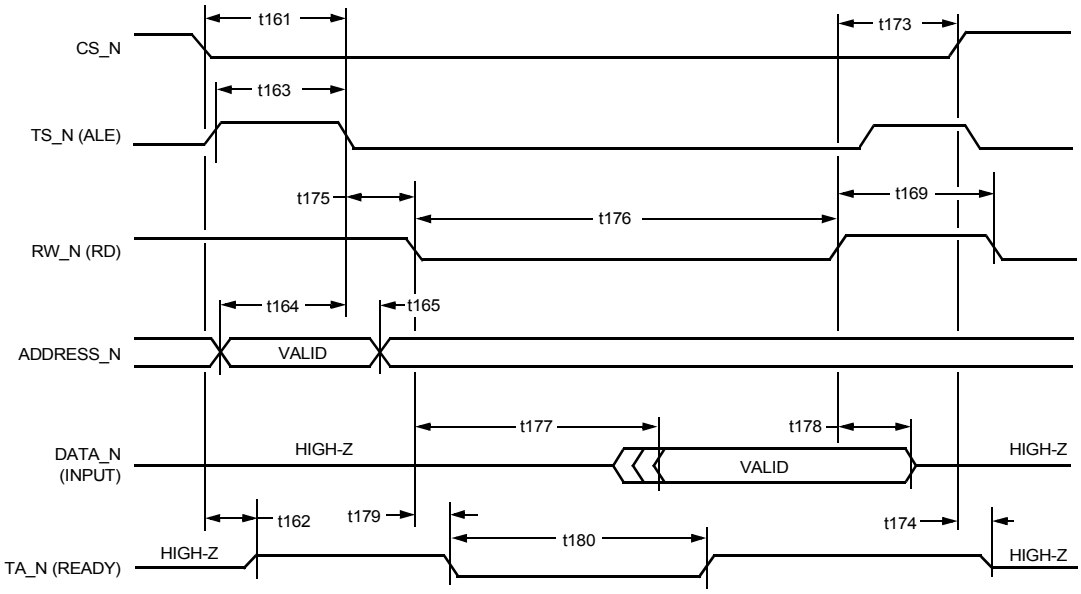


Figure 19. Microprocessor Interface Mode 4—Read Cycle Timings

Table 58. Microprocessor Interface Mode 4—Read Cycle Timing Specifications

Symbol	Parameter	Min	Max	Unit
t175	TS_N (ALE) Fall Setup to RW_N (RD) Asserted Low	0	—	ns
t176	RW_N (RD) Asserted Low Hold*	9	—	ns
t177	RW_N (RD) Asserted Low to Data Valid Delay	7	24†	tc
t178	RW_N (RD) Negated to Data 3-state Delay	0	16	ns
t179	RW_N (RD) Asserted Low to TA_N (READY) Asserted Low Delay	0	10	ns
t180	TA_N (READY) Asserted Low to Negated Delay	8	25	tc

* The rising edge of RW_N (RD) is expected to come after the rising edge of TA_N (READY).
† The typical value for most register accesses is 7 tc—10 tc.

11.4 Use of a Synchronous Microprocessor with the TFEC0410G in Asynchronous Mode

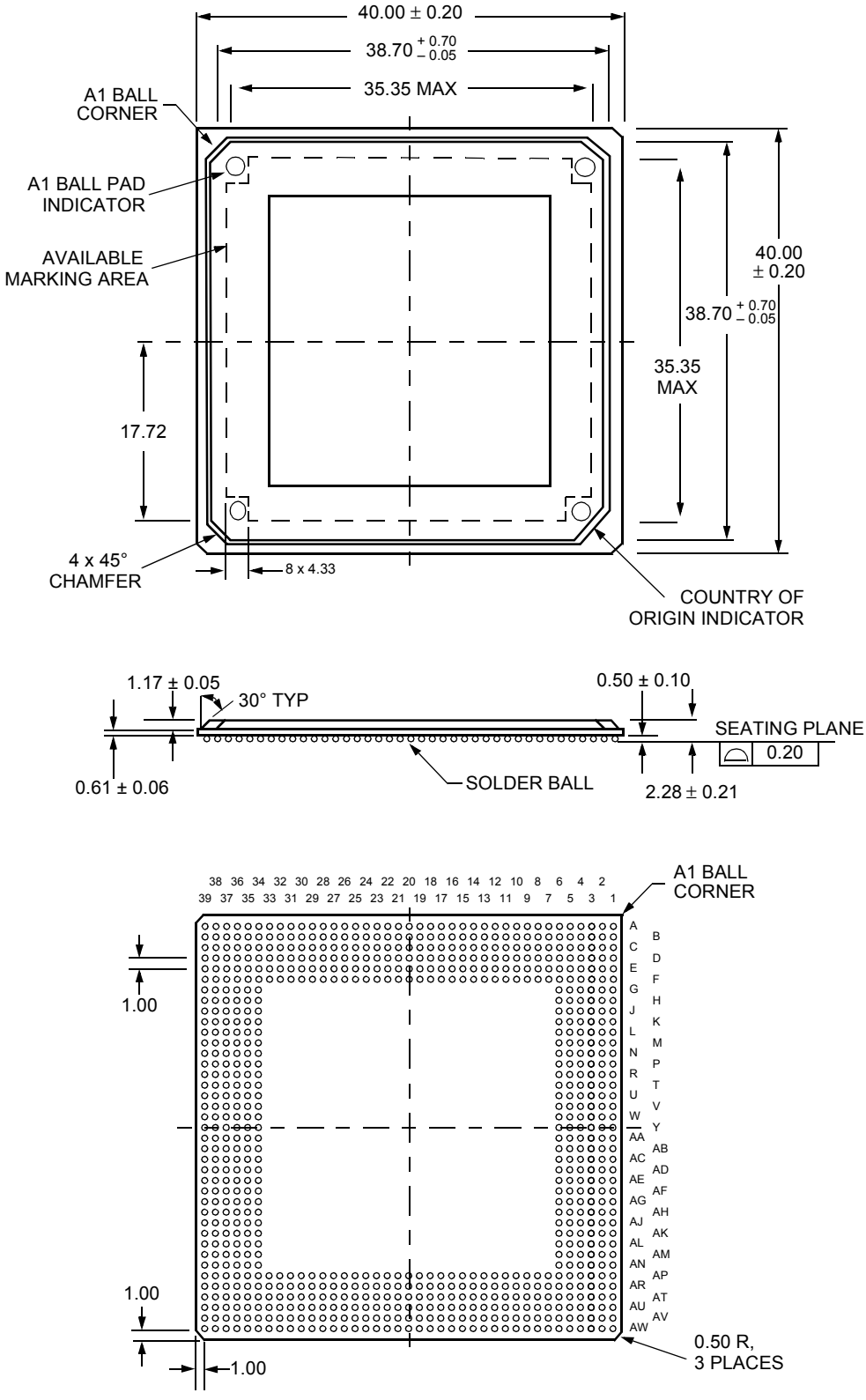
The use of a synchronous microprocessor (such as the M860/M8260) to communicate with a TFEC0410G configured for asynchronous mode (MPMODE = 2) requires one additional consideration. There is a difference between the operation of a synchronous processor (e.g., M860/M8260) and the asynchronous processors (e.g., 68360). In a synchronous processor, the data is latched on the same edge that detects the assertion of TA_N. In an asynchronous processor, the TA_N (DSACK) signal is detected, and the data is latched one clock period later.

In both cases, the TFEC0410G meets the timing required by these two different microprocessors. However, a synchronous processor operating with the TFEC0410G configured in asynchronous mode will have problems consistently latching the correct data. It will depend on the relationship between the two clocks. As is shown in Figure 15 on page 65, the data is presented on the bus after TA_N is asserted. If the microprocessor has a rising edge within this window, it will capture incorrect data.

To operate the TFEC0410G in asynchronous mode with a synchronous processor, add a delay on the TA_N signal from the TFEC0410G; otherwise, consider using synchronous mode.

12 Outline Diagram

12.1 792-Pin PBGAM1TH



13 List of Acronyms

A

ADM	Add/Drop Multiplexer
AIS	Alarm Indication Signal
AIS-L	Line Alarm Indication Signal
API	Application Program Interface
APLL	Analog Phase Locked Loop
AR	Alarm Register
AU	Administrative Unit (SDH naming for frames)

B

B1, B2, B3	Error Count Bits
BAR	Base Address Register
BCH	Bose-Chaudhuri-Hocquenguem (weak FEC cyclic code)
BDI	Backward Defect Indication
BDI-O	Backward Defect Indication Overhead
BDI-P	Backward Defect Indication Payload
BEI	Backward Error Indication
BER	Bit Error Rate
BI	Backward Indication
BIM	Byte Interleaved Multiplexer
BIP	Bit Interleaved Parity
BIP-8	Bit Interleaved Parity Level 8
BIST	Built-In Self-Test
bit	Binary Digit
BLI	Backward Line Indication
BLSR	Bidirectional Line Switch Ring
Bits/s	Bits Per Second
BS	Boundary Scan

C

C2	Expected Payload Label Bit
CBR	Constant Bit Rate
CDR	Clock Data Recovery
CM	Common Mode or Configuration Management or Connection Monitoring
CMEP	Connection Monitoring End Point
CMF	Common-Mode Failure
CML	Current-Mode Logic
CMOH	Connection Monitoring Overhead
CMR	Common Mode Rejection
CMS	Current-Mode Switching
CMV	Common-Mode Voltage
CNTD	Continuous N-Times Detect
COR	Clear on Read
CORBA	Common Object Request Broker Architecture
COW	Clear on Write
CPT	Cell Pointer Table
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check or Cyclic Redundancy Code
CV	Coding Violation
CV-L	Line Coding Violation
CV-P	Path Coding Violation
CV-S	Section Coding Violation

D

DCC	Data Communications Channel
DLL	Delay-Locked Loop
DPLL	Dedicated Phase-Locked Loop
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
DW	Digital Wrapper
DWAC	Digital Wrapper Access Channel
DWDM	Dense Wavelength Division Multiplexing
DWSFEC	Digital Wrapper Enhanced Forward Error Correction

E

EFEC	Enhanced Forward Error Correction
ES	Errored Second or Elastic Store
ESD	Electrostatic Discharge
ESF	Extended Superframe
ESI	End System Identifier
EVT	Egress VC Table
EXTEST	External Test
ExTI	Expected Trace Identifier

F

FAE	Field Application Engineer
FAS	Frame Alignment Signal
FCBGA	Flip-Chip Ball-Grid Array
FCS	Frame Check Sequence
FDI	Forward Defect Indication
FDI-O	Forward Defect Indication Overhead
FDI-P	Forward Defect Indication Payload
FE	Framing (bit) Error
FEBE	Far-End Block Error
FEC	Forward Error Correction
FIFO	First In, First Out
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
FS	Fixed Stuff
FSI	FEC Status Indicator
FSM	Finite State Machine
FTFL	Fault Type and Fault Location

13 List of Acronyms (continued)

G

GbE	Gigabit Ethernet
GND	Ground
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
GRST	Global Reset
GSR	Global Set/Reset

H

H1, H2	SONET Signal Payload Pointer Bits
HDLC	High-Level Data Link Control
HEC	Header Error Correction or Header Error Control
HSI	High-Speed Interface
HW	Hardware

I

I/O	Input/Output
IaDI	Intra-Domain Interface
IAE	Incoming Alignment Error
IDI	Initial Domain Identifier
IrDI	Inter-Domain Interface
IRQ	Interrupt Request
ISR	Interrupt Status Register
ITU	International Telecommunications Union

J

J1	Trace Byte
JEDEC	Joint Electronic Devices Engineering Council
JC	Stuff Control Byte
JTAG	Joint Test Access Group

K

K1, K2	APS Bits of SONET Signal

L

laDI	Intradomain Interface
LAN	Local Area Network
LAPI	Low-Level Application Programming Interface
LB	Loopback
LCK	Locked
LED	Light Emitting Diode
LOC	Loss of Clock
LOF	Loss of Frame
LOFA	Loss of Frame Alignment
LOH	Line Overhead
LOL	Loss of Lock
LOM	Loss of Multiframe Alignment
LOP	Loss of Pointer
LOS	Loss of Signal
LOTC	Loss of Transmit Clock
lrDI	Interdomain Interface
LSB	Least Significant Bit/Byte
LSN	Least Significant Nibble
LTE	Line Terminating Equipment
LV	Low Voltage
LVDS	Low-Voltage Differential Signal

M

MFAS	Multiframe Alignment Signal
MPI	Microprocessor Interface
MPIF	Master Processor Interface
MS	Multiplex Section
MSB	Most Significant Bit/Byte
MSI	Multiplex Structure Identifier
MSN	Most Significant Nibble
MUTEX	Mutual Exclusion
MUX	Multiplex or Multiplexor

N

NJO	Negative Justification Offset (Negative Justification Byte)
NRZ	Nonreturn to Zero
NSA	Non-Service Affecting
N-Time Detect	A received value remains the same for N consecutive frames.

13 List of Acronyms (continued)

O

OA&M	Operations Administration and Maintenance
OCh	Optical Channel (single)
OCI	Open Connection Indication
ODUk	Optical Channel Data Unit
OH	Overhead
OHP	Overhead Processor
OHPI	Overhead Processor Insertion
OHPM	Overhead Processor Monitoring
OMSn	Optical Multiplex Section Overhead
OMS	Optical Multiplexing Section
OMU	Optical Multiplexing Unit
ONNI	Optical Transport Network Node Interface
OOA	Out of Alignment
OOF	Out of Frame
OOM	Out of Multiframe Alignment
OOS	Optical Transport Module Overhead Signal
OPU	Optical Channel Payload Unit
OSC	Optical Supervisory Channel
OSI	Open System Interconnect
OTH	Optical Transport Hierarchy
OTM	Optical Transport Module
OTM-0	Optical Transport Module of Order 0
OTN	Optical Transport Network
OTS	Optical Transmission Section
OTSn	Optical Transmission Section Overhead
OTUk	Optical Channel Transport Unit

P

PA	Persistency Alarm
PBGA	Plastic Ball Grid Array
PBGAM	Plastic Ball Grid Array Multilayer
PCLK	Microprocessor Clock
PD	Phase Detector
PDI	Payload Defect Indication
PHY	Physical Layer
PJO	Positive Justification Offset Byte
PLL	Phase-Locked Loop
PM	Performance Monitoring
PMCLK	Performance Monitoring Clock
PMOH	Path Monitoring Overhead
PN	Pseudo-Random Noise Sequence or Pseudo-Random Number (i.e., PN29)
PNZ	Positive/Negative/Zero
POAC	Path Overhead Access Channel
POH	Path Overhead
POS	Packet-Over-SONET/SDH
P-P	Peak to Peak
PP	Pointer Processor
PPLL	Programmable Phase-Locked Loop
PRAM	Pointer Random Access Memory
PRBS	Pseudo-Random Bit Sequence
PSI	Payload Structure Identifier

Q

QoS	Quality of Service

R

R/W	Read/Write
RAI	Remote Alarm Indication
RDI	Remote Defect Indicator
RDI-L	Line Remote Defect Indication
REI	Remote Error Indication
REI-L	Line Remote Error Indication
RES	Reserved
RN	Random Number
RO	Read Only
RS	Reed Solomon (strong FEC)
RW	Read/Write
Rx	Receive
RZ	Return to Zero

13 List of Acronyms (continued)

S

SA	Service Affecting
SCLK	System Clock
SD	Signal Degrade
SDH	Synchronous Digital Hierarchy
SEF	Severely Errored Frame
SERDES	Serializer/Deserializer
SF	Signal Fail
SFI	SERDES Framer Interface
SFI-4	SERDES Framer Interface Level 4
SM	Section Monitoring
SNMP	Simple Network Management Protocol
SNR	Signal-to-Noise Ratio
SOH	Section Overhead
SONET	Synchronous Optical Network
SONFEC	SONET Forward Error Correction
SPA	Selected Packet Available
SPE	SONET Payload Envelope
SPIF	Slave Processor Interface
STAT	Status Indication
STE	Section Terminating Equipment
SWI	Software Interrupt

T

TA	Transfer Acknowledge
T_A	Ambient Temperature
TBD	To Be Determined
TC	Temperature Coefficient or Time Constant or Tandem Connection
T_C	Case Temperature
TCK	Test Clock
TCM	Tandem Connection Monitoring
TCMOH	Tandem Connection Monitoring Overhead
TDI	Test Data In
TDM	Time Division Multiplexer
TDMX	Transpose DeMultiplexer
TDO	Test Data Out
TEA	Transfer Error Acknowledge
TFEC	Transmission Forward Error Correcting
TIM	Trace Identifier Mismatch
T_J	Junction Temperature
TMS	Test Mode Select
TOAC	Transport Overhead Access Channel
TOH	Transport Overhead
T_{prop}	Propagation Time
TRSTN	Test Reset (Active Low)
TS	Time Slot or Tributary Slot
TSI	Time-Slot Interchange
TSM	Tributary Slot Multiplexing
TTI	Trail Trace Identifier
Tx	Transmit

U

UNEQ	Unequipped
UNI	User-Network Interface
UPSR	Unidirectional Path Switch Ring
UTOPIA	Universal Test and Operations Physical Interface for ATM

V

VBR	Variable Bit Rate
VC	Virtual Channel
VCI	Virtual Connection Indicator
VCO	Voltage-Controlled Oscillator
VP	Virtual Path
VPI	Virtual Path Indicator
VT	Virtual Tributary
VTG	Virtual Tributary Group

W

W1C	Write One Clear
WDM	Wavelength Division Multiplexing
WRR	Weighted Round Robin

X

XPIF	External Processor Interface

Z

Z0	Section Overhead Bit

14 Ordering Information

Device Code	Package	Temperature	Comcode (ordering number)
TFEC0410G-3PBGA2	792-Pin PBGAM1TH	–40 °C to 85 °C	700012029

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