FAIRCHILD SEMICONDUCTOR®

November 2001

# SSP45N20B/SSS45N20B

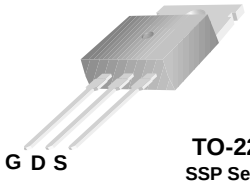
## 200V N-Channel MOSFET

### General Description

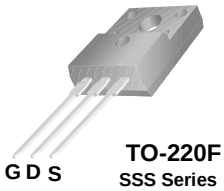
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

### Features

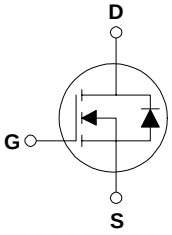
- 35A, 200V, $R_{DS(on)}$ = 0.065Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 133 nC)
- Low Crss ( typical 120 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability




**TO-220**
**SSP Series**




**TO-220F**
**SSS Series**




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | SSP45N20B | SSS45N20B | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 200 | | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 35 | 35 * | A |
| | - Continuous ($T_C$ = 100°C) | | 22.2 | 22.2 * | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 140 | 140 * | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 30 | | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 650 | | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 35 | | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 17.6 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 5.5 | | V/ns |
| $P_D$ | Power Dissipation ($T_C$ = 25°C) | | 176 | 57 | W |
| | - Derate above 25°C | | 1.41 | 0.45 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | | °C |

* Drain current limited by maximum junction temperature.

## Thermal Characteristics

| Symbol | Parameter | SSP45N20B | SSS45N20B | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case Max. | 0.71 | 2.2 | °C/W |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink Typ. | 0.5 | -- | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient Max. | 62.5 | 62.5 | °C/W |

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 200 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | -- | 0.2 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V | -- | -- | 10 | μA |
| | | $V_{DS}$ = 160 V, $T_C$ = 125°C | -- | -- | 100 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2.0 | -- | 4.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 17.5 A | -- | 0.052 | 0.065 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 40 V, $I_D$ = 17.5 A (Note 4) | -- | 36 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 3300 | 4300 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 460 | 600 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 120 | 155 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 100 V, $I_D$ = 45 A, $R_G$ = 25 Ω (Note 4, 5) | -- | 45 | 100 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 340 | 690 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 360 | 730 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 270 | 550 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 160 V, $I_D$ = 45 A, $V_{GS}$ = 10 V (Note 4, 5) | -- | 133 | 173 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 19 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 67 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 35 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 140 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 35 A | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 45 A, $dI_F$ / dt = 100 A/μs (Note 4) | -- | 245 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 2.27 | -- | μC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.8mH, $I_{AS}$ = 35A, $V_{DD}$ = 50V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD} \leq$ 45A, di/dt $\leq$ 300A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width $\leq$ 300μs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

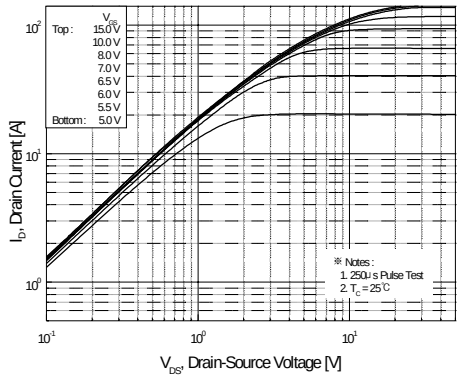



**Figure 1. On-Region Characteristics**

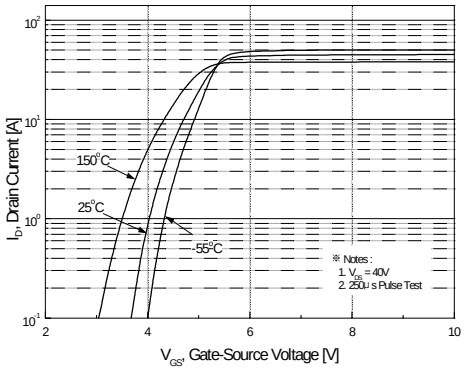



**Figure 2. Transfer Characteristics**

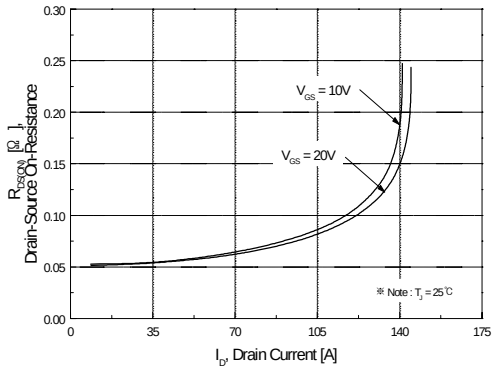



**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**

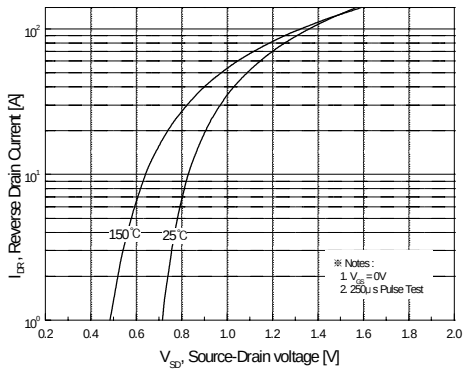



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

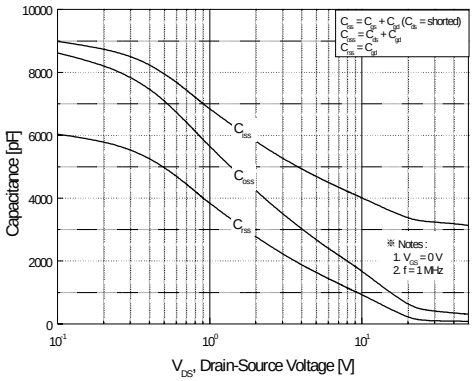



**Figure 5. Capacitance Characteristics**

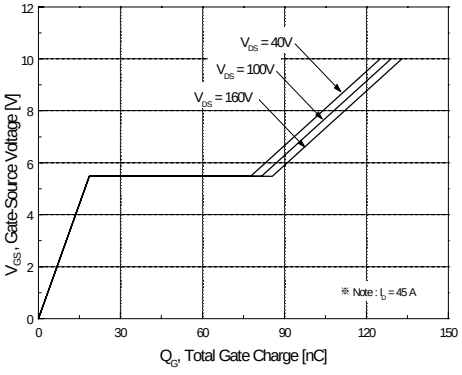



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

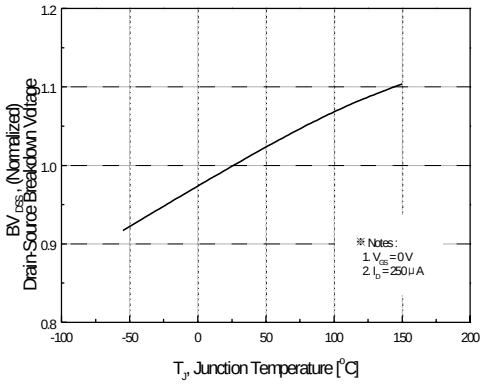



**Figure 7. Breakdown Voltage Variation vs Temperature**

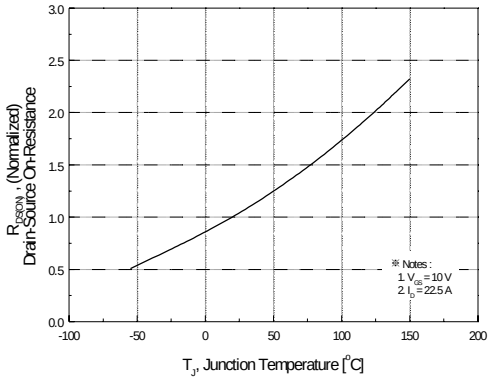



**Figure 8. On-Resistance Variation vs Temperature**

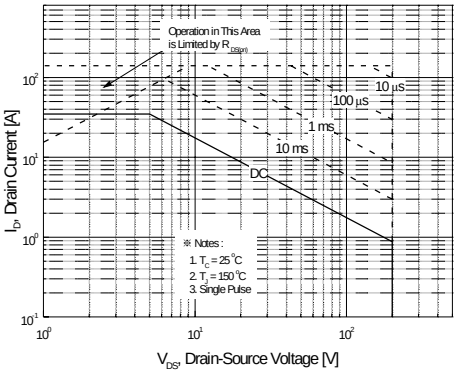



**Figure 9-1. Maximum Safe Operating Area for SSP45N20B**

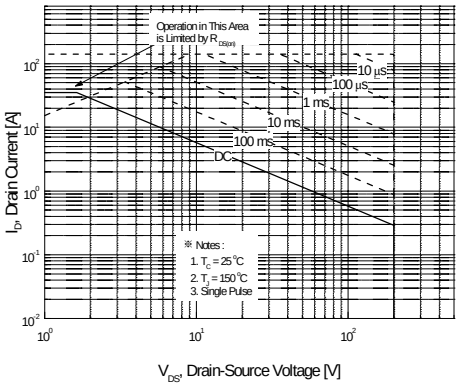



**Figure 9-2. Maximum Safe Operating Area for SSS45N20B**

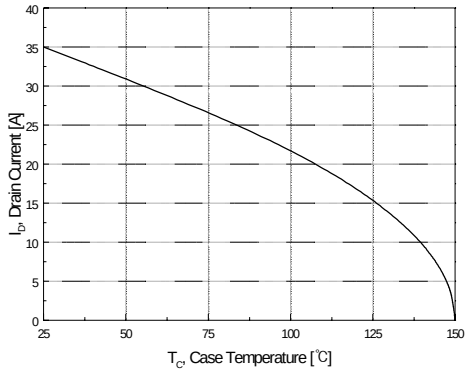



**Figure 10. Maximum Drain Current vs Case Temperature**

## Typical Characteristics (Continued)

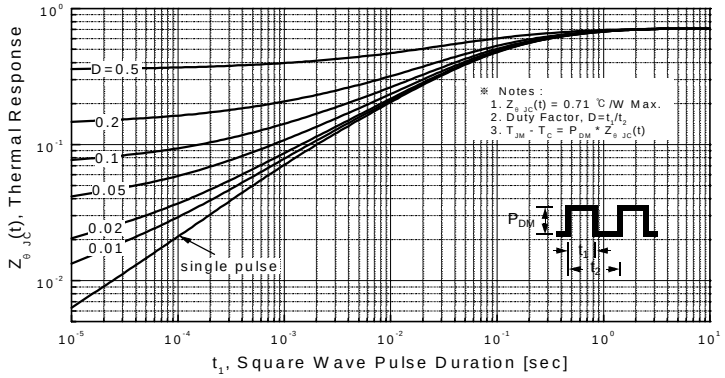



**Figure 11-1. Transient Thermal Response Curve to SSP45N20B**

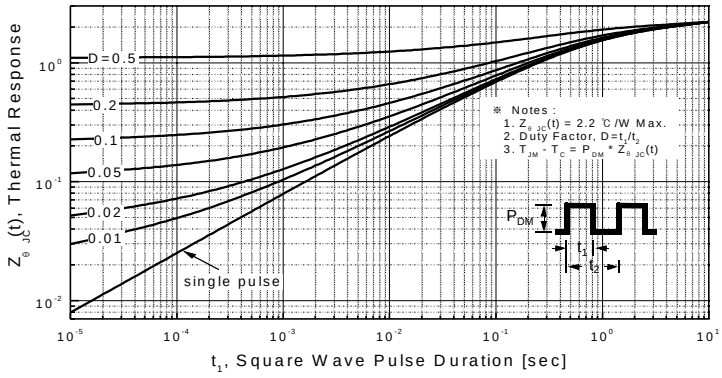
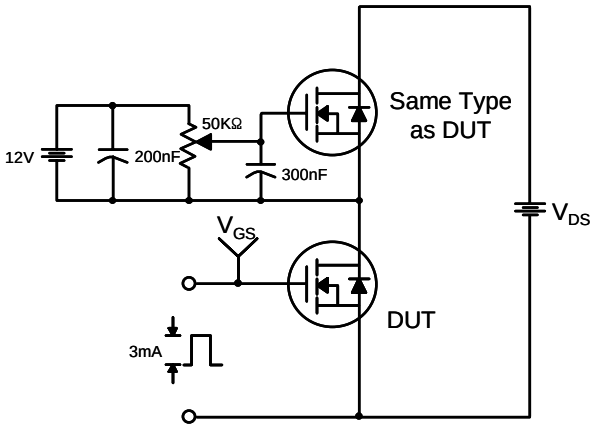
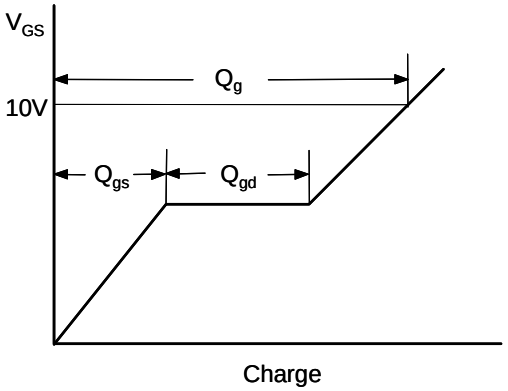


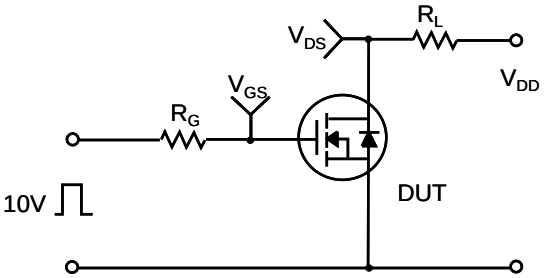

**Figure 11-2. Transient Thermal Response Curve SSS45N20B**

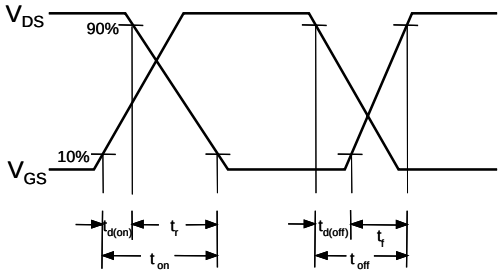
**Gate Charge Test Circuit & Waveform**



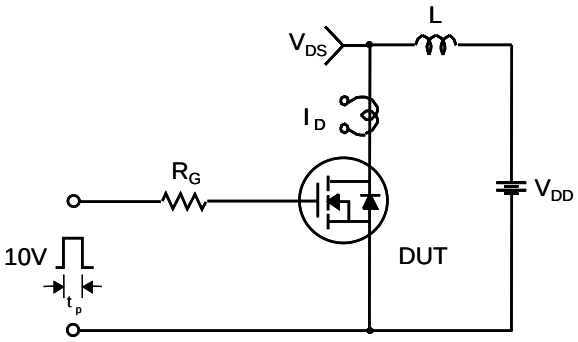




**Resistive Switching Test Circuit & Waveforms**

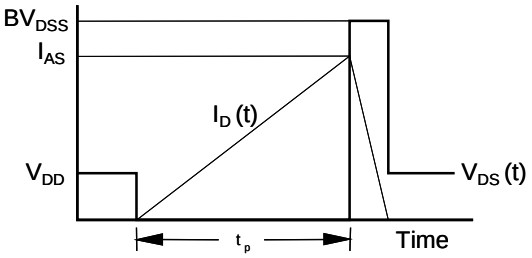


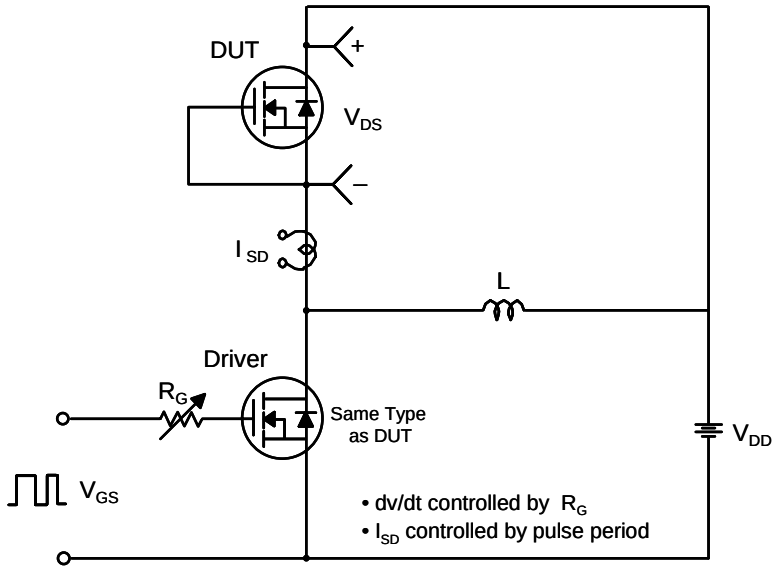

**Unclamped Inductive Switching Test Circuit & Waveforms**

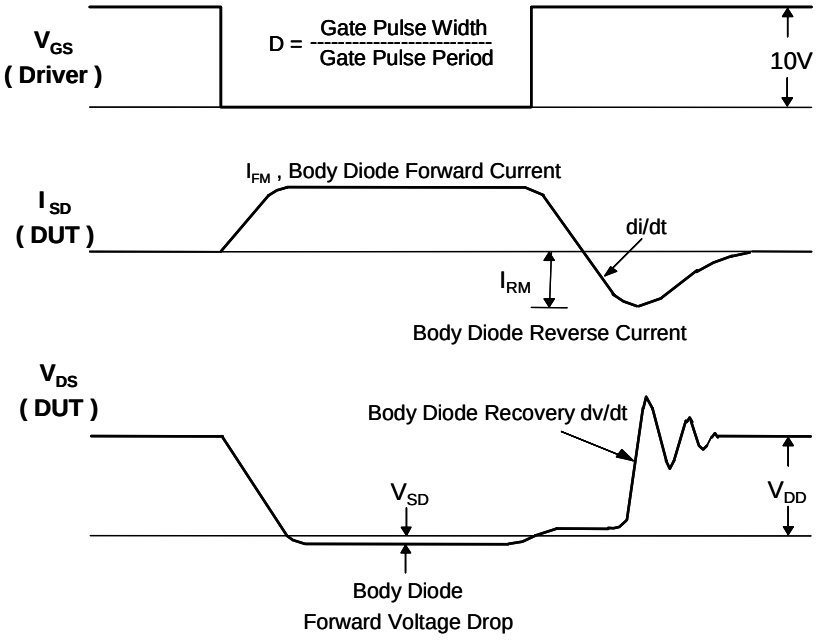



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



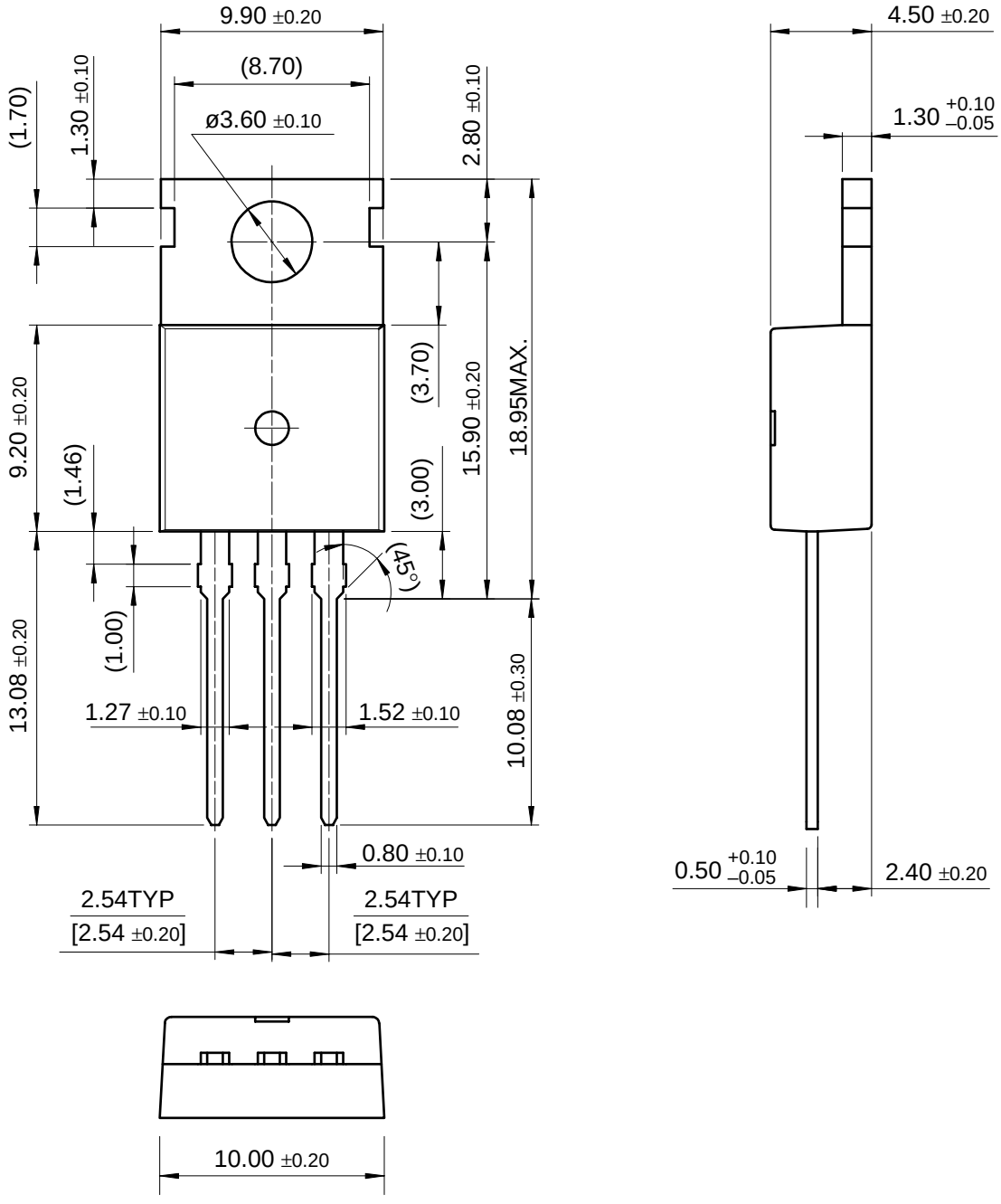
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



**Package Dimensions**

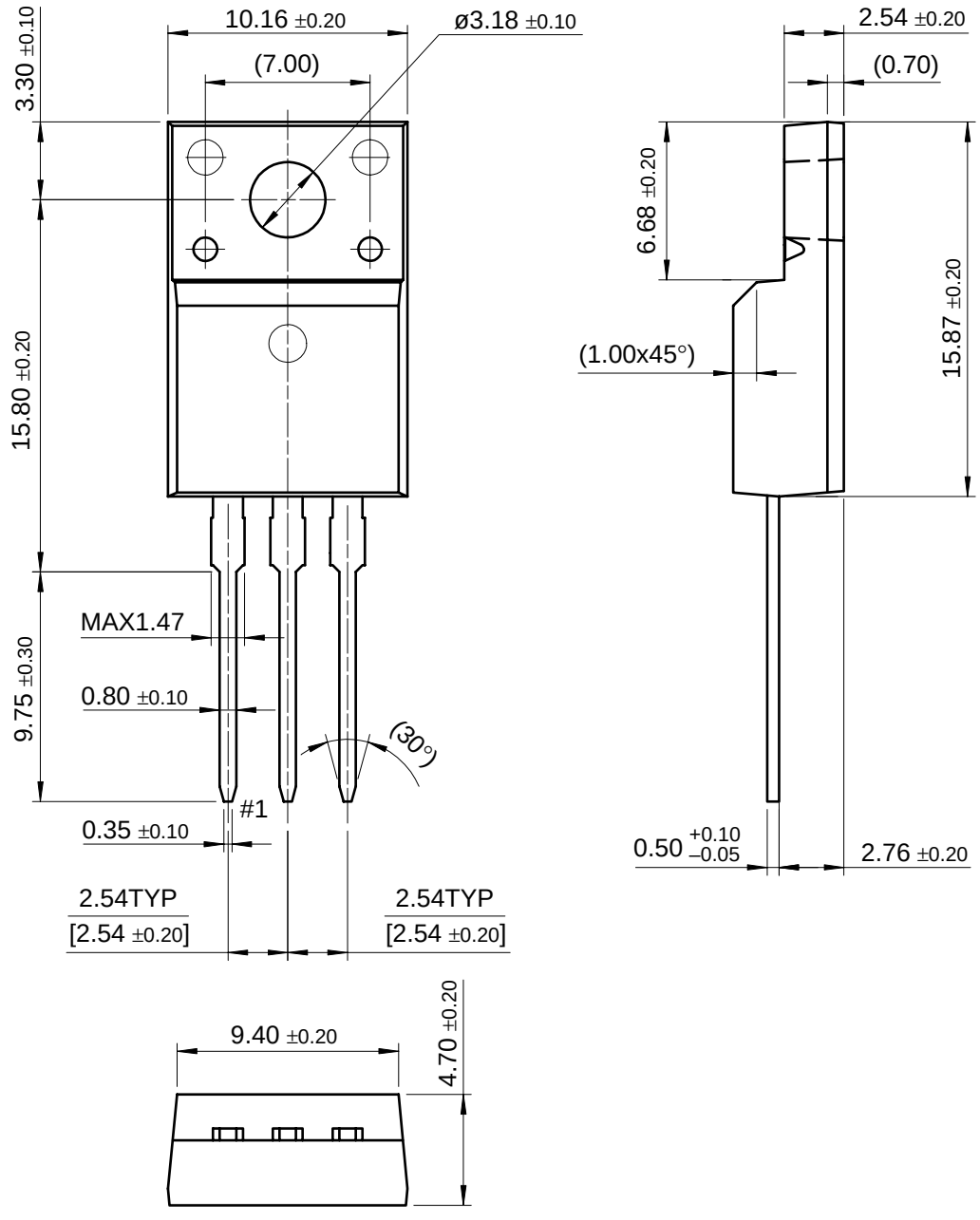
# TO-220




Dimensions in Millimeters

**Package Dimensions** (Continued)

# TO-220F




Dimensions in Millimeters

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
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| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

# SSS45N20B

200V N-Channel B-FET

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•Product status/pricing/packaging
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BUY

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- Design center

## General description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

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- Low gate charge (typical 133 nC)
- Low Crss (typical 120 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

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## Product status/pricing/packaging

BUY

| Product | Product status | Pb-free Status | Package type | Leads | Packing method | Package Marking Convention** |
|---|---|---|---|---|---|---|
| SSS45N20B_FP001 | Not recommended for new designs | | TO-220F | 3 | RAIL | Line 1: **$Y** (Fairchild logo)<br>&**Z** (Asm. Plant Code)<br>&**4** (4-Digit Date Code)<br>Line 2: SSS Line 3: 45N20B |

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product SSS45N20B is available. Click here for more information .

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**Qualification Support**

Click on a product for detailed qualification data

| Product |
|---|
| SSS45N20B_FP001 |

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