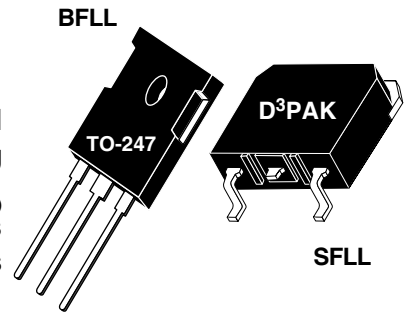
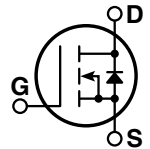


**POWER MOS 7® FREDFET**

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering  $R_{DS(ON)}$  and  $Q_g$ . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge,  $Q_g$
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D<sup>3</sup>PAK Package


**MAXIMUM RATINGS**

 All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT1201R2BFL_SFL	UNIT
$V_{DSS}$	Drain-Source Voltage	1200	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	12	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	48	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 30$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 40$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	403	Watts
	Linear Derating Factor	3.23	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	12	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	30	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	1300	

**STATIC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	1200			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, I_D = 6A$ )			1.25	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = 1200V, V_{GS} = 0V$ )			250	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 960V, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			1000	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1mA$ )	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

### DYNAMIC CHARACTERISTICS

APT1201R2BFLL\_SFL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
$C_{iss}$	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		2540		pF
$C_{oss}$	Output Capacitance			365		
$C_{rss}$	Reverse Transfer Capacitance			70		
$Q_g$	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 600V$ $I_D = 12A @ 25^\circ C$		100		nC
$Q_{gs}$	Gate-Source Charge			14		
$Q_{gd}$	Gate-Drain ("Miller") Charge			65		
$t_{d(on)}$	Turn-on Delay Time	<b>RESISTIVE SWITCHING</b> $V_{GS} = 15V$ $V_{DD} = 600V$ $I_D = 12A @ 25^\circ C$ $R_G = 1.6\Omega$		8		ns
$t_r$	Rise Time			18		
$t_{d(off)}$	Turn-off Delay Time			29		
$t_f$	Fall Time			21		
$E_{on}$	Turn-on Switching Energy ⑥	<b>INDUCTIVE SWITCHING @ 25°C</b> $V_{DD} = 800V, V_{GS} = 15V$ $I_D = 12A, R_G = 5\Omega$		465		$\mu J$
$E_{off}$	Turn-off Switching Energy			100		
$E_{on}$	Turn-on Switching Energy ⑥	<b>INDUCTIVE SWITCHING @ 125°C</b> $V_{DD} = 800V, V_{GS} = 15V$ $I_D = 12A, R_G = 5\Omega$		935		
$E_{off}$	Turn-off Switching Energy			135		

### SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$I_S$	Continuous Source Current (Body Diode)			12	Amps
$I_{SM}$	Pulsed Source Current ① (Body Diode)			48	
$V_{SD}$	Diode Forward Voltage ② ( $V_{GS} = 0V, I_S = -12A$ )			1.3	Volts
$dv/dt$	Peak Diode Recovery $dv/dt$ ⑤			18	V/ns
$t_{rr}$	Reverse Recovery Time ( $I_S = -12A, di/dt = 100A/\mu s$ )	$T_j = 25^\circ C$		210	ns
		$T_j = 125^\circ C$		710	
$Q_{rr}$	Reverse Recovery Charge ( $I_S = -12A, di/dt = 100A/\mu s$ )	$T_j = 25^\circ C$		1.0	$\mu C$
		$T_j = 125^\circ C$		3.6	
$I_{RRM}$	Peak Recovery Current ( $I_S = -12A, di/dt = 100A/\mu s$ )	$T_j = 25^\circ C$		10	Amps
		$T_j = 125^\circ C$		14	

### THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.31	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380  $\mu s$ , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting  $T_j = +25^\circ C, L = 18.06mH, R_G = 25\Omega, \text{Peak } I_L = 12A$

⑤  $dv/dt$  numbers reflect the limitations of the test circuit rather than the device itself.  $I_S \leq I_D - 12A, di/dt \leq 700A/\mu s, v_R \leq 1200, T_j \leq 150^\circ C$

⑥  $E_{on}$  includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

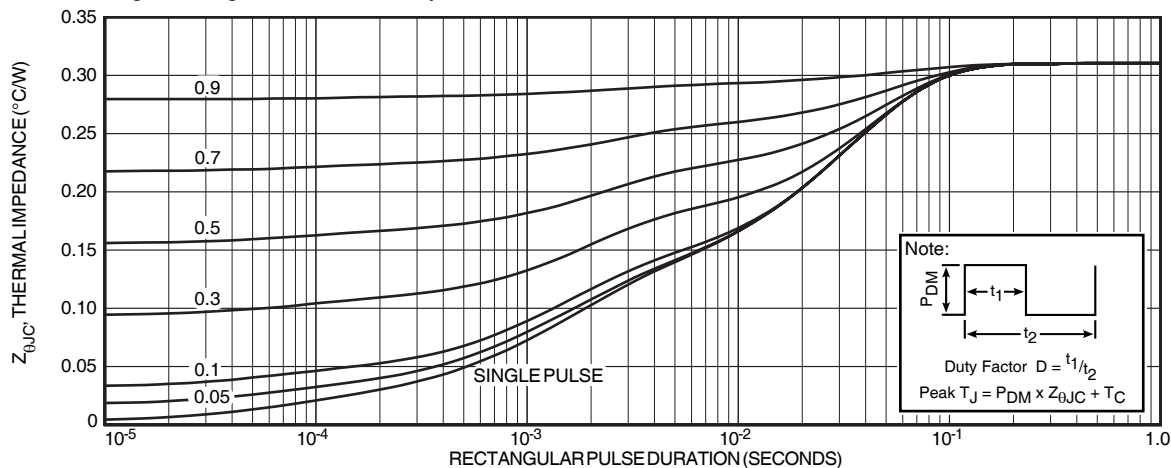


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

# Typical Performance Curves

APT1201R2BFLL\_SFL

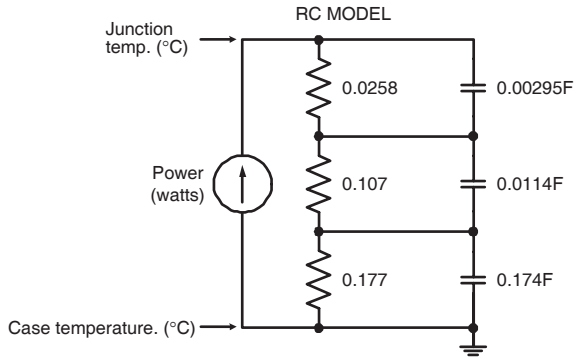


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

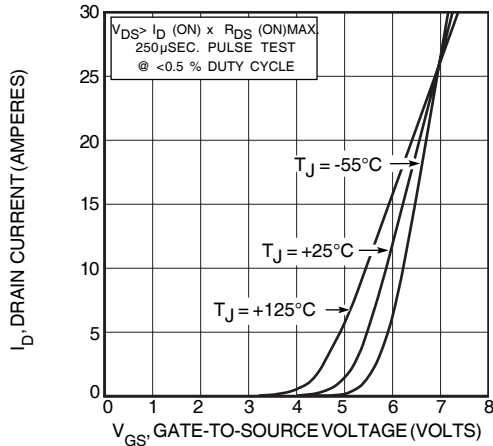


FIGURE 4, TRANSFER CHARACTERISTICS

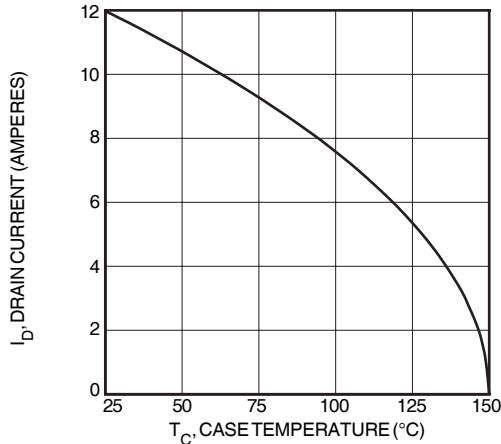


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

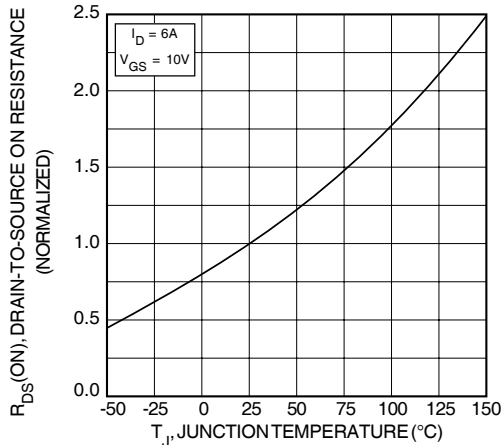


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

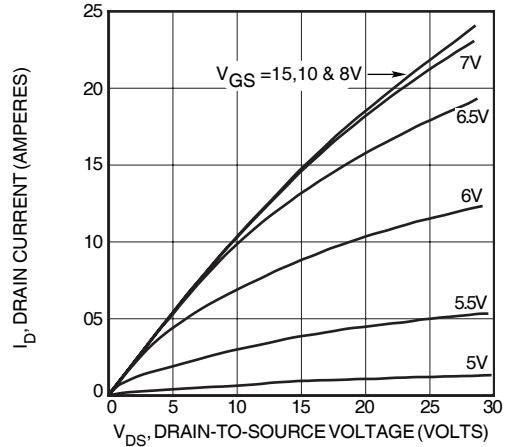


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

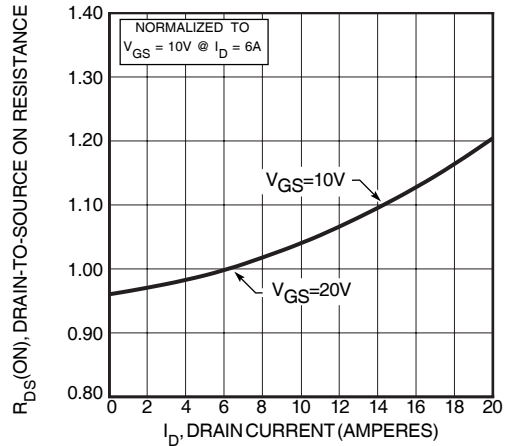


FIGURE 5,  $R_{DS(ON)}$  vs DRAIN CURRENT

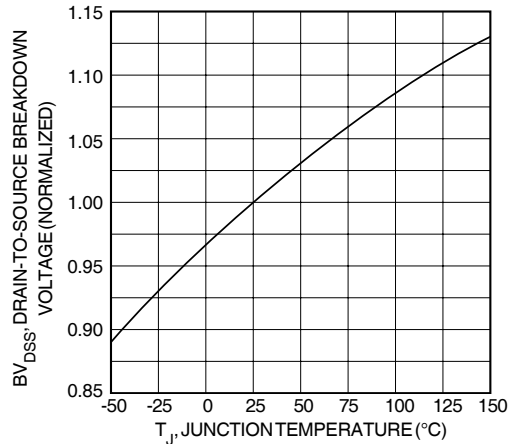


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

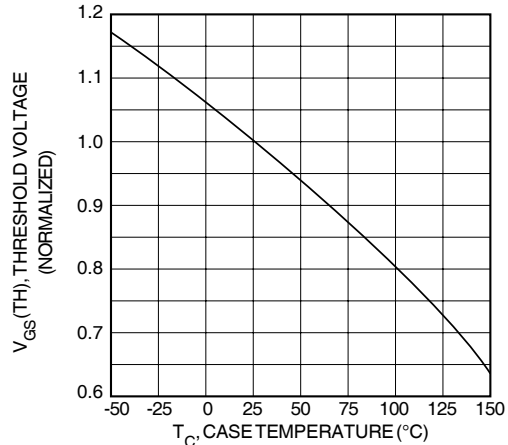


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

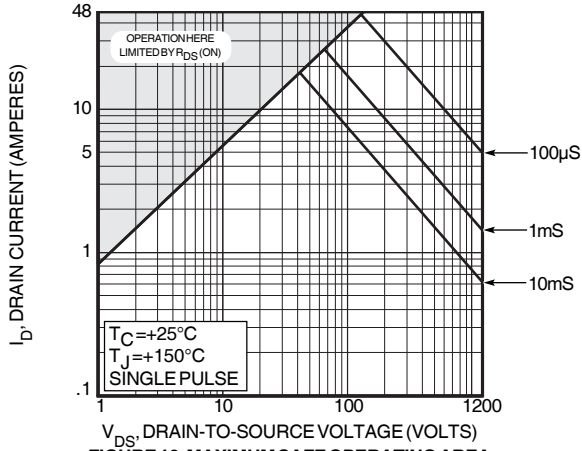


FIGURE 10, MAXIMUM SAFE OPERATING AREA

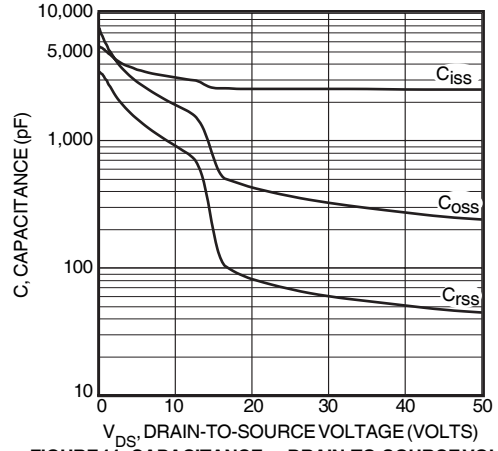


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

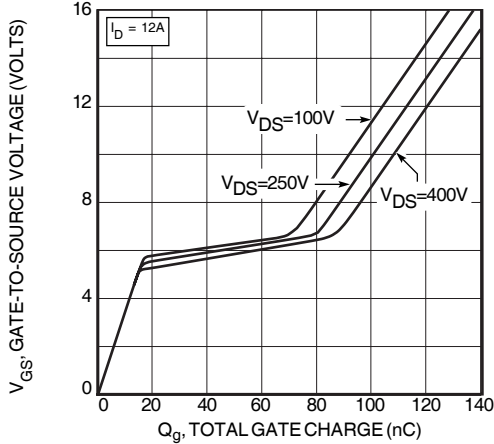


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

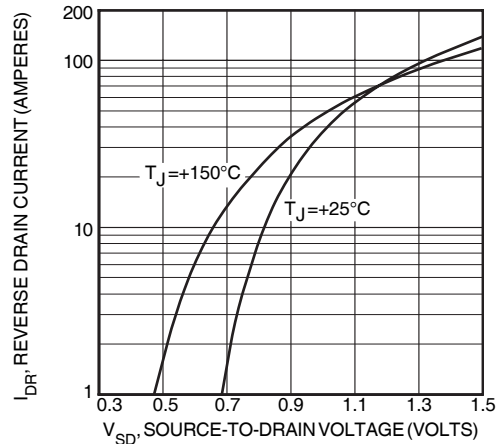


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

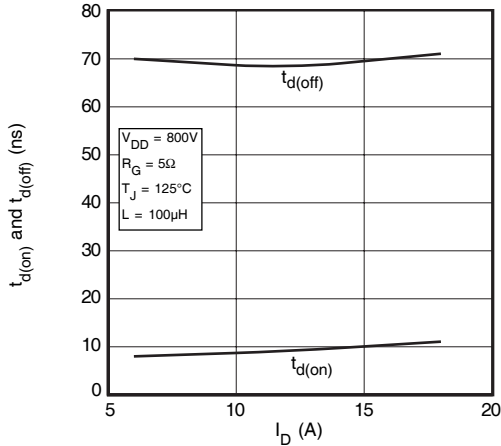


FIGURE 14, DELAY TIMES vs CURRENT

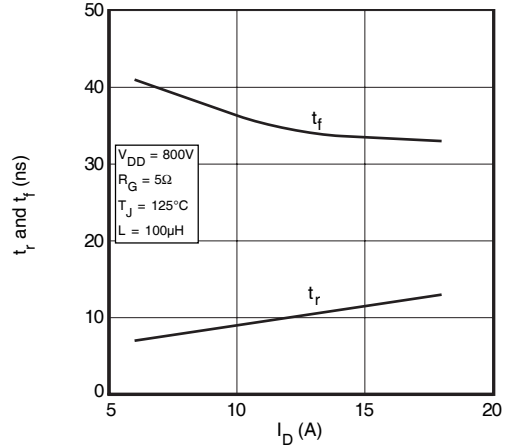


FIGURE 15, RISE AND FALL TIMES vs CURRENT

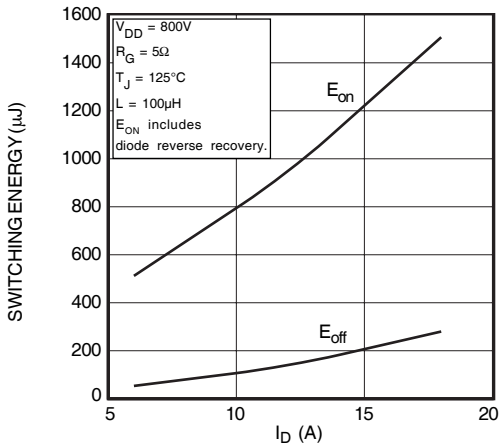


FIGURE 16, SWITCHING ENERGY vs CURRENT

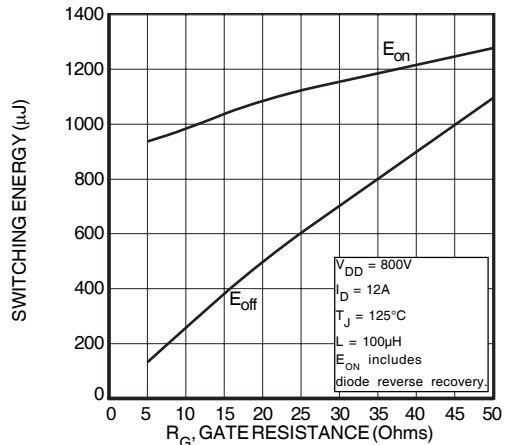


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

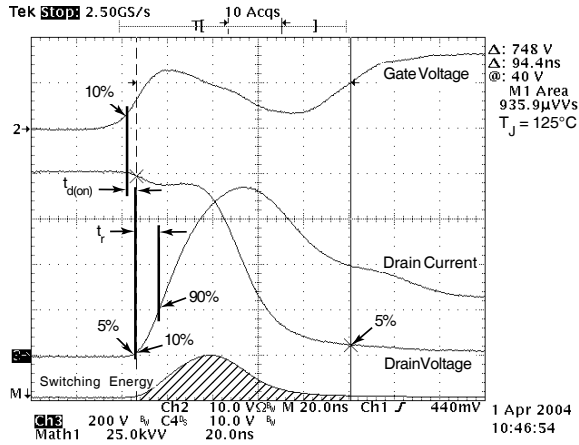


Figure 18, Turn-on Switching Waveforms and Definitions

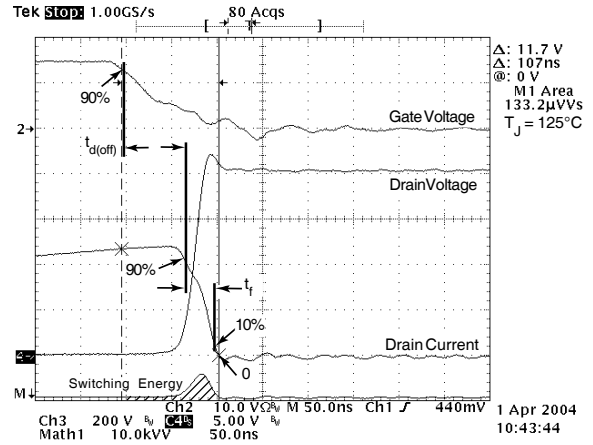


Figure 19, Turn-off Switching Waveforms and Definitions

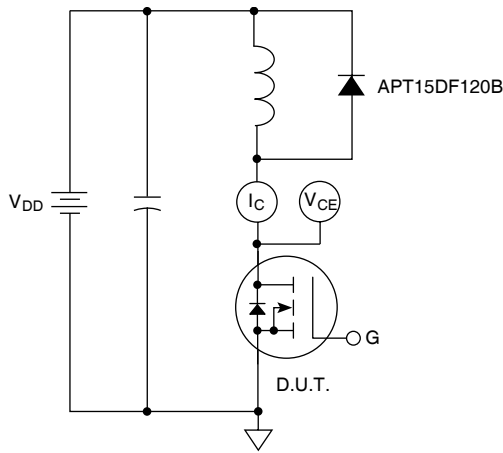
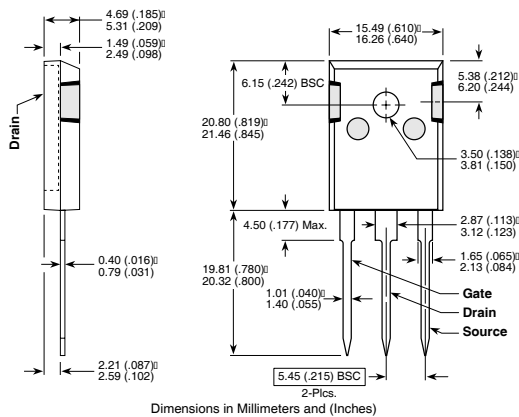
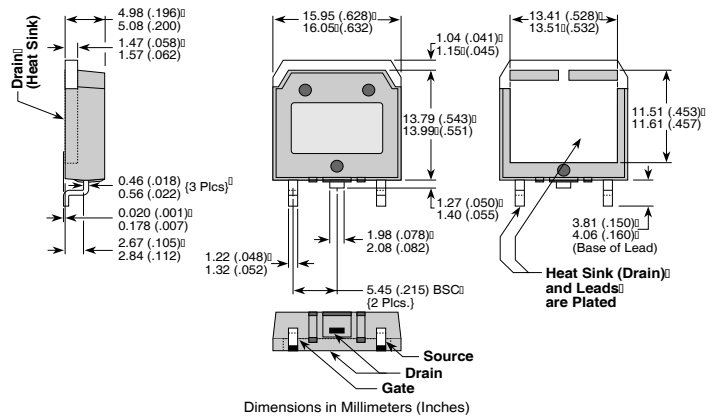


Figure 20, Inductive Switching Test Circuit

TO-247 Package Outline (BFL)



D<sup>3</sup>PAK Package Outline (SFL)



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