Logic Controlled, High-Side Power Switch

ADP190

FEATURES

Low RDS_{ON} of 105 mΩ @ 1.8 V
Low input voltage range: 1.2 V to 3.6 V
500 mA continuous operating current
Built-in level shift for control logic that can be operated by 1.2 V logic
Low 2 µA (maximum) ground current
Ultralow shutdown current: <1 µA
Ultrasmall 0.8 mm × 0.8 mm, 4-ball, 0.4 mm pitch WLCSP

APPLICATIONS

Mobile phones
Digital cameras and audio devices
Portable and battery-powered equipment

TYPICAL APPLICATIONS CIRCUIT

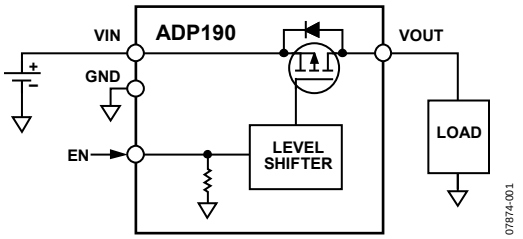

Figure 1.

GENERAL DESCRIPTION

The ADP190 is a high-side load switch designed for operation from 1.2 V to 3.6 V. This load switch provides power domain isolation for extended power battery life. The device contains a low on-resistance P-channel MOSFET that supports more than 500 mA of continuous current and minimizes power loss. The low 2 µA (maximum) of ground current and ultralow shutdown current make the ADP190 ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the ADP190 compatible with modern processors and GPIO controllers.

Beyond operating performance, the ADP190 occupies minimal printed circuit board (PCB) space with an area less than 0.64 mm^2 and a height of 0.60 mm. It is available in an ultrasmall 0.8 mm × 0.8 mm, 4-ball, 0.4 mm pitch WLCSP.

Rev. 0

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

$V_{EN} = V_{IN}$, I_{LOAD} = 200 mA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	1.2		3.6	V
EN INPUT						
EN Input Threshold	V_{EN_TH}	1.1 V ≤ V_{IN} ≤ 1.3 V, T_J = −40°C to +85°C	0.3		1.0	V
		1.3 V < V_{IN} < 1.8 V, T_J = −40°C to +85°C	0.4		1.2	V
		1.8 V ≤ V_{IN} ≤ 3.6 V, T_J = −40°C to +85°C	0.45		1.2	V
Logic High Voltage	V_{IH}	1.1 V ≤ V_{IN} ≤ 3.6 V	1.2			V
Logic Low Voltage	V_{IL}	1.1 V ≤ V_{IN} ≤ 3.6 V			0.3	V
EN Input Pull-Down Resistance	R_{EN}	V_{IN} = 1.8 V		4		MΩ
CURRENT						
Ground Current[1]	I_{GND}	V_{IN} = 3.6 V, VOUT open, T_J = −40°C to +85°C			2	µA
Shutdown Current	I_{OFF}	V_{IN} = 1.8 V, EN = GND		0.1		µA
		V_{IN} = 1.8 V, EN = GND, T_J = −40°C to +85°C			2	µA
VIN to VOUT RESISTANCE	RDS_{ON}					
		V_{IN} = 1.8 V ,V_{IN} = 3.6 V, I_{LOAD} = 200 mA, EN = 1.5 V		80		mΩ
		V_{IN} = 2.5 V, I_{LOAD} = 200 mA, EN = 1.5 V		90		mΩ
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, EN = 1.5 V		105	130	mΩ
		V_{IN} = 1.5 V, I_{LOAD} = 200 mA, EN = 1.5 V		125		mΩ
		V_{IN} = 1.2 V, I_{LOAD} = 200 mA, EN = 1 V		160		mΩ
VOUT TIME						
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 1.8 V, I_{LOAD} = 200 mA, EN = 1.5 V, C_{LOAD} = 1 µF		5		µs
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 3.6 V, I_{LOAD} = 200 mA, EN = 1.5 V, C_{LOAD} = 1 µF		1.5		µs

[1] Ground current includes EN pull-down current.

TIMING DIAGRAM

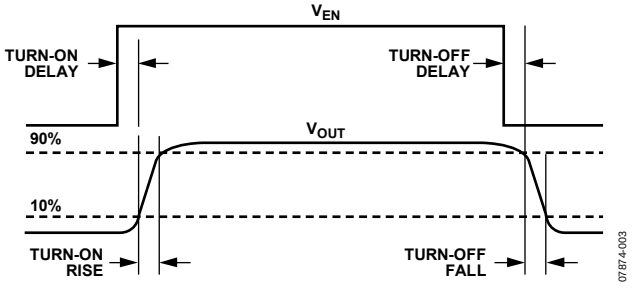

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND Pins	−0.3 V to +3.6 V
VOUT to GND Pins	−0.3 V to V_{IN}
EN to GND Pins	−0.3 V to +3.6 V
Continuous Drain Current	
T_A = 25°C	±1 A
T_A = 85°C	±500 mA
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP190 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch PCB. Refer to JESD51-7 and JESD51-9 for detailed information regarding board construction. For additional information, see the AN-617 application note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12 document, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path, as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8, JESD51-9, and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
4-Ball, 0.4 mm Pitch WLCSP	260	58.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

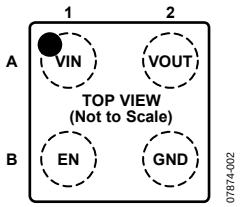

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Input Voltage.
B1	EN	Enable Input. Drive EN high to turn on the switch; drive EN low to turn off the switch.
A2	VOUT	Output Voltage.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, EN = V_{IN} > V_{IH}, I_{LOAD} = 100 mA, T_A = 25°C, unless otherwise noted.

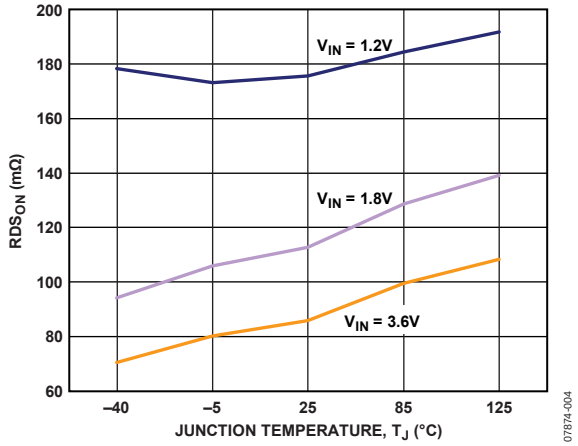

Figure 4. RDS_{ON} vs. Temperature (Includes ~15 mΩ Trace Resistance)

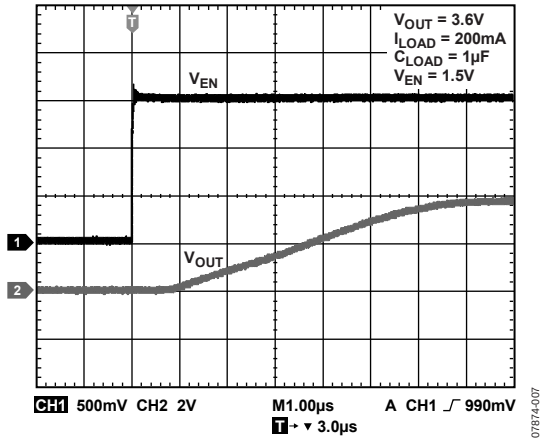

Figure 7. Turn-On Delay vs. Input Voltage = 3.6 V

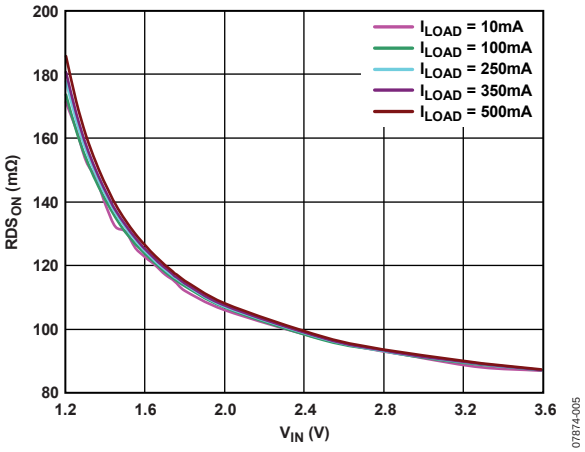

Figure 5. RDS_{ON} vs. Input Voltage, V_{IN} (Includes ~15 mΩ Trace Resistance)

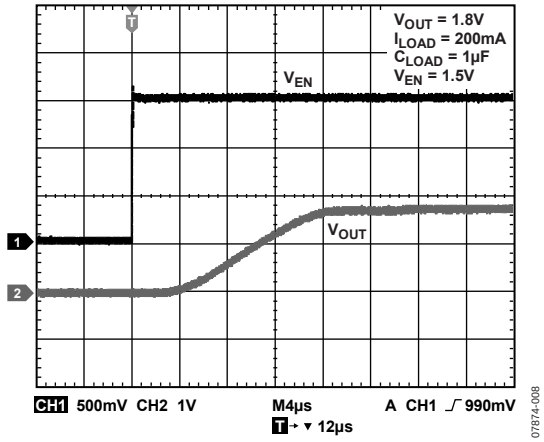

Figure 8. Turn-On Delay vs. Input Voltage = 1.8 V

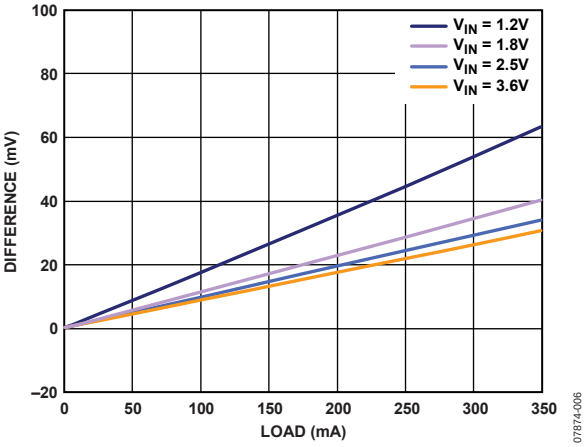

Figure 6. Voltage Drop vs. Load Current (Includes ~15 mΩ Trace Resistance)

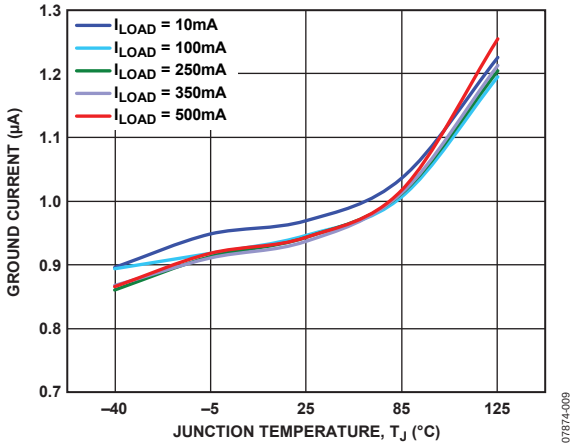

Figure 9. Ground Current vs. Temperature

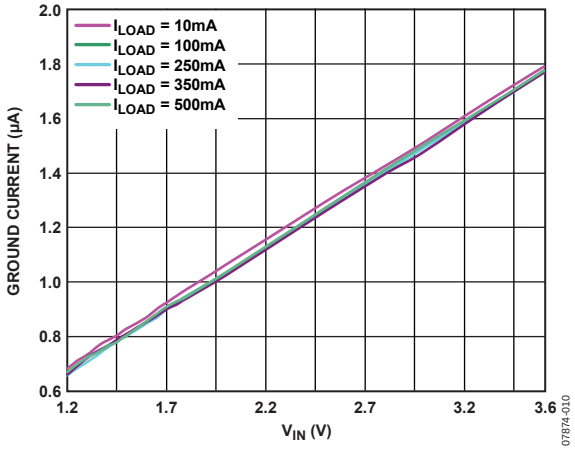

Figure 10. Ground Current vs. Input Voltage, V_{IN}

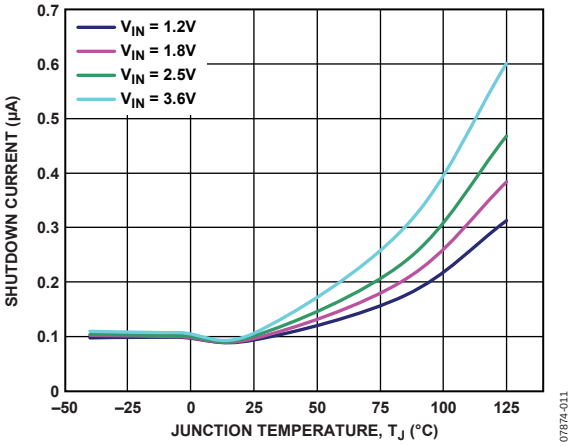

Figure 11. Shutdown Current vs. Temperature

THEORY OF OPERATION

The ADP190 is a high-side PMOS load switch. It is designed for supply operation from 1.2 V to 3.6 V. The PMOS load switch is designed for low on resistance, 105 mΩ at V_{IN} = 1.8 V, and supports 500 mA of continuous current. It is a low ground current device with a nominal 4 MΩ pull-down resistor on its enable pin. The package is a space-saving 0.8 mm × 0.8 mm, 4-ball WLCSP.

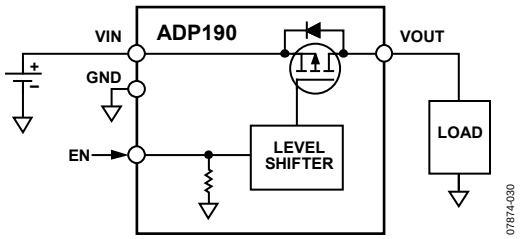

Figure 12. Functional Block Diagram

APPLICATIONS INFORMATION

GROUND CURRENT

The major source for ground current in the ADP190 is the 4 MΩ pull-down on the enable (EN) pin. Figure 13 shows typical ground current when $V_{EN} = V_{IN}$ and V_{IN} varies from 1.2 V to 3.6 V.

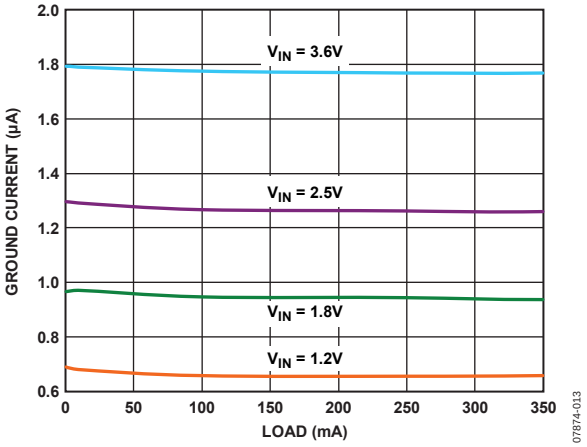

Figure 13. Ground Current vs. Load Current

As shown in Figure 14, an increase in ground current can occur when $V_{EN} \neq V_{IN}$. This is caused by the CMOS logic nature of the level shift circuitry as it translates an EN signal ≥ 1.2 V to a logic high. This increase is a function of the $V_{IN} - V_{EN}$ delta.

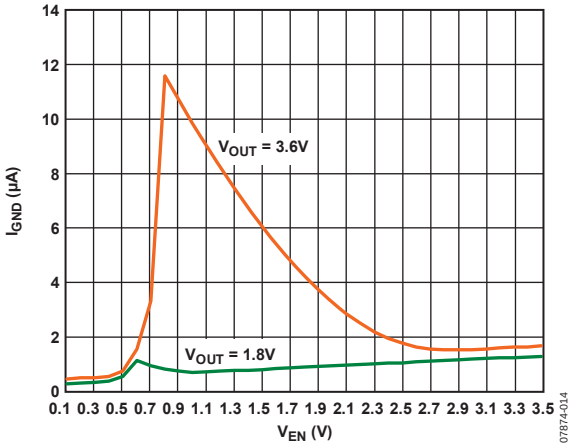

Figure 14. Typical Ground Current when $V_{EN} \neq V_{IN}$

ENABLE FEATURE

The ADP190 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 15, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

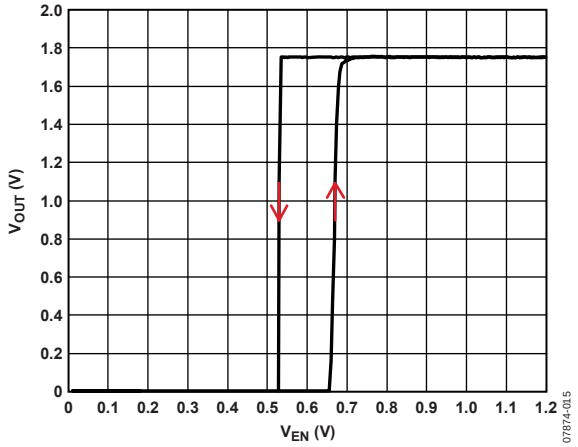

Figure 15. Typical EN Operation

As shown in Figure 15, the EN pin has built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds derive from the VIN voltage; therefore, these thresholds vary with changing input voltage. Figure 16 shows typical EN active/inactive thresholds when the input voltage varies from 1.2 V to 3.6 V.

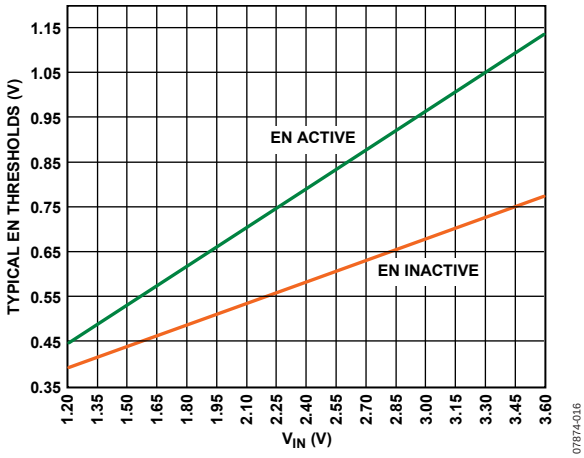

Figure 16. Typical EN Pin Thresholds vs. Input Voltage, V_{IN}

TIMING

Turn-on delay is defined as the delta between the time that EN reaches >1.2 V until VOUT rises to ~10% of its final value. The ADP190 includes circuitry to set the typical 1.5 µs turn-on delay at 3.6 V V_{IN} to limit the V_{IN} inrush current. As shown in Figure 17, the turn-on delay is dependent on the input voltage.

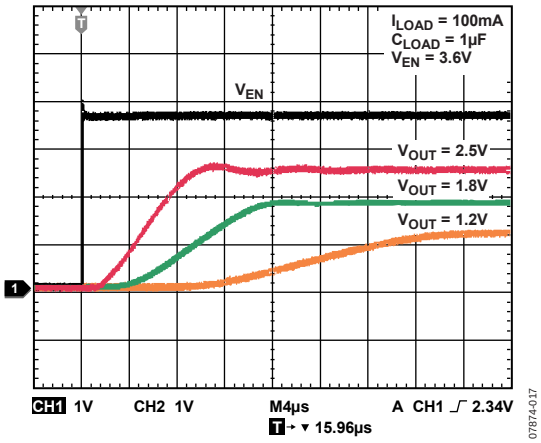

Figure 17. Typical Turn-On Delay Time with Varying Input Voltage

The rise time is defined as the delta between the time from 10% to 90% of VOUT reaching its final value. It is dependent on the RC time constant where C = load capacitance (C_{LOAD}) and R = $RDS_{ON}||R_{LOAD}$. Because RDS_{ON} is usually smaller than R_{LOAD}, an adequate approximation for RC is $RDS_{ON} \times C_{LOAD}$. The ADP190 does not need any input or load capacitor, but capacitors can be used to suppress the noise issues on the board. If significant load capacitance is connected, inrush current is a concern.

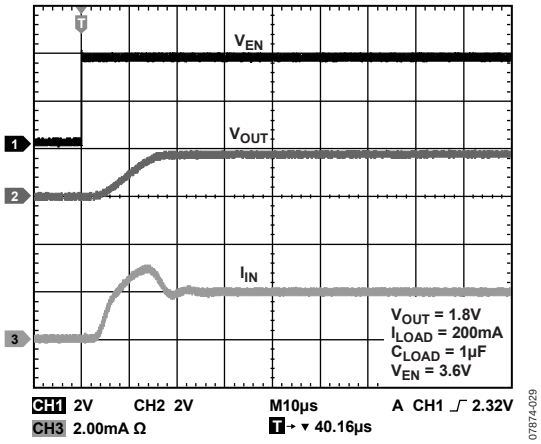

Figure 18. Typical Rise Time and Inrush Current with C_{LOAD} = 1 µF

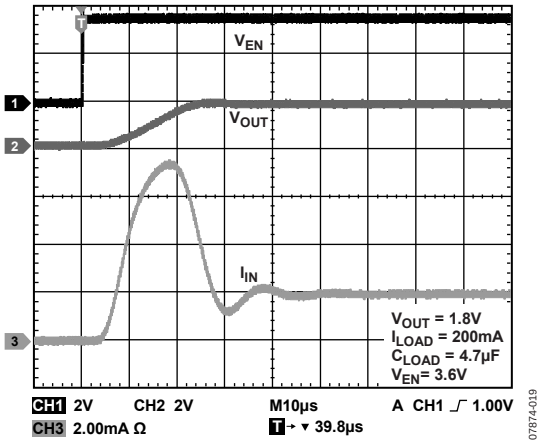

Figure 19. Typical Rise Time and Inrush Current with C_{LOAD} = 4.7 µF

The turn-off time is defined as the delta between the time from 90% to 10% of VOUT reaching its final value. It is also dependent on the RC time constant.

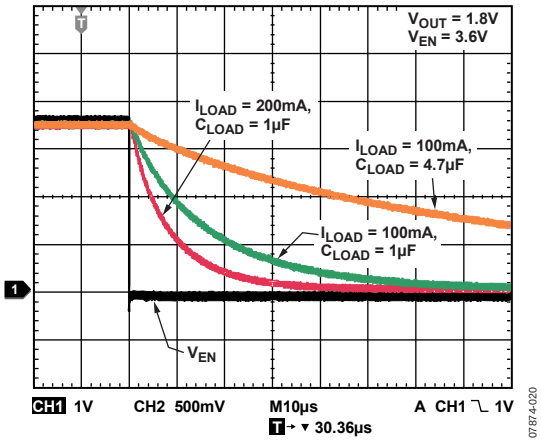

Figure 20. Typical Turn-Off Time

THERMAL CONSIDERATIONS

In most applications, the ADP190 does not dissipate much heat due to its low on-channel resistance. However, in applications with high ambient temperature and load current, the heat dissipated in the package can be large enough to cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 1.

To guarantee reliable operation, the junction temperature of the ADP190 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pin to the PCB. Table 5 shows typical θ_{JA} values of the 4-ball WLCSP for various PCB copper sizes. Table 6 shows the typical Ψ_{JB} value of the 4-ball WLCSP.

Table 5. Typical θ_{JA} Values for WLCSP

Copper Size (mm^2)	θ_{JA} (°C/W)
0[1]	260
50	159
100	157
300	153
500	151

[1] Device soldered to minimum size pin traces.

Table 6. Typical Ψ_{JB} Values

Package	Ψ_{JB}	Unit
4-Ball WLCSP	58.4	°C/W

The junction temperature of the ADP190 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (2)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are the input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (3)$$

As shown in Equation 3, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 21 to Figure 26 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

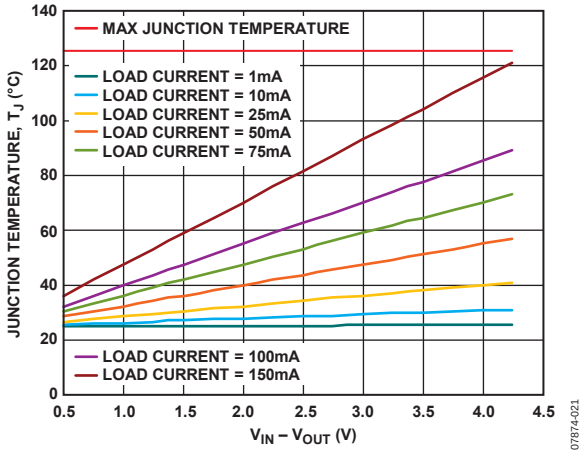

Figure 21. WLCSP, 500 mm² of PCB Copper, T_A = 25°C

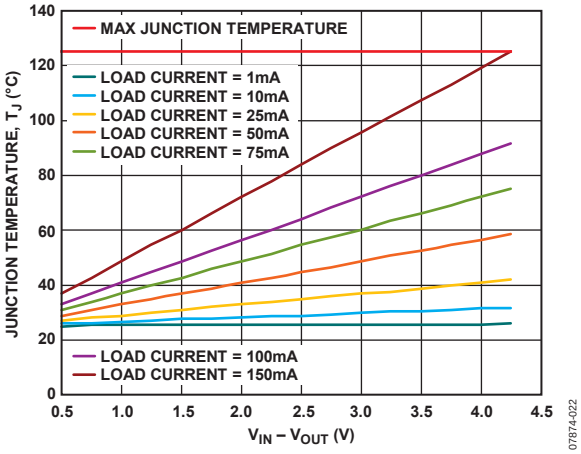

Figure 22. WLCSP, 100 mm² of PCB Copper, T_A = 25°C

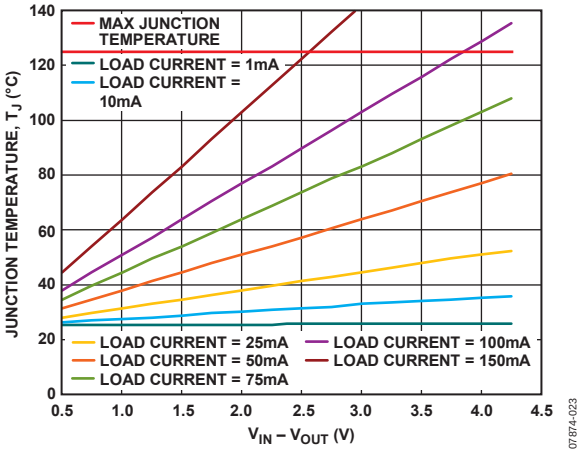

Figure 23. WLCSP, 0 mm² of PCB Copper, T_A = 25°C

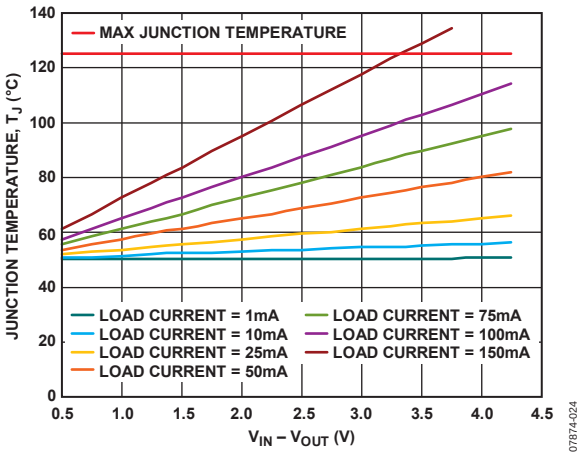

Figure 24. WLCSP, 500 mm² of PCB Copper, T_A = 50°C

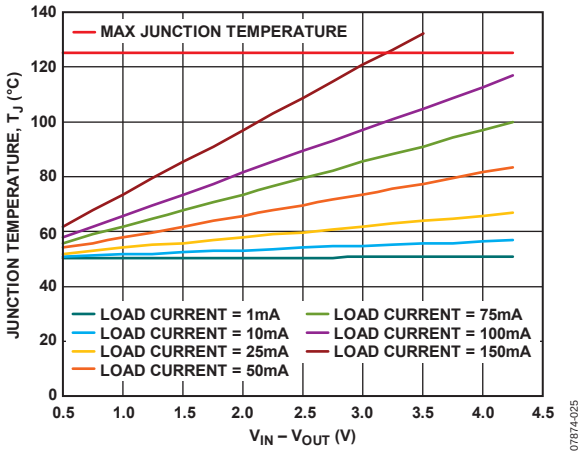

Figure 25. WLCSP, 100 mm² of PCB Copper, T_A = 50°C

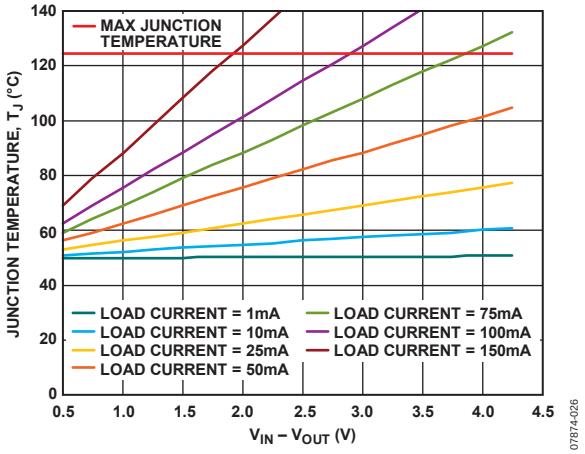

Figure 26. WLCSP, 0 mm² of PCB Copper, T_A = 50°C

In cases where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (4)$$

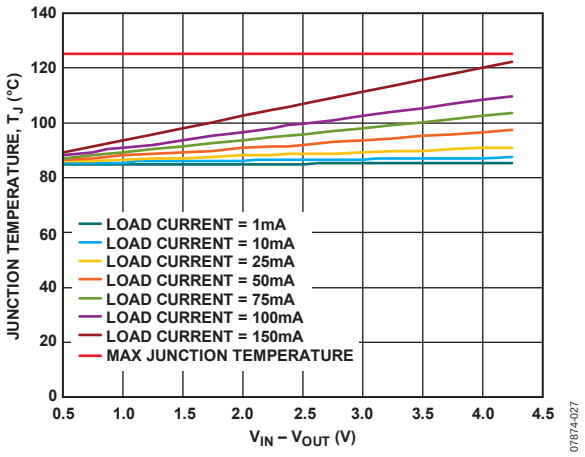

Figure 27. WLCSP, T_B = 85°C

PCB LAYOUT CONSIDERATIONS

Improve heat dissipation from the package by increasing the amount of copper attached to the pins of the ADP190. However, as listed in Table 5, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

It is critical to keep the input and output traces as wide and as short as possible to minimize the circuit board trace resistance.

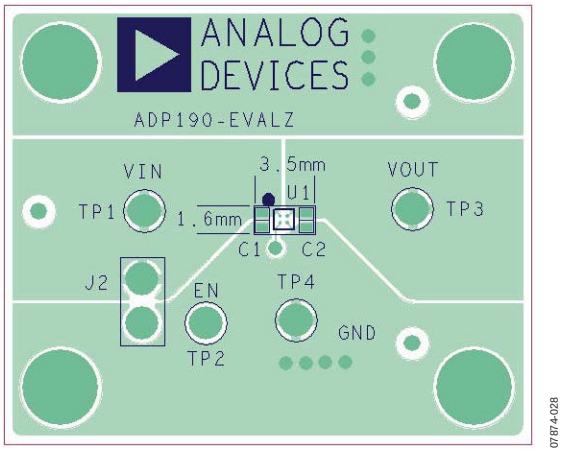

Figure 28. WLCSP PCB Layout

OUTLINE DIMENSIONS

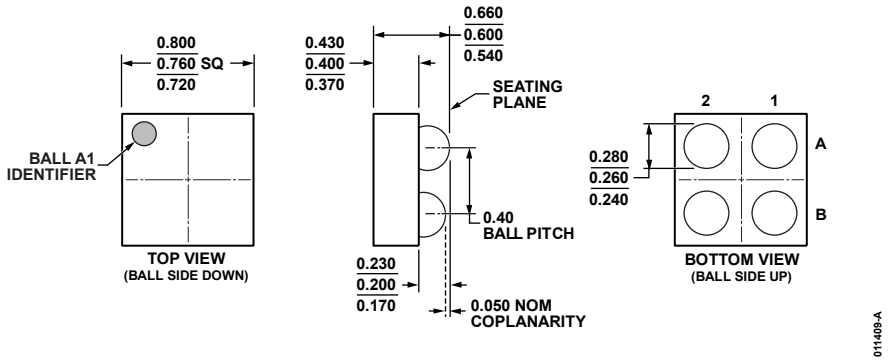

Figure 29. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADP190ACBZ-R7[1]	−40°C to +85°C	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	L9C
ADP190CB-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

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