

V850E/MS1 32-BIT SINGLE-CHIP MICROCONTROLLERS

The μ PD703101-33 and μ PD703102-33 are members of the V850 Series of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU core, ROM, RAM, interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The μ PD703100-33 and μ PD703100-40 are ROMless versions of the μ PD703101-33 and μ PD703102-33 products.

The μ PD703100A-33, μ PD703100A-40, μ PD703101A-33, and μ PD703102A-33 are also available as products having a 3.3 V power supply for external pins.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MS1 User's Manual Hardware: U12688E

V850E/MS1, V850E/MS2 User's Manual Architecture: U12197E

FEATURES

- Number of instructions: 81
- Minimum instruction execution time 25 ns (@ 40 MHz operation) μ PD703100-40
30 ns (@ 33 MHz operation) μ PD703100-33, 703101-33, 703102-33
- General-purpose registers 32 bits $\times$ 32
- Instruction set optimized for control applications
- Internal memory ROM: None (μ PD703100-33, 703100-40),
96 KB (μ PD703101-33),
128 KB (μ PD703102-33)
RAM : 4 KB
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power saving functions

APPLICATIONS

- Office automation equipment: printers, facsimile machines, PPCs, etc.
- Multimedia equipment: digital still cameras, video printers, etc.
- Consumer equipment: single-lens reflex cameras, etc.
- Industrial equipment: motor controllers, NC machine tools, etc.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

★ ORDERING INFORMATION

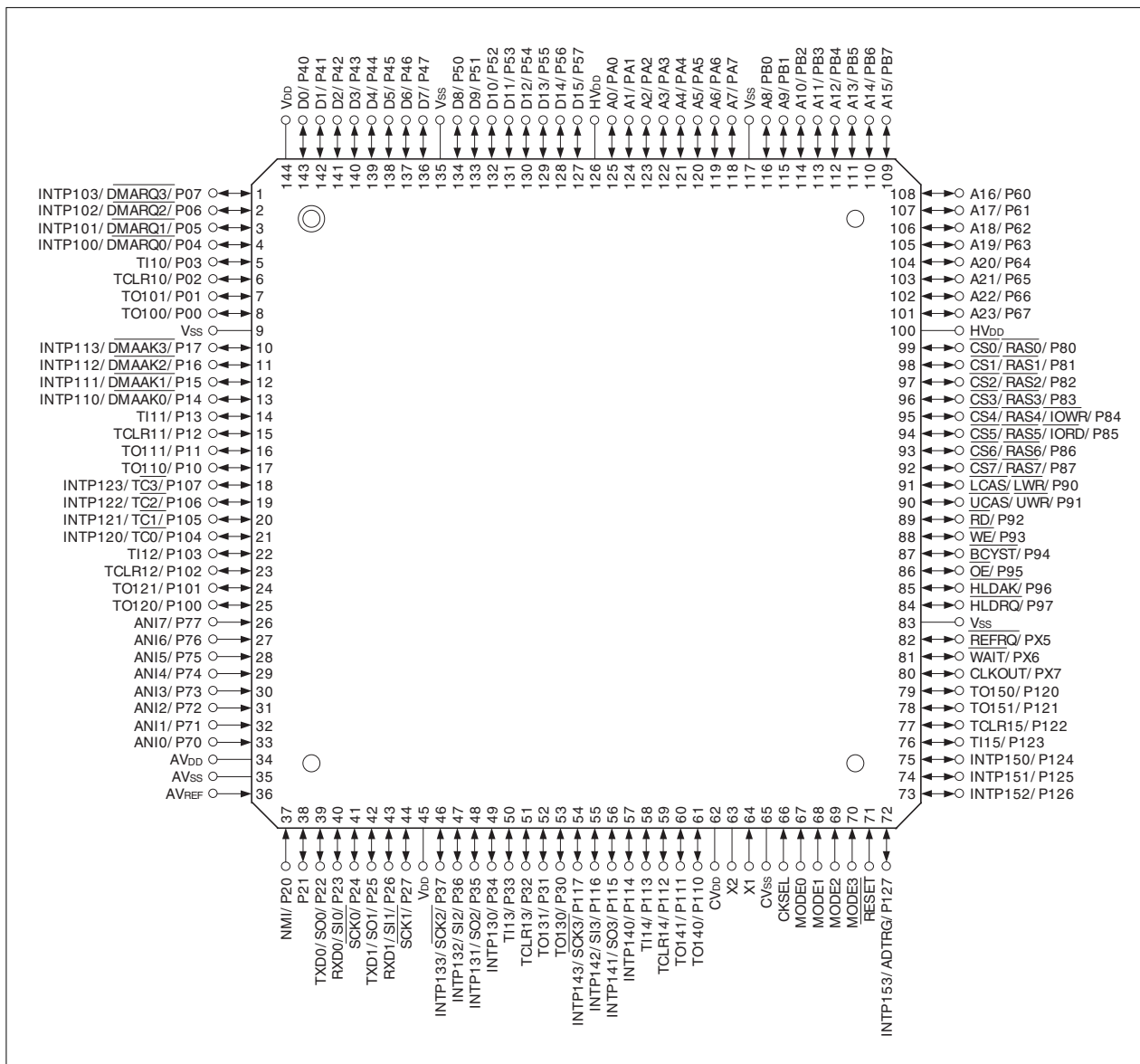
Part Number	Package	Maximum Operating Frequency	Internal ROM
μ PD703100GJ-33-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	None
μ PD703100GJ-33-UEN-A	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	None
μ PD703100GJ-40-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	40 MHz	None
μ PD703100GJ-40-UEN-A	144-pin plastic LQFP (fine pitch) (20 × 20)	40 MHz	None
μ PD703101GJ-33-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	96 KB
μ PD703101GJ-33-xxx-UEN-A	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	96 KB
μ PD703102GJ-33-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	128 KB
μ PD703102GJ-33-xxx-UEN-A	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	128 KB

- Remarks**
1. xxx indicates ROM code suffix.
 2. Products with -A at the end of the part number are lead-free products.

PIN CONFIGURATION (TOP VIEW)

144-pin plastic LQFP (fine pitch) (20 × 20)

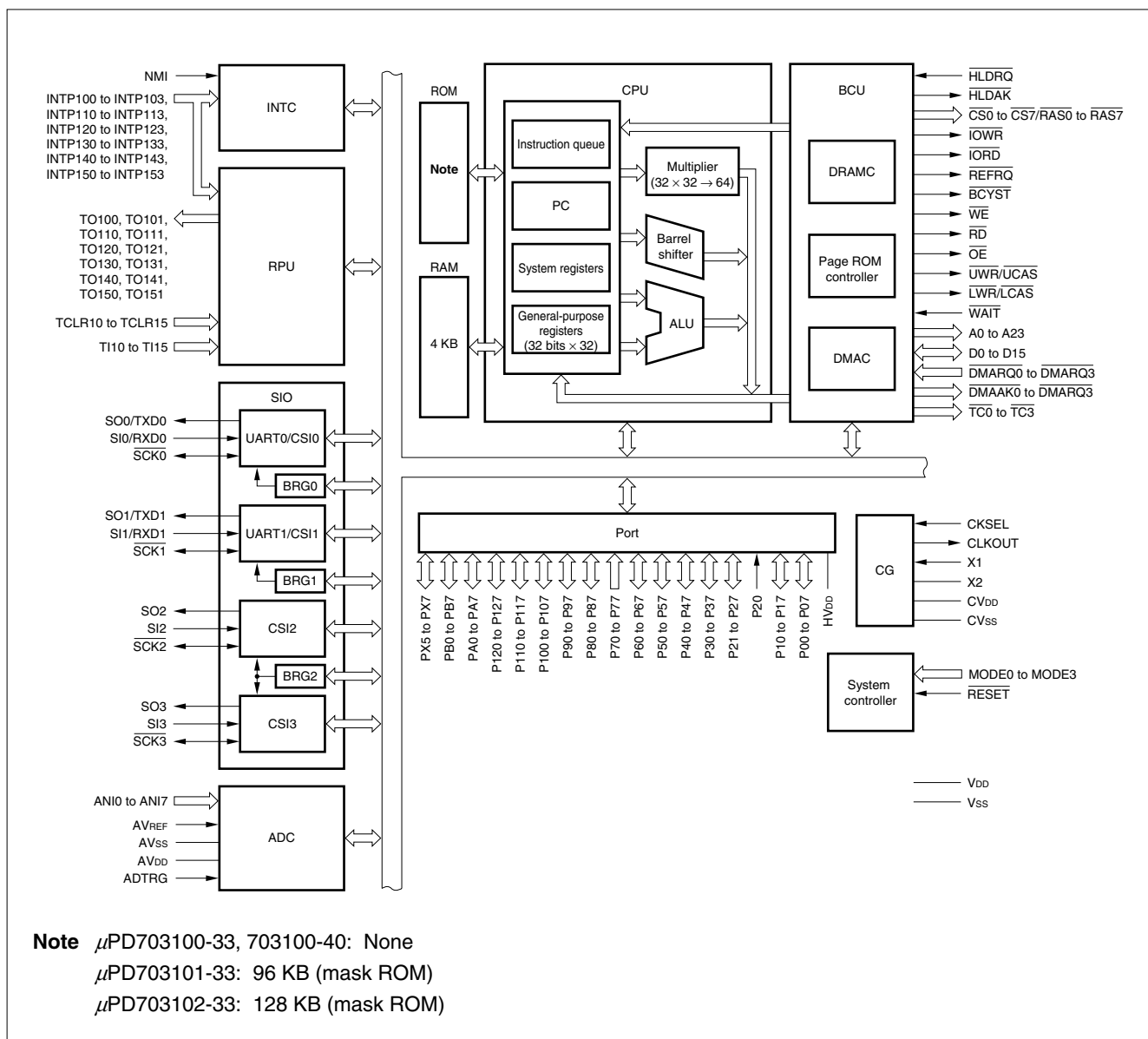
- μPD703100GJ-33-UEN
- μPD703100GJ-33-UEN-A
- μPD703100GJ-40-UEN
- μPD703100GJ-40-UEN-A
- μPD703101GJ-33-xxx-UEN
- μPD703101GJ-33-xxx-UEN-A
- μPD703102GJ-33-xxx-UEN
- μPD703102GJ-33-xxx-UEN-A



PIN NAMES

A0 to A23:	Address Bus	P50 to P57:	Port 5
ADTRG:	AD Trigger Input	P60 to P67:	Port 6
ANI0 to ANI7:	Analog Input	P70 to P77:	Port 7
AV _{DD} :	Analog Power Supply	P80 to P87:	Port 8
AV _{REF} :	Analog Reference Voltage	P90 to P97:	Port 9
AV _{SS} :	Analog Ground	P100 to P107:	Port 10
$\overline{\text{BCYST}}$:	Bus Cycle Start Timing	P110 to P117:	Port 11
CKSEL:	Clock Generator Operating Mode Select	P120 to P127:	Port 12
CLKOUT:	Clock Output	PA0 to PA7:	Port A
$\overline{\text{CS0}}$ to $\overline{\text{CS7}}$:	Chip Select	PB0 to PB7:	Port B
CV _{DD} :	Clock Generator Power Supply	PX5 to PX7:	Port X
CV _{SS} :	Clock Generator Ground	$\overline{\text{RAS0}}$ to $\overline{\text{RAS7}}$:	Row Address Strobe
D0 to D15:	Data Bus	$\overline{\text{RD}}$:	Read
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$:	DMA Acknowledge	$\overline{\text{REFRQ}}$:	Refresh Request
$\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$:	DMA Request	$\overline{\text{RESET}}$:	Reset
$\overline{\text{HLDK}}$:	Hold Acknowledge	RXD0, RXD1:	Receive Data
$\overline{\text{HLDRQ}}$:	Hold Request	$\overline{\text{SCK0}}$ to $\overline{\text{SCK3}}$:	Serial Clock
HV _{DD} :	Power Supply for External Pins	SI0 to SI3:	Serial Input
INTP100 to INTP103, :	Interrupt Request from Peripherals	SO0 to SO3:	Serial Output
INTP110 to INTP113,		$\overline{\text{TC0}}$ to $\overline{\text{TC3}}$:	Terminal Count Signal
INTP120 to INTP123,		TCLR10 to TCLR15:	Timer Clear
INTP130 to INTP133,		TI10 to TI15:	Timer Input
INTP140 to INTP143,		TO100, TO101, :	Timer Output
INTP150 to INTP153		TO110, TO111,	
$\overline{\text{IORD}}$:	I/O Read Strobe	TO120, TO121,	
$\overline{\text{IOWR}}$:	I/O Write Strobe	TO130, TO131,	
$\overline{\text{LCAS}}$:	Lower Column Address Strobe	TO140, TO141,	
$\overline{\text{LWR}}$:	Lower Write Strobe	TO150, TO151	
MODE0 to MODE3:	Mode	TXD0, TXD1:	Transmit Data
NMI:	Non-Maskable Interrupt Request	$\overline{\text{UCAS}}$:	Upper Column Address Strobe
$\overline{\text{OE}}$:	Output Enable	$\overline{\text{UWR}}$:	Upper Write Strobe
P00 to P07:	Port 0	V _{DD} :	Power Supply for Internal Unit
P10 to P17:	Port 1	V _{SS} :	Ground
P20 to P27:	Port 2	$\overline{\text{WAIT}}$:	Wait
P30 to P37:	Port 3	$\overline{\text{WE}}$:	Write Enable
P40 to P47:	Port 4	X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



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1. DIFFERENCES AMONG PRODUCTS

Product Name Item	μPD703100				μPD703101		μPD703102		μPD70F3102	
	-33	-40	A-33	A-40	-33	A-33	-33	A-33	-33	A-33
Internal ROM	None				96 KB (mask ROM)		128 KB (mask ROM)		128 KB (flash memory)	
Maximum operating frequency	33 MHz	40 MHz	33 MHz	40 MHz	33 MHz					
HV _{DD}	4.5 to 5.5 V		3.0 to 3.6 V		4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V
Operation mode										
Single-chip mode 0, 1	None				Provided					
Flash memory programming mode	None								Provided	
Flash memory programming pin	None								Provided (V _{PP})	
Electrical specifications	Power consumptions differ (refer to the data sheet of each product).									
Package	144LQFP		144LQFP 157FBGA		144LQFP					144LQFP 157FBGA
Others	Noise tolerance and noise radiation will differ due to the differences in circuit scale and mask layout.									

Remark 144LQFP: 144-pin plastic LQFP (fine pitch) (20 × 20)

157FBGA: 157-pin plastic FBGA (14 × 14)

2. PIN FUNCTIONS

2.1 Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units	TO100
P01			TO101
P02			TCLR10
P03			TI10
P04			INTP100/ $\overline{\text{DMARQ0}}$
P05			INTP101/ $\overline{\text{DMARQ1}}$
P06			INTP102/ $\overline{\text{DMARQ2}}$
P07			INTP103/ $\overline{\text{DMARQ3}}$
P10	I/O	Port 1 8-bit I/O port Input/output can be specified in 1-bit units	TO110
P11			TO111
P12			TCLR11
P13			TI11
P14			INTP110/ $\overline{\text{DMAAK0}}$
P15			INTP111/ $\overline{\text{DMAAK1}}$
P16			INTP112/ $\overline{\text{DMAAK2}}$
P17			INTP113/ $\overline{\text{DMAAK3}}$
P20	Input	Port 2	NMI
P21	I/O	P20 is an input only port. When a valid edge is input, this pin operates as NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P21 to P27 are 7-bit I/O port. Input/output can be specified in 1-bit units	—
P22			TXD0/SO0
P23			RXD0/SI0
P24			$\overline{\text{SCK0}}$
P25			TXD1/SO1
P26			RXD1/SI1
P27			$\overline{\text{SCK1}}$
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO2
P36			INTP132/SI2
P37			INTP133/ $\overline{\text{SCK2}}$
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units	D0 to D7

(2/3)

Pin Name	I/O	Function	Alternate Function
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units	A16 to A23
P70 to P77	Input	Port 7 8-bit input only port	ANI0 to ANI7
P80	I/O	Port 8 8-bit I/O port Input/output can be specified in 1-bit units	$\overline{CS0}/\overline{RAS0}$
P81			$\overline{CS1}/\overline{RAS1}$
P82			$\overline{CS2}/\overline{RAS2}$
P83			$\overline{CS3}/\overline{RAS3}$
P84			$\overline{CS4}/\overline{RAS4}/\overline{IOWR}$
P85			$\overline{CS5}/\overline{RAS5}/\overline{IORD}$
P86			$\overline{CS6}/\overline{RAS6}$
P87			$\overline{CS7}/\overline{RAS7}$
P90	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units	$\overline{LCAS}/\overline{LWR}$
P91			$\overline{UCAS}/\overline{UWR}$
P92			$\overline{RD}$
P93			$\overline{WE}$
P94			$\overline{BCYST}$
P95			$\overline{OE}$
P96			$\overline{HLDK}$
P97			$\overline{HLDRQ}$
P100	I/O	Port 10 8-bit I/O port Input/output can be specified in 1-bit units	TO120
P101			TO121
P102			TCLR12
P103			TI12
P104			$\overline{INTP120}/\overline{TC0}$
P105			$\overline{INTP121}/\overline{TC1}$
P106			$\overline{INTP122}/\overline{TC2}$
P107			$\overline{INTP123}/\overline{TC3}$
P110	I/O	Port 11 8-bit I/O port Input/output can be specified in 1-bit units	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			$\overline{INTP140}$
P115			$\overline{INTP141}/\overline{SO3}$
P116			$\overline{INTP142}/\overline{SI3}$
P117			$\overline{INTP143}/\overline{SCK3}$

(3/3)

Pin Name	I/O	Function	Alternate Function
P120	I/O	Port 12 8-bit I/O port Input/output can be specified in 1-bit units	TO150
P121			TO151
P122			TCLR15
P123			TI15
P124			INTP150
P125			INTP151
P126			INTP152
P127			INTP153/ADTRG
PA0	I/O	Port A 8-bit I/O port Input/output can be specified in 1-bit units	A0
PA1			A1
PA2			A2
PA3			A3
PA4			A4
PA5			A5
PA6			A6
PA7			A7
PB0	I/O	Port B 8-bit I/O port Input/output can be specified in 1-bit units	A8
PB1			A9
PB2			A10
PB3			A11
PB4			A12
PB5			A13
PB6			A14
PB7			A15
PX5	I/O	Port X 3-bit I/O port Input/output can be specified in 1-bit units	$\overline{\text{REFRQ}}$
PX6			$\overline{\text{WAIT}}$
PX7			CLKOUT

2.2 Non-Port Pins

(1/4)

Pin Name	I/O	Function	Alternate Function
TO100	Output	Pulse signal output for timers 10 to 15	P00
TO101			P01
TO110			P10
TO111			P11
TO120			P100
TO121			P101
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TO150			P120
TO151			P121
TCLR10	Input	External clear signal input for timers 10 to 15	P02
TCLR11			P12
TCLR12			P102
TCLR13			P32
TCLR14			P112
TCLR15			P122
TI10	Input	External count clock input for timers 10 to 15	P03
TI11			P13
TI12			P103
TI13			P33
TI14			P113
TI15			P123
INTP100	Input	External maskable interrupt request input, shared as external capture trigger input for timer 10	P04/D $\overline{\text{MARQ0}}$
INTP101			P05/D $\overline{\text{MARQ1}}$
INTP102			P06/D $\overline{\text{MARQ2}}$
INTP103			P07/D $\overline{\text{MARQ3}}$
INTP110	Input	External maskable interrupt request input, shared as external capture trigger input for timer 11	P14/D $\overline{\text{MAAK0}}$
INTP111			P15/D $\overline{\text{MAAK1}}$
INTP112			P16/D $\overline{\text{MAAK2}}$
INTP113			P17/D $\overline{\text{MAAK3}}$
INTP120	Input	External maskable interrupt request input, shared as external capture trigger input for timer 12	P104/T $\overline{\text{C0}}$
INTP121			P105/T $\overline{\text{C1}}$
INTP122			P106/T $\overline{\text{C2}}$
INTP123			P107/T $\overline{\text{C3}}$

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Pin Name	I/O	Function	Alternate Function
INTP130	Input	External maskable interrupt request input, shared as external capture trigger input for timer 13	P34
INTP131			P35/SO2
INTP132			P36/SI2
INTP133			P37/SCK2
INTP140	Input	External maskable interrupt request input, shared as external capture trigger input for timer 14	P114
INTP141			P115/SO3
INTP142			P116/SI3
INTP143			P117/SCK3
INTP150	Input	External maskable interrupt request input, shared as external capture trigger input for timer 15	P124
INTP151			P125
INTP152			P126
INTP153			P127/ADTRG
SO0	Output	Serial transmit data output (3-wire) for CSI0 to CSI3	P22/TXD0
SO1			P25/TXD1
SO2			P35/INTP131
SO3			P115/INTP141
SI0	Input	Serial receive data input (3-wire) for CSI0 to CSI3	P23/RXD0
SI1			P26/RXD1
SI2			P36/INTP132
SI3			P116/INTP142
SCK0	I/O	Serial clock I/O (3-wire) for CSI0 to CSI3	P24
SCK1			P27
SCK2			P37/INTP133
SCK3			P117/INTP143
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	P40 to P47
D8 to D15			P50 to P57
A0 to A7	Output	24-bit address bus for external memory	PA0 to PA7
A8 to A15			PB0 to PB7
A16 to A23			P60 to P67
LWR	Output	Lower byte write-enable signal output for external data bus	P90/LCAS
UWR	Output	Higher byte write-enable signal output for external data bus	P91/UCAS
RD	Output	Read strobe signal output for external data bus	P92
WE	Output	Write enable signal output for DRAM	P93
OE	Output	Output enable signal output for DRAM	P95

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Pin Name	I/O	Function	Alternate Function
LCAS	Output	Column address strobe signal output for DRAM's lower data	P90/LWR
UCAS	Output	Column address strobe signal output for DRAM's higher data	P91/UWR
RAS0 to RAS3	Output	Low address strobe signal output for DRAM	P80/CS0 to P83/CS3
RAS4			P84/CS4/IOWR
RAS5			P85/CS5/IORD
RAS6			P86/CS6
RAS7			P87/CS7
BCYST	Output	Strobe signal output indicating start of bus cycle	P94
CS0 to CS3	Output	Chip select signal output	P80/RAS0 to P83/RAS3
CS4			P84/RAS4/IOWR
CS5			P85/RAS5/IORD
CS6			P86/RAS6
CS7			P87/RAS7
WAIT	Input	Control signal input for inserting waits in bus cycle	PX6
REFRQ	Output	Refresh request signal output for DRAM	PX5
IOWR	Output	DMA write strobe signal output	P84/RAS4/CS4
IORD	Output	DMA read strobe signal output	P85/RAS5/CS5
DMARQ0 to DMARQ3	Input	DMA request signal input	P04/INTP100 to P07/INTP103
DMAAK0 to DMAAK3	Output	DMA acknowledge signal output	P14/INTP110 to P17/INTP113
TC0 to TC3	Output	DMA end (terminal count) signal output	P104/INTP120 to P107/INTP123
HLDK	Output	Bus hold acknowledge output	P96
HLDRQ	Input	Bus hold request input	P97
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
NMI	Input	Non-maskable interrupt request input	P20
CLKOUT	Output	System clock output	PX7
CKSEL	Input	Input for specifying clock generator's operation mode	—
MODE0 to MODE3	Input	Specify operation modes	—
RESET	Input	System reset input	—
X1	Input	Oscillator connection for system clock. Input is via X1 when using an external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P127/INTP153
AVREF	Input	Reference voltage input for A/D converter	—
AVDD	—	Positive power supply for A/D converter	—
AVSS	—	Ground potential for A/D converter	—

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Pin Name	I/O	Function	Alternate Function
CV _{DD}	–	Positive power supply for dedicated clock generator	–
CV _{SS}	–	Ground potential for dedicated clock generator	–
V _{DD}	–	Positive power supply (power supply for internal units)	–
HV _{DD}	–	Positive power supply (power supply for external pins)	–
V _{SS}	–	Ground potential	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

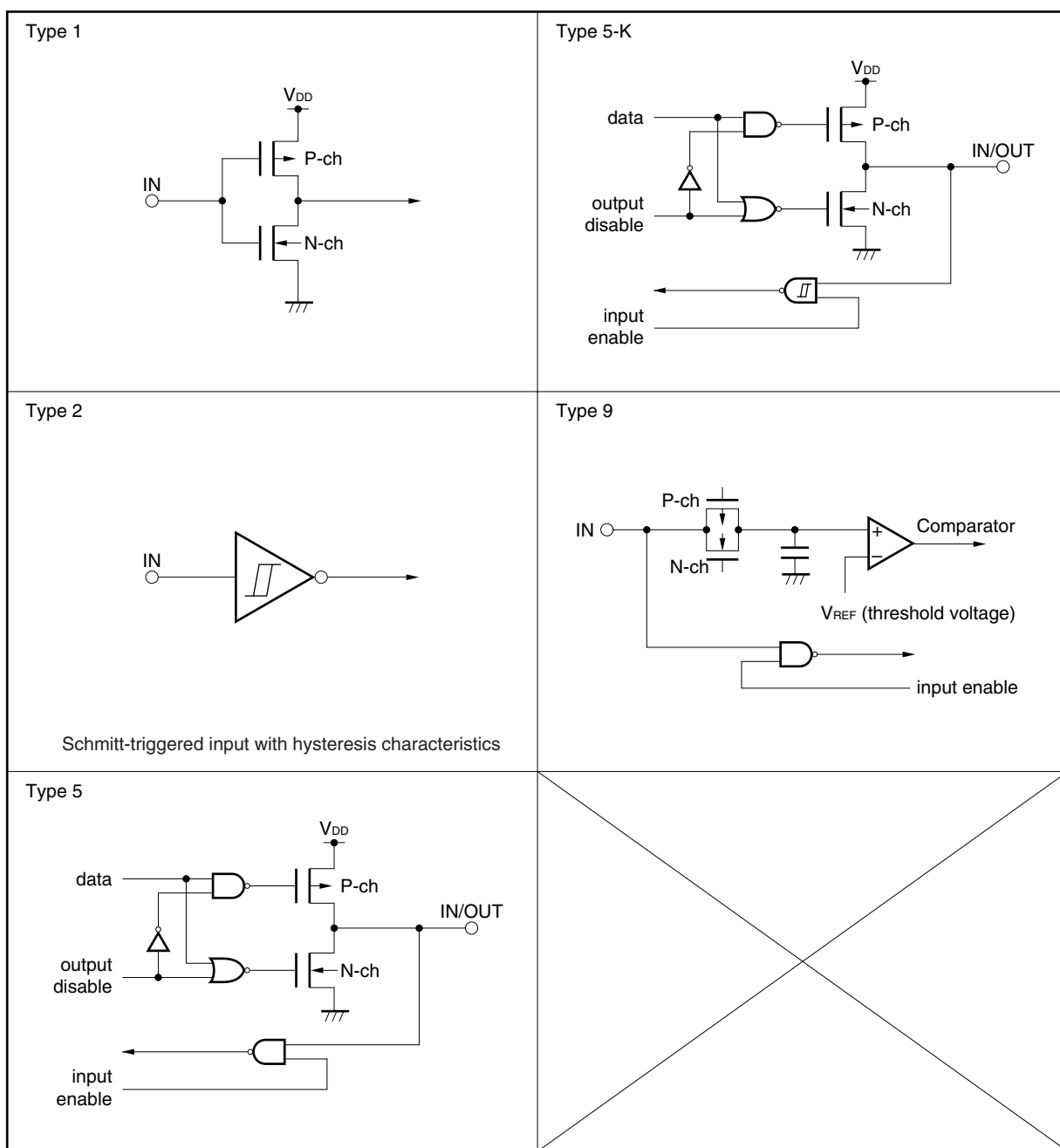
Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100, P01/TO101	5	Input: Independently connect to HV _{DD} or V _{SS} via a resistor Output: Leave open
P02/TCLR10, P03/TI10	5-K	
P04/INTP100/DMARQ0 to P07/INTP103/DMARQ3		
P10/TO110, P11/TO111	5	
P12/TCLR11, P13/TI11	5-K	
P14/INTP110/DMAAK0 to P17/INTP113/DMAAK3		
P20/NMI	2	Connect directly to V _{SS}
P21	5	Input: Independently connect to HV _{DD} or V _{SS} via a resistor Output: Leave open
P22/TXD0/SO0		
P23/RXD0/SI0	5-K	
P24/SCK0		
P25/TXD1/SO1	5	
P26/RXD1/SI1	5-K	
P27/SCK1		
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13	5-K	
P34/INTP130		
P35/INTP131/SO2		
P36/INTP132/SI2		
P37/INTP133/SCK2		
P40/D0 to P47/D7	5	
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P77/ANI7	9	Connect directly to V _{SS}
P80/CS0/RAS0 to P83/CS3/RAS3	5	Input: Independently connect to HV _{DD} or V _{SS} via a resistor Output: Leave open
P84/CS4/RAS4/IOWR, P85/CS5/RAS5/IORD		
P86/CS6/RAS6, P87/CS7/RAS7		
P90/LCAS/LWR		
P91/UCAS/UWR		

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P92/ $\overline{\text{RD}}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P93/ $\overline{\text{WE}}$		
P94/ $\overline{\text{BCYST}}$		
P95/ $\overline{\text{OE}}$		
P96/ $\overline{\text{HLDK}}$		
P97/ $\overline{\text{HLDRQ}}$		
P100/TO120, P101/TO121		
P102/TCLR12, P103/ TI12	5-K	
P104/INTP120/ $\overline{\text{TC0}}$ to P107/INTP123/ $\overline{\text{TC3}}$		
P110/TO140, P111/TO141	5	
P112/TCLR14, P113/ TI14	5-K	
P114/INTP140		
P115/INTP141/SO3		
P116/INTP142/SI3		
P117/INTP143/ $\overline{\text{SCK3}}$		
P120/TO150, P121/TO151	5	
P122/TCLR15, P123/ TI15	5-K	
P124/INTP150 to P126/INTP152		
P127/INTP153/ADTRG		
PA0/A0 to PA7/A7	5	
PB0/A8 to PB7/A15		
PX5/ $\overline{\text{REFRQ}}$		
PX6/ $\overline{\text{WAIT}}$		
PX7/CLKOUT		
CKSEL	1	
$\overline{\text{RESET}}$	2	—
MODE0 to MODE2		Connect to V_{SS} via a resistor (R_{VPP})
MODE3		
AV_{REF} , AV_{SS}	—	Connect directly to V_{SS}
AV_{DD}	—	Connect directly to HV_{DD}

Figure 2-1. Pin I/O Circuits



Caution Replace V_{DD} by HV_{DD} when referencing the circuit diagrams shown above.

★ 3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit	
Power supply voltage	V _{DD}	V _{DD} pin	−0.5 to +4.6	V	
	HV _{DD}	HV _{DD} pin, HV _{DD} ≥ V _{DD}	−0.5 to +7.0	V	
	CV _{DD}	CV _{DD} pin	−0.5 to +4.6	V	
	CV _{SS}	CV _{SS} pin	−0.5 to +0.5	V	
	AV _{DD}	AV _{DD} pin	−0.5 to HV _{DD} + 0.5	V	
	AV _{SS}	AV _{SS} pin	−0.5 to +0.5	V	
Input voltage	V _I	X1 pin, except MODE3 pin	−0.5 to HV _{DD} + 0.5	V	
		MODE3 pin	−0.5 to V _{DD} + 0.5	V	
Clock input voltage	V _K	X1, V _{DD} = 3.0 to 3.6 V	−0.5 to V _{DD} + 1.0	V	
Output current, low	I _{OL}	1 pin	4.0	mA	
		Total of all pins	100	mA	
Output current, high	I _{OH}	1 pin	−4.0	mA	
		Total of all pins	−100	mA	
Output voltage	V _O	HV _{DD} = 5.0 V ±10 %	−0.5 to HV _{DD} + 0.5	V	
Analog input voltage	V _{IAN}	P70/ANI0 to P77/ANI7 pins	AV _{DD} > HV _{DD}	−0.5 to HV _{DD} + 0.5	V
			HV _{DD} ≥ AV _{DD}	−0.5 to AV _{DD} + 0.5	V
A/D converter reference input voltage	AV _{REF}	AV _{DD} > HV _{DD}	−0.5 to HV _{DD} + 0.5	V	
		HV _{DD} ≥ AV _{DD}	−0.5 to AV _{DD} + 0.5	V	
Operating ambient temperature	T _A	μPD703100-40	−40 to +70	°C	
		μPD703100-33, 703101-33, 703102-33	−40 to +85	°C	
Storage temperature	T _{stg}		−60 to +150	°C	

- Cautions**
1. Do not make direct connections of the output (or input/output) pins of the IC product with each other, and also avoid direct connections to V_{DD}, V_{CC}, or GND. However, the open drain pins or the open collector pins can be directly connected with each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to high-impedance state.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
- The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance ($T_A = 25^\circ\text{C}$, $V_{DD} = HV_{DD} = CV_{DD} = V_{SS} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	$f_c = 1\text{ MHz}$ Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)		Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD} , HV_{DD})
Direct mode	μPD703100-40	2 to 40 MHz	-40 to +70°C	$V_{DD} = 3.0\text{ to }3.6\text{ V}$, $HV_{DD} = 5.0\text{ V} \pm 10\%$
	μPD703100-33, 703101-33, 703102-33	2 to 33 MHz	-40 to +85°C	
PLL mode ^{Note 1}	μPD703100-40 ^{Note 2}	20 to 40 MHz	-40 to +70°C	
	μPD703100-33, 703101-33, 703102-33 ^{Note 3}	20 to 33 MHz	-40 to +85°C	

Notes 1. The internal operating clock frequency in PLL mode is the value for 5× operation. When used for 1× or 1/2× operation as set by the CKDIVn (n = 0, 1) bit of the CKC register, operation at a frequency of 20 MHz or less is possible.

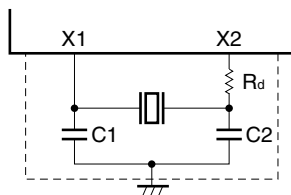
2. Set the input clock frequency used in PLL mode to 4.0 to 8.0 MHz.

3. Set the input clock frequency used in PLL mode to 4.0 to 6.6 MHz.

Recommended Oscillator

(a) Ceramic resonator ($T_A = -40$ to $+70^\circ\text{C}$... μ PD703100-40,
 $T_A = -40$ to $+85^\circ\text{C}$... μ PD703100-33, 703101-33, 703102-33)

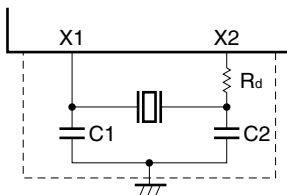
(i) Murata Mfg. Co., Ltd. ($T_A = -40$ to $+85^\circ\text{C}$)



Type	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (k Ω)	MIN. (V)	MAX. (V)	
Surface mounting	CSAC4.00MGC040	4.0	100	100	0	3.0	3.6	0.5
	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.3
	CSAC5.00MGC040	5.0	100	100	0	3.0	3.6	0.4
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.2
	CSAC6.60MT	6.6	30	30	0	3.0	3.6	0.2
	CSTCC6.60MG0H6	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSAC8.00MT	8.0	30	30	0	3.0	3.6	0.2
	CSTCC8.00MG0H6	8.0	On-chip	On-chip	0	3.0	3.6	0.3
Lead	CSA4.00MG040	4.0	100	100	0	3.0	3.6	0.5
	CST4.00MGW040	4.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA5.00MG040	5.0	100	100	0	3.0	3.6	0.5
	CST5.00MGW040	5.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA6.60MTZ	6.6	30	30	0	3.0	3.6	0.1
	CST6.60MTW	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSA8.00MTZ	8.0	30	30	0	3.0	3.6	0.1
	CST8.00MTW	8.0	On-chip	On-chip	0	3.0	3.6	0.1

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
 2. Do not wire any other signal lines in the area enclosed by broken lines.
 3. Sufficiently evaluate the matching between the μ PD703100-33, 703100-40, 703101-33, 703102-33 and the resonator.

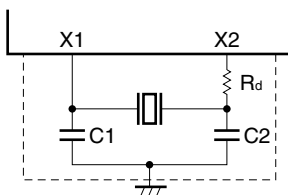
(ii) TDK ($T_A = -40$ to $+85^\circ\text{C}$)



Manufac-turer	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (k Ω)	MIN. (V)	MAX. (V)	
TDK	CCR4.0MC3	4.0	On-chip	On-chip	0	3.0	3.6	0.17
	CCR5.0MC3	5.0	On-chip	On-chip	0	3.0	3.6	0.15
	CCR8.0MC5	8.0	On-chip	On-chip	0	3.0	3.6	0.11

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
 2. Do not wire any other signal lines in the area enclosed by broken lines.
 3. Sufficiently evaluate the matching between the μ PD703100-33, 703100-40, 703101-33, 703102-33 and the resonator.

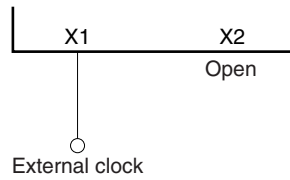
(iii) Kyocera Corporation ($T_A = -20$ to $+80^\circ\text{C}$)



Manufac-turer	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (k Ω)	MIN. (V)	MAX. (V)	
Kyocera	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.00BR-A	6.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.60BR-A	6.6	On-chip	On-chip	0	3.0	3.6	0.06

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
 2. Do not wire any other signal lines in the area enclosed by broken lines.
 3. Sufficiently evaluate the matching between the μ PD703100-33, 703100-40, 703101-33, 703102-33 and the resonator.

- (b) External clock input ($T_A = -40$ to $+70^\circ\text{C}$... μ PD703100-40,
 $T_A = -40$ to $+85^\circ\text{C}$... μ PD703100-33, μ PD703101-33, μ PD703102-33)



Caution Input CMOS-level voltage to the X1 pin.

DC Characteristics ($T_A = -40$ to $+70^\circ\text{C}$... μPD703100-40, $T_A = -40$ to $+85^\circ\text{C}$... μPD703100-33, μPD703101-33, μPD703102-33, $V_{DD} = CV_{DD} = 3.0$ to 3.6 V, $HV_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	Except Note 1		2.2		$HV_{DD} + 0.3$	V
		Note 1		$0.8HV_{DD}$		$HV_{DD} + 0.3$	V
Input voltage, low	V_{IL}	Except Note 1 and Note 2		-0.5		+0.8	V
		Note 1		-0.5		$0.2HV_{DD}$	V
Clock input voltage, high	V_{XH}	X1 pin	Direct mode	$0.8V_{DD}$		$V_{DD} + 0.3$	V
			PLL mode	$0.8V_{DD}$		$V_{DD} + 0.3$	V
Clock input voltage, low	V_{XL}	X1 pin	Direct mode	-0.3		$0.15V_{DD}$	V
			PLL mode	-0.3		$0.15V_{DD}$	V
Schmitt-triggered input threshold voltage	HVT^+	Note 1 , rising edge			3.0		V
	HVT^-	Note 1 , falling edge			2.0		V
Schmitt-triggered input hysteresis width	$HVT^+ - HVT^-$	Note 1		0.5			V
Output voltage, high	V_{OH}	$I_{OH} = -2.5$ mA		$0.7HV_{DD}$			V
		$I_{OH} = -100$ μA		$HV_{DD} - 0.4$			V
Output voltage, low	V_{OL}	$I_{OL} = 2.5$ mA				0.45	V
Input leakage current, high	I_{LIH}	Except $V_I = HV_{DD}$ or Note 2				10	μA
Input leakage current, low	I_{LIL}	Except $V_I = 0$ V or Note 2				-10	μA
Output leakage current, high	I_{LOH}	$V_O = HV_{DD}$				10	μA
Output leakage current, low	I_{LOL}	$V_O = 0$ V				-10	μA

Notes 1. P04/INTP100/DMARQ0 to P07/INTP103/DMARQ3, P14/INTP110/DMAAK0 to P17/INTP113/DMAAK3, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/SCK2, P104/INTP120/TC0 to P107/INTP123/TC3, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/SCK3, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, MODE0 to MODE2, RESET

2. When the P70/ANI0 to P77/ANI7 pins are used as analog input.

Remark TYP. values are reference values for when $T_A = 25^\circ\text{C}$, $V_{DD} = CV_{DD} = 3.3$ V, and $HV_{DD} = 5.0$ V.

DC Characteristics ($T_A = -40$ to $+70^\circ\text{C}$... μ PD703100-40, $T_A = -40$ to $+85^\circ\text{C}$... μ PD703100-33, μ PD703101-33, μ PD703102-33, $V_{DD} = CV_{DD} = 3.0$ to 3.6 V, $HV_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ V)

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit
Power supply current	Normal mode	I _{DD1}		$V_{DD} + CV_{DD}$		$2.0 \times f_x$	$3.6 \times f_x$	mA
				HV_{DD}		$1.8 \times f_x$	$3.0 \times f_x$	mA
	HALT mode	I _{DD2}		$V_{DD} + CV_{DD}$		$1.4 \times f_x$	$2.5 \times f_x$	mA
				HV_{DD}		$0.8 \times f_x$	$1.6 \times f_x$	mA
	IDLE mode	I _{DD3}		$V_{DD} + CV_{DD}$		1.5	3.0	mA
				HV_{DD}		10	50	μA
	STOP mode	I _{DD4}	μ PD703100-40	$V_{DD} + CV_{DD}$		1.0	3.0	mA
				HV_{DD}		10	50	μA
			μ PD703100-33, 703101-33, 703102-33	$V_{DD} + CV_{DD}$		20	100	μA
				HV_{DD}		10	50	μA

Remarks 1. TYP. values are reference values for when $T_A = 25^\circ\text{C}$, $V_{DD} = CV_{DD} = 3.3$ V, and $HV_{DD} = 5.0$ V.

2. Direct mode:

$f_x = 2$ to 40 MHz (μ PD703100-40)

$f_x = 2$ to 33 MHz (μ PD703100-33, μ PD703101-33, μ PD703102-33)

PLL mode:

$f_x = 20$ to 40 MHz (μ PD703100-40)

$f_x = 20$ to 33 MHz (μ PD703100-33, μ PD703101-33, μ PD703102-33)

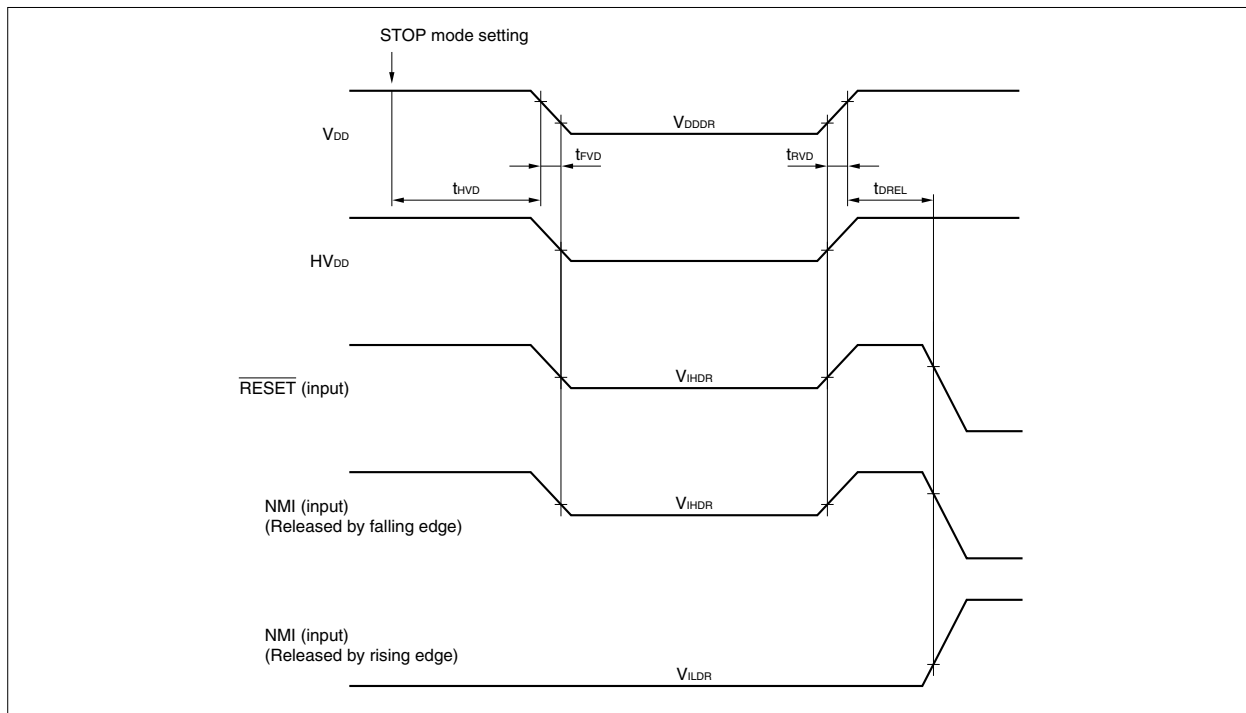
3. The unit for f_x is MHz.

Data Hold Characteristics (T_A = -40 to +70°C ... μPD703100-40, T_A = -40 to +85°C ... μPD703100-33, μPD703101-33, μPD703102-33)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V _{DDDR}	STOP mode, V _{DD} = V _{DDDR}		1.5		3.6	V
	HV _{DDDR}	STOP mode, HV _{DD} = HV _{DDDR}		V _{DDDR}		5.5	V
Data hold current	I _{DDDR}	μPD703100-40	V _{DD} = V _{DDDR}		1.0	3.0	mA
		μPD703100-33, 703101-33, 703102-33	V _{DD} = V _{DDDR}		30	150	μA
Power supply voltage rise time	trVD			200			μs
Power supply voltage fall time	tfVD			200			μs
Power supply voltage hold time (to STOP mode setting)	thVD			0			ms
STOP mode release signal input time	tdREL			0			ns
Data hold high-level input voltage	VIHDR	Note		0.8HV _{DDDR}		HV _{DDDR}	V
Data hold low-level input voltage	VILDR	Note		0		0.2HV _{DDDR}	V

Note P04/INTP100/D_{MA}RQ0 to P07/INTP103/D_{MA}RQ3, P14/INTP110/D_{MA}AK0 to P17/INTP113/D_{MA}AK3, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/SCK2, P104/INTP120/T_C0 to P107/INTP123/T_C3, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/SCK3, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, MODE0 to MODE2, RESET

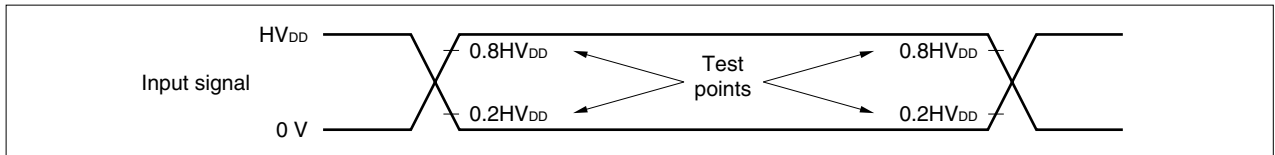
Remark TYP. values are reference values for when T_A = 25°C.



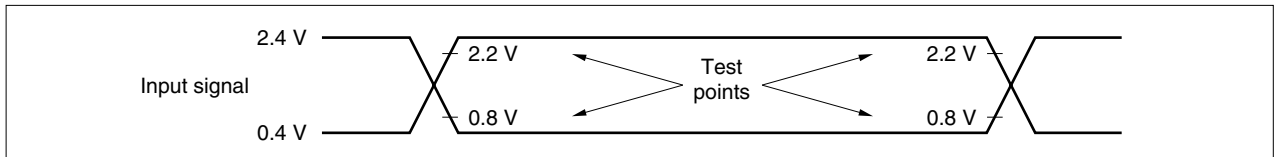
AC Characteristics ($T_A = -40$ to $+70^\circ\text{C}$... μ PD703100-40, $T_A = -40$ to $+85^\circ\text{C}$... μ PD703100-33, μ PD703101-33, μ PD703102-33, $V_{DD} = CV_{DD} = 3.0$ to 3.6 V, $HV_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ V, output pin load capacitance: $C_L = 50$ pF)

AC Test Input Waveform

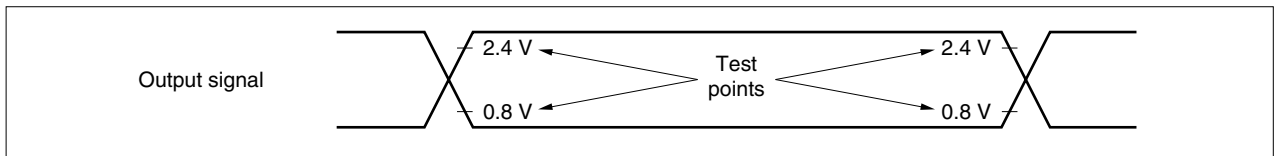
- (a) P04/INTP100/D $\overline{\text{MARQ0}}$ to P07/INTP103/D $\overline{\text{MARQ3}}$, P14/INTP110/D $\overline{\text{MAAK0}}$ to P17/INTP113/D $\overline{\text{MAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/ $\overline{\text{SCK2}}$, P104/INTP120/ $\overline{\text{TC0}}$ to P107/INTP123/ $\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/ $\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/ $\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/ $\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$



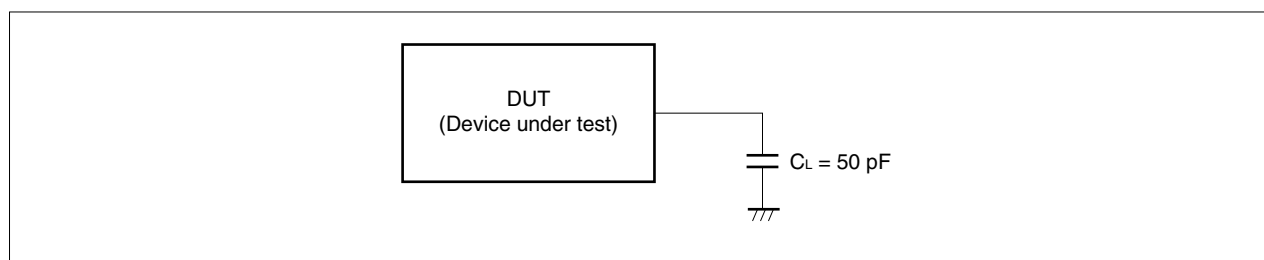
- (b) Pins other than those listed in (a) above



AC Test Output Test Points



Load Condition

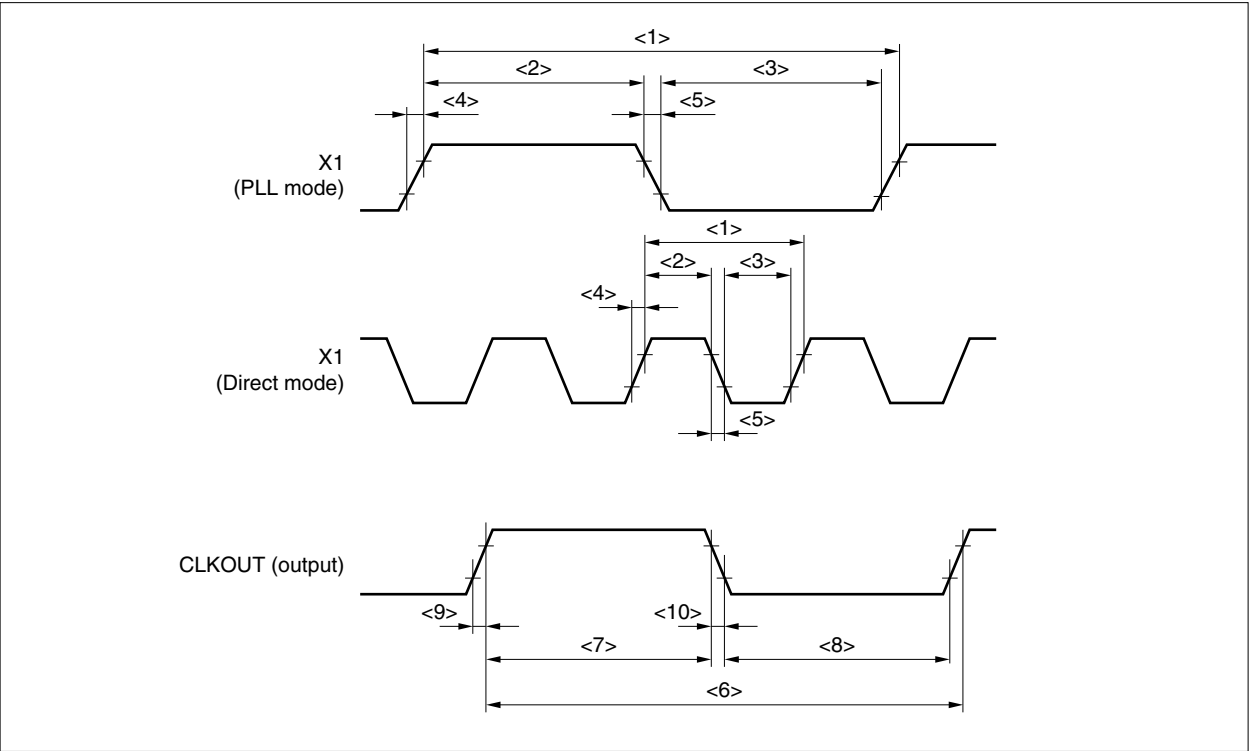


Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance 50 pF.

(1) Clock timing

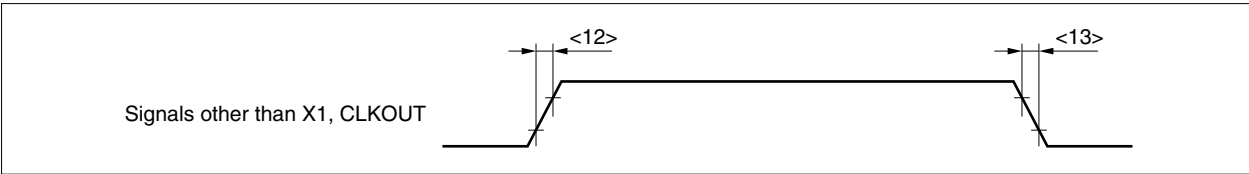
Parameter	Symbol		Condition		MIN.	MAX.	Unit
X1 input cycle	<1>	t _{CYX}	Direct mode	μPD703100-40	12.5	250	ns
				μPD703100-33, 703101-33, 703102-33	15	250	ns
			PLL mode	μPD703100-40	125	250	ns
				μPD703100-33, 703101-33, 703102-33	150	250	ns
X1 input high-level width	<2>	t _{WXH}	Direct mode		5		ns
			PLL mode		50		ns
X1 input low-level width	<3>	t _{WXL}	Direct mode		5		ns
			PLL mode		50		ns
X1 input rise time	<4>	t _{XR}	Direct mode			4	ns
			PLL mode			10	ns
X1 input fall time	<5>	t _{XF}	Direct mode			4	ns
			PLL mode			10	ns
CLKOUT output cycle	<6>	t _{CYK}	μPD703100-40		25	500	ns
			μPD703100-33, 703101-33, 703102-33		30	500	ns
CLKOUT high-level width	<7>	t _{WKH}			0.5T – 7		ns
CLKOUT low-level width	<8>	t _{WKL}			0.5T – 4		ns
CLKOUT rise time	<9>	t _{KR}				5	ns
CLKOUT fall time	<10>	t _{KF}				5	ns

Remark T = t_{CYK}



(2) Output waveform (other than X1, CLKOUT)

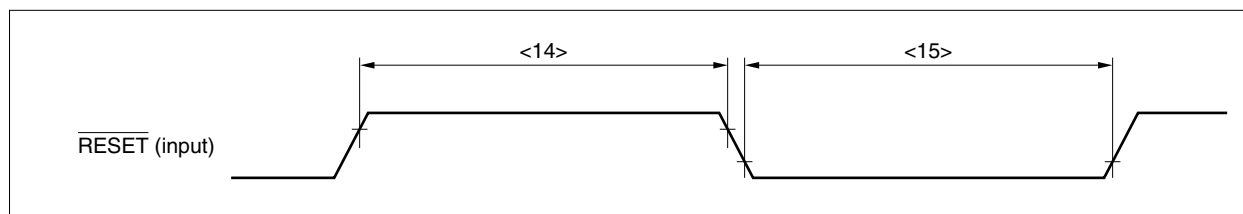
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	t _{OR}			10	ns
Output fall time	<13>	t _{OF}			10	ns



(3) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<14>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	<15>	t_{WRSL}	When power supply is on, and STOP mode has been released	$500 + T_{\text{os}}$		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

Remark T_{os} : Oscillation stabilization time



[MEMO]

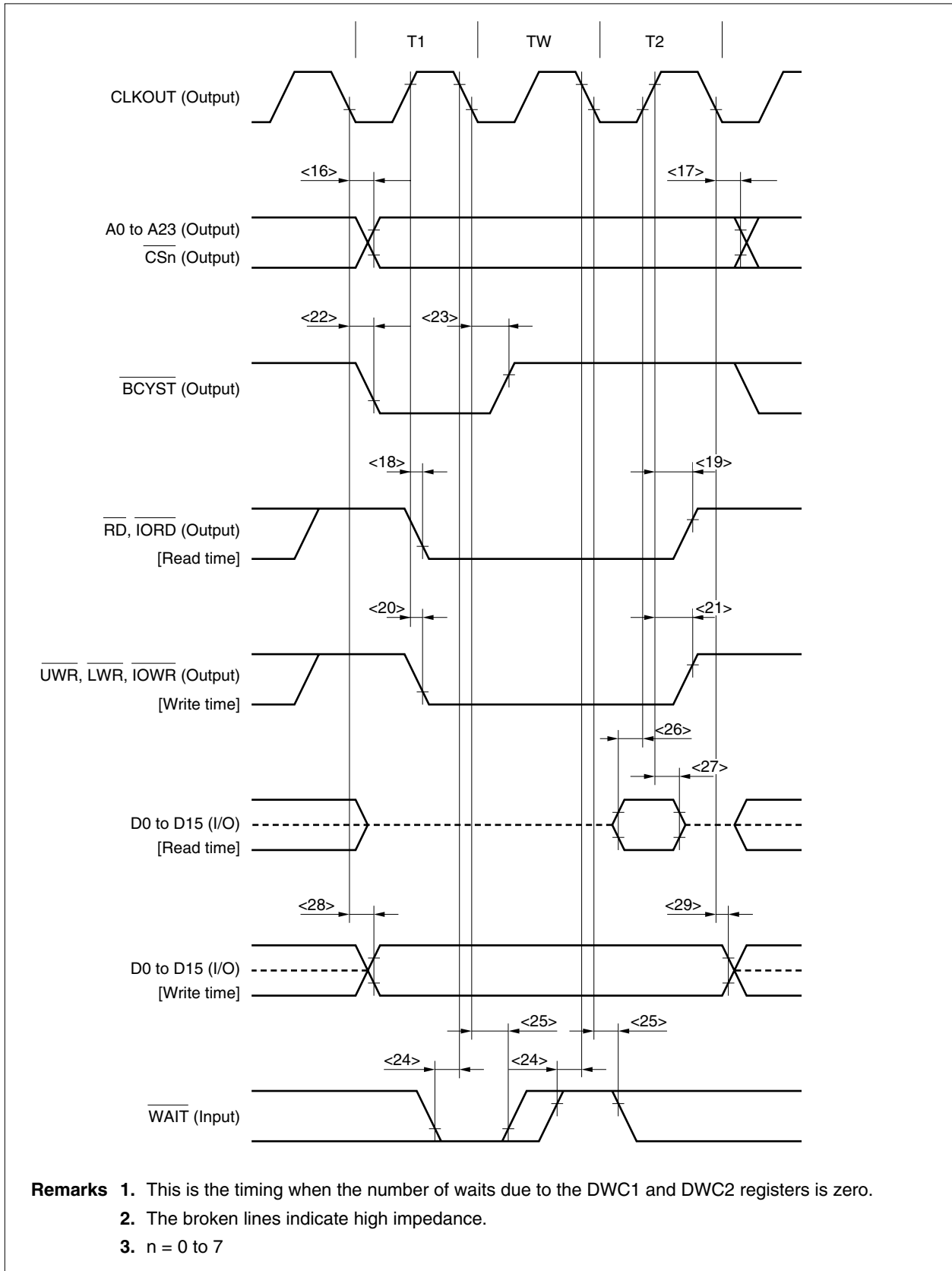
(4) SRAM, external ROM, or external I/O access timing

(a) Access timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address, $\overline{CSn}$ output delay time (from CLKOUT $\downarrow$)	<16> t_{DKA}		2	10	ns
Address, $\overline{CSn}$ output hold time (from CLKOUT $\downarrow$)	<17> t_{HKA}		2	10	ns
$\overline{RD}$, $\overline{IORD}$ $\downarrow$ delay time (from CLKOUT $\uparrow$)	<18> t_{DKRDL}		2	14	ns
$\overline{RD}$, $\overline{IORD}$ $\uparrow$ delay time (from CLKOUT $\uparrow$)	<19> t_{HKRDH}		2	14	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ $\downarrow$ delay time (from CLKOUT $\uparrow$)	<20> t_{DKWRL}		2	10	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ $\uparrow$ delay time (from CLKOUT $\uparrow$)	<21> t_{HKWRH}		2	10	ns
$\overline{BCYST}$ $\downarrow$ delay time (from CLKOUT $\downarrow$)	<22> t_{DKBSL}		2	10	ns
$\overline{BCYST}$ $\uparrow$ delay time (from CLKOUT $\downarrow$)	<23> t_{HKBSH}		2	10	ns
$\overline{WAIT}$ setup time (to CLKOUT $\downarrow$)	<24> t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT $\downarrow$)	<25> t_{HKW}		2		ns
Data input setup time (to CLKOUT $\uparrow$)	<26> t_{SKID}		18		ns
Data input hold time (from CLKOUT $\uparrow$)	<27> t_{HKID}		2		ns
Data output delay time (from CLKOUT $\downarrow$)	<28> t_{DKOD}		2	10	ns
Data output hold time (from CLKOUT $\downarrow$)	<29> t_{HKOD}		2	10	ns

- Remarks**
1. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID} .
 2. $n = 0$ to 7

(a) Access timing (SRAM, external ROM, or external I/O) (2/2)



(b) Read timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data input setup time (to address)	<30> t_{SAID}			$(1.5 + w_D + w)T - 28$	ns
Data input setup time (to $\overline{RD}$)	<31> t_{SRDID}			$(1 + w_D + w)T - 32$	ns
$\overline{RD}$, $\overline{IORD}$ low-level width	<32> t_{WRDL}		$(1 + w_D + w)T - 10$		ns
$\overline{RD}$, $\overline{IORD}$ high-level width	<33> t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$, $\overline{IORD} \downarrow$	<34> t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{RD}$, $\overline{IORD} \uparrow$ to address	<35> t_{DRDA}		$(0.5 + i)T - 10$		ns
Data input hold time (from $\overline{RD}$, $\overline{IORD} \uparrow$)	<36> t_{HRDID}		0		ns
Delay time from $\overline{RD}$, $\overline{IORD} \uparrow$ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38> t_{SAW}	Note		$T - 25$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST} \downarrow$)	<39> t_{SBSW}	Note		$T - 25$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST} \uparrow$)	<40> t_{HBSW}	Note	0		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w : the number of waits due to $\overline{WAIT}$.

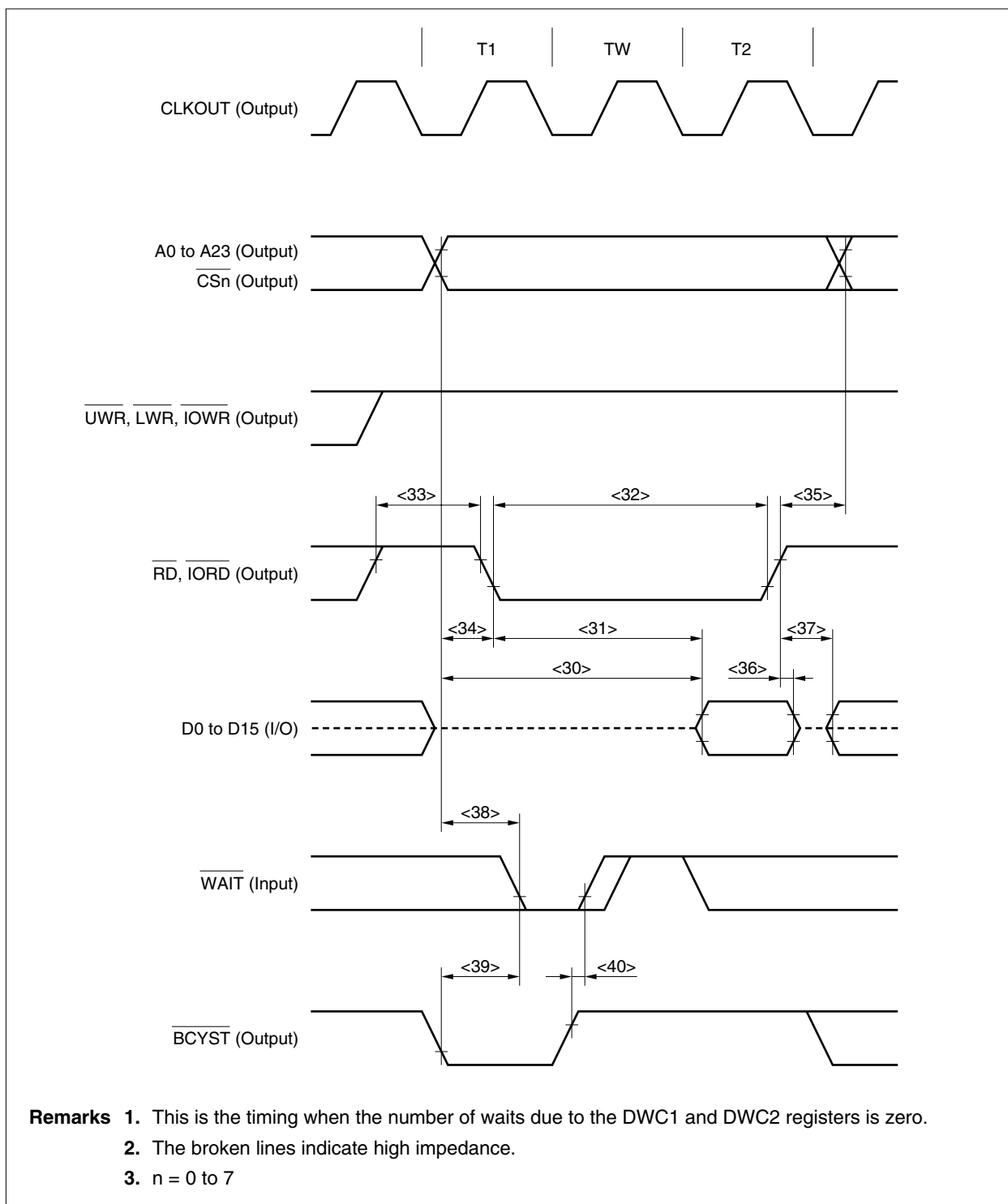
3. w_D : the number of waits due to the DWC1 and DWC2 registers.

4. i : the number of idle states that are inserted when a write cycle follows a read cycle.

5. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID} .

6. $n = 0$ to 7

(b) Read timing (SRAM, external ROM, or external I/O) (2/2)



(c) Write timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to address)	<38> t_{SAW}	Note		$T - 25$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39> t_{SBSW}	Note		$T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40> t_{HBSW}	Note	0		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↓	<41> t_{DAWR}		$0.5T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑)	<42> t_{SAWR}		$(1.5 + \text{WD} + \text{w})T - 10$		ns
Delay time from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑ to address	<43> t_{DWRA}		$0.5T - 10$		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ high-level width	<44> t_{WWRH}		$T - 10$		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ low-level width	<45> t_{WWRL}		$(1 + \text{WD} + \text{w})T - 10$		ns
Data output setup time (to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑)	<46> t_{SODWR}		$(1.5 + \text{WD} + \text{w})T - 10$		ns
Data output hold time (from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑)	<47> t_{HWROD}		$0.5T - 10$		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

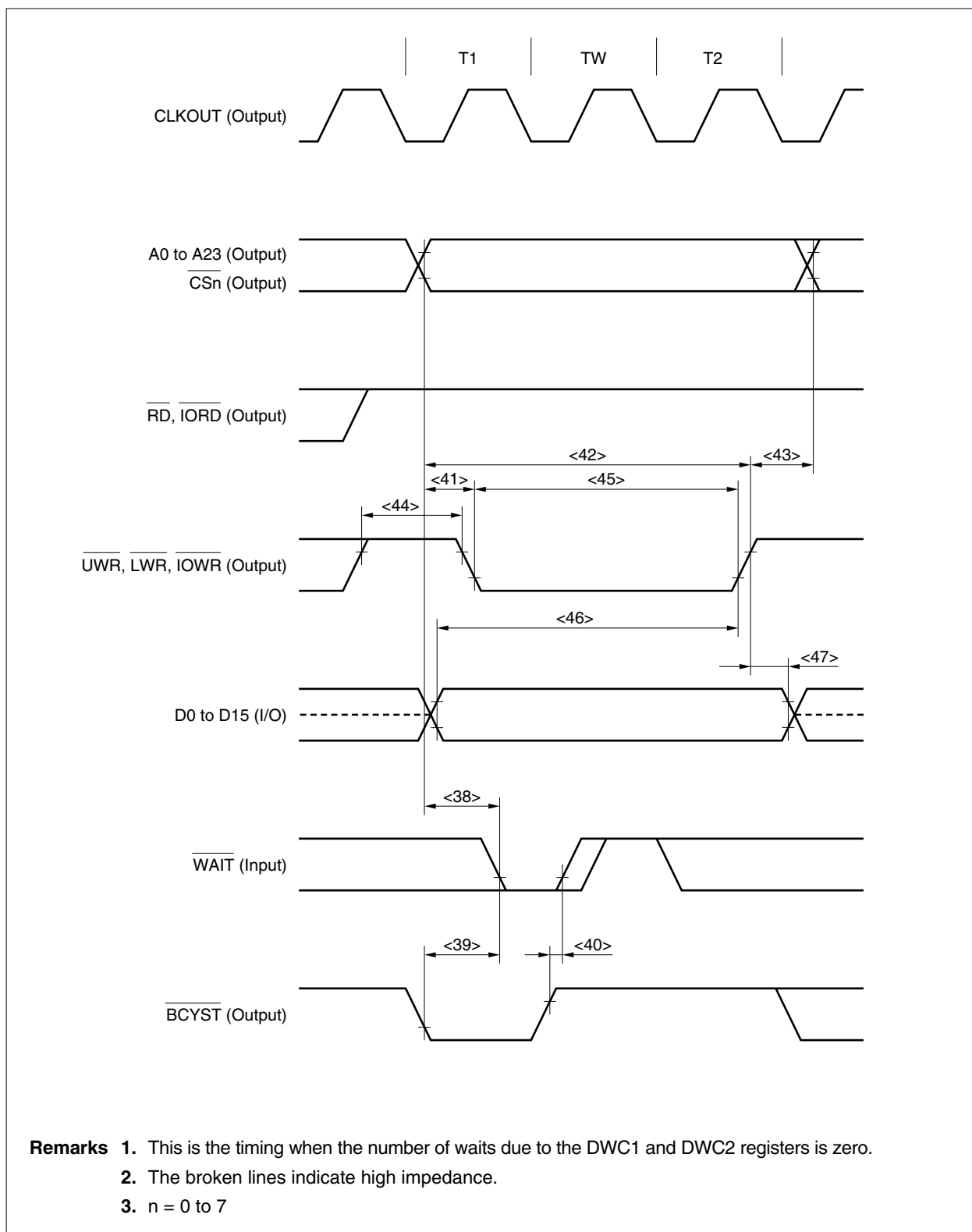
Remarks 1. $T = t_{\text{CYK}}$

2. w : the number of waits due to $\overline{\text{WAIT}}$.

3. WD : the number of waits due to the DWC1 and DWC2 registers.

4. $n = 0$ to 7

(c) Write timing (SRAM, external ROM, or external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.
 2. The broken lines indicate high impedance.
 3. $n = 0$ to 7

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24> t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25> t_{HKW}		2		ns
$\overline{\text{RD}}$ low-level width	<32> t_{WRDL}		$(1 + w_D + w_F + w)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33> t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{RD}}$ ↓	<34> t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{\text{RD}}$ ↑ to address	<35> t_{DRDA}		$(0.5 + i)T - 10$		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38> t_{SAW}	Note		$T - 25$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39> t_{SBSW}	Note		$T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40> t_{HBSW}	Note	0		ns
Delay time from address to $\overline{\text{IOWR}}$ ↓	<41> t_{DAWR}		$0.5T - 10$		ns
Address setup time (to $\overline{\text{IOWR}}$ ↑)	<42> t_{SAWR}		$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to address	<43> t_{DWRA}		$0.5T - 10$		ns
$\overline{\text{IOWR}}$ high-level width	<44> t_{WWRH}		$T - 10$		ns
$\overline{\text{IOWR}}$ low-level width	<45> t_{WWRL}		$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{RD}}$ ↑	<48> t_{DWRRD}	$w_F = 0$	0		ns
		$w_F = 1$	$T - 10$		ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{IOWR}}$ ↓	<49> t_{DDAWR}		$0.5T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{DMAAKm}}$ ↑	<50> t_{DWRDA}		$(0.5 + w_F)T - 10$		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{\text{CYK}}$

2. w : the number of waits due to $\overline{\text{WAIT}}$.

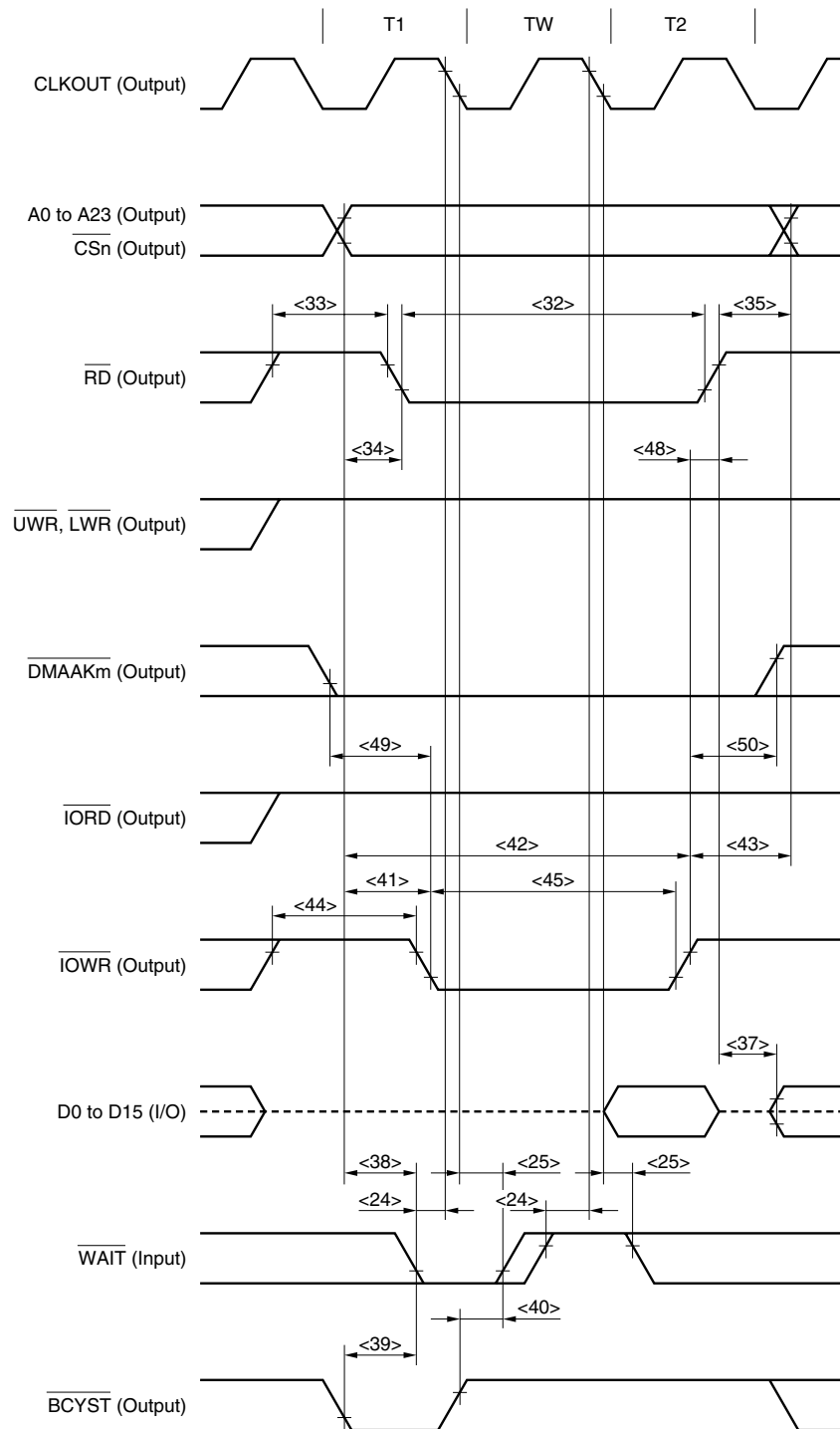
3. w_D : the number of waits due to the DWC1 and DWC2 registers.

4. w_F : the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i : the number of idle states that are inserted when a write cycle follows a read cycle.

6. $n = 0$ to 7, $m = 0$ to 3

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.
 2. The broken lines indicate high impedance.
 3. $n = 0$ to 7 , $m = 0$ to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24> t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25> t_{HKW}		2		ns
$\overline{\text{IORD}}$ low-level width	<32> t_{WRDL}		$(1 + w_D + w_F + w)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33> t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{IORD}}$ ↓	<34> t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<35> t_{DRDA}		$(0.5 + i)T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38> t_{SAW}	Note		$T - 25$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39> t_{SBSW}	Note		$T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40> t_{HBSW}	Note	0		ns
Delay time from address to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ ↓	<41> t_{DAWR}		$0.5T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ ↑)	<42> t_{SAWR}		$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ to address	<43> t_{DWRA}		$0.5T - 10$		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$ high-level width	<44> t_{WWRH}		$T - 10$		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$ low-level width	<45> t_{WWRL}		$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ ↑ to $\overline{\text{IORD}}$ ↑	<48> t_{DWRRD}	$w_F = 0$	0		ns
		$w_F = 1$	$T - 10$		ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{IORD}}$ ↓	<51> t_{DDARD}		$0.5T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to $\overline{\text{DMAAKm}}$ ↑	<52> t_{DRDDA}		$0.5T - 10$		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{\text{CYK}}$

2. w : the number of waits due to $\overline{\text{WAIT}}$.

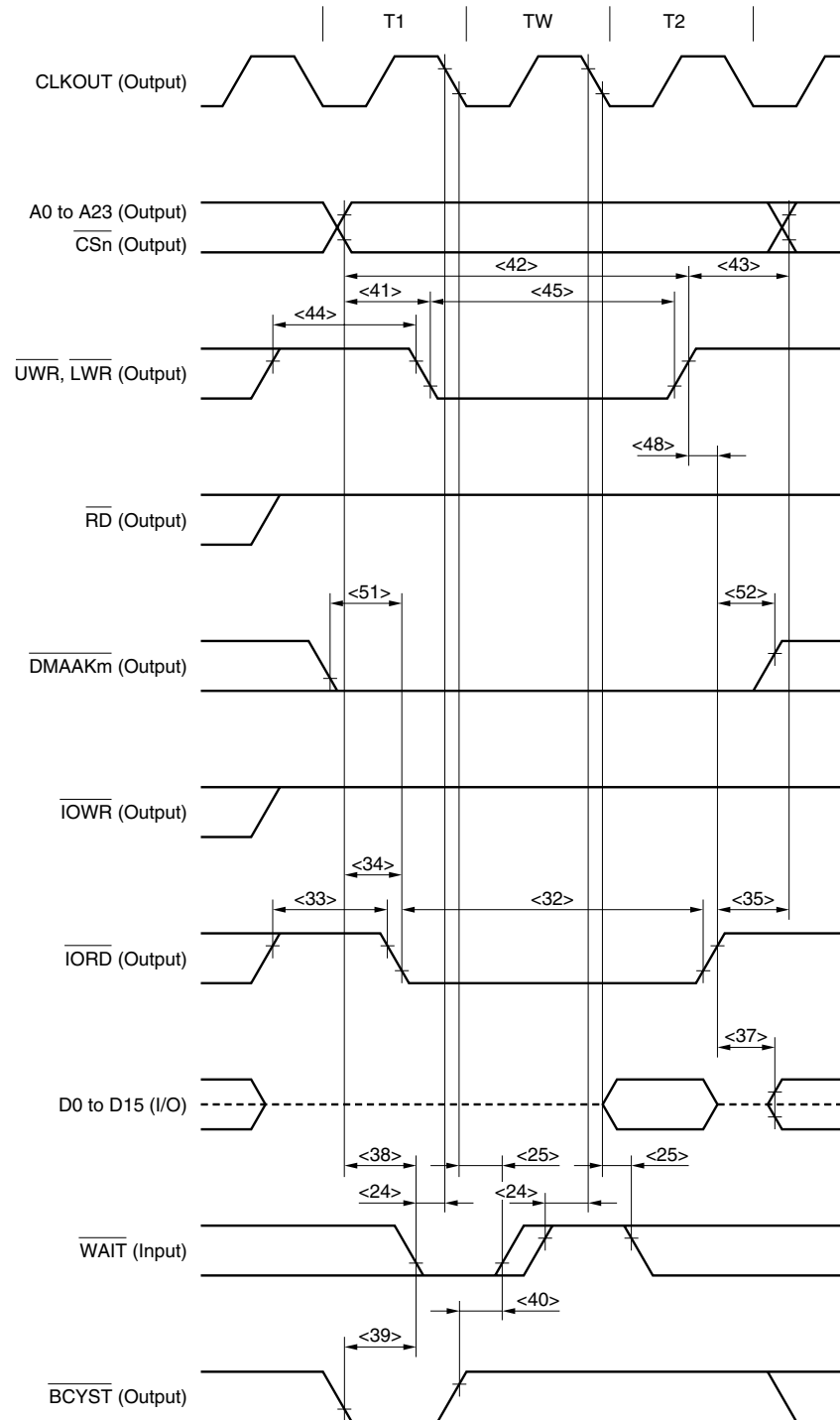
3. w_D : the number of waits due to the DWC1 and DWC2 registers.

4. w_F : the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i : the number of idle states that are inserted when a write cycle follows a read cycle.

6. $n = 0$ to 7, $m = 0$ to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



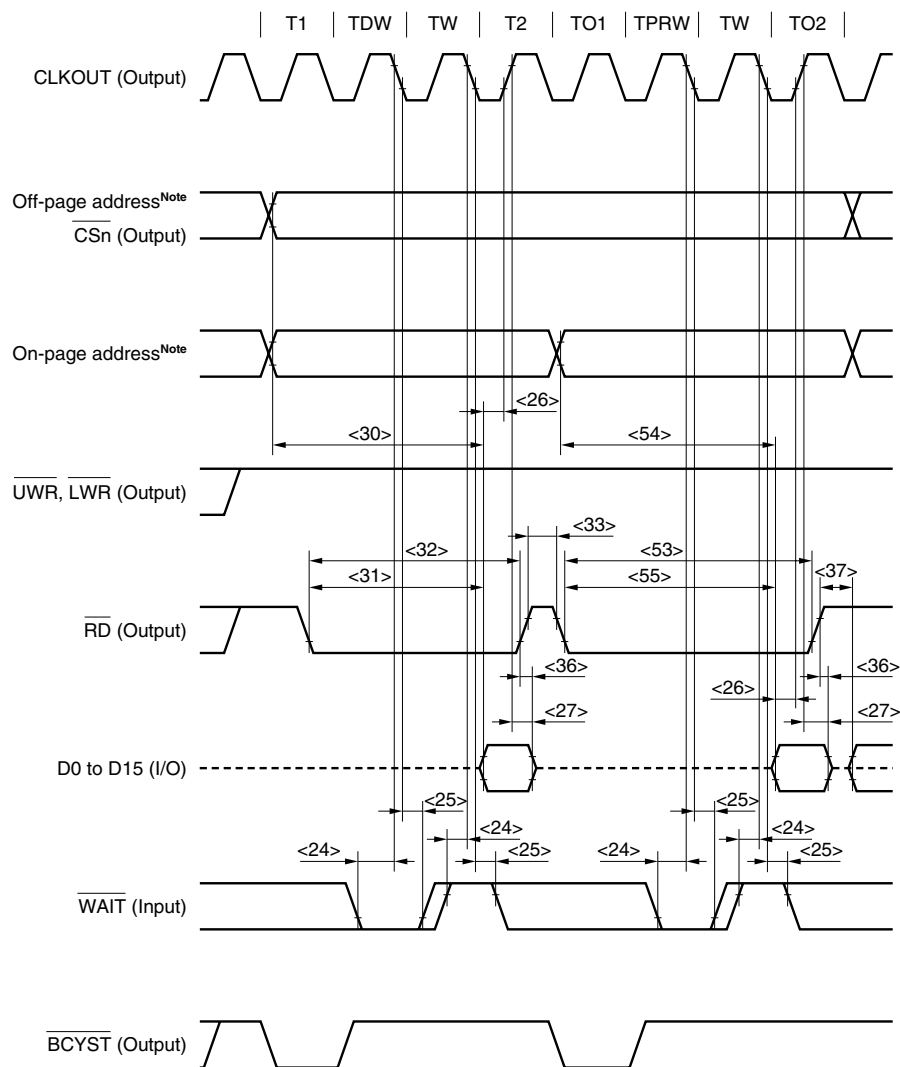
- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.
 2. The broken lines indicate high impedance.
 3. $n = 0$ to 7, $m = 0$ to 3

(5) Page ROM access timing (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT $\downarrow$)	<24> t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT $\downarrow$)	<25> t_{HKW}		2		ns
Data input setup time (to CLKOUT $\uparrow$)	<26> t_{SKID}		18		ns
Data input hold time (from CLKOUT $\uparrow$)	<27> t_{HKID}		2		ns
Off-page data input setup time (to address)	<30> t_{SAID}			$(1.5 + w_D + w)T - 28$	ns
Off-page data input setup time (to $\overline{\text{RD}}$)	<31> t_{SRDID}			$(1 + w_D + w)T - 32$	ns
Off-page $\overline{\text{RD}}$ low-level width	<32> t_{WRDL}		$(1 + w_D + w)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33> t_{WRDH}		$0.5T - 10$		ns
Data input hold time (from $\overline{\text{RD}}$)	<36> t_{HRDID}		0		ns
Delay time from $\overline{\text{RD}}$ $\uparrow$ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
On-page $\overline{\text{RD}}$ low-level width	<53> t_{WORDL}		$(1.5 + w_{\text{PR}} + w)T - 10$		ns
On-page data input setup time (to address)	<54> t_{SOAID}			$(1.5 + w_{\text{PR}} + w)T - 28$	ns
On-page data input setup time (to $\overline{\text{RD}}$)	<55> t_{SORDID}			$(1.5 + w_{\text{PR}} + w)T - 32$	ns

Remarks 1. $T = t_{\text{CYK}}$ 2. w : the number of waits due to $\overline{\text{WAIT}}$.3. w_D : the number of waits due to the DWC1 and DWC2 registers.4. w_{PR} : the number of waits due to the PRC register.5. i : the number of idle states that are inserted when a write cycle follows a read cycle.6. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID} .

(5) Page ROM access timing (2/2)



Note On-page and off-page addresses are as follows.

PRC Register			On-page Addresses	Off-page Addresses
MA5	MA4	MA3		
0	0	0	A0, A1	A2 to A23
0	0	1	A0 to A2	A3 to A23
0	1	1	A0 to A3	A4 to A23
1	1	1	A0 to A4	A5 to A23

Remarks 1. This is the timing for the following case.

Number of waits due to the DWC1 and DWC2 registers (TDW): 1

Number of waits due to the PRC register (TPRW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT $\downarrow$)	<24> t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT $\downarrow$)	<25> t_{HKW}		2		ns
Data input setup time (to CLKOUT $\uparrow$)	<26> t_{SKID}		18		ns
Data input hold time (from CLKOUT $\uparrow$)	<27> t_{HKID}		2		ns
Delay time from $\overline{\text{OE}}$ $\uparrow$ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
Row address setup time	<56> t_{ASR}		$(0.5 + W_{\text{RP}})T - 10$		ns
Row address hold time	<57> t_{RAH}		$(0.5 + W_{\text{RH}})T - 10$		ns
Column address setup time	<58> t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59> t_{CAH}		$(1.5 + W_{\text{DA}} + w)T - 10$		ns
Read/write cycle time	<60> t_{RC}		$(3 + W_{\text{RP}} + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61> t_{RP}		$(0.5 + W_{\text{RP}})T - 10$		ns
$\overline{\text{RAS}}$ pulse time	<62> t_{RAS}		$(2.5 + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63> t_{RSH}		$(1.5 + W_{\text{DA}} + w)T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64> t_{RAL}		$(2 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65> t_{CAS}		$(1 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66> t_{CRP}		$(1 + W_{\text{RP}})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67> t_{CSH}		$(2 + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{WE}}$ setup time	<68> t_{RCS}		$(2 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}$ $\uparrow$)	<69> t_{RRH}		$0.5T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ $\uparrow$)	<70> t_{RCH}		$T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71> t_{CPN}		$(2 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
Output enable access time	<72> t_{OEA}			$(2 + W_{\text{RP}} + W_{\text{RH}} + W_{\text{DA}} + w)T - 28$	ns
$\overline{\text{RAS}}$ access time	<73> t_{RAC}			$(2 + W_{\text{RH}} + W_{\text{DA}} + w)T - 28$	ns
Access time from column address	<74> t_{AA}			$(1.5 + W_{\text{DA}} + w)T - 28$	ns
$\overline{\text{CAS}}$ access time	<75> t_{CAC}			$(1 + W_{\text{DA}} + w)T - 28$	ns

Remarks 1. $T = t_{\text{CYK}}$ 2. w : the number of waits due to $\overline{\text{WAIT}}$.3. W_{RP} : the number of waits due to the RPCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).4. W_{RH} : the number of waits due to the RHCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).5. W_{DA} : the number of waits due to the DACxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).6. i : the number of idle states that are inserted when a write cycle follows a read cycle.

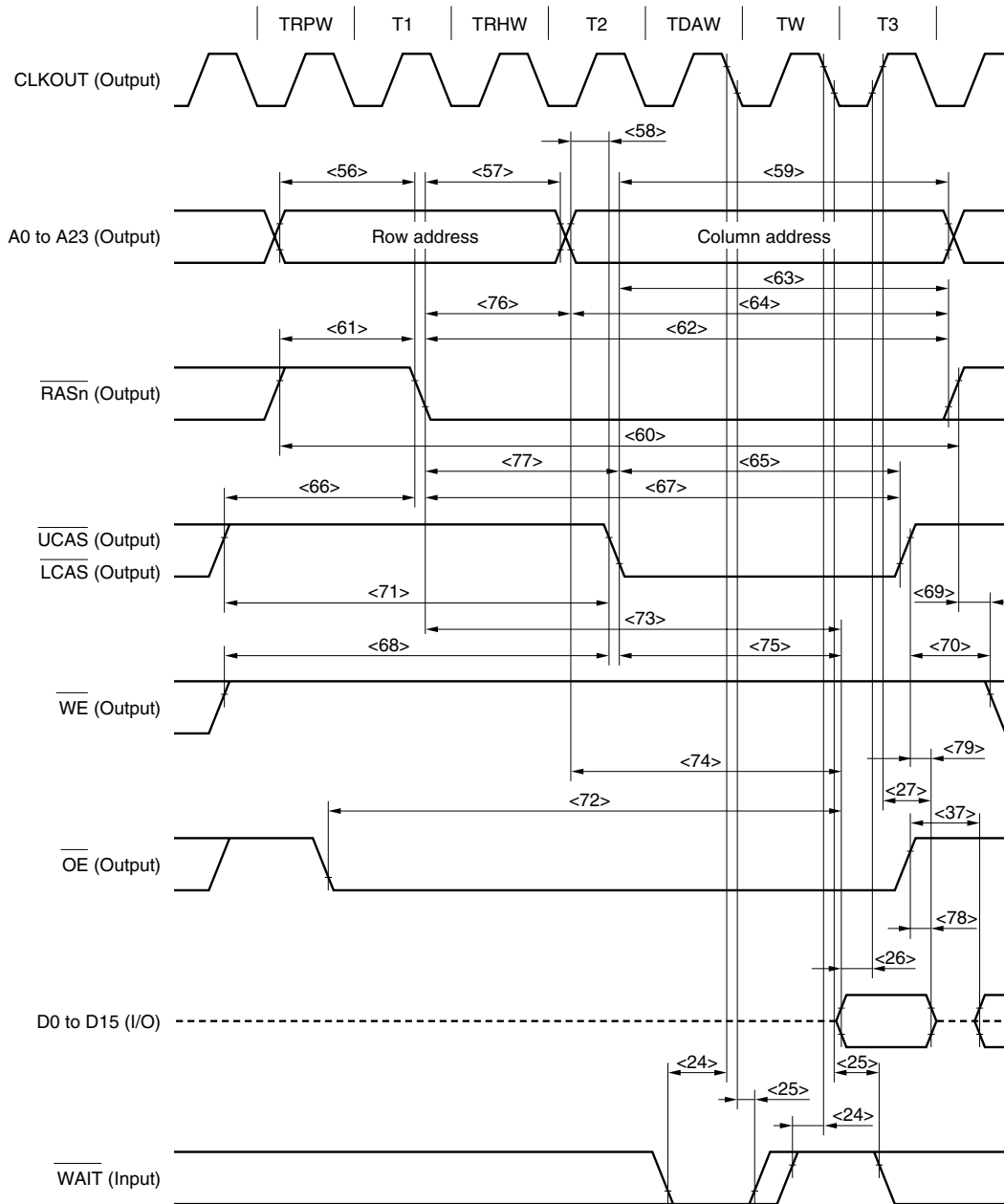
(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RAS}}$ column address delay time	<76>	t_{RAD}		$(0.5 + w_{\text{RH}})T - 10$		ns
$\overline{\text{RAS}}\text{-}\overline{\text{CAS}}$ delay time	<77>	t_{RCD}		$(1 + w_{\text{RH}})T - 10$		ns
Output buffer turn-off delay time (from $\overline{\text{OE}} \uparrow$)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{\text{CAS}} \uparrow$)	<79>	t_{OFF}		0		ns

Remarks 1. $T = t_{\text{CYK}}$

2. w_{RH} : the number of waits due to the RHCxx bit of the DRCn register ($n = 0$ to 3 , $\text{xx} = 00$ to 03 , 10 to 13).

(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



Remarks 1. This is the timing for the following case ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).

Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1

Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1

Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. $n = 0$ to 7

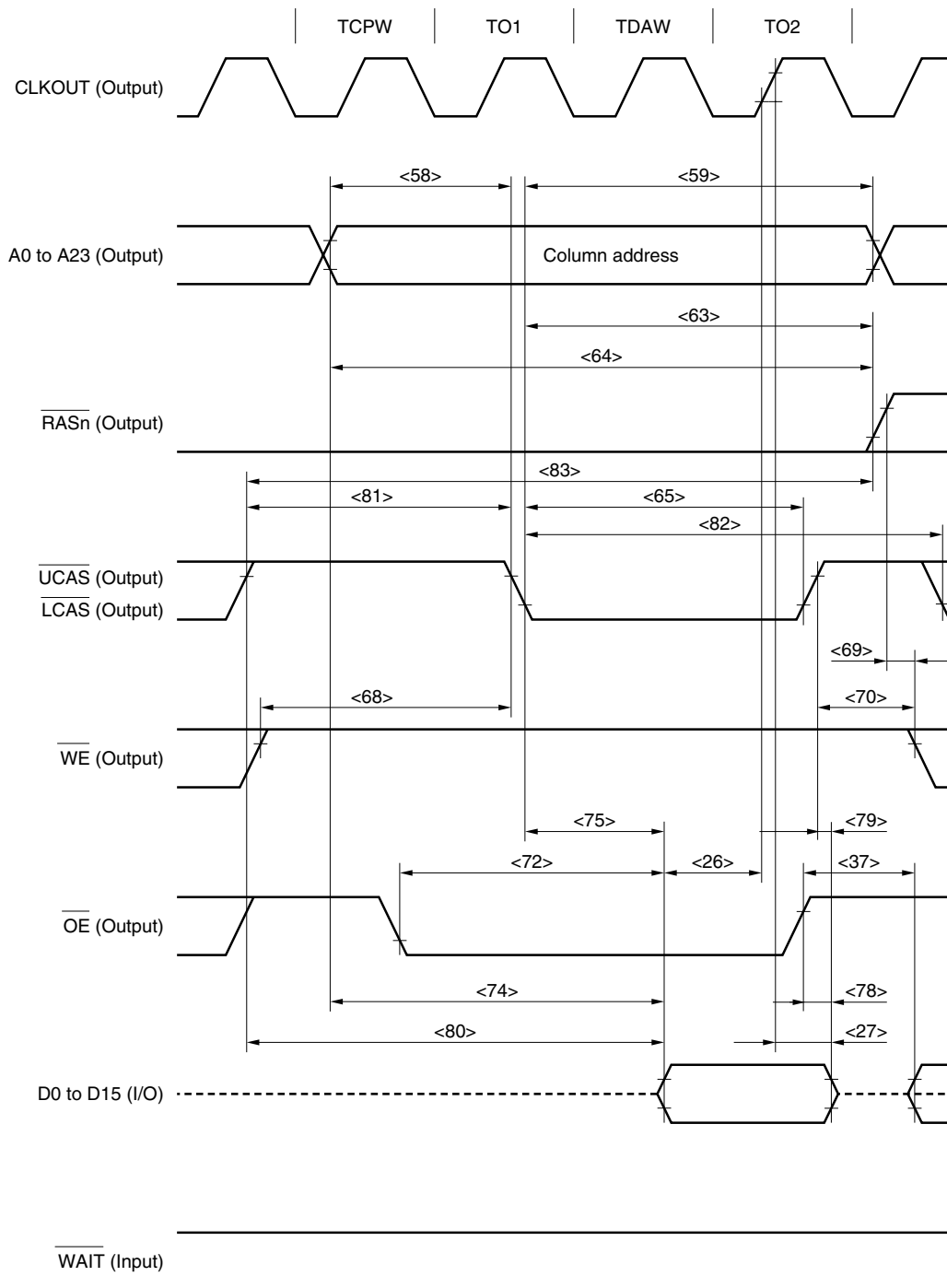
[MEMO]

(b) Read timing (high-speed page DRAM access: on-page) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT $\uparrow$)	<26> t_{SKID}		18		ns
Data input hold time (from CLKOUT $\uparrow$)	<27> t_{HKID}		2		ns
Delay time from $\overline{OE} \uparrow$ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
Column address setup time	<58> t_{ASC}		$(0.5 + W_{CP})T - 10$		ns
Column address hold time	<59> t_{CAH}		$(1.5 + W_{DA})T - 10$		ns
$\overline{RAS}$ hold time	<63> t_{RSH}		$(1.5 + W_{DA})T - 10$		ns
Column address read time for $\overline{RAS}$	<64> t_{RAL}		$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{CAS}$ pulse width	<65> t_{CAS}		$(1 + W_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS} \downarrow$)	<68> t_{RCS}		$(1 + W_{CP})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS} \uparrow$)	<69> t_{RRH}		$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS} \uparrow$)	<70> t_{RCH}		$T - 10$		ns
Output enable access time	<72> t_{OEA}			$(1 + W_{CP} + W_{DA})T - 28$	ns
Access time from column address	<74> t_{AA}			$(1.5 + W_{CP} + W_{DA})T - 28$	ns
$\overline{CAS}$ access time	<75> t_{CAC}			$(1 + W_{DA})T - 28$	ns
Output buffer turn-off delay time (from $\overline{OE} \uparrow$)	<78> t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS} \uparrow$)	<79> t_{OFF}		0		ns
Access time from $\overline{CAS}$ precharge	<80> t_{ACP}			$(2 + W_{CP} + W_{DA})T - 28$	ns
$\overline{CAS}$ precharge time	<81> t_{CP}		$(1 + W_{CP})T - 10$		ns
High-speed page mode cycle time	<82> t_{PC}		$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83> t_{RHCP}		$(2.5 + W_{CP} + W_{DA})T - 10$		ns

Remarks 1. $T = t_{CYK}$ 2. W_{CP} : the number of waits due to the CPC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).3. W_{DA} : the number of waits due to the DAC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).4. i : the number of idle states that are inserted when a write cycle follows a read cycle.

(b) Read timing (high-speed page DRAM access: on-page) (2/2)



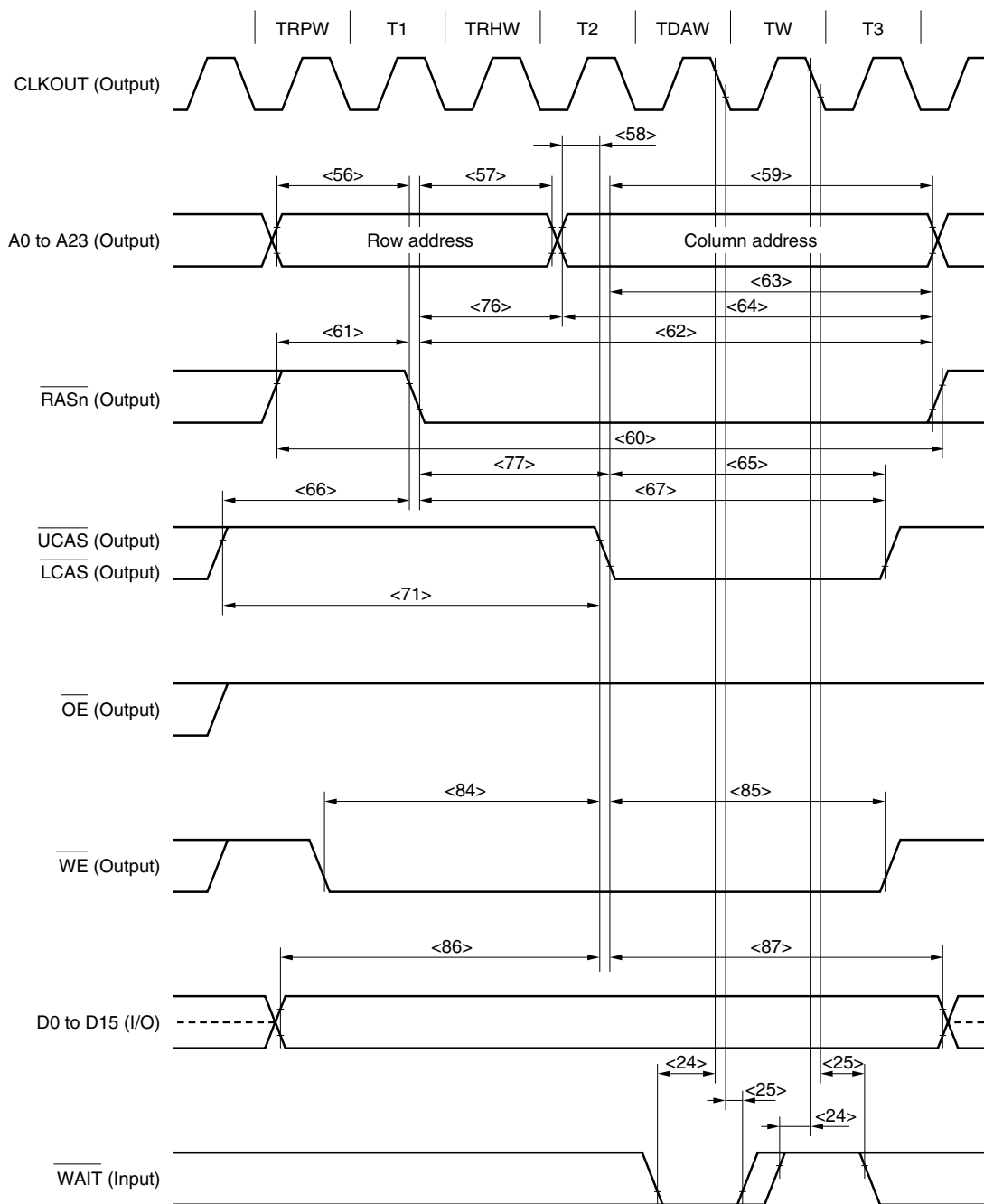
- Remarks**
1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
 2. The broken lines indicate high impedance.
 3. n = 0 to 7

(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT $\downarrow$)	<24> t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT $\downarrow$)	<25> t_{HKW}		2		ns
Row address setup time	<56> t_{ASR}		$(0.5 + W_{\text{RP}})T - 10$		ns
Row address hold time	<57> t_{RAH}		$(0.5 + W_{\text{RH}})T - 10$		ns
Column address setup time	<58> t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59> t_{CAH}		$(1.5 + W_{\text{DA}} + w)T - 10$		ns
Read/write cycle time	<60> t_{RC}		$(3 + W_{\text{RP}} + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61> t_{RP}		$(0.5 + W_{\text{RP}})T - 10$		ns
$\overline{\text{RAS}}$ pulse time	<62> t_{RAS}		$(2.5 + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63> t_{RSH}		$(1.5 + W_{\text{DA}} + w)T - 10$		ns
Column address read time (from $\overline{\text{RAS}}$ $\uparrow$)	<64> t_{RAL}		$(2 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65> t_{CAS}		$(1 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66> t_{CRP}		$(1 + W_{\text{RH}})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67> t_{CSH}		$(2 + W_{\text{RH}} + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71> t_{CPN}		$(2 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
$\overline{\text{RAS}}$ column address delay time	<76> t_{RAD}		$(0.5 + W_{\text{RH}})T - 10$		ns
$\overline{\text{RAS}}$ - $\overline{\text{CAS}}$ delay time	<77> t_{RCD}		$(1 + W_{\text{RH}})T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ $\downarrow$)	<84> t_{WCS}		$(1 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ $\downarrow$)	<85> t_{WCH}		$(1 + W_{\text{DA}} + w)T - 10$		ns
Data setup time (to $\overline{\text{CAS}}$ $\downarrow$)	<86> t_{DS}		$(1.5 + W_{\text{RP}} + W_{\text{RH}})T - 10$		ns
Data hold time (from $\overline{\text{CAS}}$ $\downarrow$)	<87> t_{DH}		$(1.5 + W_{\text{DA}} + w)T - 10$		ns

Remarks 1. $T = t_{\text{CYK}}$ 2. w : the number of waits due to $\overline{\text{WAIT}}$.3. W_{RP} : the number of waits due to the RPCxx bit of the DRCn register ($n = 0$ to 3 , $\text{xx} = 00$ to 03 , 10 to 13).4. W_{RH} : the number of waits due to the RHCxx bit of the DRCn register ($n = 0$ to 3 , $\text{xx} = 00$ to 03 , 10 to 13).5. W_{DA} : the number of waits due to the DACxx bit of the DRCn register ($n = 0$ to 3 , $\text{xx} = 00$ to 03 , 10 to 13).

(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)



Remarks 1. This is the timing for the following case ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).

Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1

Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1

Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

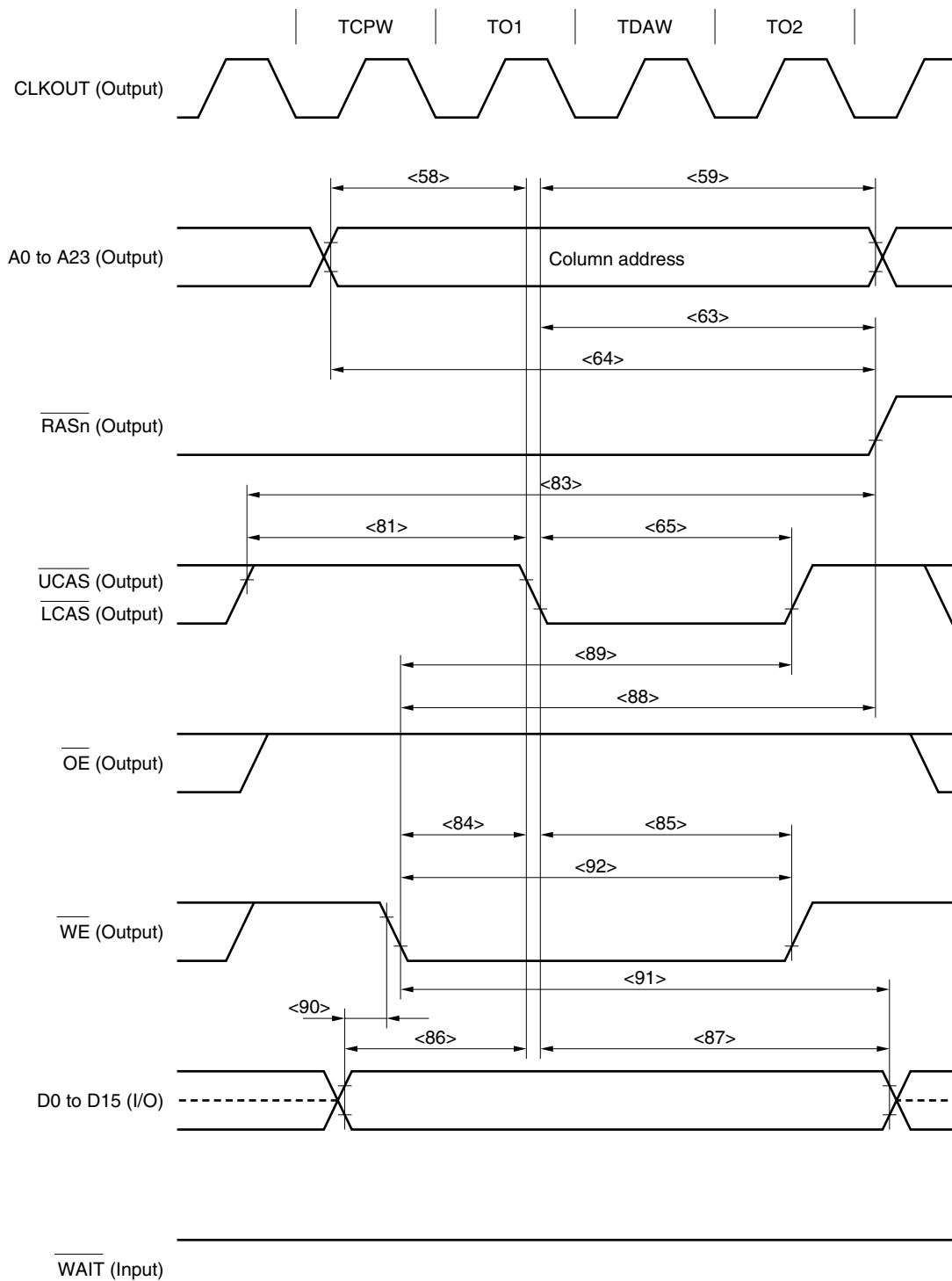
3. $n = 0$ to 7

(d) Write timing (high-speed page DRAM access: on-page) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Column address setup time	<58> t_{ASC}		$(0.5 + W_{CP})T - 10$		ns
Column address hold time	<59> t_{CAH}		$(1.5 + W_{DA})T - 10$		ns
$\overline{RAS}$ hold time	<63> t_{RSH}		$(1.5 + W_{DA})T - 10$		ns
Column address read time (from $\overline{RAS} \uparrow$)	<64> t_{RAL}		$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{CAS}$ pulse width	<65> t_{CAS}		$(1 + W_{DA})T - 10$		ns
$\overline{CAS}$ precharge time	<81> t_{CP}		$(1 + W_{CP})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83> t_{RHCP}		$(2.5 + W_{CP} + W_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS} \downarrow$)	<84> t_{WCS}	$W_{CP} \geq 1$	$W_{CPT} - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS} \downarrow$)	<85> t_{WCH}		$(1 + W_{DA})T - 10$		ns
Data setup time (to $\overline{CAS} \downarrow$)	<86> t_{DS}		$(0.5 + W_{CP})T - 10$		ns
Data hold time (from $\overline{CAS} \downarrow$)	<87> t_{DH}		$(1.5 + W_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS} \uparrow$)	<88> t_{RWL}	$W_{CP} = 0$	$(1.5 + W_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{CAS} \uparrow$)	<89> t_{CWL}	$W_{CP} = 0$	$(1 + W_{DA})T - 10$		ns
Data setup time (to $\overline{WE} \downarrow$)	<90> t_{DSWE}	$W_{CP} = 0$	$0.5T - 10$		ns
Data hold time (from $\overline{WE} \downarrow$)	<91> t_{DHWE}	$W_{CP} = 0$	$(1.5 + W_{DA})T - 10$		ns
$\overline{WE}$ pulse width	<92> t_{WP}	$W_{CP} = 0$	$(1 + W_{DA})T - 10$		ns

Remarks 1. $T = t_{CYK}$ 2. W_{CP} : the number of waits due to the CPCxx bit of the DRCn register ($n = 0$ to 3, xx = 00 to 03, 10 to 13).3. W_{DA} : the number of waits due to the DACxx bit of the DRCn register ($n = 0$ to 3, xx = 00 to 03, 10 to 13).

(d) Write timing (high-speed page DRAM access: on-page) (2/2)



- Remarks**
1. This is the timing for the following case ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
 2. The broken lines indicate high impedance.
 3. $n = 0$ to 7

(e) Read timing (EDO DRAM) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26> t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27> t_{HKID}		2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
Row address setup time	<56> t_{ASR}		$(0.5 + WRP)T - 10$		ns
Row address hold time	<57> t_{RAH}		$(0.5 + WRH)T - 10$		ns
Column address setup time	<58> t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59> t_{CAH}		$(0.5 + WDA)T - 10$		ns
$\overline{RAS}$ precharge time	<61> t_{RP}		$(0.5 + WRP)T - 10$		ns
Column address read time (from $\overline{RAS}$ ↑)	<64> t_{RAL}		$(2 + WCP + WDA)T - 10$		ns
$\overline{CAS}$ -RAS precharge time	<66> t_{CRP}		$(1 + WRP)T - 10$		ns
$\overline{CAS}$ hold time	<67> t_{CSH}		$(1.5 + WRH + WDA)T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<68> t_{RCS}		$(2 + WRP + WRH)T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69> t_{RRH}		$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70> t_{RCH}		$1.5T - 10$		ns
$\overline{RAS}$ access time	<73> t_{RAC}			$(2 + WRH + WDA)T - 28$	ns
Access time from column address	<74> t_{AA}			$(1.5 + WDA)T - 28$	ns
$\overline{CAS}$ access time	<75> t_{CAC}			$(1 + WDA)T - 28$	ns
Delay time from $\overline{RAS}$ to column address	<76> t_{RAD}		$(0.5 + WRH)T - 10$		ns
$\overline{RAS}$ -CAS delay time	<77> t_{RCD}		$(1 + WRH)T - 10$		ns
Output buffer turn-off delay time (from $\overline{OE}$)	<78> t_{OEZ}		0		ns
Access time from $\overline{CAS}$ precharge	<80> t_{ACP}			$(1.5 + WCP + WDA)T - 28$	ns
$\overline{CAS}$ precharge time	<81> t_{CP}		$(0.5 + WCP)T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83> t_{RHCP}		$(2 + WCP + WDA)T - 10$		ns
Read cycle time	<93> t_{HPC}		$(1 + WDA + WCP)T - 10$		ns
$\overline{RAS}$ pulse width	<94> t_{RASP}		$(2.5 + WRH + WDA)T - 10$		ns
$\overline{CAS}$ pulse width	<95> t_{HCAS}		$(0.5 + WDA)T - 10$		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<96> t_{OCH1}		$(2 + WRH + WDA)T - 10$	ns
	On-page	<97> t_{OCH2}		$(0.5 + WDA)T - 10$	ns
Data input hold time (from $\overline{CAS}$ ↓)	<98> t_{DHC}		0		ns

Remarks 1. $T = t_{CYK}$

2. WRP : the number of waits due to the RPC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
3. WRH : the number of waits due to the RHC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
4. WDA : the number of waits due to the DAC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
5. WCP : the number of waits due to the CPC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
6. i : the number of idle states that are inserted when a write cycle follows a read cycle.

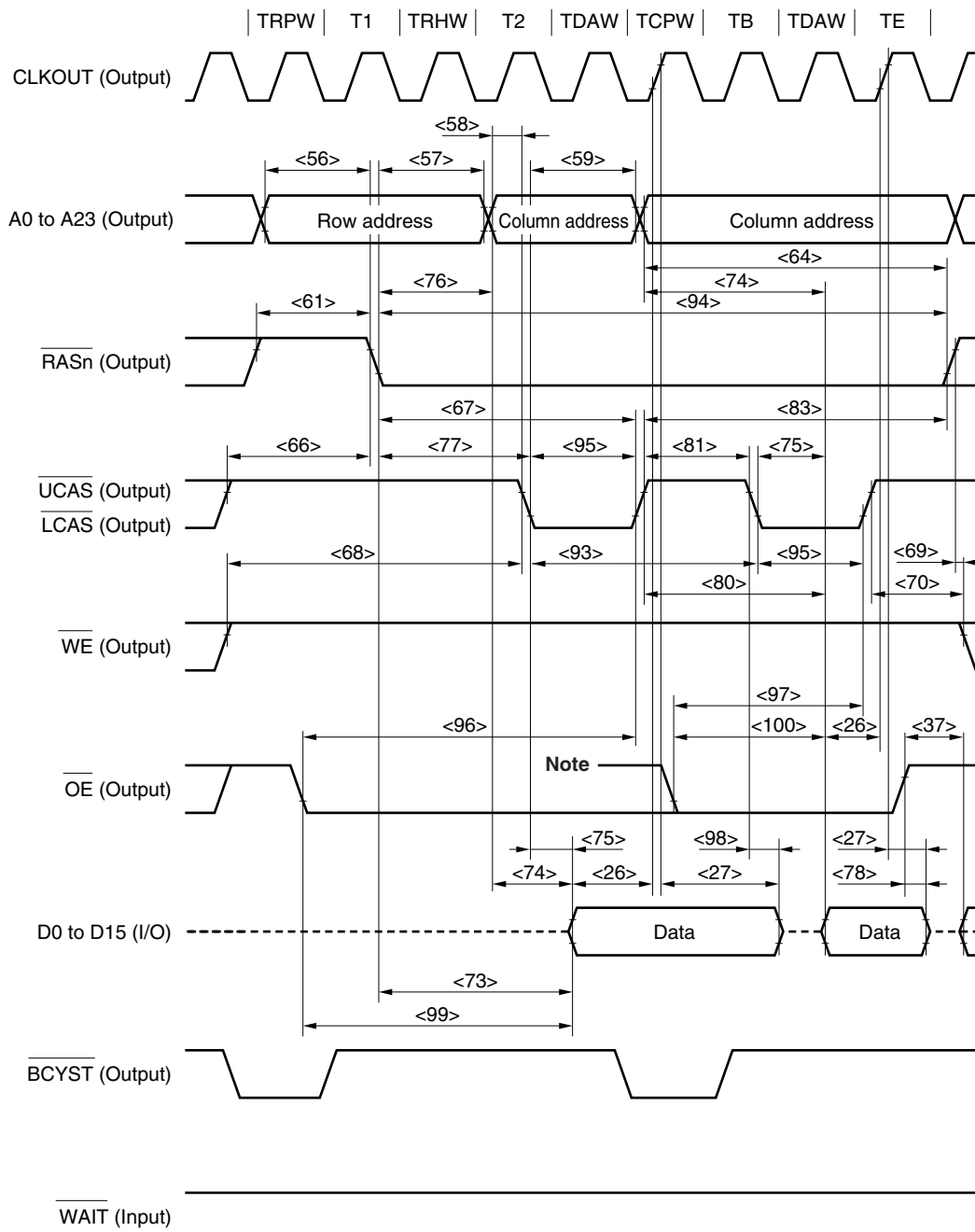
(e) Read timing (EDO DRAM) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	t _{OE1}			$(2 + W_{RP} + W_{RH} + W_{DA})T - 28$	ns
	On-page	<100>	t _{OE2}			$(1 + W_{CP} + W_{DA})T - 28$	ns

Remarks 1. T = t_{CYK}

2. W_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. W_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. W_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. W_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(e) Read timing (EDO DRAM) (3/3)



Note For on-page access from another cycle during the $\overline{\text{RASn}}$ low-level signal.

Remarks 1. This is the timing for the following case ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).

Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1

Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1

Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. $n = 0$ to 7

[MEMO]

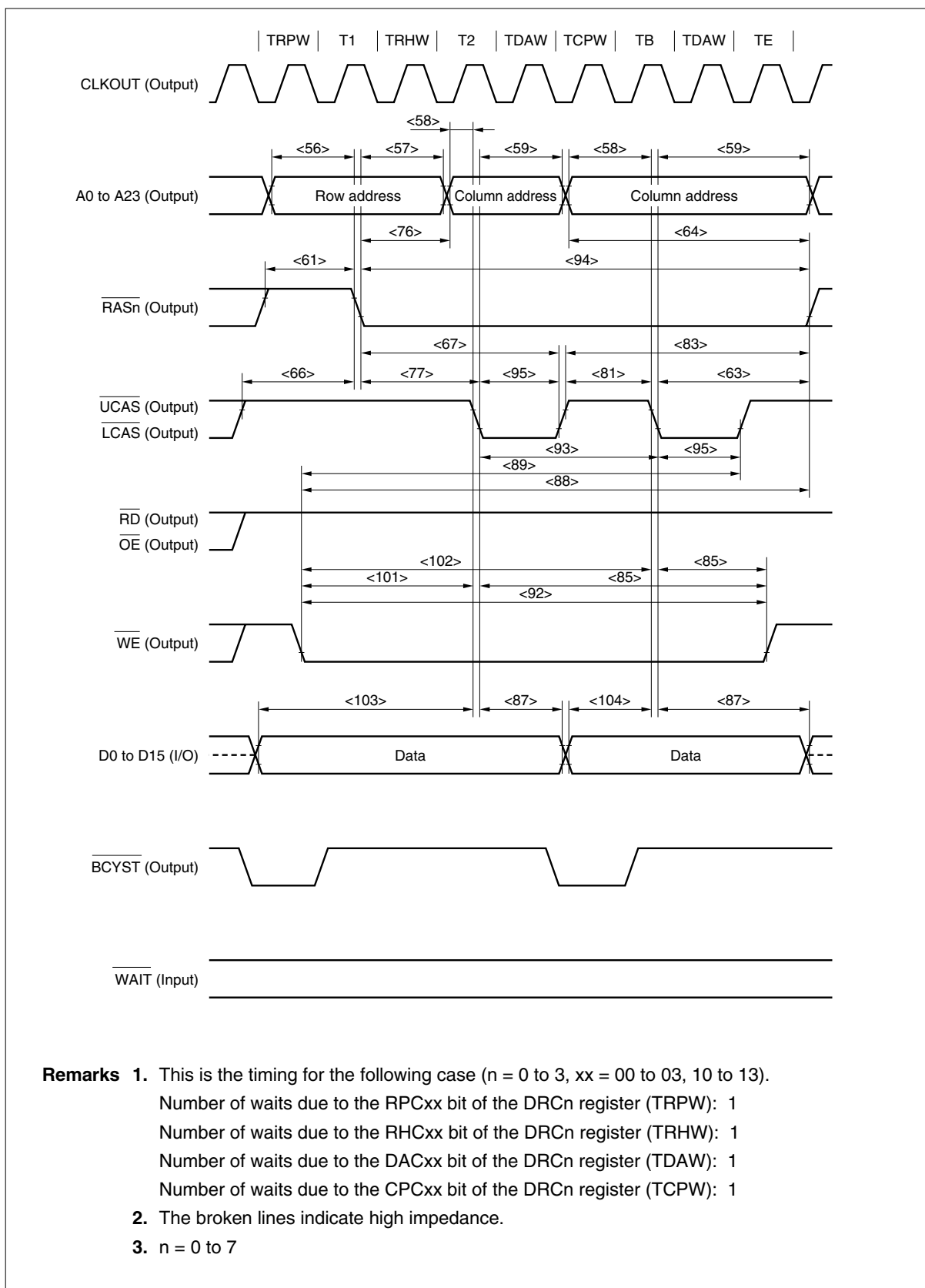
(f) Write timing (EDO DRAM) (1/2)

Parameter		Symbol	Condition	MIN.	MAX.	Unit
Row address setup time		<56>	t_{ASR}	$(0.5 + W_{RP})T - 10$		ns
Row address hold time		<57>	t_{RAH}	$(0.5 + W_{RH})T - 10$		ns
Column address setup time		<58>	t_{ASC}	$0.5T - 10$		ns
Column address hold time		<59>	t_{CAH}	$(0.5 + W_{DA})T - 10$		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}	$(0.5 + W_{RP})T - 10$		ns
$\overline{RAS}$ hold time		<63>	t_{RSH}	$(1.5 + W_{DA})T - 10$		ns
Column address read time (from $\overline{RAS} \uparrow$)		<64>	t_{RAL}	$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{CAS}$ - $\overline{RAS}$ precharge time		<66>	t_{CRP}	$(1 + W_{RP})T - 10$		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}	$(1.5 + W_{RH} + W_{DA})T - 10$		ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}	$(0.5 + W_{RH})T - 10$		ns
$\overline{RAS}$ - $\overline{CAS}$ delay time		<77>	t_{RCD}	$(1 + W_{RH})T - 10$		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}	$(0.5 + W_{CP})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}	$(2 + W_{CP} + W_{DA})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS} \downarrow$)		<85>	t_{WCH}	$(1 + W_{DA})T - 10$		ns
Data hold time (from $\overline{CAS} \downarrow$)		<87>	t_{DH}	$(0.5 + W_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS} \uparrow$)	On-page	<88>	t_{RWL}	$W_{CP} = 0$	$(1.5 + W_{DA})T - 10$	ns
$\overline{WE}$ read time (from $\overline{CAS} \uparrow$)	On-page	<89>	t_{CWL}	$W_{CP} = 0$	$(0.5 + W_{DA})T - 10$	ns
$\overline{WE}$ pulse width	On-page	<92>	t_{WP}	$W_{CP} = 0$	$(1 + W_{DA})T - 10$	ns
Write cycle time		<93>	t_{HPC}		$(1 + W_{DA} + W_{CP})T - 10$	ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + W_{RH} + W_{DA})T - 10$	ns
$\overline{CAS}$ pulse width		<95>	t_{HCAS}		$(0.5 + W_{DA})T - 10$	ns
$\overline{WE}$ setup time (to $\overline{CAS} \downarrow$)	Off-page	<101>	t_{WCS1}		$(1 + W_{RP} + W_{RH})T - 10$	ns
	On-page	<102>	t_{WCS2}	$W_{CP} \geq 1$	$W_{CP}T - 10$	ns
Data setup time (to $\overline{CAS} \downarrow$)	Off-page	<103>	t_{DS1}		$(1.5 + W_{RP} + W_{RH})T - 10$	ns
	On-page	<104>	t_{DS2}		$(0.5 + W_{CP})T - 10$	ns

Remarks 1. $T = t_{CYK}$

2. W_{RP} : the number of waits due to the RPC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
3. W_{RH} : the number of waits due to the RHC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
4. W_{DA} : the number of waits due to the DAC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).
5. W_{CP} : the number of waits due to the CPC_{xx} bit of the DRC_n register ($n = 0$ to 3, $xx = 00$ to 03, 10 to 13).

(f) Write timing (EDO DRAM) (2/2)



(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24> t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25> t_{HKW}		2		ns
Delay time from $\overline{\text{OE}}$ ↑ to data output	<37> t_{DRDOD}		$(0.5 + i)T - 10$		ns
Delay time from address to $\overline{\text{IOWR}}$ ↓	<41> t_{DAWR}		$(0.5 + \text{WRP})T - 10$		ns
Address setup time (to $\overline{\text{IOWR}}$ ↑)	<42> t_{SAWR}		$(2 + \text{WRP} + \text{WRH} + \text{WDA} + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to address	<43> t_{DWRA}		$0.5T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{RD}}$ ↑	<48> t_{DWRD}	$\text{WF} = 0$	0		ns
		$\text{WF} = 1$	$T - 10$		ns
$\overline{\text{IOWR}}$ low-level width	<50> t_{WWRL}		$(2 + \text{WRH} + \text{WDA} + w)T - 10$		ns
Row address setup time	<56> t_{ASR}		$(0.5 + \text{WRP})T - 10$		ns
Row address hold time	<57> t_{RAH}		$(0.5 + \text{WRH})T - 10$		ns
Column address setup time	<58> t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59> t_{CAH}		$(1.5 + \text{WDA} + \text{WF} + w)T - 10$		ns
Read/write cycle time	<60> t_{RC}		$(3 + \text{WRP} + \text{WRH} + \text{WDA} + \text{WF} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61> t_{RP}		$(0.5 + \text{WRP})T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63> t_{RSH}		$(1.5 + \text{WDA} + \text{WF} + w)T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64> t_{RAL}		$(2 + \text{WCP} + \text{WDA} + \text{WF} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65> t_{CAS}		$(1 + \text{WDA} + \text{WF} + w)T - 10$		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66> t_{CRP}		$(1 + \text{WRP})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67> t_{CSH}		$(2 + \text{WRH} + \text{WDA} + \text{WF} + w)T - 10$		ns

Remarks 1. $T = t_{\text{CYK}}$ 2. w : the number of waits due to $\overline{\text{WAIT}}$.3. WRP : the number of waits due to the RPCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).4. WRH : the number of waits due to the RHCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).5. WDA : the number of waits due to the DACxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).6. WCP : the number of waits due to the CPCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).7. WF : the number of waits that are inserted for a source-side access during a DMA flyby transfer.8. i : the number of idle states that are inserted when a write cycle follows a read cycle.

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Symbol	Condition	MIN.	MAX.	Unit
$\overline{WE}$ setup time (to $\overline{CAS} \downarrow$)		<68>	t_{RCS}	$(2 + W_{RP} + W_{RH})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS} \uparrow$)		<69>	t_{RRH}	$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS} \uparrow$)		<70>	t_{RCH}	$1.5T - 10$		ns
$\overline{CAS}$ precharge time		<71>	t_{CPN}	$(2 + W_{RP} + W_{RH})T - 10$		ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}	$(0.5 + W_{RH})T - 10$		ns
$\overline{RAS}$ - $\overline{CAS}$ delay time		<77>	t_{RCD}	$(1 + W_{RH})T - 10$		ns
Output buffer turn-off delay time (from $\overline{OE} \uparrow$)		<78>	t_{OEZ}	0		ns
Output buffer turn-off delay time (from $\overline{CAS} \uparrow$)		<79>	t_{OFF}	0		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}	$(0.5 + W_{CP})T - 10$		ns
High-speed page mode cycle time		<82>	t_{PC}	$(2 + W_{CP} + W_{DA} + W_F + w)T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}	$(2.5 + W_{CP} + W_{DA} + W_F + w)T - 10$		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}	$(2.5 + W_{RH} + W_{DA} + W_F + w)T - 10$		ns
$\overline{CAS}$ hold time from $\overline{OE}$ (from $\overline{CAS} \uparrow$)	Off-page	<96>	t_{OCH1}	$(2.5 + W_{RP} + W_{RH} + W_{DA} + W_F + w)T - 10$		ns
	On-page	<97>	t_{OCH2}	$(1.5 + W_{CP} + W_{DA} + W_F + w)T - 10$		ns
Delay time from $\overline{DMAAKm} \downarrow$ to $\overline{CAS} \downarrow$		<105>	t_{DDACS}	$(1.5 + W_{RH})T - 10$		ns
Delay time from $\overline{IOWR} \downarrow$ to $\overline{CAS} \downarrow$		<106>	t_{DRDCS}	$(1 + W_{RH})T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w : the number of waits due to $\overline{WAIT}$.

3. W_{CP} : the number of waits due to the $CPCxx$ bit of the $DRCn$ register ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).

4. W_{DA} : the number of waits due to the $DACxx$ bit of the $DRCn$ register ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).

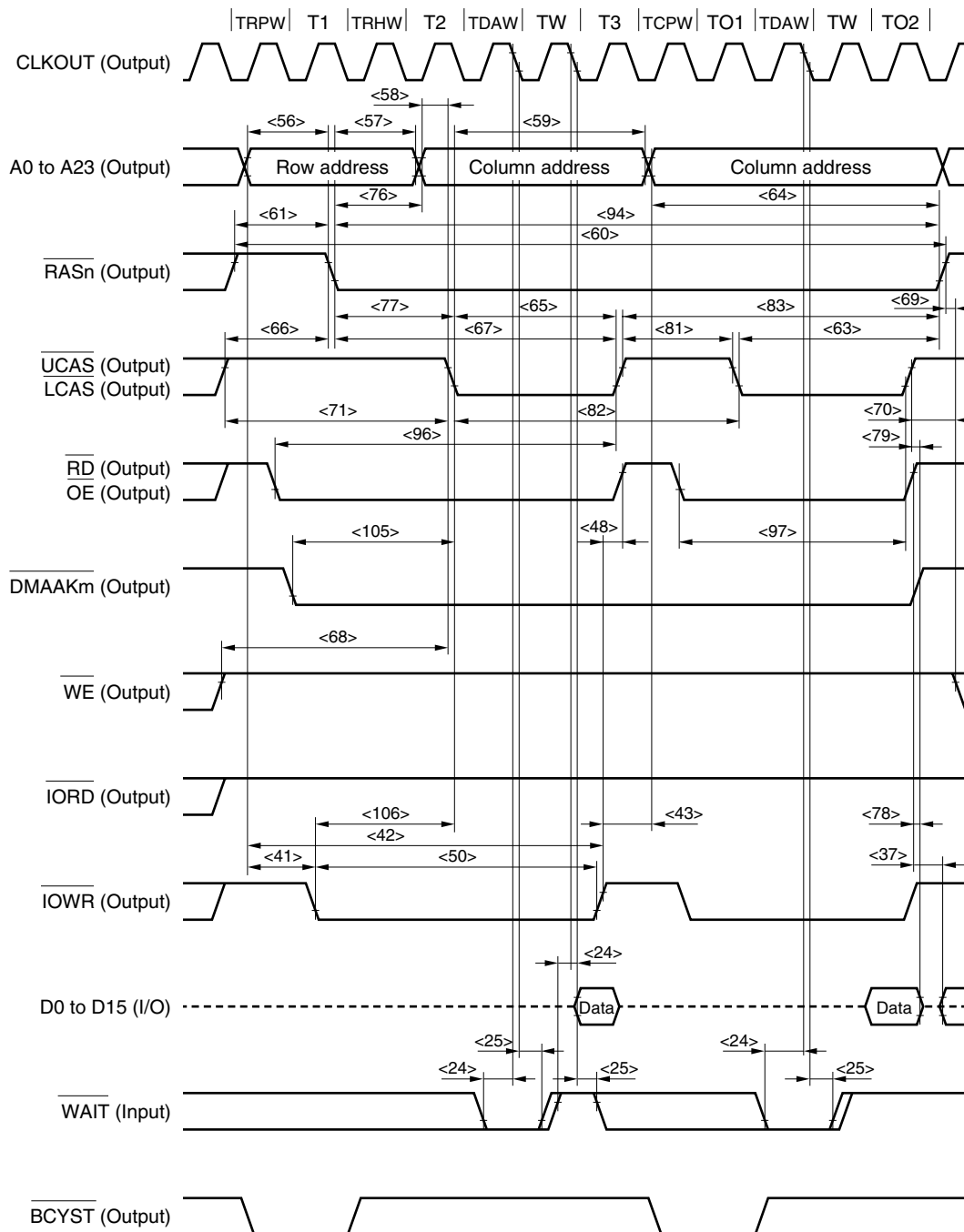
5. W_{RH} : the number of waits due to the $RHCxx$ bit of the $DRCn$ register ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).

6. W_{RP} : the number of waits due to the $RPCxx$ bit of the $DRCn$ register ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).

7. w_F : the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. $m = 0$ to 3

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)



- Remarks**
- This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
 Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
 Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
 Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0
 - The broken lines indicate high impedance.
 - n = 0 to 7, m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t _{SWK}	15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t _{HKW}	2		ns
$\overline{\text{IORD}}$ low-level width	<32>	t _{WRDL}	$(2 + \text{WRH} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33>	t _{WRDH}	$\text{T} - 10$		ns
Delay time from address to $\overline{\text{IORD}}$ ↑	<34>	t _{DARD}	$0.5\text{T} - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<35>	t _{DRDA}	$(0.5 + \text{i})\text{T} - 10$		ns
Row address setup time	<56>	t _{ASR}	$(0.5 + \text{WRP})\text{T} - 10$		ns
Row address hold time	<57>	t _{RAH}	$(0.5 + \text{WRH})\text{T} - 10$		ns
Column address setup time	<58>	t _{ASC}	$0.5\text{T} - 10$		ns
Column address hold time	<59>	t _{CAH}	$(1.5 + \text{WDA} + \text{WF})\text{T} - 10$		ns
Read/write cycle time	<60>	t _{RC}	$(3 + \text{WRP} + \text{WRH} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	t _{RP}	$(0.5 + \text{WRP})\text{T} - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t _{RSH}	$(1.5 + \text{WDA} + \text{WF})\text{T} - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64>	t _{RAL}	$(2 + \text{WCP} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t _{CAS}	$(1 + \text{WDA} + \text{WF})\text{T} - 10$		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66>	t _{CRP}	$(1 + \text{WRP})\text{T} - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	t _{CSH}	$(2 + \text{WRH} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71>	t _{CPN}	$(2 + \text{WRP} + \text{WRH} + \text{w})\text{T} - 10$		ns
Delay time from $\overline{\text{RAS}}$ to column address	<76>	t _{RAD}	$(0.5 + \text{WRH})\text{T} - 10$		ns
$\overline{\text{RAS}}$ - $\overline{\text{CAS}}$ delay time	<77>	t _{RCD}	$(1 + \text{WRH} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ precharge time	<81>	t _{CP}	$(0.5 + \text{WCP} + \text{w})\text{T} - 10$		ns
High-speed page mode cycle time	<82>	t _{PC}	$(2 + \text{WCP} + \text{WDA} + \text{WF} + \text{w})\text{T} - 10$		ns
$\overline{\text{RAS}}$ hold time for $\overline{\text{CAS}}$ precharge	<83>	t _{RHCP}	$(2.5 + \text{WCP} + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↓)	<85>	t _{WCH}	$(1 + \text{WDA})\text{T} - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{RAS}}$ ↑)	<88>	t _{RWL}	$\text{WCP} = 0$ $(1.5 + \text{WDA} + \text{w})\text{T} - 10$		ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{\text{WAIT}}$.

3. WRH: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. WDA: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. WRP: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. WCP: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. wf: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. i: the number of idle states that are inserted when a write cycle follows a read cycle.

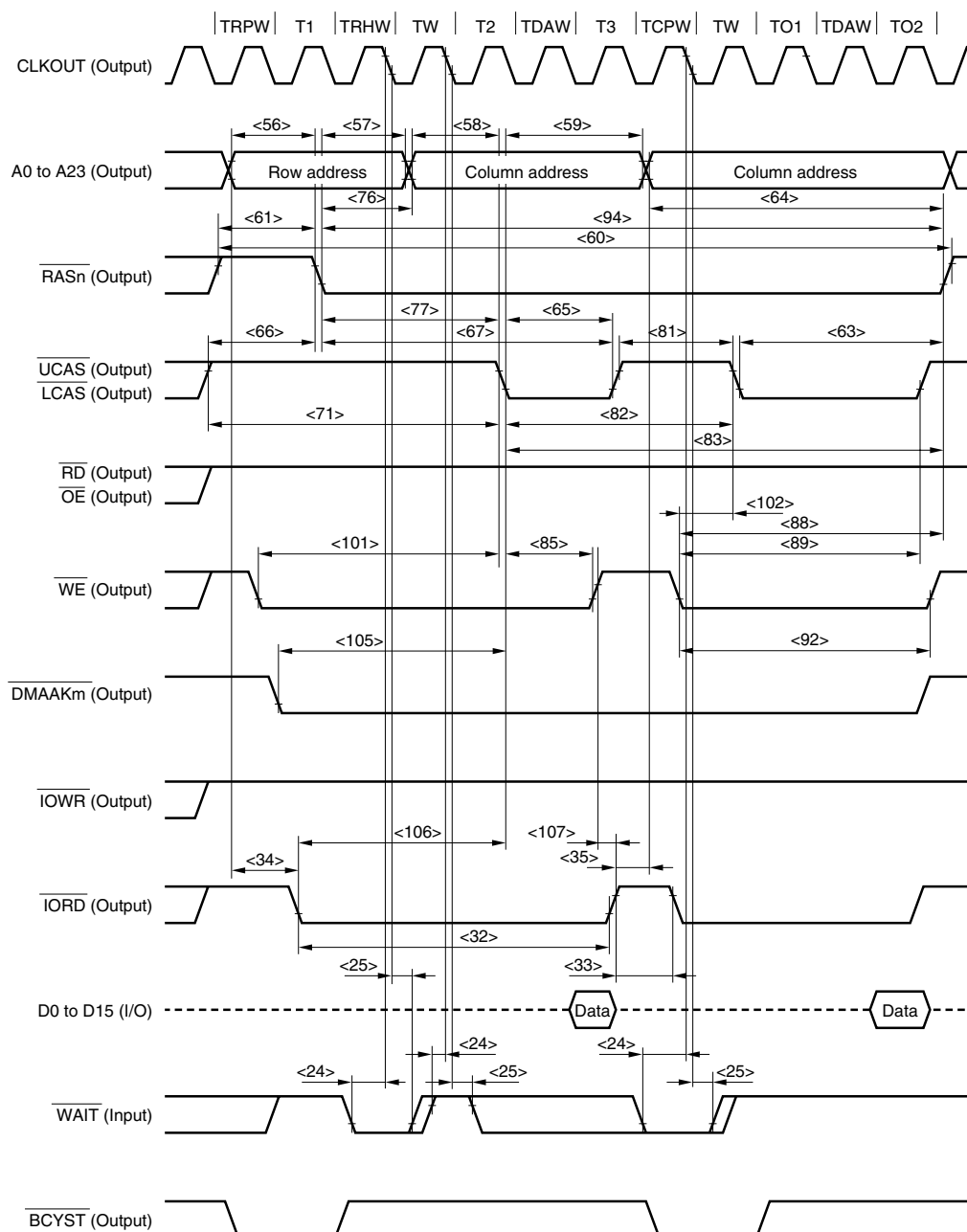
9. n = 0 to 7

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

Parameter		Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WE}}$ read time (from $\overline{\text{CAS}} \uparrow$)		<89> t_{CWL}	$W_{\text{CP}} = 0$	$(1 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{WE}}$ pulse width		<92> t_{WP}	$W_{\text{CP}} = 0$	$(1 + W_{\text{DA}} + w)T - 10$		ns
$\overline{\text{RAS}}$ pulse width		<94> t_{RASP}		$(2.5 + W_{\text{RH}} + W_{\text{DA}} + W_{\text{F}} + w)T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}} \downarrow$)	Off-page	<101> t_{WCS1}	$W_{\text{CP}} = 0$	$(1 + W_{\text{RH}} + W_{\text{RP}} + w)T - 10$		ns
	On-page	<102> t_{WCS2}	$W_{\text{CP}} \geq 1$	$W_{\text{CP}}T - 10$		ns
Delay time from $\overline{\text{DMAAKm}} \downarrow$ to $\overline{\text{CAS}} \downarrow$		<105> t_{DDACS}		$(1.5 + W_{\text{RH}} + w)T - 10$		ns
Delay time from $\overline{\text{IORD}} \downarrow$ to $\overline{\text{CAS}} \downarrow$		<106> t_{DRDCS}		$(1 + W_{\text{RH}} + w)T - 10$		ns
Delay time from $\overline{\text{WE}} \uparrow$ to $\overline{\text{IORD}} \uparrow$		<107> t_{DWERD}	$W_{\text{F}} = 0$	0		ns
			$W_{\text{F}} = 1$	$T - 10$		ns

Remarks 1. $T = t_{\text{CYK}}$ 2. w : the number of waits due to $\overline{\text{WAIT}}$.3. W_{RH} : the number of waits due to the RHCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).4. W_{DA} : the number of waits due to the DACxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).5. W_{RP} : the number of waits due to the RPCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).6. W_{CP} : the number of waits due to the CPCxx bit of the DRCn register ($n = 0$ to 3, $\text{xx} = 00$ to 03, 10 to 13).7. W_{F} : the number of waits that are inserted for a source-side access during a DMA flyby transfer.8. $m = 0$ to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)



- Remarks**
- This is the timing for the following case ($n = 0$ to 3 , $xx = 00$ to 03 , 10 to 13).
 Number of waits due to the $RPCxx$ bit of the $DRCn$ register ($TRPW$): 1
 Number of waits due to the $RHCxx$ bit of the $DRCn$ register ($TRHW$): 1
 Number of waits due to the $DACxx$ bit of the $DRCn$ register ($TDAW$): 1
 Number of waits due to the $CPCxx$ bit of the $DRCn$ register ($TCPW$): 1
 Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0
 - The broken lines indicate high impedance.
 - $n = 0$ to 7 , $m = 0$ to 3

(i) CBR refresh timing

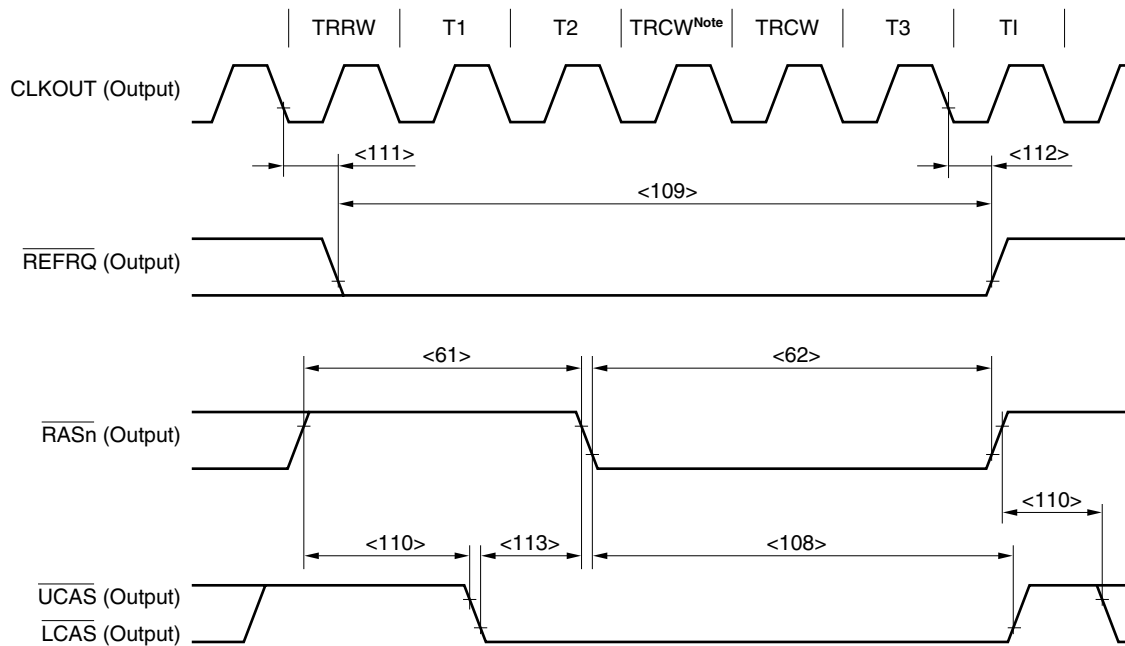
Parameter	Symbol	Condition	MIN.	MAX.	Unit
RAS precharge time	<61> t_{RP}		$(1.5 + W_{RRW})T - 10$		ns
RAS pulse width	<62> t_{RAS}		$(1.5 + W_{RCW}^{Note})T - 10$		ns
CAS hold time	<108> t_{CHR}		$(1.5 + W_{RCW}^{Note})T - 10$		ns
REFRQ pulse width	<109> t_{WRFL}		$(3 + W_{RRW} + W_{RCW}^{Note})T - 10$		ns
RAS precharge CAS hold time	<110> t_{RPC}		$(0.5 + W_{RRW})T - 10$		ns
REFRQ active delay time (from CLKOUT ↓)	<111> t_{DKRF}		2	10	ns
REFRQ inactive delay time (from CLKOUT ↓)	<112> t_{HKRF}		2	10	ns
CAS setup time	<113> t_{CSR}		$T - 10$		ns

Note At least one clock cycle is inserted by default for w_{rcw} regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. $T = t_{CYK}$

2. w_{RRW} : the number of waits due to the RRW0 and RRW1 bits of the RWC register.

3. w_{RCW} : the number of waits due to the RCW0 to RCW2 bits of the RWC register.



Note This TRCW is always inserted regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. This is the timing for the following case.

Number of waits due to the RRW0 and RRW1 bits of the RWC register ($TRRW$): 1

Number of waits due to the RCW0 to RCW2 bits of the RWC register ($TRCW$): 2

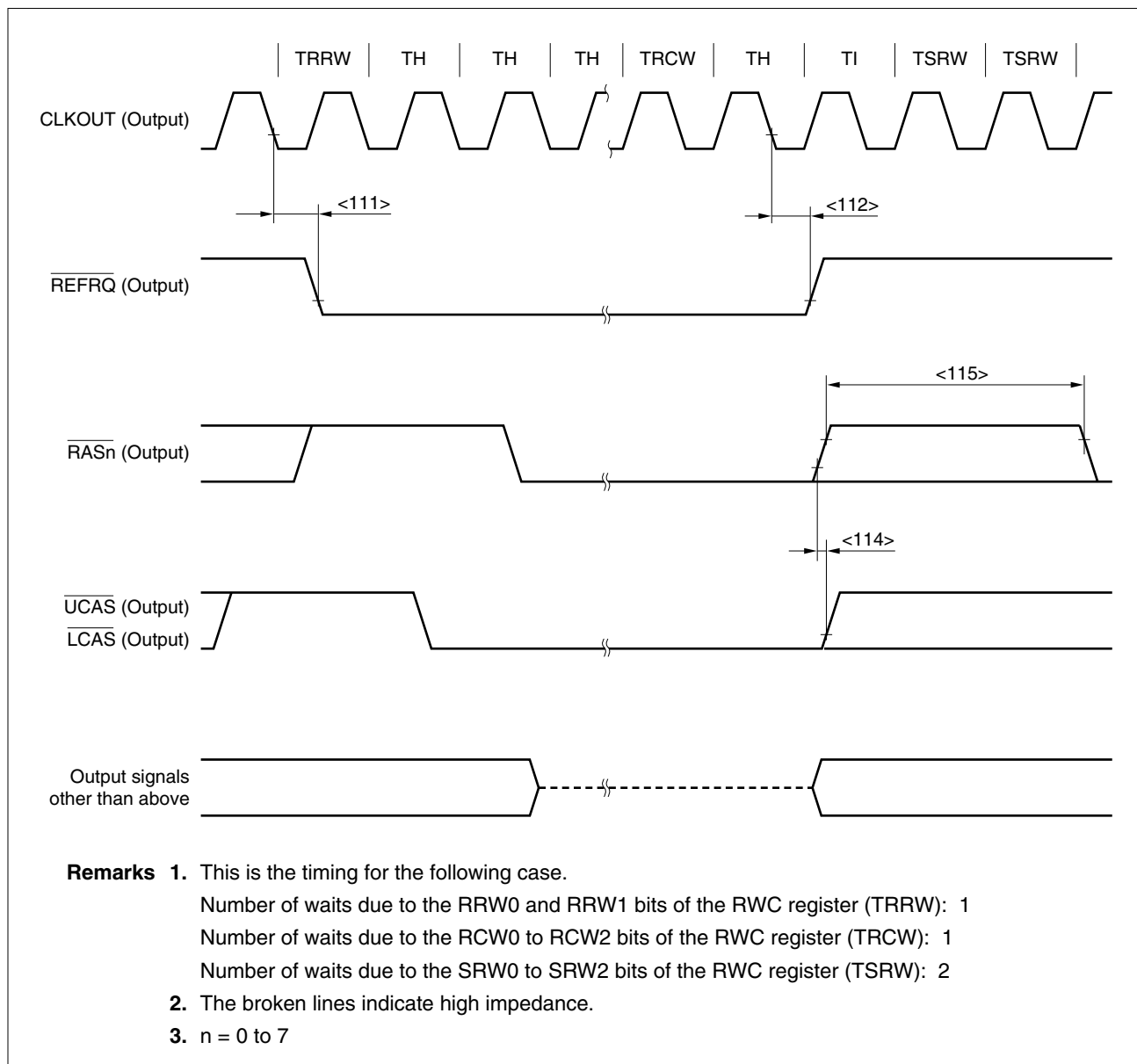
2. $n = 0$ to 7

(j) CBR self-refresh timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT $\downarrow$)	<111>	t_{DKRF}	2	10	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT $\downarrow$)	<112>	t_{HKRF}	2	10	ns
$\overline{\text{CAS}}$ hold time	<114>	t_{CHS}	-5		ns
RAS precharge time	<115>	t_{RPS}	$(1 + 2W_{\text{SRW}})T - 10$		ns

Remarks 1. $T = t_{\text{CYK}}$

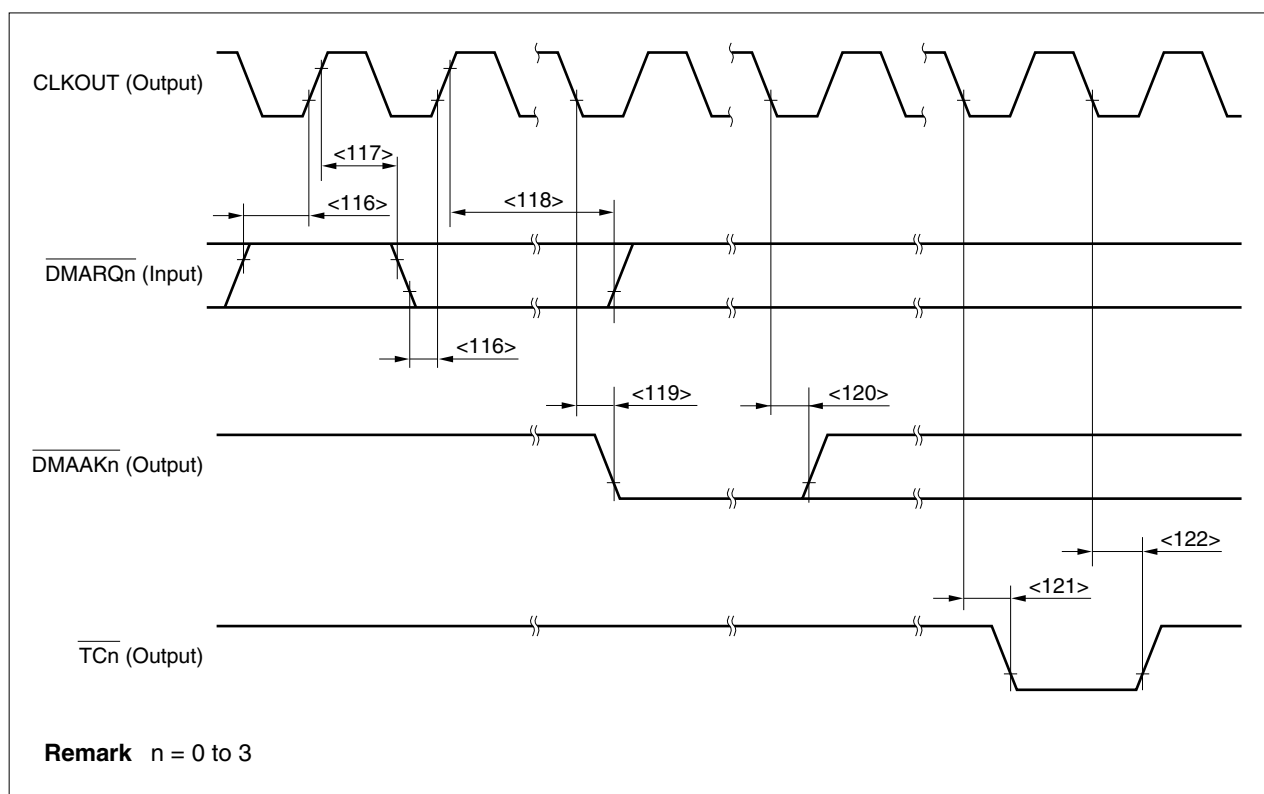
2. W_{SRW} : the number of waits due to the SRW0 to SRW2 bits of the RWC register.



(7) DMAC timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{DMARQ}}_n$ setup time (to CLKOUT ↑)	<116> t_{SDRK}		15		ns
$\overline{\text{DMARQ}}_n$ hold time (from CLKOUT ↑)	<117> t_{HKDR1}		2		ns
	<118> t_{HKDR2}		Until $\overline{\text{DMAAK}}_n \downarrow$		ns
$\overline{\text{DMAAK}}_n$ output delay time (from CLKOUT ↓)	<119> t_{DKDA}		2	10	ns
$\overline{\text{DMAAK}}_n$ output hold time (from CLKOUT ↓)	<120> t_{HKDA}		2	10	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT ↓)	<121> t_{DKTC}		2	10	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT ↓)	<122> t_{HKTC}		2	10	ns

Remark n = 0 to 3



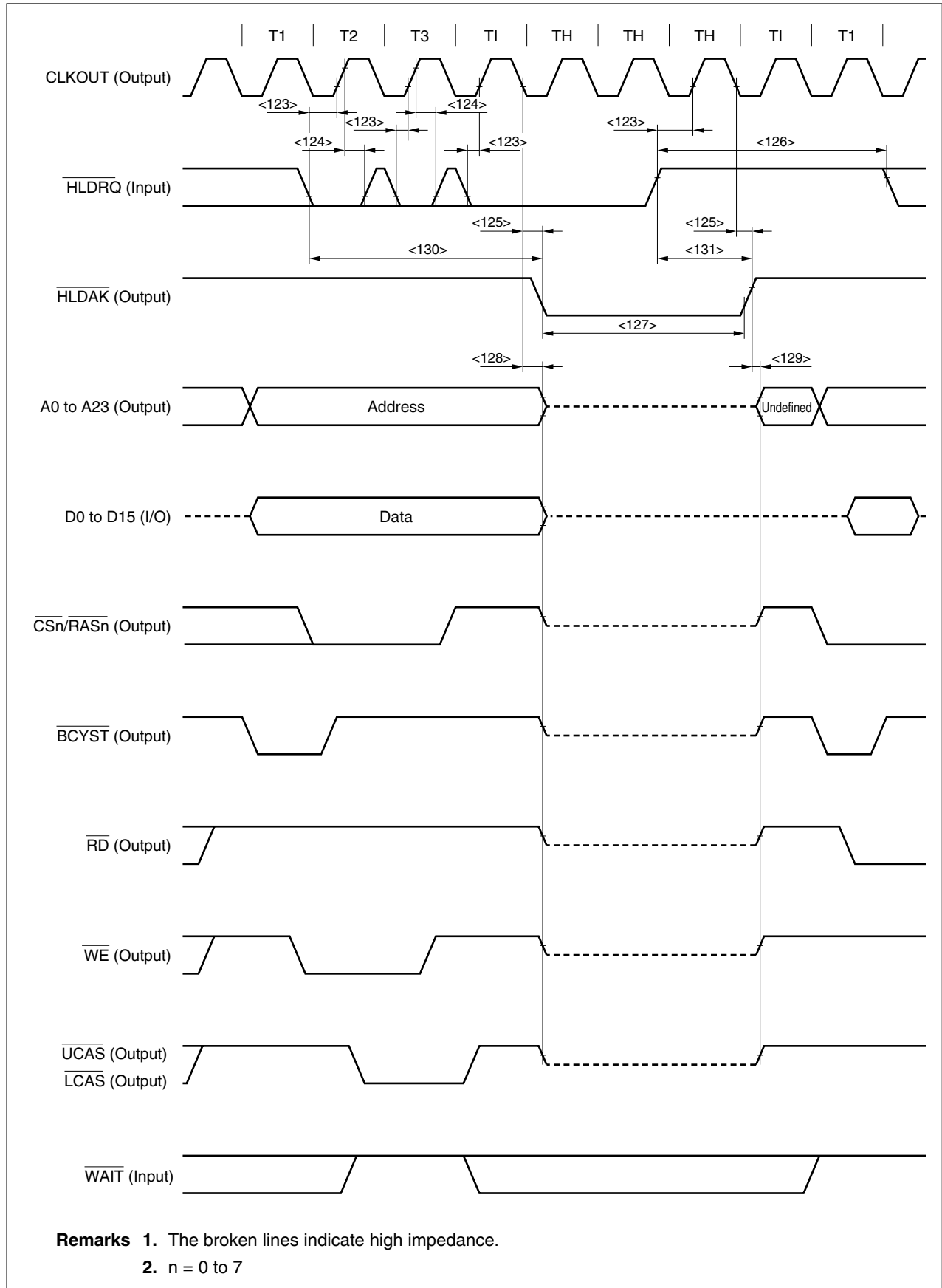
[MEMO]

(8) Bus hold timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT $\uparrow$)	<123>	t_{SHRK}		15		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT $\uparrow$)	<124>	t_{HKHR}		2		ns
Delay time from CLKOUT $\downarrow$ to $\overline{\text{HLD\!A\!K}}$	<125>	t_{DKHA}		2	10	ns
$\overline{\text{HLDRQ}}$ high-level width	<126>	t_{WHQH}		$T + 17$		ns
$\overline{\text{HLD\!A\!K}}$ low-level width	<127>	t_{WHAL}		$T - 8$		ns
Delay time from $\overline{\text{CLKOUT}} \downarrow$ to bus float	<128>	t_{DKCF}			10	ns
Delay time from $\overline{\text{HLD\!A\!K}} \uparrow$ to bus output	<129>	t_{DHAC}		0		ns
Delay time from $\overline{\text{HLDRQ}} \downarrow$ to $\overline{\text{HLD\!A\!K}} \downarrow$	<130>	t_{DHQHA1}		2.5T		ns
Delay time from $\overline{\text{HLDRQ}} \uparrow$ to $\overline{\text{HLD\!A\!K}} \uparrow$	<131>	t_{DHQHA2}		0.5T	1.5T	ns

Remark T = t_{CYK}

(8) Bus hold timing (2/2)

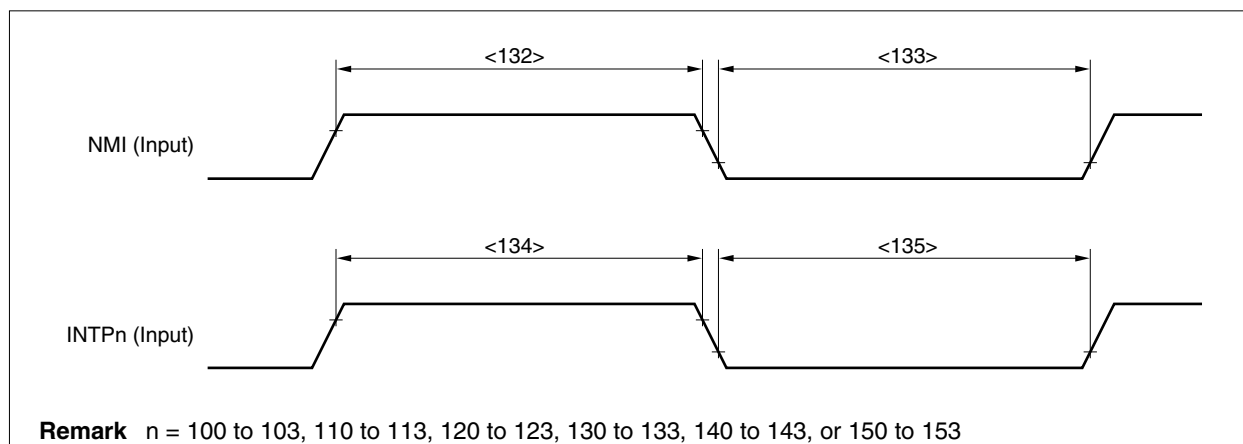


(9) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<132>	t_{WNIH}		500		ns
NMI low-level width	<133>	t_{WNIL}		500		ns
INTPn high-level width	<134>	t_{WITH}		$4T + 10$		ns
INTPn low-level width	<135>	t_{WITL}		$4T + 10$		ns

Remarks 1. $n = 100$ to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153

2. $T = t_{CYK}$

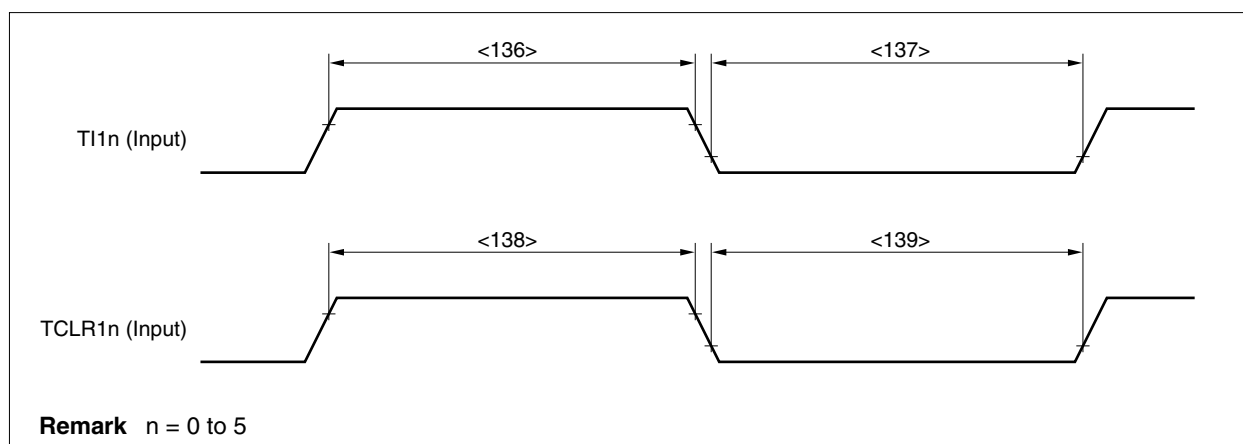


(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1n high-level width	<136>	t_{WTIH}		$3T + 18$		ns
TI1n low-level width	<137>	t_{WTIL}		$3T + 18$		ns
TCLR1n high-level width	<138>	t_{WTCH}		$3T + 18$		ns
TCLR1n low-level width	<139>	t_{WTCL}		$3T + 18$		ns

Remarks 1. $n = 0$ to 5

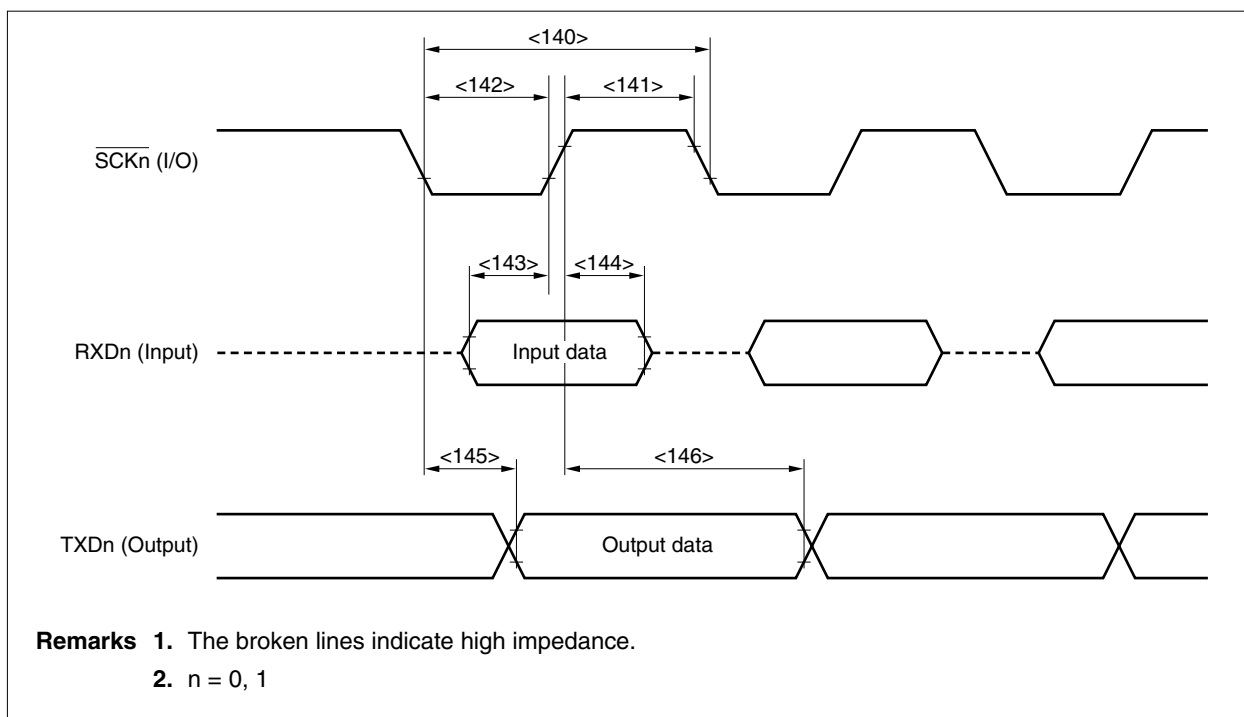
2. $T = t_{CYK}$



(11) UART0, UART1 timing (clock-synchronized or master mode only)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<140>	t_{CYSK0}	Output	250	ns
$\overline{\text{SCKn}}$ high-level width	<141>	t_{WSK0H}	Output	$0.5t_{\text{CYSK0}} - 20$	ns
$\overline{\text{SCKn}}$ low-level width	<142>	t_{WSK0L}	Output	$0.5t_{\text{CYSK0}} - 20$	ns
RxDn setup time (to $\overline{\text{SCKn}} \uparrow$)	<143>	t_{SRXSK}		30	ns
RxDn hold time (from $\overline{\text{SCKn}} \uparrow$)	<144>	t_{HSKRX}		0	ns
TxDn output delay time (from $\overline{\text{SCKn}} \downarrow$)	<145>	t_{DSKTX}		20	ns
TxDn output hold time (from $\overline{\text{SCKn}} \uparrow$)	<146>	t_{HSKTX}		$0.5t_{\text{CYSK0}} - 5$	ns

Remark n = 0, 1



(12) CSI0 to CSI3 timing

(a) Master mode

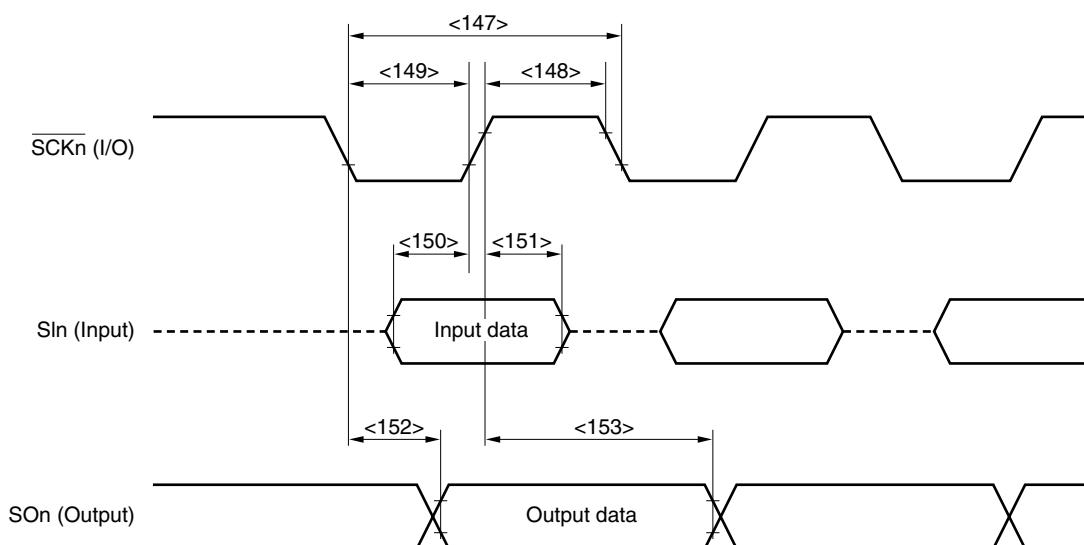
Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<147> t_{CYSK1}	Output	100		ns
$\overline{\text{SCKn}}$ high-level width	<148> t_{WSK1H}	Output	$0.5t_{\text{CYSK1}} - 20$		ns
$\overline{\text{SCKn}}$ low-level width	<149> t_{WSK1L}	Output	$0.5t_{\text{CYSK1}} - 20$		ns
SIn setup time (to $\overline{\text{SCKn}} \uparrow$)	<150> t_{SSISK}		30		ns
SIn hold time (from $\overline{\text{SCKn}} \uparrow$)	<151> t_{HSKSI}		0		ns
SOn output delay time (from $\overline{\text{SCKn}} \downarrow$)	<152> t_{DSKSO}			20	ns
SOn output hold time (from $\overline{\text{SCKn}} \uparrow$)	<153> t_{HSKSO}		$0.5t_{\text{CYSK1}} - 5$		ns

Remark n = 0 to 3

(b) Slave mode

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<147> t_{CYSK1}	Input	100		ns
$\overline{\text{SCKn}}$ high-level width	<148> t_{WSK1H}	Input	30		ns
$\overline{\text{SCKn}}$ low-level width	<149> t_{WSK1L}	Input	30		ns
SIn setup time (to $\overline{\text{SCKn}} \uparrow$)	<150> t_{SSISK}		10		ns
SIn hold time (from $\overline{\text{SCKn}} \uparrow$)	<151> t_{HSKSI}		10		ns
SOn output delay time (from $\overline{\text{SCKn}} \downarrow$)	<152> t_{DSKSO}			30	ns
SOn output hold time (from $\overline{\text{SCKn}} \uparrow$)	<153> t_{HSKSO}		t_{WSK1H}		ns

Remark n = 0 to 3



Remarks 1. The broken lines indicate high impedance.

2. n = 0 to 3

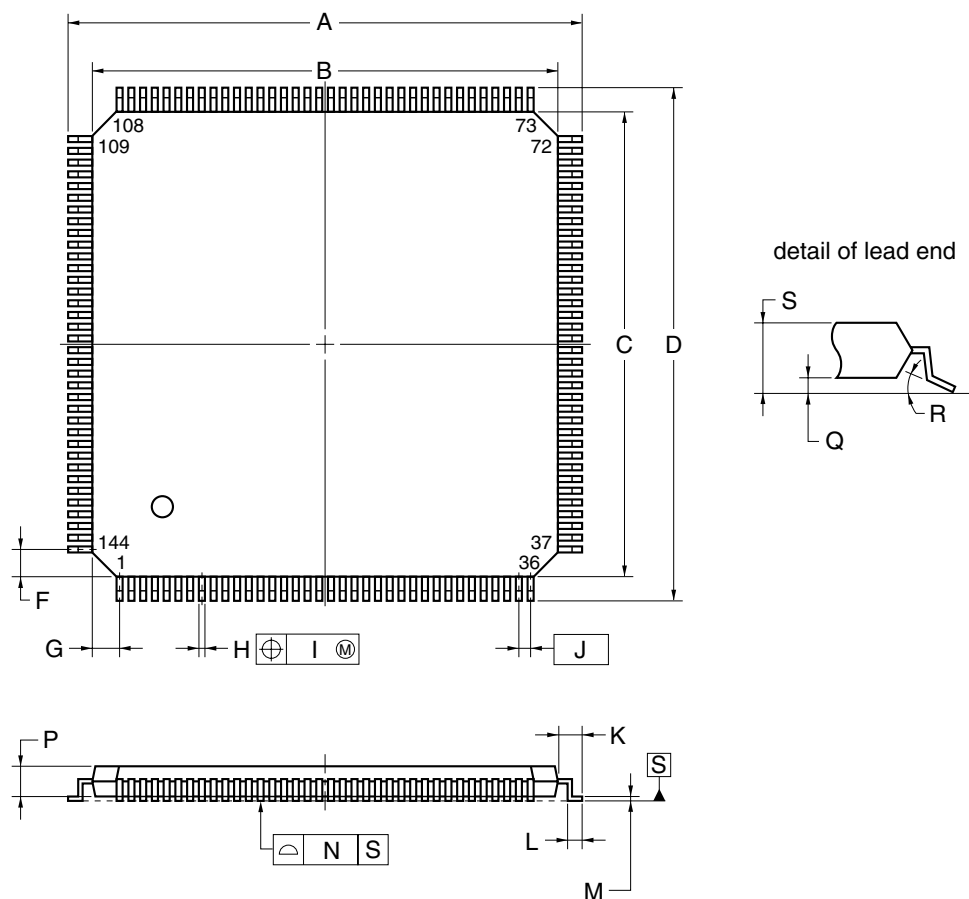
A/D Converter Characteristics ($T_A = -40$ to $+70^\circ\text{C}$... μ PD703100-40,
 $T_A = -40$ to $+85^\circ\text{C}$... μ PD703100-33, 703101-33, 703102-33,
 $V_{DD} = CV_{DD} = 3.0$ to 3.6 V, $HV_{DD} = 5.0$ V $\pm 10\%$, $V_{SS} = 0$ V,
 $HV_{DD} - 0.5$ V $\leq AV_{DD} \leq HV_{DD}$, output pin load capacitance: $C_L = 50$ pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	—		10			bit
Total error	—				± 4	LSB
Quantization error	—				$\pm 1/2$	LSB
Conversion time	t_{CONV}		5		10	μs
Sampling time	t_{SAMP}		Conversion clock ^{Note} /6			ns
Zero scale error	—				± 4	LSB
Scale error	—				± 4	LSB
Linearity error	—				± 3	LSB
Analog input voltage	V_{IAN}		-0.3		$AV_{REF} + 0.3$	V
Analog input resistance	R_{AN}			2		M Ω
AV_{REF} input voltage	AV_{REF}	$AV_{REF} = AV_{DD}$	4.5		5.5	V
AV_{REF} input current	AI_{REF}				2.0	mA
AV_{DD} current	AI_{DD}				6	mA

Note Conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWING

★ 144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.4
Q	0.10±0.05
R	3°+4° -3°
S	1.5±0.1
S144GJ-50-UEN	

★ 5. RECOMMENDED SOLDERING CONDITIONS

The μPD703100-33, 703100-40, 703101-33, and 703102-33 should be soldered and mounted under the following recommended conditions.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Table 5-1. Surface Mounting Type Soldering Conditions (1/2)

- (1) μPD703100GJ-40-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
 μPD703100GJ-33-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
 μPD703101GJ-33-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
 μPD703102GJ-33-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: two times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds max. (at 200°C or higher), Count: two times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, consult an NEC Electronics sales representative.

- (2) μPD703100GJ-33-UEN-A: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 20 to 72 hours)	IR60-203-3
Wave soldering	For details, consult an NEC Electronics sales representative.	—
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remarks 1. Products with -A at the end of the part number are lead-free products.
 2. For soldering methods and conditions other than those recommended above, consult an NEC Electronics sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions (2/2)

- (3) μPD703100GJ-40-UEN-A: 144-pin plastic LQFP (fine pitch) (20 × 20)
 μPD703101GJ-33-xxx-UEN-A: 144-pin plastic LQFP (fine pitch) (20 × 20)
 μPD703102GJ-33-xxx-UEN-A: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	For details, consult an NEC Electronics sales representative.	—
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

- Remarks**
1. Products with -A at the end of the part number are lead-free products.
 2. For soldering methods and conditions other than those recommended above, consult an NEC Electronics sales representative.

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Related documents μ PD70F3102-33 Data Sheet (U13844E)
 μ PD703100A-33, 703100A-40, 703101A-33, 703102A-33 Data Sheet (U14168E)
 μ PD70F3102A-33 Data Sheet (U13845E)

Reference materials Electrical Characteristics for Microcomputer (U15170J^{Note})

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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