一般積層セラミックコンデンサ
（高誘電率系・Class 2）
STANDARD MULTILAYER CERAMIC CAPACITORS
(CLASS2 :HIGH DIELECTRIC CONSTANT TYPE)

	code	Temp.characteristics	operating Temp. range
OPERATING TEMP.	B/BJ	B	−25～+85℃
		X7R	−55～+125℃
		X5R	−55～+85℃
	F	F	−25～+85℃
		Y5V	−30～+85℃

フロー／WAVE　　リフロー／REFLOW

特長　FEATURES

・実装密度の向上が図れます
・モノリシックの構造のため、信頼性が高い
・同一形状、静電容量範囲が広い

・Improve Higher Mounting Densities.
・Multilayer block structure provides higher reliability
・A wide range of capacitance values available in standard case sizes.

用途　APPLICATIONS

・一般電子機器用
・通信機器用（携帯電話、PHS、コードレス電話 etc.）

・General electronic equipment
・Communication equipment (portable telephones, PHS, other wireless applications, etc.)

形名表記法　ORDERING CODE

1 定格電圧〔VDC〕

A	4
J	6.3
L	10
E	16
T	25
U	50

2 シリーズ名

M	積層コンデンサ

3 端子電極

K	メッキ品

4 形状寸法(EIA)L×W〔mm〕

063(0201)	0.6×0.3
105(0402)	1.0×0.5
107(0603)	1.6×0.8

5 温度特性

△B,BJ	±10%
△F	$^{+30}_{-80}$%

△=スペース

6 公称静電容量〔pF〕

例	
102	1000
223	22000

7 容量許容差〔%〕

K	± 10
M	± 20
Z	$^{+80}_{-20}$

8 製品厚み〔mm〕

P	0.3
V	0.5
Z	0.8

9 個別仕様

―	標準

10 包装

B	単品(袋詰め)
F	テーピング(2mmピッチ・178φ)
T	テーピング(4mmピッチ・178φ)

11 当社管理記号

△	標準

△=スペース

L M K 1 0 5 B J 1 0 4 K V – F ○
1 2 3 4 5 6 7 8 9 10 11

1 Rated voltage〔VDC〕

A	4
J	6.3
L	10
E	16
T	25
U	50

2 Series name

M	Multilayer ceramic capacitors

3 End termination

K	Plated

4 Dimensions (case size)(LXW)〔mm〕

063(0201)	0.6×0.3
105(0402)	1.0×0.5
107(0603)	1.6×0.8

5 Temperature characteristics code

△B BJ	X7R	−55～+125℃ ±15%
	X5R	−55～+85℃ ±15%
△F	Y5V	−30～+85℃ $^{+22}_{-82}$%

△=Blank space

6 Nominal Capacitance〔pF〕

example	
102	1000
223	22000

7 Capacitance Tolerance〔%〕

K	± 10
M	± 20
Z	$^{+80}_{-20}$

8 Thickness〔mm〕

P	0.3
V	0.5
Z	0.8

9 Special code

―	Standard products

10 Packaging

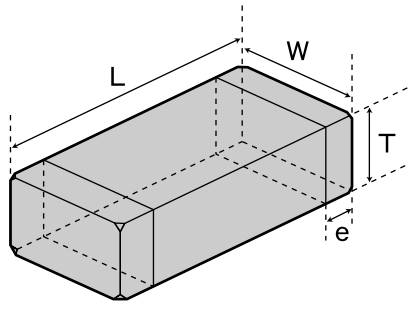
B	Bulk
F	Tape&Reel(2mm pitch・178φ)
T	Tape&Reel(4mm pitch・178φ)

11 Internal code

△	Standard Products

△=Blank space

外形寸法　EXTERNAL DIMENSIONS



Type(EIA)	L	W	T		e
□MK063 (0201)	0.6±0.03 (0.024±0.001)	0.3±0.03 (0.012±0.001)	0.3±0.03 (0.012±0.001)	P	0.15±0.05 (0.006±0.002)
□MK105 (0402)	1.0±0.05 (0.039±0.002)	0.5±0.05 (0.020±0.002)	0.5±0.05 (0.020±0.002)	V	0.25±0.10 (0.010±0.002)
□MK107 (0603)	1.6±0.10 (0.063±0.004)	0.8±0.10 (0.031±0.004)	0.8±0.10 (0.031±0.004)	Z	0.35±0.25 (0.014±0.010)

Unit：mm(inch)

概略バリエーション　AVAILABLE CAPACITANCE RANGE

■汎用積層セラミックコンデンサ（General Multilayer Ceramic capacitors）

Type		063					105										107			
Temp.char.		B/X5R			F/Y5V		B/X7R					F/Y5V					B/X7R		F/Y5V	
	WV	16V	10V	6.3V	6.3V	4V	50V	25V	16V	10V	6.3V	50V	25V	16V	10V	6.3V	50V	25V	50V	25V
Cap [pF]	[pF 3digits]																			
100	101	P					V										Z			
150	151																			
220	221																			
330	331		P					V				V						Z		
470	471																			
680	681																			
1000	102								V				V						Z	
1500	152																			
2200	222			P	P									V					Z	Z
3300	332																			
4700	472			P	P										V					Z
6800	682																			
10000	103			P		P			V	V *1	V *1 *1				V					Z
15000	153																			
22000	223																			
33000	333																			
47000	473																			
68000	683																			
100000	104																			
220000	224																			
470000	474																			
1000000	105																			

注：グラフの記号は製品厚み記号です。　Note：Letter codes in shaded areas are thickness codes.　*1 Items are only available in X5R

温度特性　Temperature Characteristics

温度特性 Temperature Characteristics	温度範囲 Operating temp. range [℃]	基準温度 Ref. Temp. [℃]	静電容量変化率 Capacitance Change [%]
B	−25～85	20	±10
X7R	−55～125	25	±15
X5R	−55～85	25	±15
F	−25～85	20	+30 −80
Y5V	−30～85	25	+22 −82

静電容量許容差　Capacitance Tolerance

記号 Code	許容差 Tolerance	区分 Item
K	±10%	B Char.
M	±20%	B Char.
Z	+80% −20%	F Char.

tan δ

Type	tan δ ※1	区分 Item
063	≦3.5%	B Char. 16V
	≦5.0%	B Char. 10V
	≦10%	B Char. 0.022～0.1μF
	≦16%	F Char. 6.3V
	≦20%	F Char. 4V
105	≦2.5%	B Char. 50V, 25V (0.0068μF)
	≦3.5%	B Char. 16V, 0.027～0.047μF, 25V (0.01μF)
	≦5.0%	F Char. 50V, 25V B Char. 0.056～0.22μF
	≦7.0%	F Char. 0.033μF, 0.047μF
	≦9.0%	F Char. 0.068μF～0.1μF
	≦10%	B Char. 0.47μF～1μF
	≦11%	F Char. 0.22μF
	≦16%	F Char. 0.47μF
	≦20%	F Char. 1μF
107	≦2.5%	B Char.
	≦5.0%	F Char.

※1　測定周波数　Measurement frequency=1±0.1kHz
　　測定電圧　Measurement voltage　=1±0.2Vrms

セレクションガイド Selection Guide P.8 etc
アイテム一覧 Part Numbers P.52
特性図 Electrical Characteristics
梱包 Packaging P.76
信頼性 Reliability Data P.78
使用上の注意 Precautions P.89

063TYPE(0201 case size)

定格電圧 Rated Voltage (DC)	形名 Ordering code		公称静電容量 Capacitance [pF]	温度特性 Temp.Char	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance [%]	厚み Thickness [mm](inch)
16V	EMK063 BJ101□P		100	B/X5R	3.5	R	±10% ±20%	0.3±0.03 (0.012±0.001)
	EMK063 BJ151□P		150					
	EMK063 BJ221□P		220					
	EMK063 BJ331□P		330					
	EMK063 BJ471□P		470					
	EMK063 BJ681□P		680					
	EMK063 BJ102□P		1000					
10V	LMK063 BJ152□P		1500		5			
	LMK063 BJ222□P		2200					
	LMK063 BJ332□P		3300					
	LMK063 BJ472□P		4700					
	LMK063 BJ682□P		6800					
	LMK063 BJ103□P		10000					
6.3V	JMK063 BJ223□P		22000		10			
	JMK063 BJ473□P		47000					
	JMK063 BJ104□P*		100000	X5R				
	JMK063 F223ZP		22000	F/Y5V	16		+80% −20%	0.3±0.03 (0.012±0.001)
	JMK063 F473ZP		47000					
4V	AMK063 F104ZP		100000		20			

形名の□には静電容量許容差記号が入ります。

□Please specify the capacitance tolerance code.

105TYPE(0402 case size)

定格電圧 Rated Voltage (DC)	形名 Ordering code		公称静電容量 Capacitance [pF]	温度特性 Temp.Char	tanδ Dissipation factor [%]Max.	実装条件 Soldering method R:リフロー Reflow soldering W:フロー Wave soldering	静電容量許容差 Capacitance tolerance [%]	厚み Thickness [mm](inch)
50V	UMK105 BJ221□V		220	B/X7R	2.5	R	±10% ±20%	0.5±0.05 (0.020±0.002)
	UMK105 BJ331□V		330					
	UMK105 BJ471□V		470					
	UMK105 BJ681□V		680					
	UMK105 BJ102□V		1000					
	UMK105 BJ152□V		1500					
	UMK105 BJ222□V		2200					
	UMK105 BJ332□V		3300					
25V	TMK105 BJ472□V		4700		3.5			
	TMK105 BJ682□V		6800					
	TMK105 BJ103□V		10000					
16V	TDK105 BJ153□V		15000					
	TDK105 BJ223□V		22000					
	EMK105 BJ333□V		33000					
	EMK105 BJ473□V		47000					
	EMK105 BJ104□V*		100000	B/X5R	5			
10V	LMK105 BJ104□V		100000					
	LMK105 BJ224□V*		220000					
6.3V	JMK105 BJ224□V		220000					
	JMK105 BJ474□V*		470000	X5R	10			
	JMK105 BJ105□V*		1000000					
50V	UMK105 F103ZV		10000	F/Y5V	5		+80% −20%	
25V	TMK105 F223ZV		22000					
16V	EMK105 F473ZV		47000		7			
	EMK105 F104ZV		100000		9			
10V	LMK105 F224ZV		220000		11			
6.3V	JMK105 F474ZV		470000		16			
	JMK105 F105ZV*		1000000		20			

形名の□には静電容量許容差記号が入ります。　□Please specify the capacitance tolerance code.

* 高温負荷試験の試験電圧は定格電圧の1.5倍　* Test voltage of Loading at high temperature test is 1.5 time of the rated voltage.

107TYPE(0603 case size)

定　格 電　圧 Rated Voltage (DC)	形　　名 Ordering code		公　　称 静電容量 Capacitance 〔pF〕	温度特性 Temp.Char	tan δ Dissipation factor 〔%〕Max.	実装条件 Soldering method R:リフロー Reflow soldering W: フロー Wave soldering	静電容量 許 容 差 Capacitance tolerance [%]	厚　　み Thickness 〔mm〕(inch)
50V	UMK107　B102□Z		1000	B/X7R	2.5	W, R	±10% ±20%	0.8±0.10 (0.031±0.004)
	UMK107　B152□Z		1500					
	UMK107　B222□Z		2200					
	UMK107　B332□Z		3300					
	UMK107　B472□Z		4700					
	UMK107　B682□Z		6800					
	UMK107　B103□Z		10000					
25V	TMK107　B153□Z		15000					
	TMK107　B223□Z		22000					
50V	UMK107　F103ZZ		10000	F/Y5V	5	W, R	+80% −20%	0.8±0.10 (0.031±0.004)
	UMK107　F223ZZ		22000					
25V	TMK107　F473ZZ		47000					
	TMK107　F104ZZ		100000					

形名の□には静電容量許容差記号が入ります。

□Please specify the capacitance tolerance code.

梱包　PACKAGING

①最小受注単位数 Minimum Quantity

■袋づめ梱包 Bulk packaging

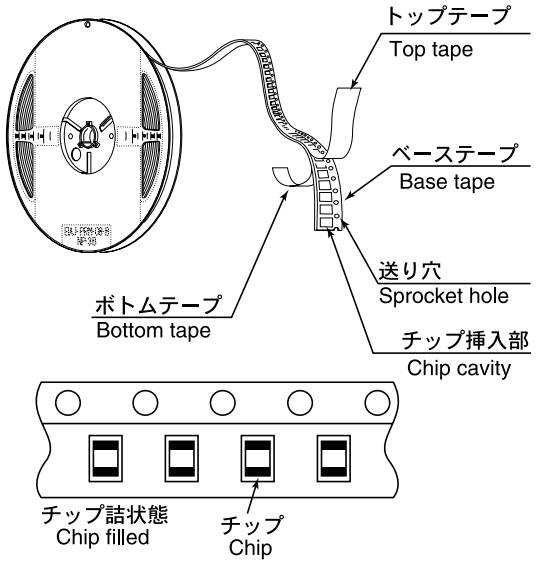
形式(EIA) Type	製品厚み Thickness		標準数量 Standard quantity [pcs]
	mm(inch)	code	
□MK105(0402)	0.5 (0.020)	V, W	1000
U VK105(0402)		W	
□MK107(0603)	0.8 (0.031)	A	
		Z	
□2K110(0504)	0.8 (0.031)	A	
	0.6 (0.024)	B	
□MK212(0805)	0.85 (0.033)	D	
	1.25 (0.049)	G	
□4K212(0805)	0.85 (0.033)	D	
□2K212(0805)	0.85 (0.033)	D	
□MK316(1206)	0.85 (0.033)	D	
	1.15 (0.045)	F	
	1.25 (0.049)	G	
	1.6 (0.063)	L	
□MK325(1210)	0.85 (0.033)	D	
	1.15 (0.045)	F	
	1.5 (0.059)	H	
	1.9 (0.075)	N	
	2.0max (0.079)	Y	
	2.5 (0.098)	M	

■テーピング梱包　Taped packaging

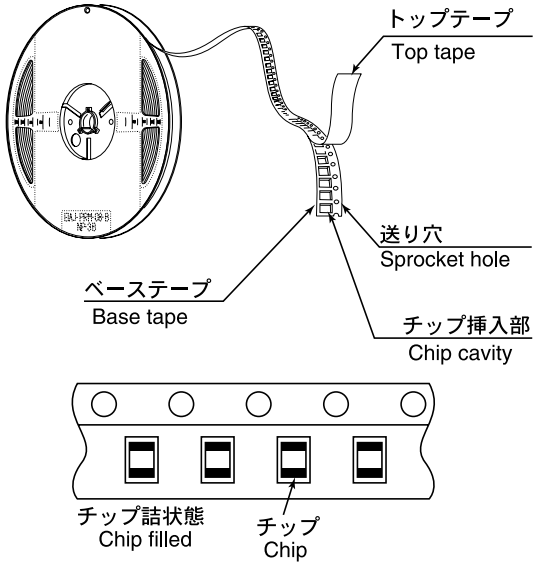
形式(EIA) Type	製品厚み Thickness		標準数量 Standard quantity [pcs]	
	mm(inch)	code	紙テープ paper	エンボステープ Embossed tape
□MK063(0201)	0.3 (0.012)	P	15000	—
□MK105(0402)	0.5 (0.020)	V, W	10000	—
U VK105(0402)		W		
□MK107(0603)	0.5 (0.020)	V	4000	—
	0.45 (0.018)	K	4000	—
	0.8 (0.031)	A	4000	—
		Z		
□2K110(0504)	0.8 (0.031)	A	4000	—
	0.6 (0.024)	B	4000	—
□MK212(0805)	0.45 (0.018)	K	4000	—
	0.85 (0.033)	D	4000	—
	1.25 (0.049)	G	—	3000
□4K212(0805)	0.85 (0.033)	D	4000	—
□2K212(0805)	0.85 (0.033)	D	4000	—
□MK316(1206) □4K316(1206)	0.85 (0.033)	D	4000	—
	1.15 (0.045)	F	—	3000
	1.25 (0.049)	G		
	1.6 (0.063)	L	—	2000
□MK325(1210)	0.85 (0.033)	D	—	2000
	1.15 (0.045)	F		
	1.5 (0.059)	H		
	1.9 (0.075)	N		
	2.0max (0.079)	Y	—	2000
	2.5 (0.098)	M	—	500
□MK432(1812)	1.9 (0.075)	Y	—	1000
	2.5 (0.098)	M	—	500
	3.2 (0.125)	U		

②テーピング材質　Taping material

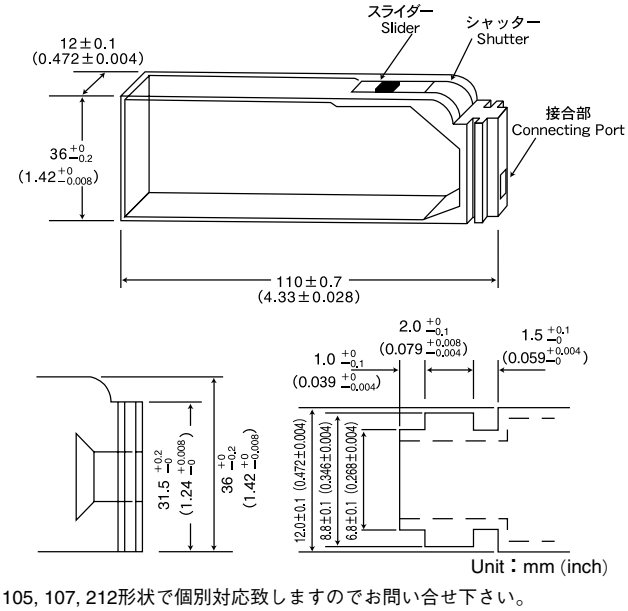
紙テープ
Card board carrier tape



エンボステープ
Embossed Tape



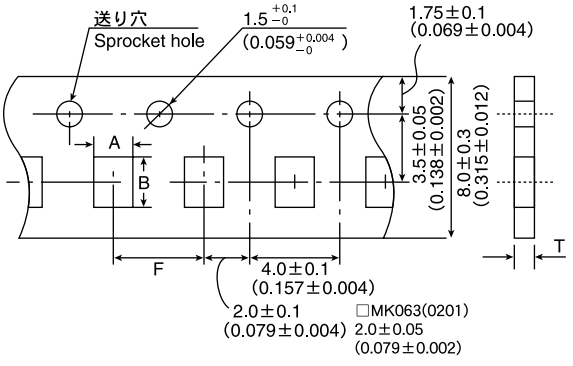
③バルクカセット　Bulk Cassette



105, 107, 212形状で個別対応致しますのでお問い合せ下さい。
Please contact any of our offices for accepting your requirement according to dimensions 0402, 0603, 0805.(inch)

③テーピング寸法　Taping dimensions

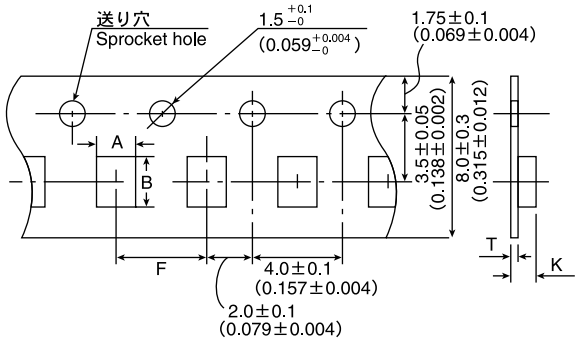
紙テープ　Paper Tape（8mm幅）(0.315inches wide)



Type (EIA)	チップ挿入部 Chip Cavity		挿入ピッチ Insertion Pitch	テープ厚み Tape Thickness
	A	B	F	T
□MK063(0201)	0.37±0.06 (0.06±0.002)	0.67±0.06 (0.027±0.002)	2.0±0.05 (0.079±0.002)	0.45max. (0.018max.)
□MK105(0402) U VK105(0402)	0.65±0.1 (0.026±0.004)	1.15±0.1 (0.045±0.004)	2.0±0.05 (0.079±0.002)	0.8max. (0.031max.)
□MK107(0603)	1.0±0.2 (0.039±0.008)	1.8±0.2 (0.071±0.008)	4.0±0.1 (0.157±0.004)	1.1max. (0.043max.)
□2K110(0504)	1.15±0.2 (0.045±0.008)	1.55±0.2 (0.061±0.008)	4.0±0.1 (0.157±0.004)	1.0max. (0.039max.)
□MK212(0805) □4K212(0805) □2K212(0805)	1.65±0.2 (0.065±0.008)	2.4±0.2 (0.094±0.008)	4.0±0.1 (0.157±0.004)	1.1max. (0.043max.)
□MK316(1206)	2.0±0.2 (0.079±0.008)	3.6±0.2 (0.142±0.008)		

Unit：mm(inch)

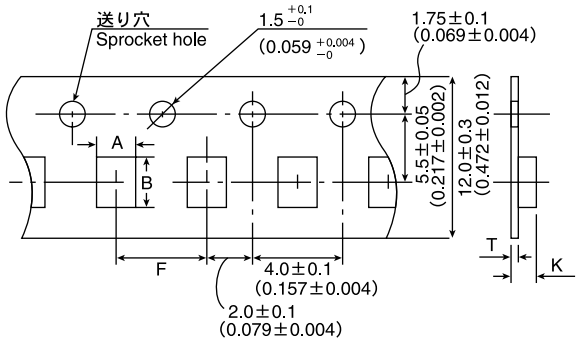
エンボステープ　Embossed tape（8mm幅）(0.315inches wide)



Type (EIA)	チップ挿入部 Chip cavity		挿入ピッチ Insertion Pitch	テープ厚み Tape Thickness	
	A	B	F	K	T
□MK212(0805)	1.65±0.2 (0.065±0.008)	2.4±0.2 (0.094±0.008)			
□MK316(1206) □4K316(1206)	2.0±0.2 (0.079±0.008)	3.6±0.2 (0.142±0.008)	4.0±0.1 (0.157±0.004)	2.5max. (0.098max.)	0.6max (0.024max.)
□MK325(1210)	2.8±0.2 (0.110±0.008)	3.6±0.2 (0.142±0.008)		3.4max. (0.134max.)	

Unit：mm(inch)

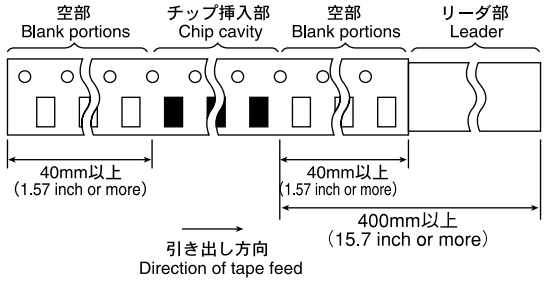
エンボステープ　Embossed tape（12mm幅）(0.472inches wide)



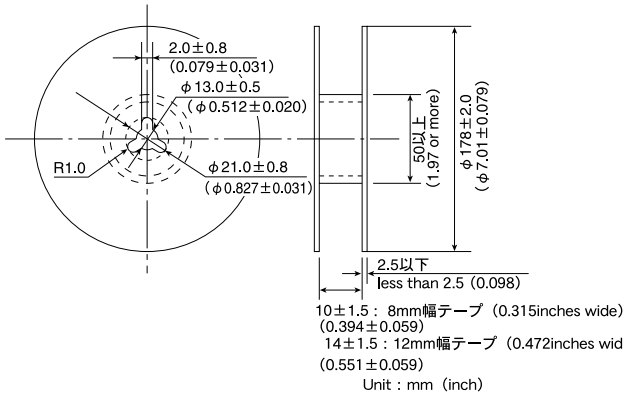
Type (EIA)	チップ挿入部 Chip cavity		挿入ピッチ Insertion Pitch	テープ厚み Tape Thickness	
	A	B	F	K	T
□MK432(1812)	3.7±0.2 (0.146±0.008)	4.9±0.2 (0.193±0.008)	8.0±0.1 (0.315±0.004)	4.0max. (0.157max.)	0.6max. (0.024max.)

Unit：mm(inch)

④リーダ部／空部　Leader and Blank portion

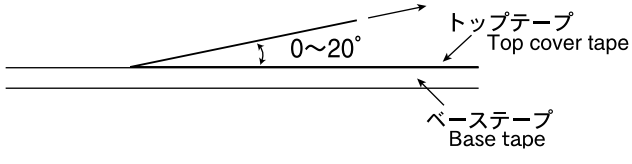


⑤リール寸法　Reel size

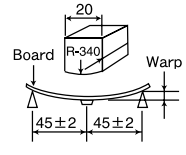


⑥トップテープ強度　Top Tape Strength

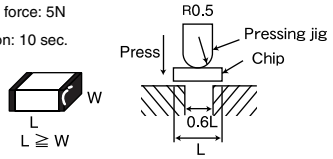
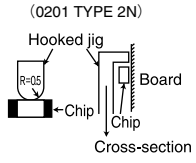
トップテープのはがし力は下図矢印方向にて0.1～0.7Nとなります。
The top tape requires a peel-off force of 0.1～0.7N in the direction of the arrow as illustrated below.



Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permitivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
1.Operating Temperature Range	−55 to +125℃		B：−55 to +125℃ F：−25 to +85℃	−25 to +85℃	High Capacitance Type BJ(X7R)：−55～+125℃, BJ(X5R)：−55～+85℃ C(X5S)：−55～+85℃, C(X6S)：−55～+105℃ E(Y5U)：−30～+85℃, F(Y5V)：−30～+85℃
2.Storage Temperature Range	−55 to +125℃		B：−55 to +125℃ F：−25 to +85℃	−25 to +85℃	High Capacitance Type BJ(X7R)：−55～+125℃, BJ(X5R)：−55～+85℃ C(X5S)：−55～+85℃, C(X6S)：−55～+105℃ E(Y5U)：−30～+85℃, F(Y5V)：−30～+85℃
3.Rated Voltage	50VDC,25VDC, 16VDC	16VDC	50VDC,25VDC	50VDC,35VDC,25VDC 16VDC,10VDC,6.3VDC 4DVC	
4.Withstanding Voltage Between terminals	No breakdown or damage	No abnormality	No breakdown or damage		Applied voltage: Rated voltage×3 (Class 1) Rated voltage×2.5 (Class 2) Duration: 1 to 5 sec. Charge/discharge current: 50mA max. (Class 1,2)
5.Insulation Resistance	10000 MΩ min.		500 MΩ μF. or 10000 MΩ., whichever is the smaller. Note 5		Applied voltage: Rated voltage Duration: 60±5 sec. Charge/discharge current: 50mA max.
6.Capacitance (Tolerance)	0.5 to 5 pF: ±0.25 pF 1 to 10pF: ±0.5 pF 5 to 10 pF: ±1 pF 11 pF or over: ± 5% ±10% 105TYPER△, S△, T△, U△ only 0.5～2pF: ±0.1pF 2.2～20pF: ±5%	0.5 to 2 pF : ±0.1 pF 2.2 to 5.1 pF : ±5%	B: ±10%, ±20% F：$^{+80}_{-20}$ %	B：±10%、±20% C：±10%、±20% E：−20%／+80% F：−20%／+80%	Measuring frequency： Class1： 1MHz±10%(C≦1000pF) 1 k Hz±10%(C>1000pF) Class2： 1 k Hz±10%(C≦22μF) 120Hz±10Hz(C>22μF) Measuring voltage： Class1：0.5～5Vrms(C≦1000pF) 1±0.2Vrms(C>1000pF) Class2： 1±0.2Vrms(C≦22μF) 0.5±0.1Vrms(C>22μF) Bias application: None
7.Q or Tangent of Loss Angle (tan δ)	Under 30 pF : Q≧400 + 20C 30 pF or over : Q≧1000 C= Nominal capacitance	Refer to detailed specification	B: 2.5% max.(50V, 25V) F: 5.0% max. (50V, 25V)	B：2.5% max. C、E、F：7% max. Note 4	Multilayer: Measuring frequency： Class1： 1MHz±10%(C≦1000pF) 1 k Hz±10%(C>1000pF) Class2： 1 k Hz±10%(C≦22μF) 120Hz±10Hz(C>22μF) Measuring voltage： Class1：0.5～5Vrms(C≦1000pF) 1±0.2Vrms(C>1000pF) Class2： 1±0.2Vrms(C≦22μF) 0.5±0.1Vrms(C>22μF) Bias application: None High-Frequency-Multilayer: Measuring frequency: 1GHz Measuring equipment: HP4291A Measuring jig: HP16192A
8.Temperature Characteristic of Capacitance (Without voltage application)	CK：0±250 CJ：0±120 CH：0±60 CG：0±30 PK：−150±250 PJ：−150±120 PH：−150±60 RK：−220±250 RJ：−220±120 RH：−220±60 SK：−330±250 SJ：−330±120 SH：−330±60 TK：−470±250 TJ：−470±120 TH：−470±60 UK：−750±250 UJ：−750±120 SL：+350 to -1000 (ppm/℃)	CH：0±60 RH：−220±60 (ppm/℃)	B：±10%(−25～85℃) F：$^{+30}_{-80}$ %(−25～85℃) B(X7R)：±15% F(Y5V)：$^{+22}_{-82}$%	B：±10% (−25～+85℃) C：±20% (−25～+85℃) E：+20%／−55% (−25～+85℃) F：+30%／−80% (−25～+85℃) B(X7R、X5R)： ±15% C(X5S、X6S)： ±22% E(Y5U)： +22%／−56% F(Y5V)： +22%／−82%	According to JIS C 5102 clause 7.12. Temperature compensating: Measurement of capacitance at 20℃ and 85℃ shall be made to calculate temperature characteristic by the following equation. $\frac{(C_{85} - C_{20})}{C_{20} \times \triangle T} \times 10^{6}$ (ppm/℃) High permitivity: Change of maximum capacitance deviation in step 1 to 5 Temperature at step 1: +20℃ Temperature at step 2: minimum operating temperature Temperature at step 3: +20℃ (Reference temperature) Temperature at step 4: maximum operating temperature Temperature at step 5: +20℃ Reference temperature for X7R, X5R, X5S, X6S, Y5U and Y5V shall be +25℃
9.Resistance to Flexure of Substrate	Appearance: No abnormality Capacitance change: Within ±5% or ±0.5 pF, whichever is larger.	Appearance: No abnormality Capacitance change: Within±0.5 pF	Appearance: No abnormality Capacitance change: B, BJ, C: Within ±12.5% E, F: Within ±30%		Warp: 1mm Testing board: glass epoxy-resin substrate Thickness: 1.6mm (063 TYPE : 0.8mm) The measurement shall be made with board in the bent position.  (Unit: mm)

Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
10.Body Strength	—	No mechanical damage.	—	—	High Frequency Multilayer: Applied force: 5N Duration: 10 sec. 
11.Adhesion of Electrode	No separation or indication of separation of electrode.				Applied force: 5N Duration: 30±5 sec. 
12.Solderability	At least 95% of terminal electrode is covered by new solder.				Solder temperature: 230±5℃ Duration: 4±1 sec.
13.Resistance to soldering	Appearance: No abnormality Capacitance change: Within ± 2.5% or ±0.25pF, whichever is larger. Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±2.5% Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±7.5% (B, BJ) Within ±15% (C) Within ±20% (E, F) tan δ: Initial value Note 4 Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality		Preconditioning: Thermal treatment (at 150℃ for 1 hr) (Applicable to Class 2.) Solder temperature: 270±5℃ Duration: 3±0.5 sec. Preheating conditions: 80 to 100℃, 2 to 5 min. or 5 to 10 min. 150 to 200℃, 2 to 5 min. or 5 to 10 min. Recovery: Recovery for the following period under the standard condition after the test. 24±2 hrs (Class 1) 48±4 hrs (Class 2)
14.Thermal shock	Appearance: No abnormality Capacitance change: Within ± 2.5% or ±0.25pF, whichever is larger. Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±0.25pF Q: Initial value Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality	Appearance: No abnormality Capacitance change: Within ±7.5% (B, BJ) Within ±15% (C) Within ±20% (E , F) tan δ: Initial value Note 4 Insulation resistance: Initial value Withstanding voltage (between terminals): No abnormality		Preconditioning: Thermal treatment (at 150℃ for 1 hr) (Applicable to Class 2.) Conditions for 1 cycle: Step 1: Minimum operating temperature $^{+0}_{-3}$ ℃ 30±3 min. Step 2: Room temperature 2 to 3 min. Step 3: Maximum operating temperature $^{-0}_{+3}$ ℃ 30±3 min. Step 4: Room temperature 2 to 3 min. Number of cycles: 5 times Recovery after the test: 24±2 hrs (Class 1) 48±4 hrs (Class 2)
15.Damp Heat (steady state)	Appearance: No abnormality Capacitance change: Within ±5% or ±0.5pF, whichever is larger. Q: C≧30 pF : Q≧350 10≦C＜30 pF: Q≧275 + 2.5C C＜10 pF : Q≧200 + 10C C: Nominal capacitance Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: Within ±0.5pF, Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: B: 5.0% max. F: 7.5% max. Note 4 Insulation resistance: 50 MΩ μF or 1000 MΩ whichever is smaller. Note 5	Appearance: No abnormality Capacitance change: BJ:Within ±12.5% C(X6S) Within ±25% C(X5S),E,F Within ±30% tan δ: Note 4 BJ: 5.0% max. C, E, F: 11.0% max. Insulation resistance: 50 MΩ μF or 1000 MΩ whichever is smaller. Note 5	Multilayer： Preconditioning: Thermal treatment (at 150℃ for 1 hr) (Applicable to Class 2.) Temperature: 40±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 60±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1)

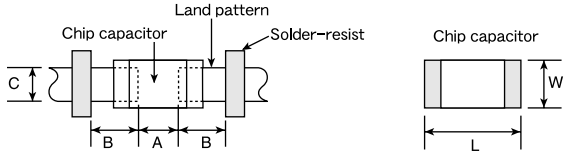
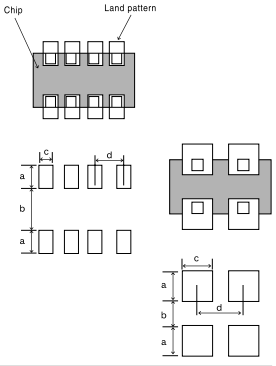
Multilayer Ceramic Capacitor Chips

Item	Specified Value				Test Methods and Remarks
	Temperature Compensating (Class 1)		High Permittivity (Class 2)		
	Standard	High Frequency Type	Standard Note1	High Value	
16.Loading under Damp Heat	Appearance: No abnormality Capacitance change: Within ± 7.5% or ±0.75pF, whichever is larger. Q: C≧30 pF: Q≧200 C＜30 pF: Q≧100 + 10C/3 C： Nominal capacitance Insulation resistance: 500 MΩ min.	Appearance: No abnormality Capacitance change: C≦2 pF: Within ±0.4 pF C>2 pF: Within ±0.75 pF C： Nominal capacitance Insulation resistance: 500 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: B: 5.0% max. F: 7.5% max. Note 4 Insulation resistance: 25 MΩ μF or 500 MΩ, whichever is the smaller. Note 5	Appearance: No abnormality Capacitance change: BJ：Within±12.5% C、E、F：Within±30% tanδ： Note 4 BJ：5.0%max. C、E、F：11%max. Insulation resistance: 25 MΩ μF or 500 MΩ, whichever is the smaller. Note 5	According to JIS C 5102 Clause 9. 9. Multilayer: Preconditioning: Voltage treatment (Class 2) Temperature: 40±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Applied voltage: Rated voltage Charge and discharge current: 50mA max. (Class 1,2) Recovery: Recovery for the following period under the standard condition after the removal from test chamber. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 60±2℃ Humidity: 90 to 95% RH Duration: 500 $^{+24}_{-0}$ hrs Applied voltage: Rated voltage Charge and discharge current: 50mA max. Recovery: 24±2 hrs of recovery under the standard condition after the removal from test chamber.
17.Loading at High Temperature	Appearance: No abnormality Capacitance change: Within ±3% or ±0.3pF, whichever is larger. Q: C≧30 pF : Q≧350 10≦C＜30 pF: Q≧275 + 2.5C C＜10 pF: Q≧200 + 10C C： Nominal capacitance Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: Within ±3% or ±0.3pF, whichever is larger. Insulation resistance: 1000 MΩ min.	Appearance: No abnormality Capacitance change: B: Within ±12.5% F: Within ±30% tan δ: Note 4 B: 4.0% max. F: 7.5% max. Insulation resistance: 50 MΩ μF or 1000 MΩ, whichever is smaller. Note 5	Appearance: No abnormality Capacitance change: BJ：Within±12.5% Within±20%※※ Within±25%※※ C：Within±25%(X6S) Within±30%(X5S) E、F：Within±30% tanδ： Note 4 BJ：5.0%max. C、F、F：11%max. Insulation resistance: 50 MΩ μF or 1000 MΩ, whichever is smaller. Note 5	According to JIS C 5102 clause 9.10. Multilayer: Preconditioning: Voltage treatment (Class 2) Temperature:125±3℃(Class 1, Class 2: B, BJ(X7R)) 85±2℃ (Class 2: BJ,F) Duration: 1000 $^{+48}_{-0}$ hrs Applied voltage: Rated voltage×2 Note 6 Recovery: Recovery for the following period under the standard condition after the removal from test chamber. As for Ni product, thermal treatment shall be performed prior to the recovery. 24±2 hrs (Class 1) 48±4 hrs (Class 2) High-Frequency Multilayer: Temperature: 125±3℃ (Class 1) Duration: 1000 $^{+48}_{-0}$ hrs Applied voltage: Rated voltage×2 Recovery: 24±2 hrs of recovery under the standard condition after the removal from test chamber.

Note 1 :For 105 type, specified in "High value".
Note 2 :Thermal treatment (Multilayer): 1 hr of thermal treatment at 150 +0 /−10 ℃ followed by 48±4 hrs of recovery under the standard condition shall be performed before the measurement.
Note 3 :Voltage treatment (Multilayer): 1 hr of voltage treatment under the specified temperature and voltage for testing followed by 48±4 hrs of recovery under the standard condition shall be performed before the measurement.
Note 4, 5 :The figure indicates typical inspection. Please refer to individual specifications.
Note 6 :Some of the parts are applicable in rated voltage×1.5. Please refer to individual specifications.

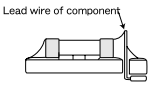
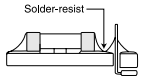
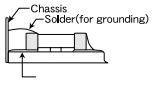
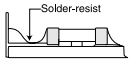
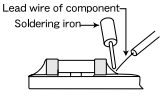
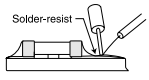
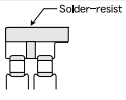
Note on standard condition: "standard condition" referred to herein is defined as follows: 5 to 35℃ of temperature, 45 to 85% relative humidity, and 86 to 106kPa of air pressure.
When there are questions concerning measurement results: In order to provide correlation data, the test shall be conducted under condition of 20±2℃ of temperature, 65 to 70% relative humidity, and 86 to 106kPa of air pressure. Unless otherwise specified, all the tests are conducted under the "standard condition."

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
1.Circuit Design	Verification of operating environment, electrical rating and performance 1. A malfunction in medical equipment, spacecraft, nuclear reactors, etc. may cause serious harm to human life or have severe social ramifications. As such, any capacitors to be used in such equipment may require higher safety and/or reliability considerations and should be clearly differentiated from components used in general purpose applications. Operating Voltage (Verification of Rated voltage) 1. The operating voltage for capacitors must always be lower than their rated values. If an AC voltage is loaded on a DC voltage, the sum of the two peak voltages should be lower than the rated value of the capacitor chosen. For a circuit where both an AC and a pulse voltage may be present, the sum of their peak voltages should also be lower than the capacitor's rated voltage. 2. Even if the applied voltage is lower than the rated value, the reliability of capacitors might be reduced if either a high frequency AC voltage or a pulse voltage having rapid rise time is present in the circuit.	
2.PCB Design	Pattern configurations (Design of Land-patterns) 1. When capacitors are mounted on a PCB, the amount of solder used (size of fillet) can directly affect capacitor performance. Therefore, the following items must be carefully considered in the design of solder land patterns: (1) The amount of solder applied can affect the ability of chips to withstand mechanical stresses which may lead to breaking or cracking. Therefore, when designing land-patterns it is necessary to consider the appropriate size and configuration of the solder pads which in turn determines the amount of solder necessary to form the fillets. (2) When more than one part is jointly soldered onto the same land or pad, the pad must be designed so that each component's soldering point is separated by solder-resist.	1.The following diagrams and tables show some examples of recommended patterns to prevent excessive solder amourts.(larger fillets which extend above the component end terminations) Examples of improper pattern designs are also shown. (1) Recommended land dimensions for a typical chip capacitor land patterns for PCBs  Recommended land dimensions for wave-soldering (unit: mm) Type / Size L / Size W / A / B / C 107: 1.6 / 0.8 / 0.8~1.0 / 0.5~0.8 / 0.6~0.8 212: 2.0 / 1.25 / 1.0~1.4 / 0.8~1.5 / 0.9~1.2 316: 3.2 / 1.6 / 1.8~2.5 / 0.8~1.7 / 1.2~1.6 325: 3.2 / 2.5 / 1.8~2.5 / 0.8~1.7 / 1.8~2.5 Recommended land dimensions for reflow-soldering (unit: mm) Type / Size L / Size W / A / B / C 063: 0.6 / 0.3 / 0.20~0.30 / 0.20~0.30 / 0.25~0.40 105: 1.0 / 0.5 / 0.45~0.55 / 0.40~0.50 / 0.45~0.55 107: 1.6 / 0.8 / 0.6~0.8 / 0.6~0.8 / 0.6~0.8 212: 2.0 / 1.25 / 0.8~1.2 / 0.8~1.2 / 0.9~1.6 316: 3.2 / 1.6 / 1.8~2.5 / 1.0~1.5 / 1.2~2.0 325: 3.2 / 2.5 / 1.8~2.5 / 1.0~1.5 / 1.8~3.2 432: 4.5 / 3.2 / 2.5~3.5 / 1.5~1.8 / 2.3~3.5 Excess solder can affect the ability of chips to withstand mechanical stresses. Therefore, please take proper precautions when designing land-patterns. Type / Size L / Size W / a / b / c / d 316 (4 circuits): 3.2 / 1.6 / 0.7~0.9 / 1 / 0.4~0.5 / 0.8 212 (4 circuits): 2.0 / 1.25 / 0.5~0.6 / 0.5~0.6 / 0.2~0.3 / 0.5 Type / Size L / Size W / a / b / c / d 212 (2 circuits): 2.0 / 1.25 / 0.5~0.6 / 0.5~0.6 / 0.5~0.6 / 1.0 110 (2 circuits): 1.37 / 1.0 / 0.35~0.45 / 0.55~0.65 / 0.3~0.4 / 0.64 

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
2.PCB Design		(2) Examples of good and bad solder application

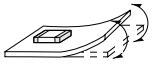
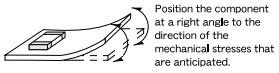
Items	Not recommended	Recommended
Mixed mounting of SMD and leaded components		
Component placement close to the chassis		
Hand-soldering of leaded components near mounted components		
Horizontal component placement		

Pattern configurations

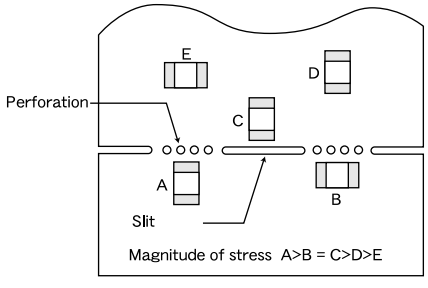
(Capacitor layout on panelized [breakaway] PC boards)

1. After capacitors have been mounted on the boards, chips can be subjected to mechanical stresses in subsequent manufacturing processes (PCB cutting, board inspection, mounting of additional parts, assembly into the chassis, wave soldering the reflow soldered boards etc.) For this reason, planning pattern configurations and the position of SMD capacitors should be carefully performed to minimize stress.

1-1. The following are examples of good and bad capacitor layout; SMD capacitors should be located to minimize any possible mechanical stresses from board warp or deflection.

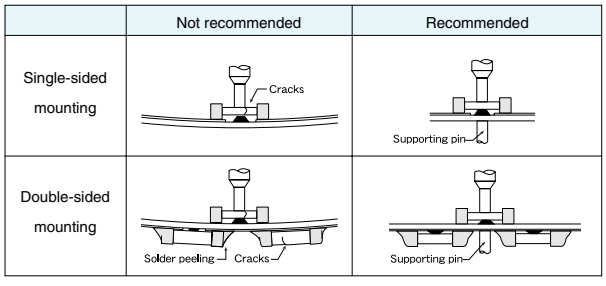
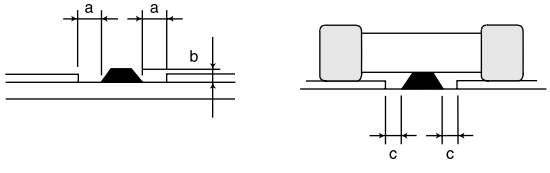
	Not recommended	Recommended
Deflection of the board		

1-2. To layout the capacitors for the breakaway PC board, it should be noted that the amount of mechanical stresses given will vary depending on capacitor layout. The example below shows recommendations for better design.

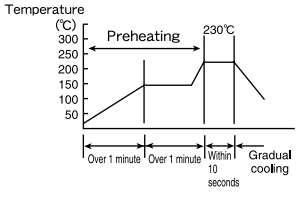
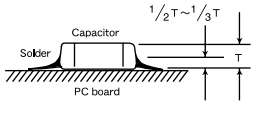
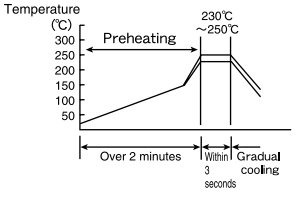


1-3. When breaking PC boards along their perforations, the amount of mechanical stress on the capacitors can vary according to the method used. The following methods are listed in order from least stressful to most stressful: push-back, slit, V-grooving, and perforation. Thus, any ideal SMD capacitor layout must also consider the PCB splitting procedure.

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
3.Considerations for automatic placement	Adjustment of mounting machine 1. Excessive impact load should not be imposed on the capacitors when mounting onto the PC boards. 2. The maintenance and inspection of the mounters should be conducted periodically.	1. If the lower limit of the pick-up nozzle is low, too much force may be imposed on the capacitors, causing damage. To avoid this, the following points should be considered before lowering the pick-up nozzle: (1)The lower limit of the pick-up nozzle should be adjusted to the surface level of the PC board after correcting for deflection of the board. (2)The pick-up pressure should be adjusted between 1 and 3 N static loads. (3)To reduce the amount of deflection of the board caused by impact of the pick-up nozzle, supporting pins or back-up pins should be used under the PC board. The following diagrams show some typical examples of good pick-up nozzle placement:  2. As the alignment pin wears out, adjustment of the nozzle height can cause chipping or cracking of the capacitors because of mechanical impact on the capacitors. To avoid this, the monitoring of the width between the alignment pin in the stopped position, and maintenance, inspection and replacement of the pin should be conducted periodically.
	Selection of Adhesives 1. Mounting capacitors with adhesives in preliminary assembly, before the soldering stage, may lead to degraded capacitor characteristics unless the following factors are appropriately checked; the size of land patterns, type of adhesive, amount applied, hardening temperature and hardening period. Therefore, it is imperative to consult the manufacturer of the adhesives on proper usage and amounts of adhesive to use.	1. Some adhesives may cause reduced insulation resistance. The difference between the shrinkage percentage of the adhesive and that of the capacitors may result in stresses on the capacitors and lead to cracking. Moreover, too little or too much adhesive applied to the board may adversely affect component placement, so the following precautions should be noted in the application of adhesives. (1)Required adhesive characteristics a. The adhesive should be strong enough to hold parts on the board during the mounting & solder process. b. The adhesive should have sufficient strength at high temperatures. c. The adhesive should have good coating and thickness consistency. d. The adhesive should be used during its prescribed shelf life. e. The adhesive should harden rapidly f. The adhesive must not be contaminated. g. The adhesive should have excellent insulation characteristics. h. The adhesive should not be toxic and have no emission of toxic gasses. (2)The recommended amount of adhesives is as follows; Figure / 212/316 case sizes as examples a / 0.3mm min b / 100 ~120 μm c / Adhesives should not contact the pad Amount of adhesive After capacitors are bonded 

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
4. Soldering	Selection of Flux 1. Since flux may have a significant effect on the performance of capacitors, it is necessary to verify the following conditions prior to use; (1)Flux used should be with less than or equal to 0.1 wt% (equivelent to chroline) of halogenated content. Flux having a strong acidity content should not be applied. (2)When soldering capacitors on the board, the amount of flux applied should be controlled at the optimum level. (3)When using water-soluble flux, special care should be taken to properly clean the boards.	1-1. When too much halogenated substance (Chlorine, etc.) content is used to activate the flux, or highly acidic flux is used, an excessive amount of residue after soldering may lead to corrosion of the terminal electrodes or degradation of insulation resistance on the surface of the capacitors. 1-2. Flux is used to increase solderability in flow soldering, but if too much is applied, a large amount of flux gas may be emitted and may detrimentally affect solderability. To minimize the amount of flux applied, it is recommended to use a flux-bubbling system. 1-3. Since the residue of water-soluble flux is easily dissolved by water content in the air, the residue on the surface of capacitors in high humidity conditions may cause a degradation of insulation resistance and therefore affect the reliability of the components. The cleaning methods and the capability of the machines used should also be considered carefully when selecting water-soluble flux.
	Soldering Temperature, time, amount of solder, etc. are specified in accordance with the following recommended conditions.	1-1. Preheating when soldering Heating: Ceramic chip components should be preheated to within 100 to 130℃ of the soldering. Cooling: The temperature difference between the components and cleaning process should not be greater than 100℃. Ceramic chip capacitors are susceptible to thermal shock when exposed to rapid or concentrated heating or rapid cooling. Therefore, the soldering process must be conducted with great care so as to prevent malfunction of the components due to excessive thermal shock.
	And please contact us about peak temperature when you use lead-free paste.	Recommended conditions for soldering [Reflow soldering] Temperature profile  Caution 1. The ideal condition is to have solder mass (fillet) controlled to 1/2 to 1/3 of the thickness of the capacitor, as shown below:  2. Because excessive dwell times can detrimentally affect solderability, soldering duration should be kept as close to recommended times as possible. [Wave soldering] Temperature profile  Caution 1. Make sure the capacitors are preheated sufficiently. 2. The temperature difference between the capacitor and melted solder should not be greater than 100 to130℃ 3. Cooling after soldering should be as gradual as possible. 4. Wave soldering must not be applied to the capacitors designated as for reflow soldering only.

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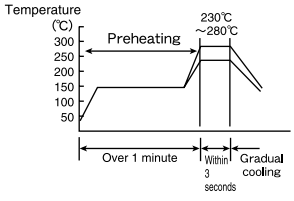
Stages	Precautions	Technical considerations
4. Soldering		[Hand soldering] Temperature profile  Caution 1. Use a 20W soldering iron with a maximum tip diameter of 1.0 mm. 2. The soldering iron should not directly touch the capacitor.
5.Cleaning	Cleaning conditions 1. When cleaning the PC board after the capacitors are all mounted, select the appropriate cleaning solution according to the type of flux used and purpose of the cleaning (e.g. to remove soldering flux or other materials from the production process.) 2. Cleaning conditions should be determined after verifying, through a test run, that the cleaning process does not affect the capacitor's characteristics.	1. The use of inappropriate solutions can cause foreign substances such as flux residue to adhere to the capacitor or deteriorate the capacitor's outer coating, resulting in a degradation of the capacitor's electrical properties (especially insulation resistance). 2. Inappropriate cleaning conditions (insufficient or excessive cleaning) may detrimentally affect the performance of the capacitors. (1)Excessive cleaning In the case of ultrasonic cleaning, too much power output can cause excessive vibration of the PC board which may lead to the cracking of the capacitor or the soldered portion, or decrease the terminal electrodes' strength. Thus the following conditions should be carefully checked; Ultrasonic output Below 20 W/ℓ Ultrasonic frequency Below 40 kHz Ultrasonic washing period 5 min. or less
6.Post cleaning processes	1. With some type of resins a decomposition gas or chemical reaction vapor may remain inside the resin during the hardening period or while left under normal storage conditions resulting in the deterioration of the capacitor's performance. 2. When a resin's hardening temperature is higher than the capacitor's operating temperature, the stresses generated by the excess heat may lead to capacitor damage or destruction. The use of such resins, molding materials etc. is not recommended.	
7.Handling	Breakaway PC boards (splitting along perforations) 1. When splitting the PC board after mounting capacitors and other components, care is required so as not to give any stresses of deflection or twisting to the board. 2. Board separation should not be done manually, but by using the appropriate devices. Mechanical considerations 1. Be careful not to subject the capacitors to excessive mechanical shocks. (1)If ceramic capacitors are dropped onto the floor or a hard surface, they should not be used. (2)When handling the mounted boards, be careful that the mounted components do not come in contact with or bump against other boards or components.	

Precautions on the use of Multilayer Ceramic Capacitors

Stages	Precautions	Technical considerations
8.Storage conditions	Storage 1. To maintain the solderability of terminal electrodes and to keep the packaging material in good condition, care must be taken to control temperature and humidity in the storage area. Humidity should especially be kept as low as possible. ・Recommended conditions Ambient temperature Below 40℃ Humidity Below 70% RH The ambient temperature must be kept below 30℃. Even under ideal storage conditions capacitor electrode solderability decreases as time passes, so should be used within 6 months from the time of delivery. ・Ceramic chip capacitors should be kept where no chlorine or sulfur exists in the air. 2. The capacitance value of high dielectric constant capacitors (type 2 &3) will gradually decrease with the passage of time, so this should be taken into consideration in the circuit design. If such a capacitance reduction occurs, a heat treatment of 150℃ for 1hour will return the capacitance to its initial level.	1. If the parts are stored in a high temperature and humidity environment, problems such as reduced solderability caused by oxidation of terminal electrodes and deterioration of taping/packaging materials may take place. For this reason, components should be used within 6 months from the time of delivery. If exceeding the above period, please check solderability before using the capacitors.