

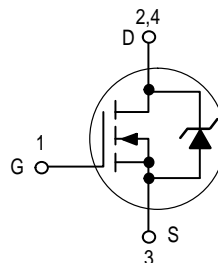
Product Preview

TMOS E-FET™
High Energy Power FET

N-Channel Enhancement-Mode Silicon Gate

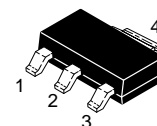
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor – Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



MMFT2N25E

TMOS POWER FET
2.0 AMPERES
250 VOLTS
R_{DS(on)} = 3.5 Ω



CASE 318E-04, STYLE 3
TO-261AA

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	250	Vdc
Drain-to-Gate Voltage, R _{GS} = 1.0 mΩ	V _{DGR}	250	Vdc
Gate-to-Source Voltage — Continuous	V _{GS}	±20	Vdc
Gate-to-Source Voltage — Single Pulse (tp ≤ 50 μs)	V _{GSM}	±40	Vdc
Drain Current — Continuous @ T _C = 25°C	I _D	2.0	Adc
— Continuous @ T _C = 100°C	I _D	0.6	
— Single Pulse (tp ≤ 10 μs)	I _{DM}	7.0	Apk
Total Power Dissipation @ T _C = 25°C	P _D	0.77	Watts
Derate above 25°C		6.2	mW/°C
Total P _D @ T _A = 25°C mounted on 1" Sq. Drain Pad on FR-4 Bd. Material		1.0	Watts
Total P _D @ T _A = 25°C mounted on 0.7" Sq. Drain Pad on FR-4 Bd. Material		1.2	
Total P _D @ T _A = 25°C mounted on min. Drain Pad on FR-4 Bd. Material		0.8	
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — Starting T _J = 25°C (V _{DD} = 80 V, V _{GS} = 10 V, Peak I _L = 4.0 Apk, L = 3.0 mH, R _G = 25 Ω)	E _{AS}	26	mJ
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THERMAL CHARACTERISTICS

— Junction-to-Ambient on 1" Sq. Drain Pad on FR-4 Bd. Material	R _{θJA}	90	°C/W
— Junction-to-Ambient on 0.7" Sq. Drain Pad on FR-4 Bd. Material		103	
— Junction-to-Ambient on min. Drain Pad on FR-4 Bd. Material		162	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

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E-FET is a trademark of Motorola, Inc.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA) Temperature Coefficient (Positive)	BV _{DSS}	250 —	— 324	— —	V _{dc} V/°C
Zero Gate Voltage Drain Current (V _{DS} = 250 V, V _{GS} = 0) (V _{DS} = 250 V, V _{GS} = 0, T _J = 125°C)	I _{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 V, V _{DS} = 0)	I _{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 —	2.8 5.7	4.0 —	V _{dc} mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 10 V, I _D = 1.0 Adc)	R _{DS(on)}	—	2.1	3.5	Ohms
Drain-to-Source On-Voltage (V _{GS} = 10 V, I _D = 2.0 A) (V _{GS} = 10 V, I _D = 1.0 A, T _J = 125°C)	V _{DS(on)}	— —	— —	8.40 7.35	V _{dc}
Forward Transconductance (V _{DS} = 8.0 V, I _D = 2.0 Adc)	g _{FS}	0.44	1.2	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	—	137	190	pF
Output Capacitance		C _{oss}	—	30	40	
Transfer Capacitance		C _{rss}	—	7.0	10	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{DS} = 125 V, I _D = 2.0 A, R _G = 9.1 Ohms, V _{GS} = 10 V)	t _{d(on)}	—	9.2	20	ns
Rise Time		t _r	—	6.6	10	
Turn-Off Delay Time		t _{d(off)}	—	13	30	
Fall Time		t _f	—	8.5	20	
Gate Charge	(V _{DS} = 200 V, I _D = 2.0 A, V _{GS} = 10 V)	Q _T	—	4.7	10	nC
		Q ₁	—	1.3	—	
		Q ₂	—	3.2	—	
		Q ₃	—	2.3	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	I _S = 2.0 A, V _{GS} = 0 V	V _{SD}	—	0.94	2.0	V _{dc}
	I _S = 2.0 A, V _{GS} = 0 V, T _J = 125°C	V _{SD}	—	0.83	—	
Reverse Recovery Time	(I _S = 2.0 A, di _S /dt = 100 A/μs)	t _{rr}	—	104	—	nS
		t _a	—	63	—	
		t _b	—	41	—	
Reverse Recovery Stored Charge		q _{rr}	—	0.365	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

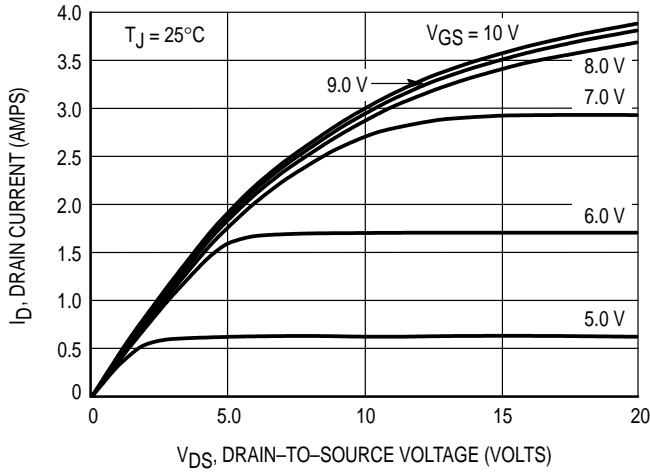


Figure 1. On-Region Characteristics

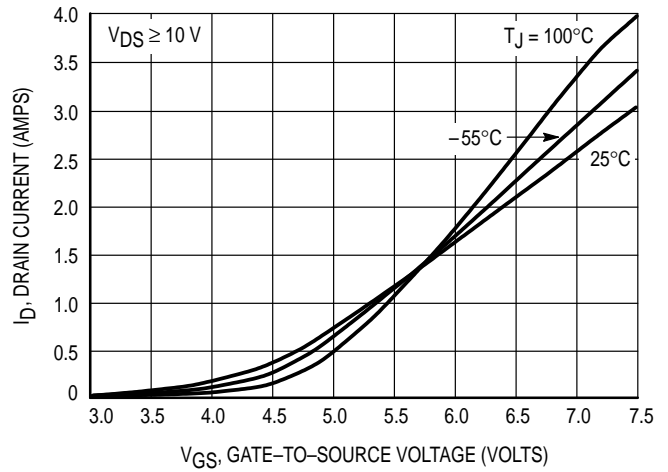


Figure 2. Transfer Characteristics

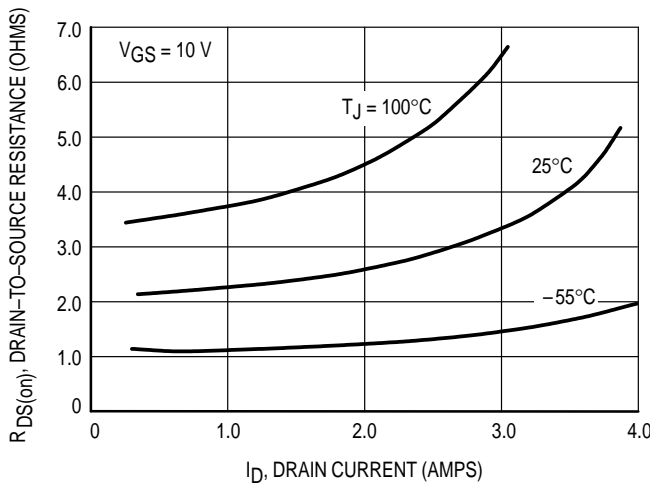


Figure 3. On-Resistance versus Drain Current and Temperature

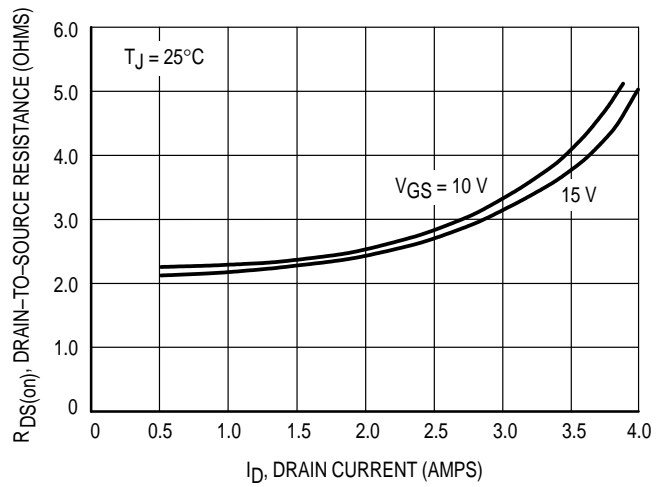


Figure 4. On-Resistance versus Drain Current and Gate Voltage

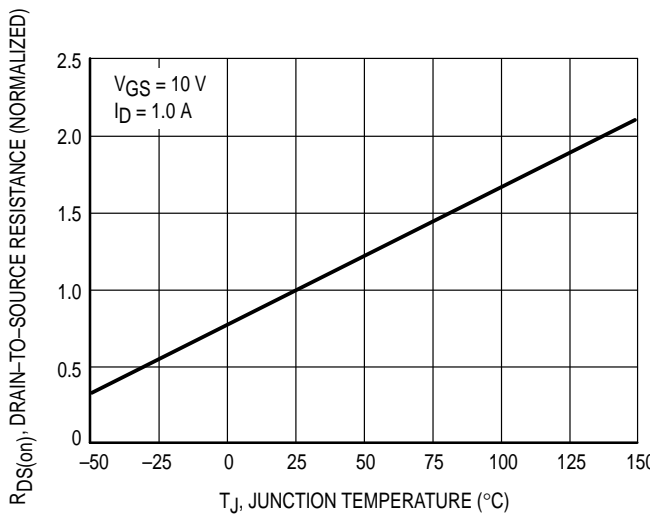


Figure 5. On-Resistance Variation versus Temperature

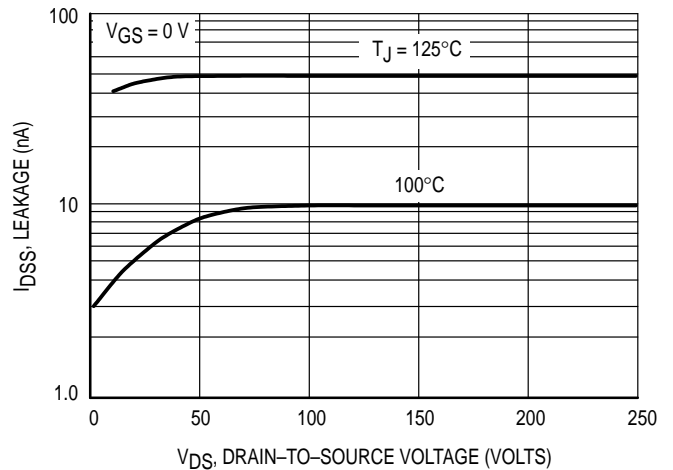


Figure 6. Drain-to-Source Leakage Current versus Voltage

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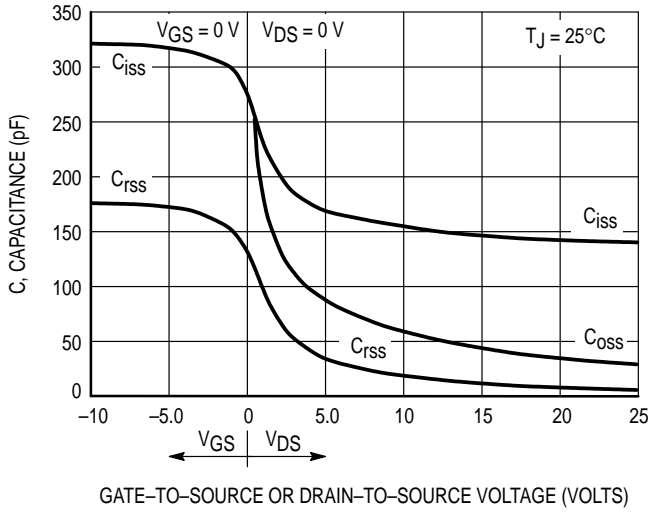


Figure 7. Capacitance Variation

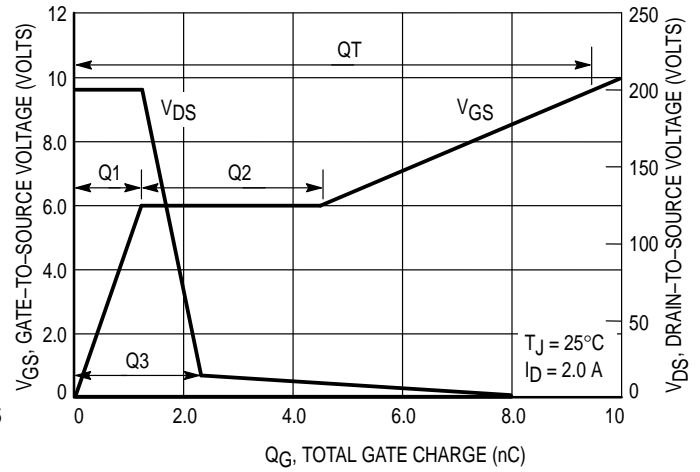


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

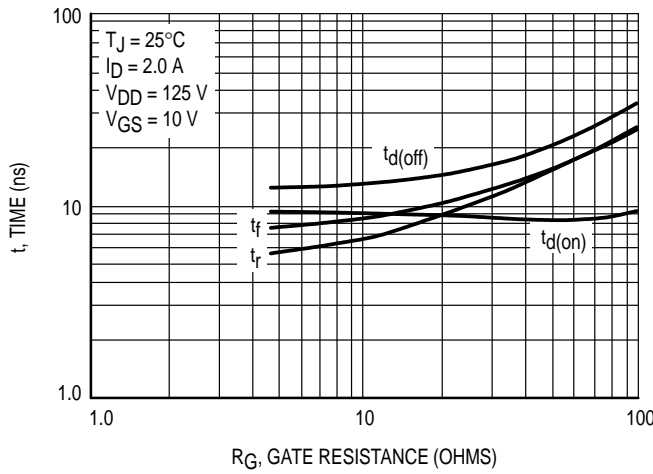


Figure 9. Resistive Switching Time Variation versus Gate Resistance

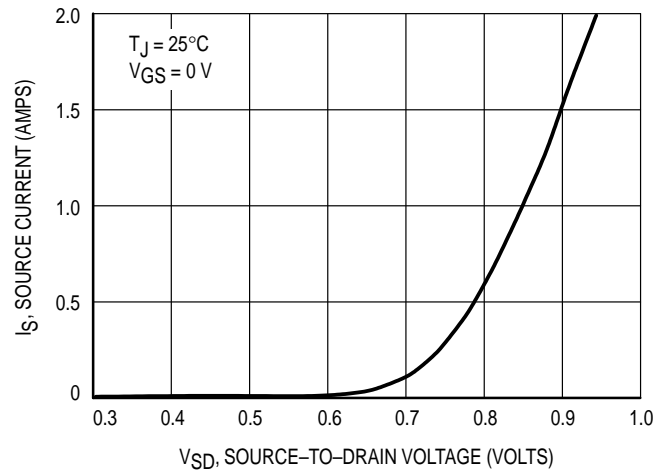


Figure 10. Diode Forward Voltage versus Current

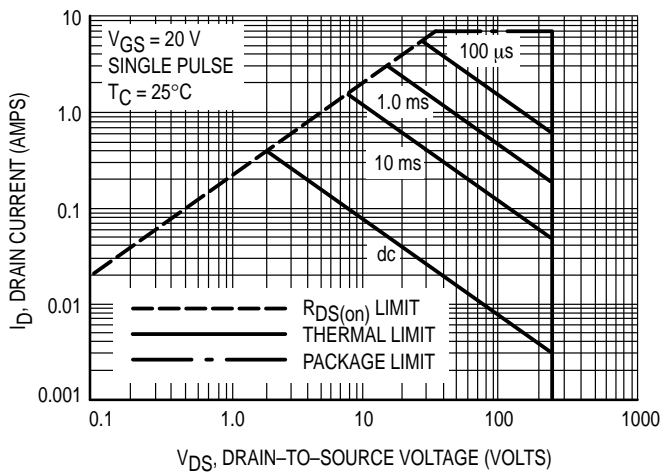


Figure 11. Maximum Rated Forward Biased Safe Operating Area

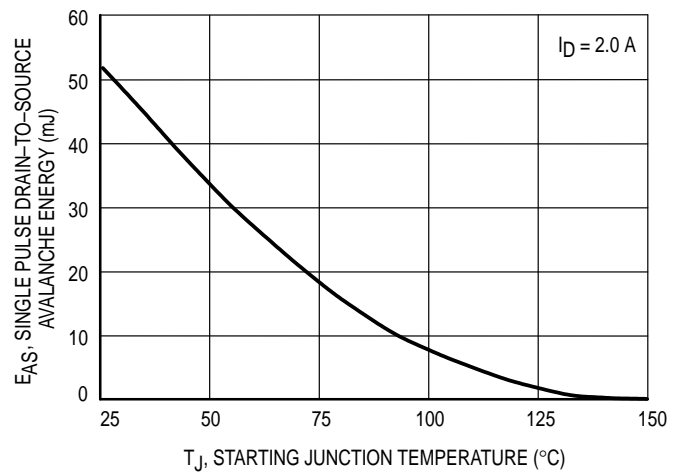


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

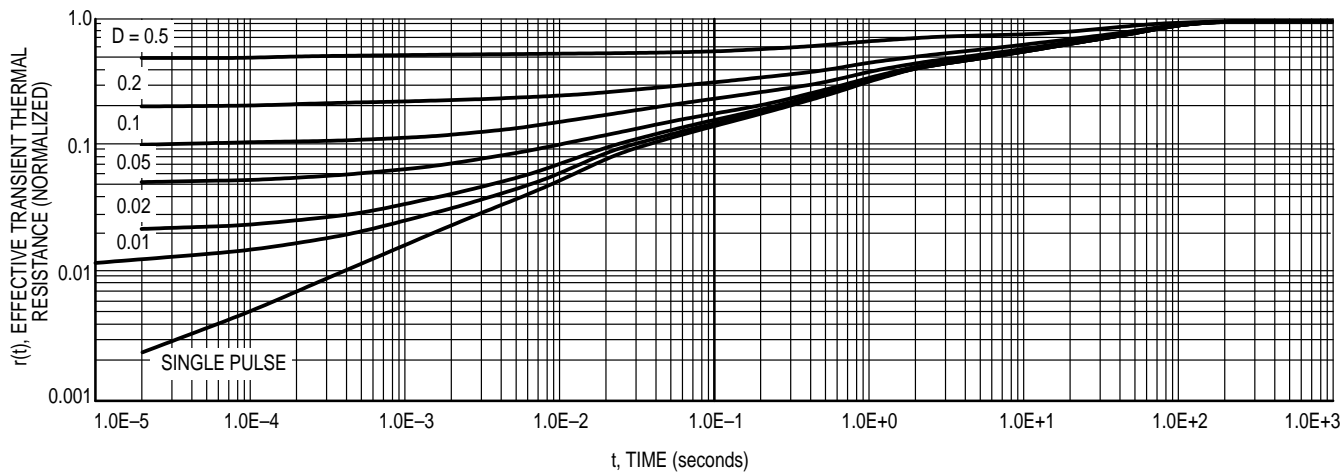
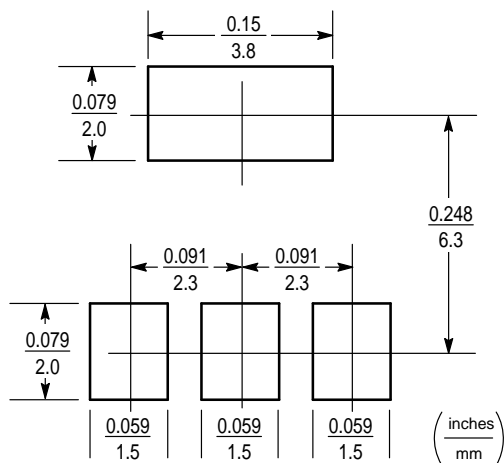


Figure 13. Thermal Response

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

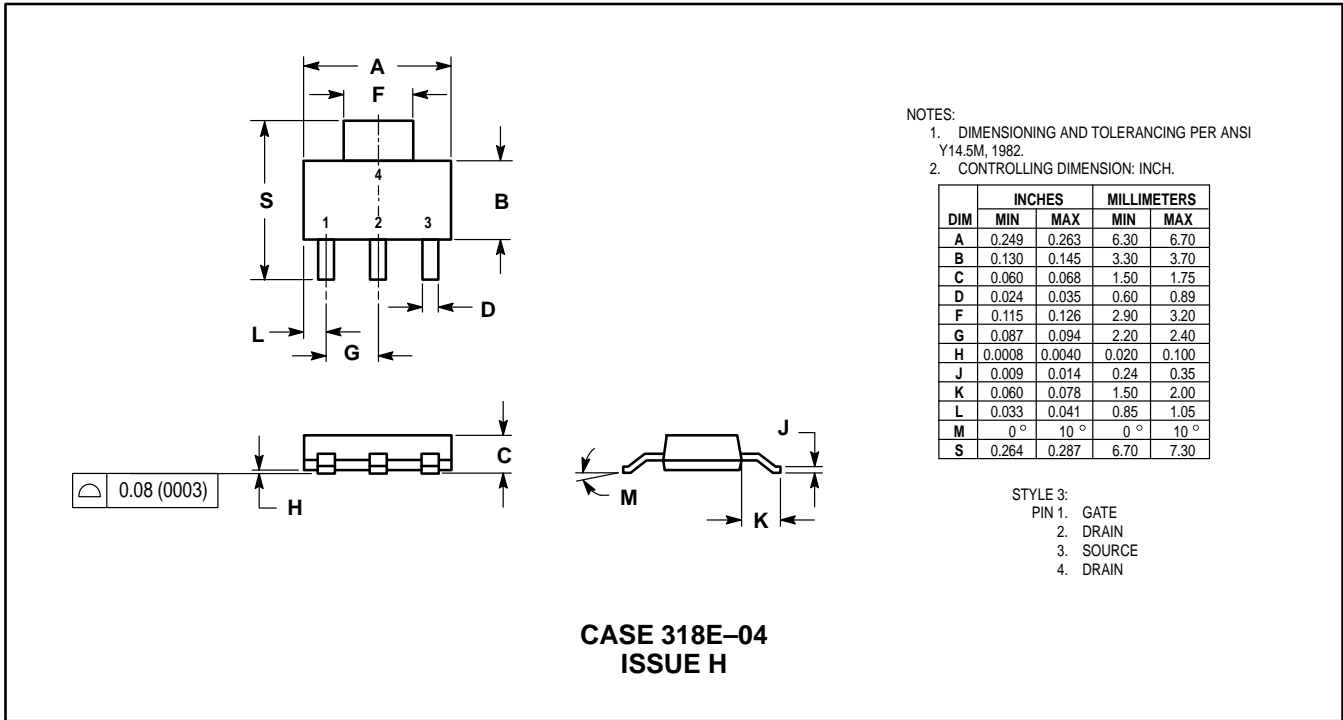
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface

between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-223

PACKAGE DIMENSIONS



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