



DM9301F Product Brief

100Mbps Ethernet Fiber/Twisted Pair Single Chip Media Converter

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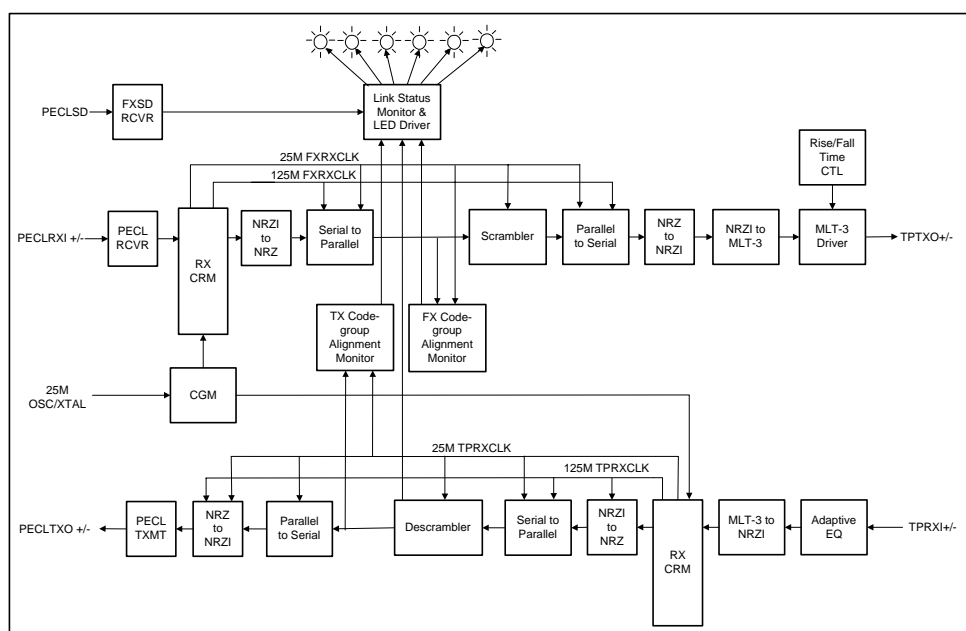
The DM9301 is a physical-layer, single-chip, low-power media converter for 100BASE-TX/FX full duplex repeater applications. On the TX media side, it provides a direct interface to Unshielded Twisted Pair Cable 5 (UTP5) for 100BASE-TX Fast Ethernet. On the FX media side, it provides a direct interface to a Pseudo Emitter Coupled Logic level interface (PECL).

The DM9301 uses a low power and high performance CMOS process. It contains the entire physical layer functions of 100BASE-TX as defined by IEEE802.3u, including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD) and a PECL compliant interface for a fiber optic module, compliant with ANSI X3.166. The DM9301 provides two independent clock recovery circuits to minimize bit delay through the converter (no FIFO are used to buffer data between the FX and TX interfaces). Furthermore, due to the excellent rise/fall time control by a built-in wave-shaping filter, the DM9301 needs no external filter to transport signals to the media on the 100Base-TX interface.

Patent-Pending Circuits: Smart adaptive receiver equalizer

- Digital algorithm for high frequency clock/data recovery circuit
- High speed wave-shaping circuit

Block Diagram



Specifications

- 100BASE-TX/FX single-chip media converter
- Total bit delay from FX to TX interface is 20 bit times (10 bit times each direction).
- Optional propagate HALT on no Link condition
- Compliant with IEEE802.3u 100BASE-TX standard, Compliant with ANSI X3T12 TP-PMD 1995 standard, Compliant with ANSI X3.166 FDDI-PMD
- Supports Half and Full Duplex operation 100Mbps, the DM9301 operates in Full Duplex mode at all times
- High performance 100Mbps clock generator and data recovery circuit
- Controlled output edge rates in the 100Base-TX transmitter without the need for an external filter
- LED support for FX Link, TX link, FX receive data, TX receive data, FX code group error and TX code group error.
- Built in LED test, all LED will light during a reset condition on the DM9301
- Digital clock recovery and regeneration circuit using an advanced digital algorithm to minimize jitter
- Supports diagnostic TX to TX analog loopback and FX to FX analog loopback (Loopback at the NRZI interface)
- Supports diagnostic TX to TX digital loopback and FX to FX digital loopback (Loopback at the 5B symbol interface)
- Low-power, high-performance CMOS process Available in a 100 QFP package

Application

1-to-1 100M Fiber converter

Fiber IP STB, IPC, Internet Radio

Ordering Information

Part Number	Pin Count	Package
DM9301F	100	QFP

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