

## 300-mA Ultra Low-Noise LDO Regulator With Discharge Option

### FEATURES

- Ultra Low Dropout—300 mV at 300-mA Load
- Ultra Low Noise—30  $\mu\text{V}_{\text{RMS}}$  (10-Hz to 100-kHz)
- Shutdown Control
- 130- $\mu\text{A}$  Ground Current at 300-mA Load
- 1.5% Guaranteed Output Voltage Accuracy
- 400-mA Peak Output Current Capability
- Uses Low ESR Ceramic Capacitors
- Fast Start-Up (50  $\mu\text{s}$ )
- Fast Line and Load Transient Response ( $\leq 30 \mu\text{s}$ )
- 1- $\mu\text{A}$  Maximum Shutdown Current
- Output Current Limit
- Reverse Battery Protection
- Built-in Short Circuit and Thermal Protection

- Output, Auto-Discharge In Shutdown Mode
- Fixed 1.2, 1.5, 1.8, 2.0, 2.2, 2.5, 2.6, 2.7, 2.8, 2.85, 2.9, 3.0, 3.3, 3.5, 3.6, 5.0-V Output Voltage Options
- MLP33-5 PowerPAK<sup>®</sup> Package

### APPLICATIONS

- Cellular Phones, Wireless Handsets
- Noise-Sensitive Electronic Systems, Laptop and Palmtop Computers
- PDAs
- Pagers
- Digital Cameras
- MP3 Player
- Wireless Modem

### DESCRIPTION

The Si91871 is a 300-mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current makes this part attractive for battery operated power systems. The Si91871 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source, such as RF applications, will benefit from the Si91871's ultra low output noise. An external noise bypass capacitor connected to the device's BP pin can further reduce the noise level. The Si91871 is designed to maintain regulation while delivering 400-mA peak current, making it ideal for systems that have a high surge current upon turn-on.

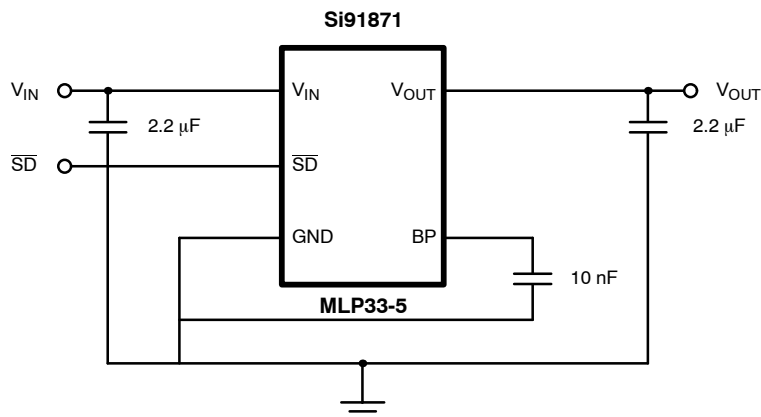
pull-down circuit is built into the Si91871 to clamp the output voltage when it rises beyond normal regulation. The Si91871 automatically discharges the output voltage by connecting the output to ground through a 100- $\Omega$  n-channel MOSFET when the device is put in shutdown mode.

The Si91871 features reverse battery protection to limit reverse current flow to approximately 1- $\mu\text{A}$  in the event reversed battery is applied at the input, thus preventing damage to the IC.

The Si91871 is available in both the standard and lead (Pb)-free 5-pin MLP33 PowerPAK packages and is specified to operate over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

For better transient response and regulation, an active

### TYPICAL APPLICATION CIRCUIT





## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	
Input Voltage, $V_{IN}$ to GND	-6.0 to 6.5 V
$\overline{V_{SD}}$ (See Detailed Description)	-0.3 V to $V_{IN}$
Output Current, $I_{OUT}$	Short Circuit Protected
Output Voltage, $V_{OUT}$	-0.3 V to $V_{IN} + 0.3$ V
Package Power Dissipation, $(P_d)^b$	2.3 W

Thermal Resistance ( $\theta_{JA}$ ) <sup>a</sup>	55°C/W
$R_{(\theta JA)}$ <sup>a</sup>	8°C/W
Maximum Junction Temperature, $T_{J(max)}$	150°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Notes	
a. Device mounted with all leads soldered or welded to PC board.	
b. Derate 20 mW/°C above $T_A = 25^\circ\text{C}$	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Input Voltage, $V_{IN}$	2 V to 6 V
Input Voltage, $\overline{V_{SD}}$	0 V to $V_{IN}$
Output Current	0 to 300 mA
$C_{IN}$ , $C_{OUT}^a$ (Ceramic)	2.2 $\mu\text{F}$

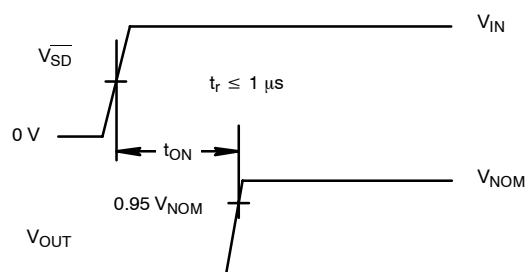
$C_{EB}$ (Ceramic)	0.01 $\mu\text{F}$
Operating Ambient Temperature, $T_A$	-40°C to 85°C
Operating Junction Temperature, $T_J$	-40°C to 125°C
Notes	
a. Maximum ESR of $C_{OUT}$ : 0.2 $\Omega$ .	

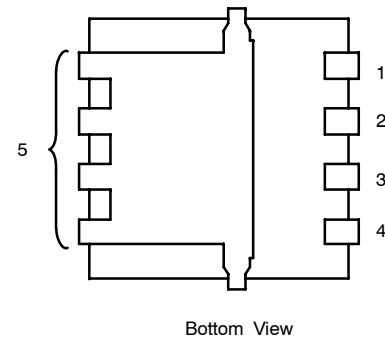
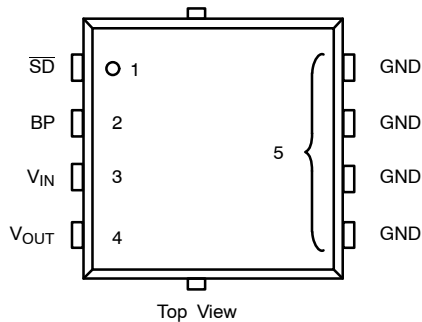
SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$ , $V_{IN} = V_{OUT(nom)} + 1$ V $I_{OUT} = 1$ mA, $C_{IN} = 2$ $\mu\text{F}$ , $C_{OUT} = 2.0$ $\mu\text{F}$ $\overline{V_{SD}} = 1.5$ V		Temp <sup>a</sup>	Limits -40 to 85°C			Unit
					Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
Start-Up BP Current	$I_{OUT}$	ON/OFF = High		Room		1		mA
Input Voltage Range	$V_{IN}$			Full	2		6	V
Output Voltage Accuracy		$1 \text{ mA} \leq I_{OUT} \leq 300 \text{ mA}$	$V_{OUT} \geq 1.8 \text{ V}$	Room	-2.0	1	2.0	%
				Full	-3.0	1	3.0	
				Room	-2.5	1	2.5	
				Full	-3.5	1	3.5	
Line Regulation ( $V_{OUT} \leq 3$ V)	$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$	From $V_{IN} = V_{OUT(nom)} + 1$ V to $V_{OUT(nom)} + 2$ V	Full	-0.06		0.18	%V	
Line Regulation (3.0 V < $V_{OUT} \leq 3.6$ V)			Full	0		0.3		
Line Regulation (5-V Version)			Full	0		0.4		
Dropout Voltage <sup>d, g</sup> ( $V_{OUT(nom)} \geq 2.6$ V)	$V_{IN} - V_{OUT}$	$I_{OUT} = 1$ mA	Room		1		mV	
			Room		45	80		
			Full		50	90		
			Room		300	350		
			Full			415		
			Room		65	100		
Dropout Voltage <sup>d, g</sup> ( $V_{OUT(nom)} < 2.6$ V, $V_{IN} \geq 2$ V)	$V_{IN} - V_{OUT}$	$I_{OUT} = 50$ mA	Room			120	mV	
			Full			120		
			Room		400	520		
			Full			570		
			Room		100	150		
			Full			180		
Ground Pin Current <sup>e, g</sup> ( $V_{OUT(nom)} \leq 3$ V)	$I_{GND}$	$I_{OUT} = 0$ mA	Room			130	$\mu\text{A}$	
			Full			200		
			Room		110	170		
			Full			200		
			Room		150	225		
			Full			275		
Ground Pin Current <sup>e</sup> ( $V_{OUT(nom)} > 3$ V)	$I_{GND}$	$I_{OUT} = 300$ mA	Room			150	$\mu\text{A}$	
			Full			200		
			Room		110	170		
			Full			200		
			Room		150	225		
			Full			275		
Peak Output current	$I_{O(peak)}$	$V_{OUT} \geq 0.95 \times V_{OUT(nom)}$ , $t_{PW} = 2$ ms		Full	400			mA

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$ , $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ $I_{OUT} = 1\text{ mA}$ , $C_{IN} = 2\ \mu\text{F}$ , $C_{OUT} = 2.0\ \mu\text{F}$ $V_{SD} = 1.5\text{ V}$	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
Output Noise Voltage	$e_N$	$V_{NOM} = 2.6\text{ V}$ , BW = 10 Hz to 100 kHz, $0\text{ mA} < I_{OUT} < 300\text{ mA}$ , $C_{NOISE} = 0.01\ \mu\text{F}$	Room		30		$\mu\text{V(rms)}$
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} = 300\text{ mA}$	$f = 1\text{ kHz}$	Room	60		dB
			$f = 10\text{ kHz}$	Room	40		
			$f = 100\text{ kHz}$	Room	30		
Dynamic Line Regulation	$\Delta V_{O(line)}$	$V_{IN} : V_{OUT(nom)} + 1\text{ V}$ to $V_{OUT(nom)} + 2\text{ V}$ $t_r/t_f = 2\ \mu\text{s}$ , $I_{OUT} = 300\text{ mA}$	Room		20		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	$I_{OUT} : 1\text{ mA}$ to $300\text{ mA}$ , $t_r/t_f = 2\ \mu\text{s}$	Room		20		
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$		Room		150		°C
Thermal Hysteresis	$T_{HYST}$		Room		20		
Reverse current	$I_R$	$V_{IN} = -6.0\text{ V}$	Room		1		$\mu\text{A}$
Short Circuit Current	$I_{SC}$	$V_{OUT} = 0\text{ V}$	Room		700		mA
Shutdown							
Shutdown Supply Current	$I_{CC(off)}$	$V_{SD} = 0\text{ V}$	Room		0.1	1	$\mu\text{A}$
$\overline{\text{SD}}$ Pin Input Voltage	$V_{SD}$	High = Regulator ON (Rising)	Full	1.5		$V_{IN}$	V
		Low = Regulator OFF (Falling)	Full			0.4	
Auto Discharge Resistance	$R_{DIS}$		Room		100		$\Omega$
$\overline{\text{SD}}$ Pin Input Current <sup>f</sup>	$I_{IN(SD)}$	$V_{SD} = 1.5\text{ V}$ , $V_{IN} = 6\text{ V}$	Room		0.7		$\mu\text{A}$
$\overline{\text{SD}}$ Hysteresis	$V_{HYST(SD)}$		Full		150		mV
$V_{OUT}$ Turn-On Time	$t_{ON}$	$V_{SD}$ (See Figure 1), $I_{LOAD} = 100\text{ nA}$			50		$\mu\text{s}$

**Notes**

- Room = 25°C, Full = -40 to 85°C.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at  $V_{OUT} \geq 2\text{ V}$  are measured at  $V_{OUT} = 3.3\text{ V}$ , while typical values for dropout voltage at  $V_{OUT} < 2\text{ V}$  are measured at  $V_{OUT} = 1.8\text{ V}$ .
- Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that  $V_{IN}$  does not drop below 2.0 V.
- Ground current is specified for normal operation as well as “drop-out” operation.
- The device’s shutdown pin includes a typical 2-M $\Omega$  internal pull-down resistor connected to ground.
- $V_{OUT(nom)}$  is  $V_{OUT}$  when measured with a 1-V differential to  $V_{IN}$ .

**TIMING WAVEFORMS**

**FIGURE 1.** Timing Diagram for Power-Up

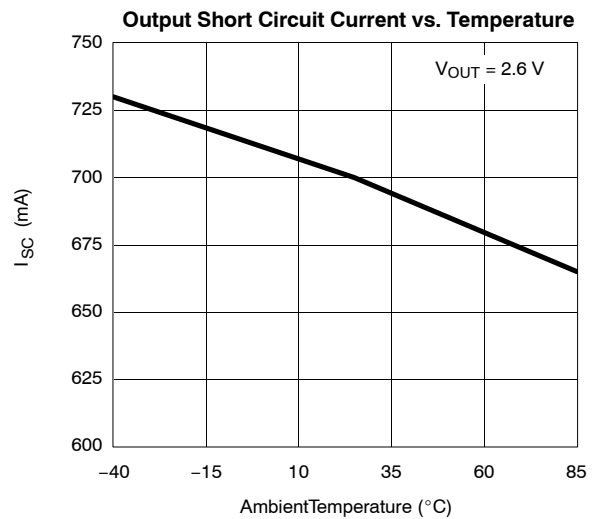
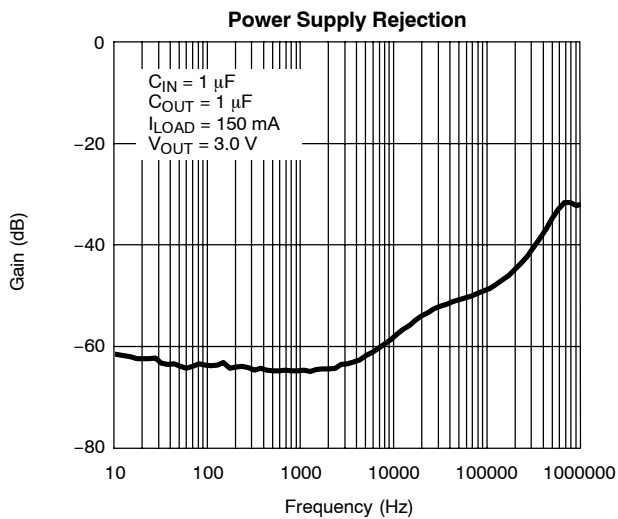
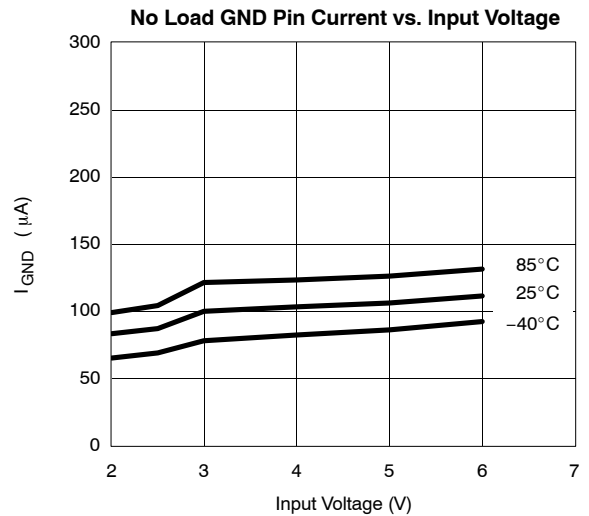
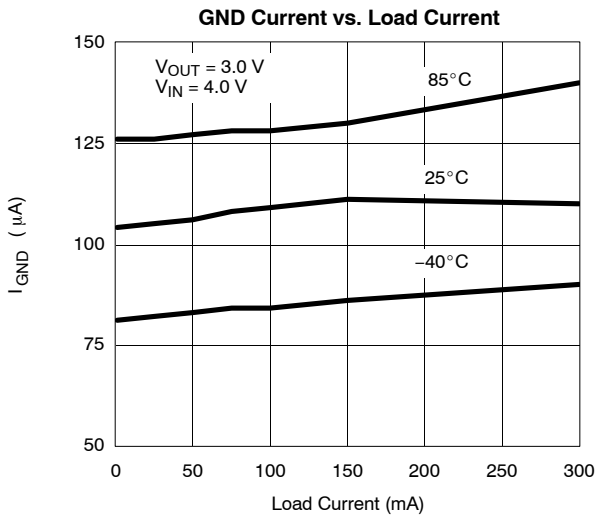
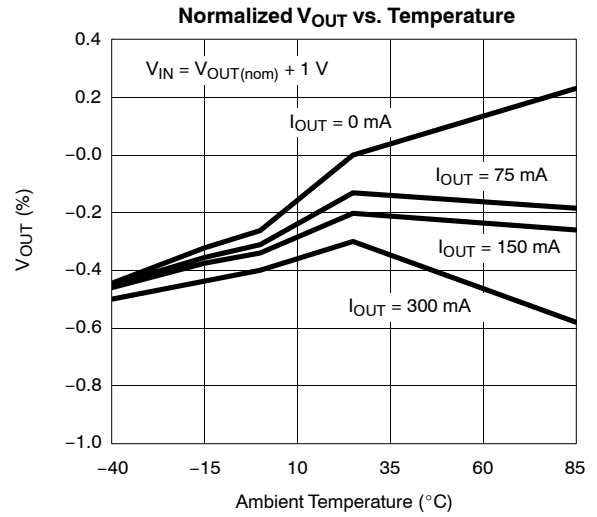
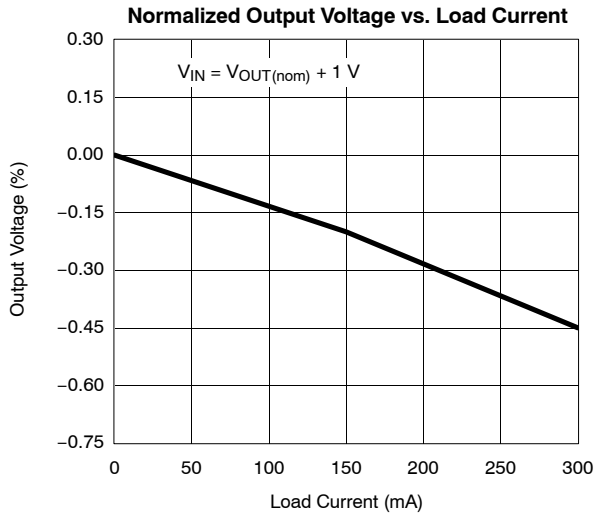
**PIN CONFIGURATION**
**MLP33-5 PowerPAK**

**PIN DESCRIPTION**

Pin Number	Name	Function
1	$\overline{SD}$	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to $V_{IN}$ if unused
2	BP	Noise bypass pin. For low noise applications, a 0.01 $\mu\text{F}$ ceramic capacitor should be connected from this pin to ground.
3	$V_{IN}$	Input supply pin. Bypass this pin with a 1- $\mu\text{F}$ ceramic or tantalum capacitor to ground
4	$V_{OUT}$	Output voltage. Connect $C_{OUT}$ between this pin and ground.
5	GND	Ground pin. For better thermal capability, directly connected to large ground plane

**ORDERING INFORMATION**

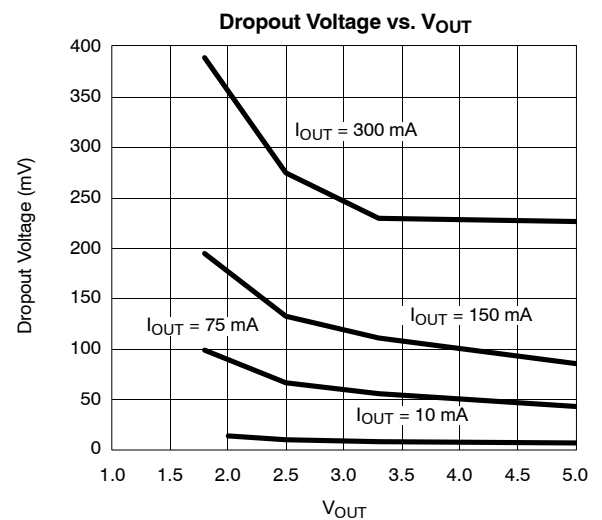
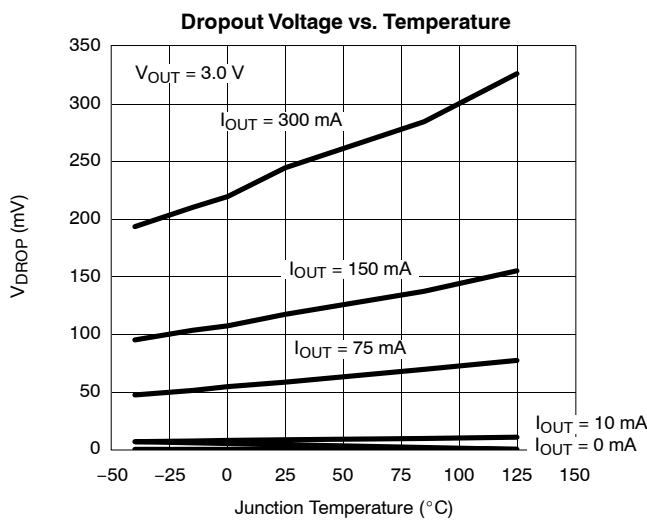
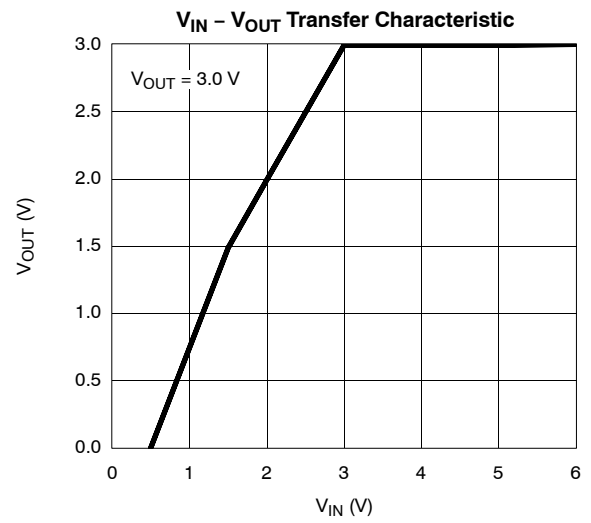
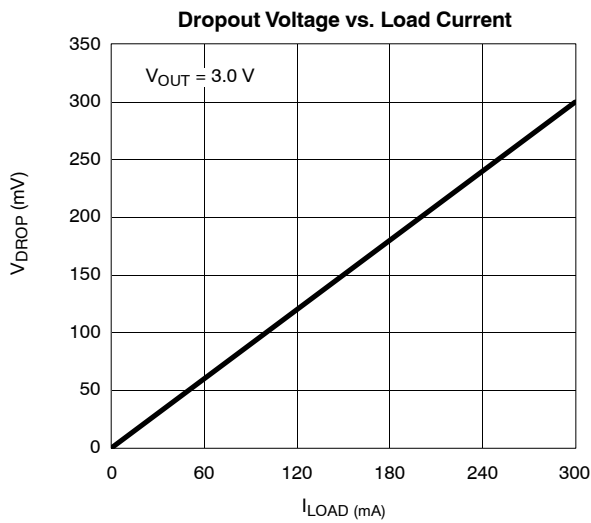
Standard Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temp. Range	Pkg.
Si91871DMP-12-T1	Si91871DMP-12-E3	7112	1.2	-40 to 85°C	MLP33-5
Si91871DMP-15-T1	Si91871DMP-15-E3	7115	1.5		
Si91871DMP-18-T1	Si91871DMP-18-E3	7118	1.8		
Si91871DMP-20-T1	Si91871DMP-20-E3	7120	2.0		
Si91871DMP-22-T1	Si91871DMP-22-E3	7122	2.2		
Si91871DMP-25-T1	Si91871DMP-25-E3	7125	2.5		
Si91871DMP-26-T1	Si91871DMP-26-E3	7126	2.6		
Si91871DMP-27-T1	Si91871DMP-27-E3	7127	2.7		
Si91871DMP-28-T1	Si91871DMP-28-E3	7128	2.8		
Si91871DMP-285-T1	Si91871DMP-285-E3	71285	2.85		
Si91871DMP-29-T1	Si91871DMP-29-E3	7129	2.9		
Si91871DMP-30-T1	Si91871DMP-30-E3	7130	3.0		
Si91871DMP-33-T1	Si91871DMP-33-E3	7133	3.3		
Si91871DMP-35-T1	Si91871DMP-35-E3	7135	3.5		
Si91871DMP-36-T1	Si91871DMP-36-E3	7136	3.6		
Si91871DMP-50-T1	Si91871DMP-50-E3	7150	5.0		

**TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)**



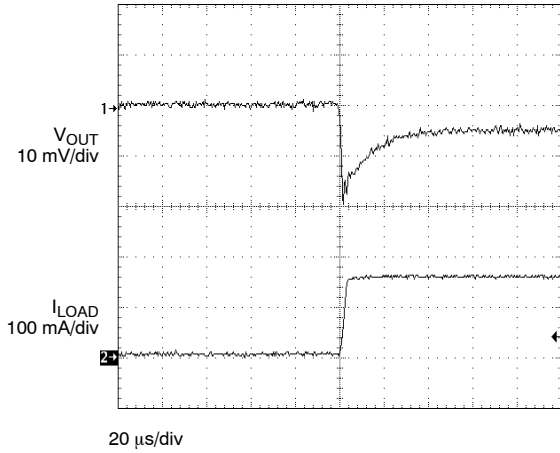


**TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)**



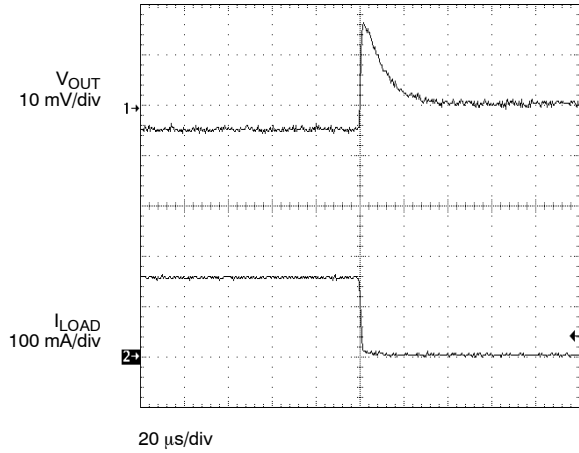
**TYPICAL WAVEFORMS**

**Load Transient Response-1**



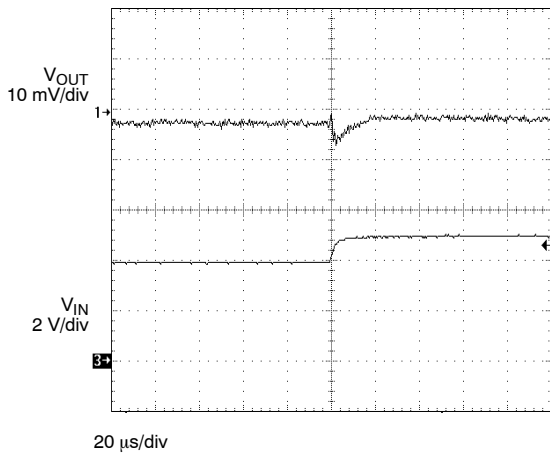
$V_{OUT} = 3.0\text{ V}$   
 $C_{OUT} = 1\ \mu\text{F}$   
 $I_{LOAD} = 1\ \text{to}\ 150\ \text{mA}$   
 $t_{rise} = 2\ \mu\text{sec}$

**Load Transient Response-2**



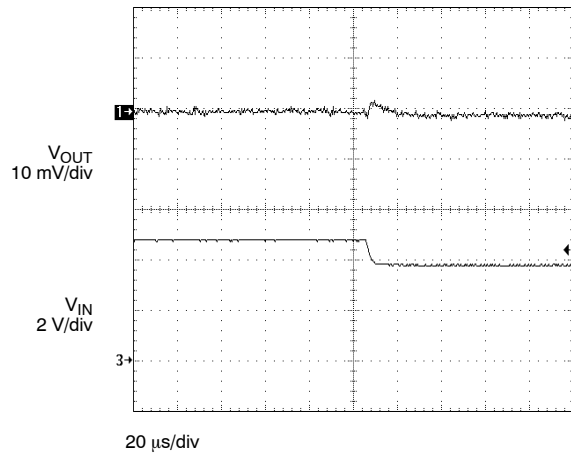
$V_{OUT} = 3.0\text{ V}$   
 $C_{OUT} = 1\ \mu\text{F}$   
 $I_{LOAD} = 150\ \text{to}\ 1\ \text{mA}$   
 $t_{fall} = 2\ \mu\text{sec}$

**Line Transient Response-1**



$V_{INSTEP} = 4\ \text{to}\ 5\ \text{V}$   
 $V_{OUT} = 3\ \text{V}$   
 $C_{OUT} = 1\ \mu\text{F}$   
 $C_{IN} = 1\ \mu\text{F}$   
 $I_{LOAD} = 150\ \text{mA}$   
 $t_{rise} = 5\ \mu\text{sec}$

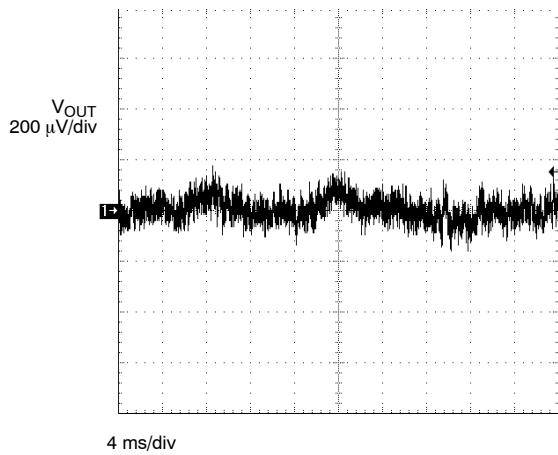
**Line Transient Respons-2**



$V_{INSTEP} = 5\ \text{to}\ 4\ \text{V}$   
 $V_{OUT} = 3\ \text{V}$   
 $C_{OUT} = 1\ \mu\text{F}$   
 $C_{IN} = 1\ \mu\text{F}$   
 $I_{LOAD} = 150\ \text{mA}$   
 $t_{fall} = 5\ \mu\text{sec}$

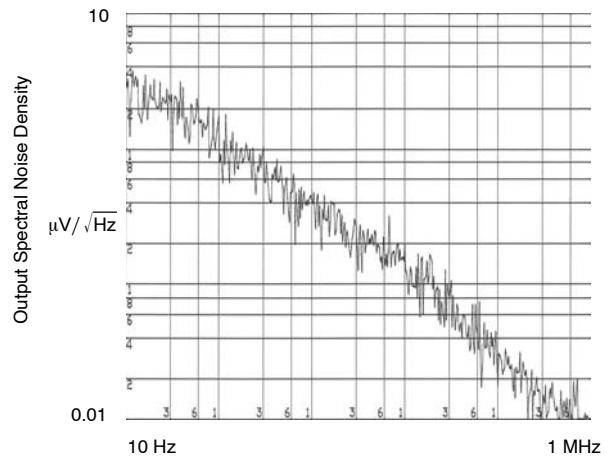
**TYPICAL WAVEFORMS**

**Output Noise**



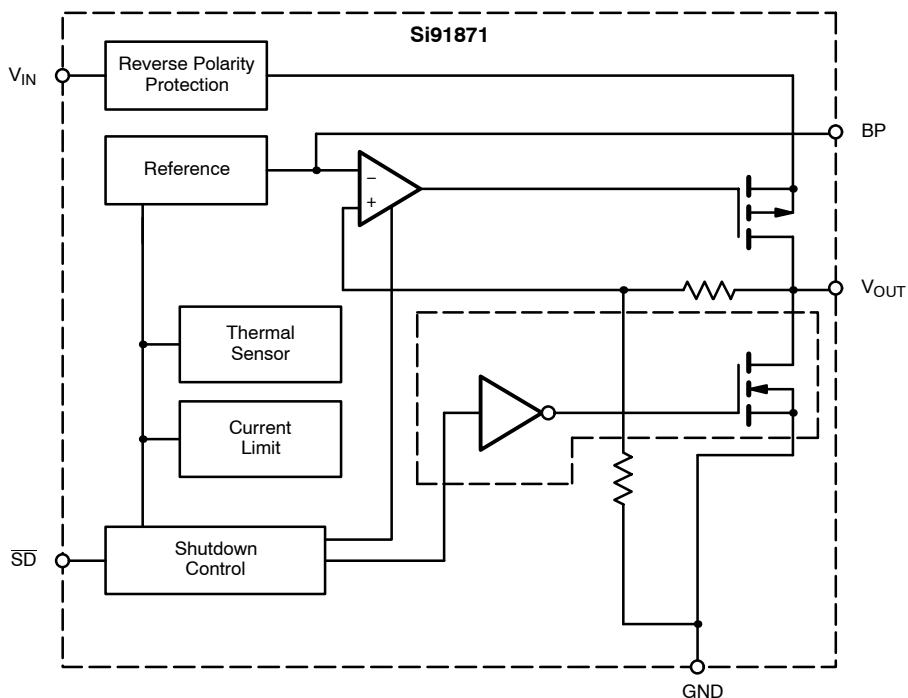
$V_{IN} = 4\text{ V}$   
 $V_{OUT} = 3\text{ V}$   
 $I_{LOAD} = 150\text{ mA}$   
 $C_{NOISE} = 0.01\text{ }\mu\text{F}$   
 $BW = 10\text{ Hz to }100\text{ kHz}$

**Noise Spectrum**



$V_{IN} = 4\text{ V}$   
 $V_{OUT} = 3\text{ V}$   
 $I_{LOAD} = 150\text{ mA}$   
 $C_{NOISE} = 0.01\text{ }\mu\text{F}$

**FUNCTIONAL BLOCK DIAGRAM**





**DETAILED DESCRIPTION**

The Si91871 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint MLP33-5 package. The Si91871 can supply loads up to 300 mA. As shown in the block diagram, the circuit consists of a bandgap reference error, amplifier, p-channel pass transistor and feedback resistor string. An external bypass capacitor connected to the BP pin reduces noise at the output. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection and thermal sensor.

**Thermal Overload Protection**

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°C, the device turns the p-channel pass transistor off.

**Reverse Battery Protection**

The Si91871 has a battery reverse protection circuitry that disconnects the internal circuitry when  $V_{IN}$  drops below the GND voltage. There is no current drawn in such an event. When the  $\overline{SD}$  pin is hardwired to  $V_{IN}$ , the user must connect the  $\overline{SD}$  pin to  $V_{IN}$  via a 100-kΩ resistor if reverse battery protection is desired. Hardwiring the  $\overline{SD}$  pin directly to the  $V_{IN}$  pin is allowed when reverse battery protection is not desired.

**Noise Reduction**

An external 10-nF bypass capacitor at BP is used to create a low pass filter for noise reduction. The start-up time is fast, since a power-on circuit pre-charges the bypass capacitor. After the power-up sequence the pre-charge circuit is switched to standby mode in order to save current. It is therefore not recommended to use larger bypass capacitor values than 50 nF. When the circuit is used without a capacitor, stable operation is guaranteed.

**Auto-Discharge**

The Si91871  $V_{OUT}$  has an internal 100-Ω (typ.) discharge path to ground when the  $\overline{SD}$  pin is low.

**Stability**

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 2 μF @ 300 mA). Since the bandwidth of the error amplifier is around 1–3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.2 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.

**Safe Operating Area**

The ability of the Si91871 to supply current is ultimately dependent on the junction temperature of the pass device.

Junction temperature is in turn dependent on power dissipation in the pass device, the thermal resistance of the package and the circuit board, and the ambient temperature. The power dissipation is defined as

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT}$$

Junction temperature is defined as

$$T_J = T_A + ((P_D * (R_{\theta_{JC}} + R_{\theta_{CA}}))$$

To calculate the limits of performance, these equations must be rewritten.

Allowable power dissipation is calculated using the equation

$$P_D = (T_J - T_A) / (R_{\theta_{JC}} + R_{\theta_{CA}})$$

While allowable output current is calculated using the equation

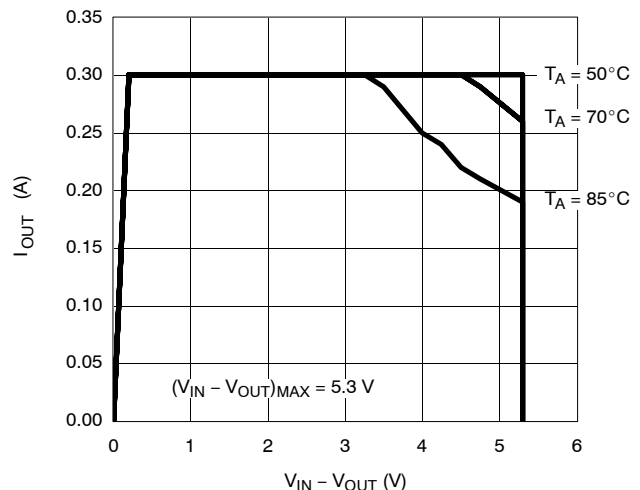
$$I_{OUT} = (T_J - T_A) / (R_{\theta_{JC}} + R_{\theta_{CA}}) * (V_{IN} - V_{OUT})$$

Ratings of the Si91871 that must be observed are

$$T_{Jmax} = 125\text{ }^\circ\text{C}, T_{Amax} = 85\text{ }^\circ\text{C}, (V_{IN} - V_{OUT})_{max} = 5.3\text{ V}, R_{\theta_{JC}} = 8\text{ }^\circ\text{C/W}$$

The value of  $R_{\theta_{CA}}$  is dependent on the PC board used. The value of  $R_{\theta_{CA}}$  for the board used in device characterization is approximately 46 °C/W.

Figure 1 shows the performance limits graphically for the Si91871 mounted on the circuit board used for thermal characterization.



**Figure 1. Safe Operating Area**