

Features

- High speed access times
 - Com'l: 12, 15, 17, 20 and 25 ns
 - Ind'l: 15, 17, 20, 25, and 35 ns
- Low power operation
 - PDM41027SA
 - Active: 400 mW (typ.)
 - Standby: 150 mW (typ.)
 - PDM41027LA
 - Active: 350 mW (typ.)
 - Standby: 100 mW (typ.)
- Single +5V ($\pm 10\%$) power supply
- Packages
 - Plastic SOJ (300 mil) - TSO
 - Plastic SOJ (400 mil) - SO

Description

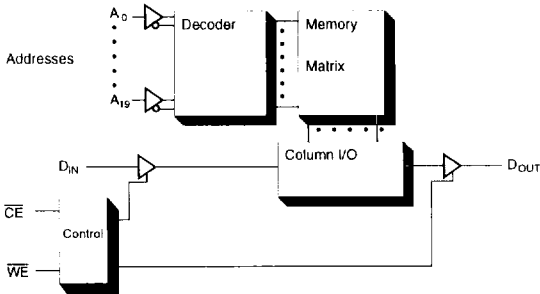
The PDM41027 is a high-performance CMOS static RAM organized as 1,048,576 x 1 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable (\overline{WE}) and the chip enable (\overline{CE}) inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} goes LOW.

The PDM41027 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41027 comes in two versions, the standard power version PDM41027SA and a low power version the PDM41027LA. The two versions are functionally the same and only differ in their power consumption.

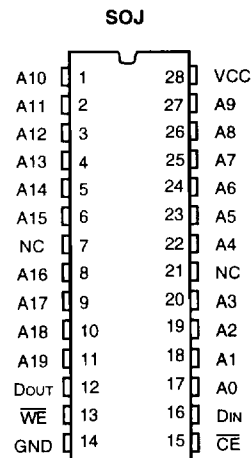
The PDM41027 is available in a 28-pin 400 mil DIP, 28-pin 300 mil SOJ, and a 28-pin 400 mil SOJ for surface mount applications.

4

Functional Block Diagram



Pin Configuration



Truth Table⁽¹⁾

WE	CE	D _{OUT}	MODE
X	H	Hi-Z	Standby
H	L	D _{OUT}	Read
L	L	Hi-Z	Write

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions		PDM41027SA		PDM41027LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	$V_{CC} = \text{MAX.}, V_{IN} = \text{GND to } V_{CC}$	Com'/' Ind.	-5 -10	5 10	-5 -10	2 5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{MAX.},$ $CE = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	Com'/' Ind.	-5 -10	5 10	-5 -10	2 5	μA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			-0.5 ⁽¹⁾	0.8	-0.5 ⁽¹⁾	0.8	V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$ $I_{OL} = 10 \text{ mA}, V_{CC} = \text{Min.}$		—	0.4 0.5	—	0.4 0.5	V V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$		2.4	—	2.4	—	V

NOTE: 1. $V_{IL}(\text{min}) = -3.0\text{V}$ for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter		-12	-15	-17	-20	-25	-35	Unit
I_{CC}	Operating Current $CE = V_{IL}, \text{ and } CE2 = V_{IH}$	SA	230	185	165	155	145	135	mA
	$f = f_{\text{MAX}} = 1/t_{RC}$ $V_{CC} = \text{Max.}$ $I_{OUT} = 0 \text{ mA}$	LA	210	165	155	140	135	125	mA
I_{SB}	Standby Current $CE1 = V_{IH} \text{ or } CE2 = V_{IL}$	SA	70	55	50	45	40	35	mA
	$f = f_{\text{MAX}} = 1/t_{RC}$ $V_{CC} = \text{Max.}$	LA	65	50	45	40	35	30	mA
I_{SB1}	Full Standby Current $CE1 \geq V_{HC} \text{ or } CE2 \leq V_{LC}$	SA	15	10	10	10	10	15	mA
	$f = 0$ $V_{CC} = \text{Max.},$ $V_{IN} \geq V_{CC} - 0.2\text{V} \text{ or } \leq 0.2\text{V}$	LA	10	5	5	5	5	10	mA

NOTES: All values are maximum guaranteed values.

$V_{LC} \leq 0.2\text{V}, V_{HC} \geq V_{CC} - 0.2\text{V}$

Capacitance⁽¹⁾ ($T_A = +25^\circ\text{C}, f = 1.0 \text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

4

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

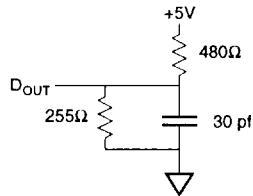


Figure 1. Output Load Equivalent

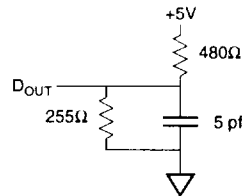


Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZCE} , t_{LZWE} , t_{HZWE})

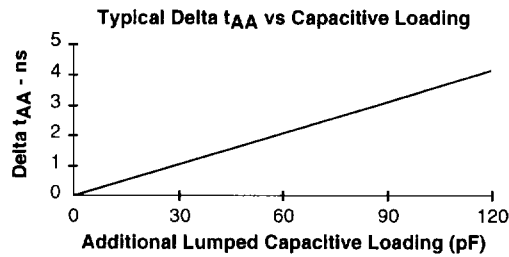
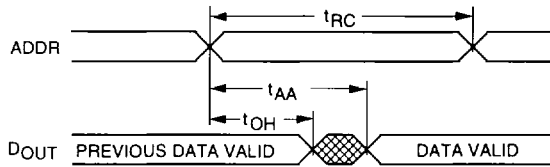
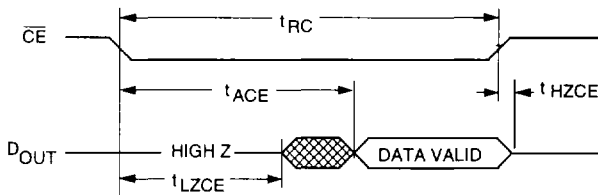


Figure 4.

Read Cycle No. 1^(4, 5)



Read Cycle No. 2^(2, 4, 6)



 UNDEFINED

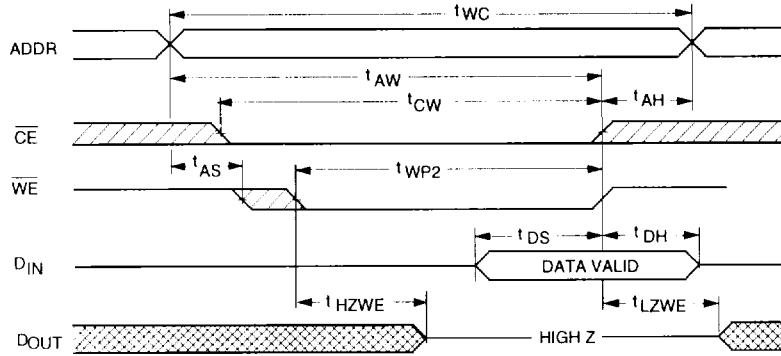
4

AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

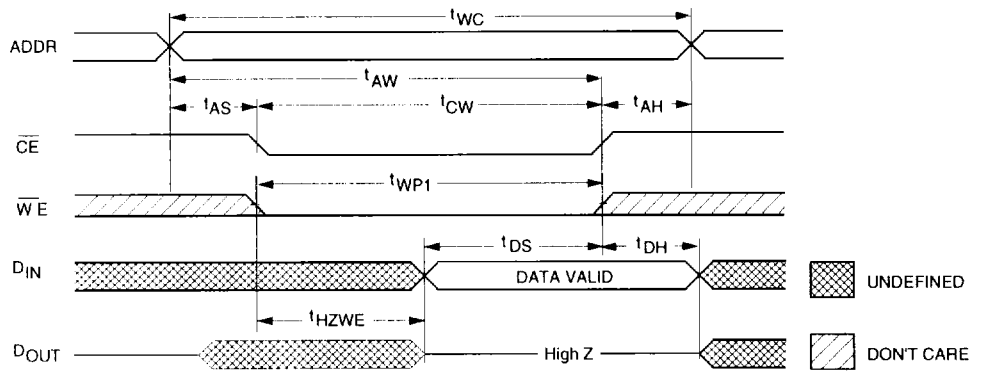
Description		-12 ⁽⁷⁾		-15		-17		-20		-25		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ cycle time	t _{RC}	12		15		17		20		25		35		ns
Address access time	t _{AA}		12		15		17		20		25		35	ns
Chip enable access time	t _{ACE}		12		15		17		20		25		35	ns
Output hold from address change	t _{OH}	3		3		3		3		3		3		ns
Chip enable to output in low Z ^(1, 3)	t _{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z ^(1, 2, 3)	t _{HCZE}		6		7		7		8		10		15	ns
Chip enable to power up time ⁽³⁾	t _{PU}	0		0		0		0		0		0		ns
Chip disable to power down time ⁽³⁾	t _{PD}		12		15		17		20		25		35	ns
Output enable access time	t _{AOE}		6		6		6		6		8		12	ns
Output Enable to output in low Z ^(1, 3)	t _{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z ^(1, 3)	t _{HZOE}		6		6		6		6		8		12	ns

SHADED AREA = PRELIMINARY DATA.
Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)



NOTE: Output Enable (\overline{OE}) is inactive (high)

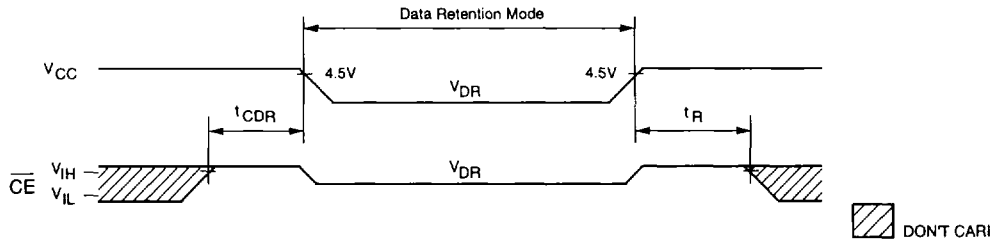
AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

Description	Sym	-12 ⁽⁷⁾		-15		-17		-20		-25		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE Cycle time	t_{WC}	12		15		17		20		25		35		ns
Chip enable access time	t_{CW}	10		15		17		15		15		20		ns
Address Valid to end of write	t_{AW}	10		15		17		15		15		20		ns
Address setup time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP1}	10		10		11		12		15		20		ns
Write pulse width	t_{WP2}	11		13		14		15		15		20		ns
Data setup time	t_{DS}	7		7		7		8		10		15		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low Z ^(1, 3)	t_{LZ}	0		0		0		0		0		0		ns
Write enable to output in high ^(1, 3)	t_{HZWE}		7		7		7		8		10		15	ns

4

SHADED AREA = PRELIMINARY DATA

Low V_{CC} Data Retention Waveform



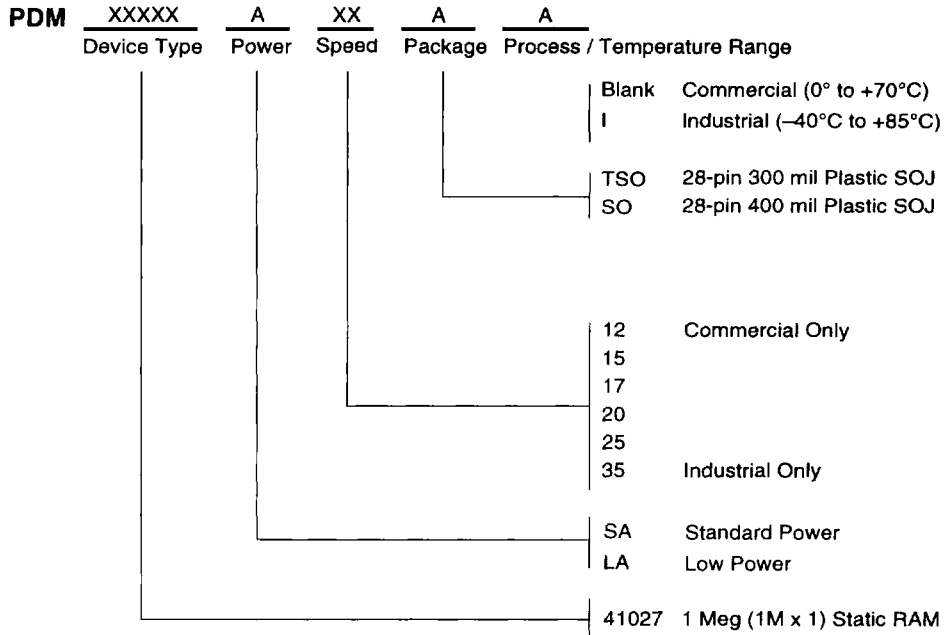
Data Retention Electrical Characteristics (LA Version Only) for JEDEC Version

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data		2	—	—	V
I_{CCDR}	Data Retention Current	$CE1 \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$				
		$V_{CC} = 2V$	—	95	500	μA
		$V_{CC} = 3V$	—	350	750	μA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(3)}$	Operation Recovery Time		$t_{RC}^{(5)}$	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. The parameter is tested with $CL = 5\text{ pF}$ as shown in Fig. #2. Transition is measured $\pm 200\text{ mV}$ from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .
3. This parameter is sampled.
4. WE is HIGH for a READ cycle.
5. The device is continuously selected. All the Chip Enables are held in their active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.

Ordering Information



Chip	Package Type
PDM41027	28-pin Plastic SOJ 300 Mil
	28-pin Plastic SOJ 400 Mil