NN5216405 / NN5216805 series
CMOS 16Mbit (2,097,152 words x 4 bits x 2 banks)
CMOS 16Mbit (1,048,576 words x 8 bits x 2 banks)
Synchronous Dynamic RAM

NPNX

Preliminary Specification

DESCRIPTION

This product is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) organized as 2,097,152 words x4bits x 2banks (NN5216405).1,048,576 words x8bits x 2banks (NN5216805)

This product features a fully synchronous operation referenced to a positive edge of clock input. The read/write operation can be performed in burst mode where data is transferred in either a 2, 4, 8 words or full page (1,024 (NN5216405) / 512 (NN5216805) words) burst accesses, using a two bank architecture, and allows continual read/write operation.

Refresh is accomplished by Auto refresh or Self refresh.

This product is available in 44-pin plastic TSOP TYPE II.

All inputs and outputs are compatible with Low Voltage TTL (LVTTL).

FEATURES

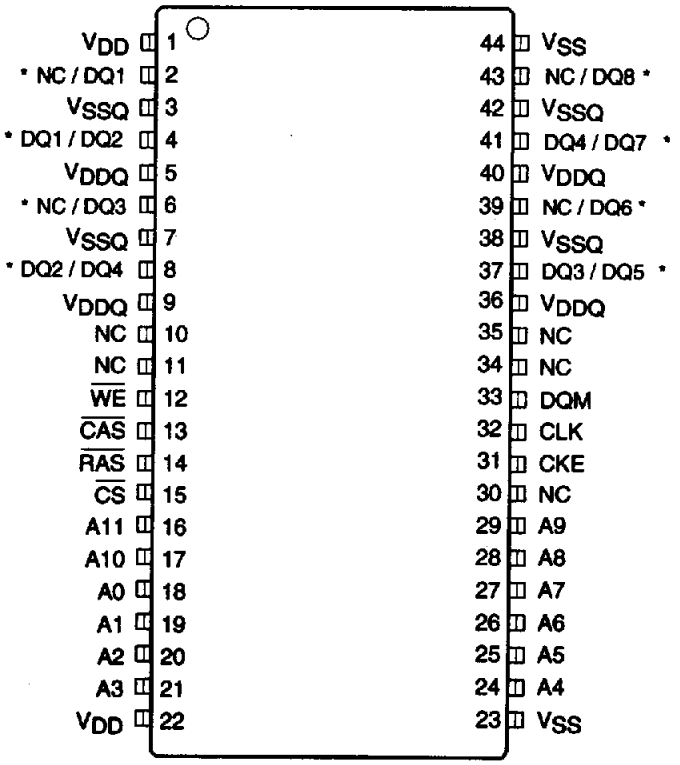
- Organization
  1,048,576words x8bits x2banks (NN5216805)
  2,097,152 words x4bits x 2banks (NN5216405)
- Single 3.3V ±0.3V Power Supply
- Performance Ranges

Parameter		-10	-12
Min. Clock Cycle Time (tCK)	CL=3	10ns	12ns
	CL=2	15ns	18ns
	CL=1	30ns	36ns
Max. RAS Access Time[2] (tRCD+tACK)	CL=3	57ns	63ns
	CL=2	54ns	60ns
	CL=1	55ns	60ns
Max. Read Command Access Time (tACK)	CL=3	27ns	33ns
	CL=2	24ns	30ns
	CL=1	25ns	30ns
Max. CLK Access Time (tAC)	CL=3	7ns	9ns
	CL=2	9ns	12ns
	CL=1	25ns	30ns
Max. Active Command Cycle Time[1] (tRC)		90ns	108ns

NOTE : 1. Same bank
2. Clock cycle = tCK

- Single Pulsed $\overline{RAS}$
- 2 Bank Operation (simultaneously and independently)
- Read/Write Operation Type
  - Burst Read / Write Operation
  - Burst Read / Single Write Operation
- Programmable Burst Sequence
  - Sequential
  - Interleaved
- Programmable Burst Length
  (1, 2, 4, 8, and Full Page)
- Full Page Burst Stop Capability
- Programmable CAS Latency
  (1, 2, and 3)
- Fully LVTTL compatible Inputs/Outputs and Clock
- 4,096 Refresh Cycles / 64ms
- Refresh Modes
  Auto Refresh
  Self Refresh
- High Reliability Package
  Plastic 44pin TSOP TYPE II (P44TP-3B-L)

PIN CONFIGURATION (TOP VIEW)



* NOTE : NN5216405 / NN5216805

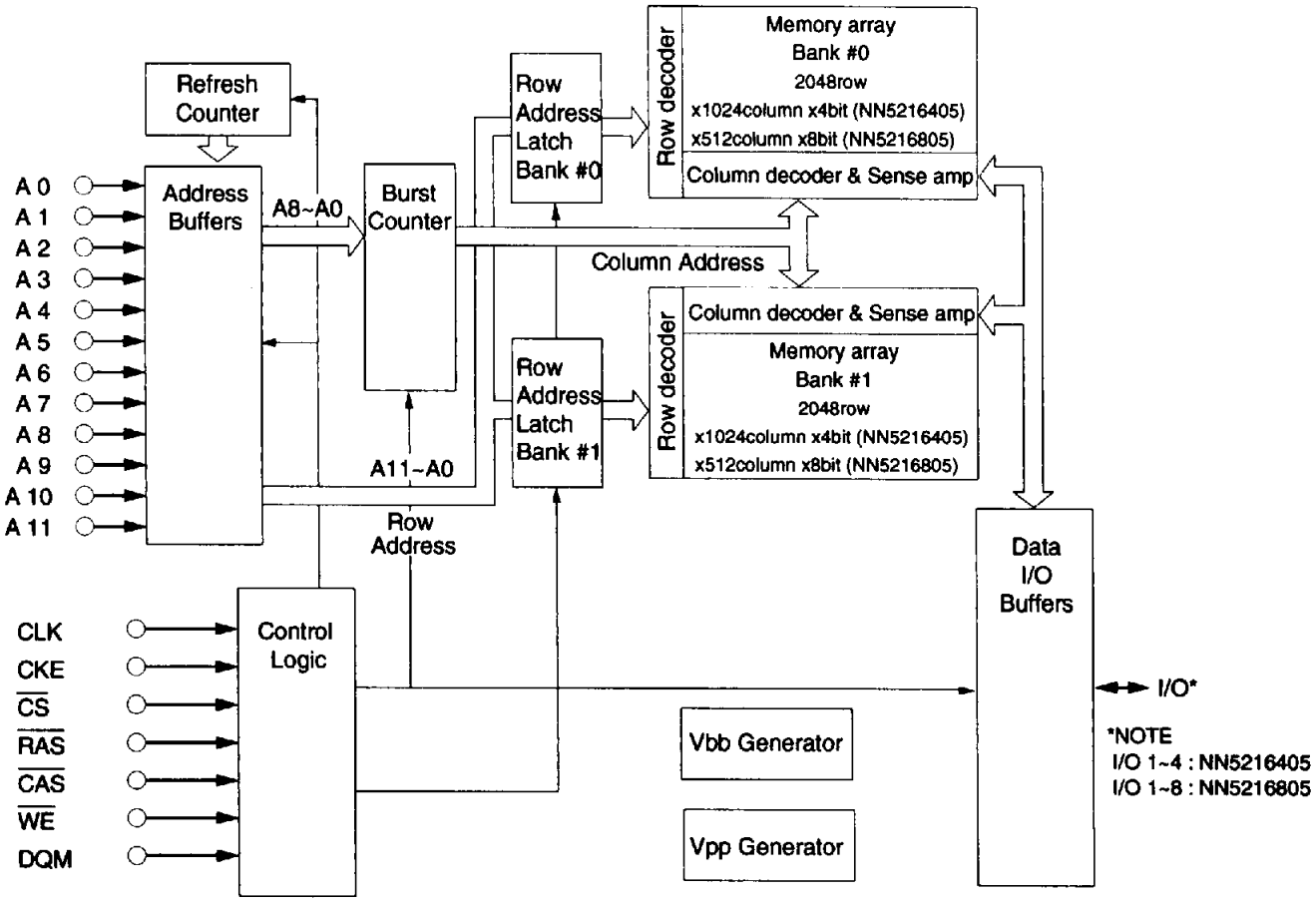
44-pin TSOP TYPE (II)(400mil)

P44TP-3B-L

PIN NAMES

A0 - A11	Address Input Row Address :A0 - A10 Column Address :A0 - A8 Bank Select Address :A11	DQM	Input / Output Mask
		CLK	Clock Input
		CKE	Clock Enable
DQ1 - DQ4 DQ1 - DQ8	Data Input/Output (NN5216405) (NN5216805)	V_{DD}	Power Supply (for Internal Circuit)
$\overline{CS}$	Chip Select	V_{DDQ}	Power Supply (for DQ Buffer) Isolated from V_{DD}
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground (for Internal Circuit)
$\overline{CAS}$	Column Address Strobe	V_{SSQ}	Ground(for DQ Buffer) Isolated from V_{SS}
$\overline{WE}$	Write Enable	NC	No Connection

FUNCTIONAL BLOCK DIAGRAM

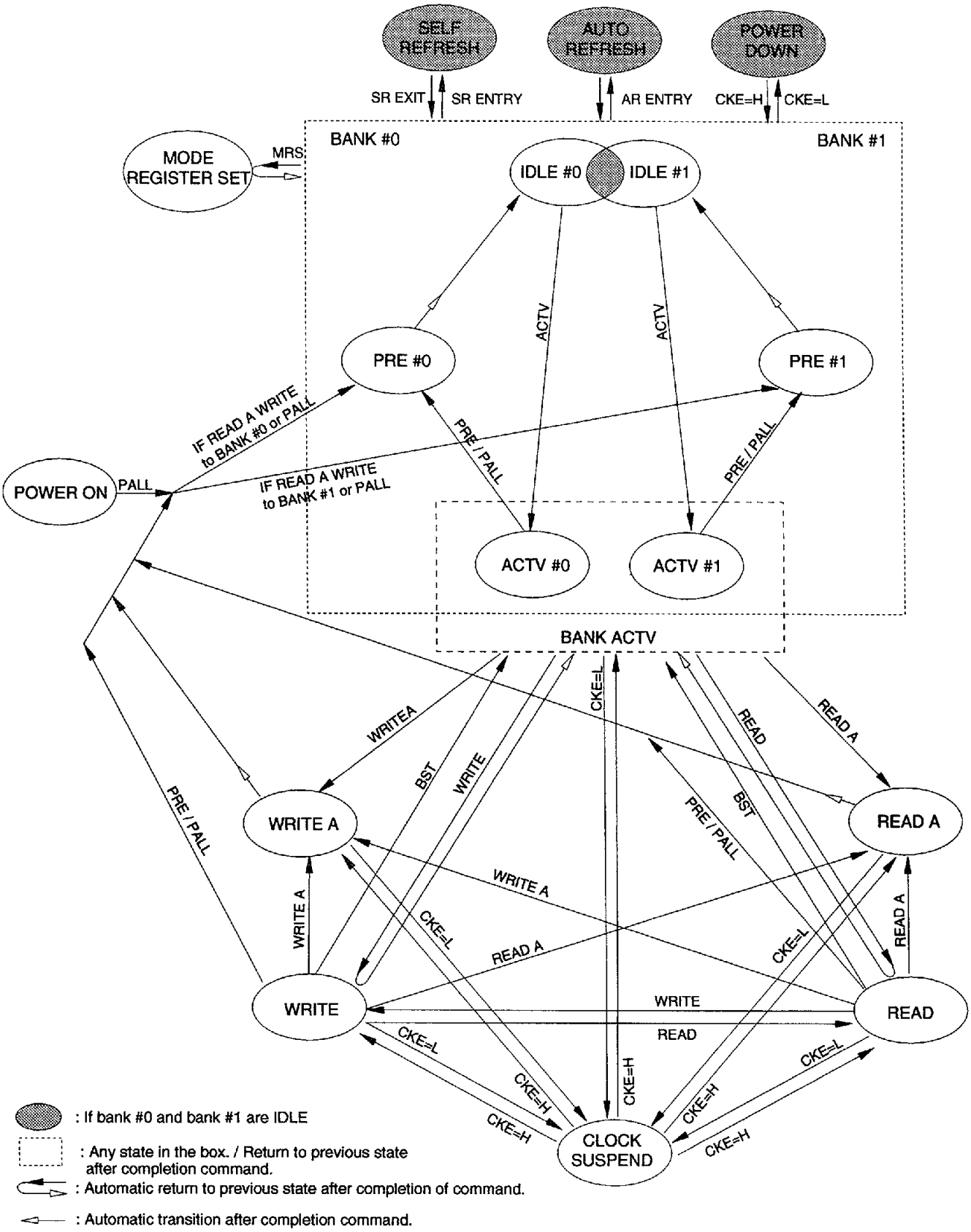


PIN FUNCTIONS

CLK	input	CLK is the master clock. All inputs and data out are referenced to positive edge of CLK.
$\overline{CS}$	input	When $\overline{CS}$ is low, the device starts a command input cycle on rising edge of CLK; if $\overline{CS}$ is high, all new commands are ignored but internal operations are continued.
$\overline{RAS}$ **$\overline{CAS}$** **$\overline{WE}$**	input	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ have the same signal name with conventional DRAMs but different functions. Most of the commands are defined by these pins.
A0 - A11	input	Row Address is determined by A0-A10 in the active command cycle. Column Address is determined by A0-*A9/A8 in the read or write command cycle. Bank Address is determined by A11. During a read or write command cycle, A10 determines if auto-precharge is enabled or disabled. During a precharge command cycle, A10 determines if only the selected bank is precharged or if both banks are precharged. A0-A9 are used to select operating modes during a mode register set command.
CKE	input	CKE determines the device operation of next clock(CLK) cycle. If CKE is high, device is active at the next clock cycle. If CKE is low, the internal clock is suspended and device is not active at the next clock cycle.When in the Idle mode and CKE goes low, the device enters power down mode. To remain in power down mode, CKE must be kept at a low level. When at least one bank is active and CKE goes low, the device enters clock suspend mode.
DQM	input	These pins control Input/Output buffers. During read mode cycle, DQM controls the output buffers. If DQM is high during a read cycle, the associated output buffers assume a high impedance state two clock cycles later. Likewise, if DQM is low during a read cycle, the associated output buffers are enabled (low impedance) two cycles later. DQM control the output impedance state of DQ1 through *DQ4/DQ8 . In write mode cycles, DQM perform as a write mask. If DQM is high, the input data is not written.
DQ	input /output	These pins are the data input/output lines of SDRAM. DQ0 - DQ3 : NN5216405 DQ0 - DQ7 : NN5216805
V_{DD} **V_{SS}**	power supply	VDD and VSS are power supply pins for internal circuits.
V_{DDQ} **V_{SSQ}**	power supply	V_{DDQ} and V_{SSQ} are power supply pins for output buffers. V_{DDQ} and V_{SSQ} are isolated from V_{DD} and V_{SS}.

*NOTE : NN5216405 / NN5216805

Simplified State Diagram



EXPLANATION OF COMMANDS

1	**Mode Register Set**	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low , A0-A11 = OP-Code
Mode register defines how the device operates. A0-A11 are operation codes (OP-Codes) in this cycle. The default value of the mode register after power-on is undefined. Therefore, this command must be executed to set the mode register before any other commands are executed.		
2	**Bank Active**	$\overline{CS}$, $\overline{RAS}$ = Low , $\overline{CAS}$, $\overline{WE}$ = High , A11 = Bank , A0-A10 = Row Address
Bank Active command activates a bank selected by A11. Row addresses are latched on A0 to A10 at the time of this command and the cell data is read out to the sense amplifiers. This command corresponds to $\overline{RAS}$ going low on conventional DRAM's.		
3	**Read**	$\overline{CS}$, $\overline{CAS}$ = Low , $\overline{RAS}$, $\overline{WE}$ = High , A11 = Bank , A10 = Low A0-*A9/A8 = Column Address
Read command initiates a burst read operation to the bank selected by A11. Burst start address is given by A0-*A9/A8 (column address). After a read burst has completed, the output buffers become High-Z.		
4	**Read with Auto-Precharge**	$\overline{CS}$, $\overline{CAS}$ = Low , $\overline{RAS}$, $\overline{WE}$ = High , A11 = Bank , A10 = High A0-*A9/A8=Column Address
Read with Auto-Precharge command initiates an automatic precharge operation after the completion of a read burst operation. When the burst length is full page, this command is illegal.		
5	**Write**	$\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = Low , $\overline{RAS}$ = High , A11 = Bank , A10 = Low A0-*A9/A8 = Column Address
Write command initiates a burst write operation to the bank selected by A11. Burst start address is given by A0-*A9/A8 (column address). When the single write mode (WT=1 in Mode Register), this command initiates a single write operation to the selected bank. In this case data is only written to the location specified by A0-*A9/A8.		
6	**Write with Auto-Precharge**	$\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = Low , $\overline{RAS}$ = High , A11 = Bank , A10 = High A0-*A9/A8 = Column Address
Write with Auto-Precharge command initiates an automatic precharge operation after the completion of a write burst operation. When the burst length is full page, this command is illegal.		
7	**Single Bank Precharge**	$\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low , $\overline{CAS}$ = High , A11 = Bank, A10 = Low A0-A9 = Don't care
Single Bank Precharge command precharges the bank selected by A11. The precharged bank is switched from the active state to the idle state.		

*NOTE : NN5216405 / NN5216805

EXPLANATION OF COMMANDS (cont.)

8	**Precharge All Bank**	$\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low , $\overline{CAS}$ = High , A10 = High , A0-A9 / A11 = Don't care
Precharge All Banks command precharges both banks simultaneously. Both banks are switched to the idle state.		
9	**Auto Refresh**	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = Low , $\overline{WE}$ = High , A0-A11 = Don't care , CKE = High
Auto-Refresh command initiates auto refresh operation. Auto-refresh is the same as CAS-before-RAS refresh on conventional DRAMs. Row addresses are generated by internal refresh counter. The refresh operation must be performed 4096 times within 64ms. Before executing auto refresh, the device must be in the Idle state. After this cycle, precharge command is not necessary. Precharge operation starts automatically after a refresh operation.		
10	**Burst Stop**	$\overline{CS}$, $\overline{WE}$ = Low , $\overline{RAS}$, $\overline{CAS}$ = High , A0-A11 = Don't care
Burst Stop command stops full page burst operation. Full page burst continues until this command is issued. If burst mode is not full page, this command is ignored.		
11	**Enter Self-Refresh**	CKE = Low , $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = Low , $\overline{WE}$ = High , A0-A11 = Don't care
Once in Self-Refresh mode, self refresh operation is maintained as long as CKE stays low. While in self refresh mode, the refresh operation is automatically performed, so there is no need to control refresh operation externally. The self refresh mode is exited by Exit Self-Refresh command.		
12	**Exit Self-Refresh**	CKE = High , $\overline{CS}$ = Low , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High or $\overline{CS}$ = High
Exit Self-Refresh command is used to exit from the self refresh mode. After exiting from self refresh mode, both banks are in the idle state.		
13	**No Operation**	$\overline{CS}$ = Low , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High , A0-A9 = Don't care
No Operation command initiates nothing. This command is similar to Device Deselect command.		
14	**Device Deselect**	$\overline{CS}$ = High , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, A0-A11 = Don't care
When Device Deselect command is executed, the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address input are ignored. This command is similar to No Operation command.		
15	**Enter Power Down**	CKE = Low
When both banks are in the idle state, Enter Power Down command switches device into the power down mode. In the power down mode, all input and output buffers are turned off.		
16	**Exit Power Down**	CKE = High , $\overline{CS}$ = Low , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High or CKE, $\overline{CS}$ = High
Exit Power Down command is used to exit from power down mode. After exiting this mode, both banks are in the idle state.		

EXPLANATION OF COMMANDS (cont.)

17	**Enter Clock Suspend**	CKE = Low
When either bank is in the active state, Enter Clock Suspend command switches device into the clock suspend mode. The device operation is held while CLK is low.		
18	**Exit Clock Suspend**	CKE = High, $\overline{CS}$ = Low , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High , or CKE, $\overline{CS}$ = High
Exit Clock Suspend command is used to exit from clock suspend mode.		

COMMAND OPERATION

Simplified Functional Truth Table

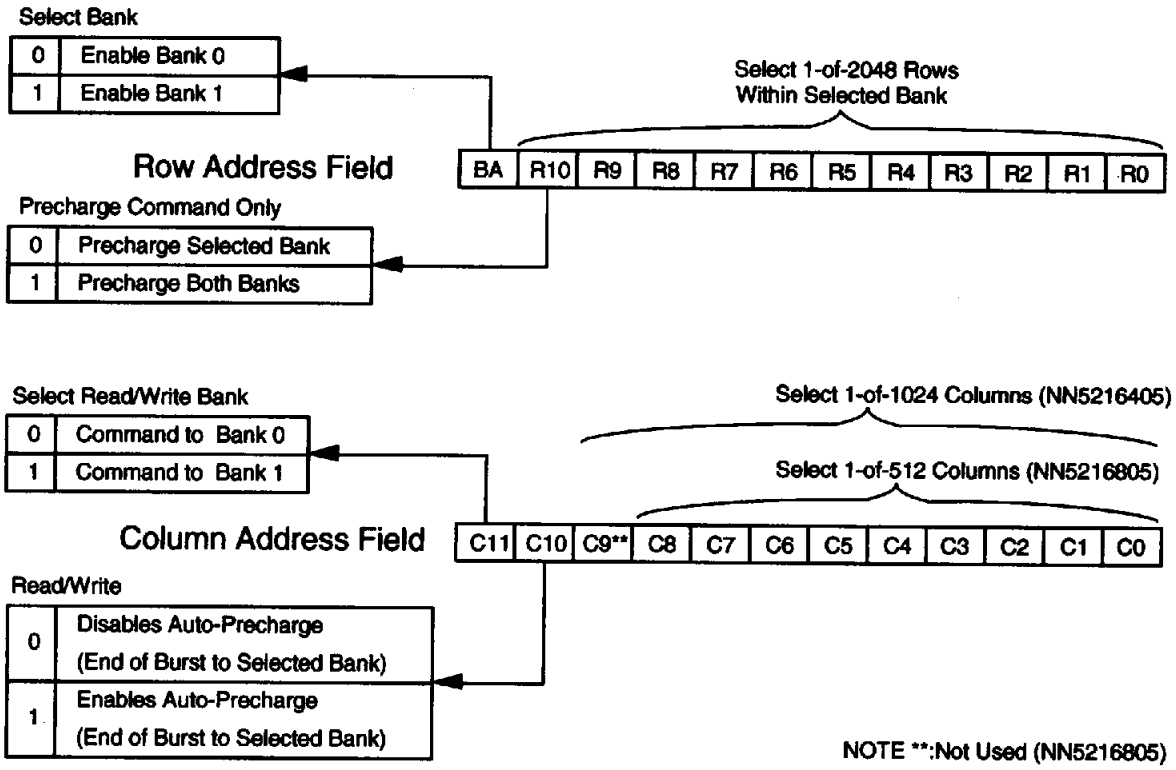
	Function	Command	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9	A8-A0
1	Mode Register Set [4]	MRS	H	X[5]	L	L	L	L	X	← Op-Code →			
9	Auto-Refresh (CBR-Refresh)	REF	H	H	L	L	L	H	X	X	X	X	X
11	Enter Self-Refresh	SELF	H	L[6]	L	L	L	H	X	X	X	X	X
12	Exit Self-Refresh	XSELF	L	H	L	H	H	H	X	X	X	X	X
			L	H	H	X	X	X	X	X	X	X	X
2	Bank Active	ACTV	H	X[5]	L	L	H	H	X	BA	← Row →		
3	Read	READ	H	X[5]	L	H	L	H	H/L[1]	BA	L	*Col/X	Col
4	Read with Auto-Precharge	READA	H	X[5]	L	H	L	H	H/L[1]	BA	H	*Col/X	Col
10	Burst Stop	BST	H	X[5]	L	H	H	L	X	X	X	X	X
5	Write	WRITE	H	X[5]	L	H	L	L	H/L[2]	BA	L	*Col/X	Col
6	Write with Auto-Precharge	WRITEA	H	X[5]	L	H	L	L	H/L[2]	BA	H	*Col/X	Col
7	Single Bank Precharge	PRE	H	X[5]	L	L	H	L	X	BA	L	X	X
8	Precharge All Banks	PALL	H	X[5]	L	L	H	L	X	X	H	X	X
13	No Operation	NOP	H	X[5]	L	H	H	H	X	X	X	X	X
14	Device Deselect	DESEL	H	X[5]	H	X	X	X	X	X	X	X	X
15	Clock Suspend	CLKS	L	L[6]	X	X	X	X	X	X	X	X	X
17	Power Down	PD											
16	Exit Clock Suspend	XCLKS	L	H	L	H	H	H	X	X	X	X	X
18	Power Down	XPD	L	H	H	X	X	X	X	X	X	X	X

*NOTE : NN5216405 / NN5216805

Notes :

1. Operation depends on the state of DQM;
   if DQM=H, then the associated output is High-Z after 2 clock latency
   and if DQM=L then the associated output is Low-Z after 2 clock latency.
2. Operation depends on the state of DQM;
   if DQM=H, then the associated byte is not written
   but if DQM=L, then the associated byte data is written.
3. Device that has one or more banks active will enter "Clock Suspend" and device that has all banks "Idle" will enter "Power Down".
4. Banks do not have to be in "Idle" state to execute these commands, but read or write operations simultaneously with these commands are prohibited.
5. If CKE=L, then a "Clock Suspend" or "Power Down" will occur on next clock cycle.
6. CKE(n) must remain low in order to remain in "Clock Suspend" or in "Power Down" mode.
   When in "Power Down" mode, exiting occurs when CKE(n) goes high, but "NOP" must be executed during exiting.
   When in "Clock Suspend", CKE(n) going high exits "Clock Suspend" mode and normal operation will be resumed on the next clock.

ROW/COLUMN ADDRESS FIELDS



FUNCTIONAL TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Address	Action	Note
Idle	H	X	X	X	DESEL	X	NOP	
	L	H	H	H	NOP	X	NOP	
	L	H	H	L	BST	X	ILLEGAL	2
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	2
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	2
	L	L	H	H	ACTV	RA11(BA),RA10	Bank Active, RA Latch	
	L	L	H	L	PRE	RA11(BA),RA10	NOP	
	L	L	L	H	REF	X	Auto-Refresh	
	L	L	L	L	MRS	OP-code	Mode Register Set	
	UNDEFINED			-	-		ILLEGAL	
Row Active	H	X	X	X	DESEL	X	NOP	
	L	H	H	H	NOP	X	NOP	
	L	H	H	L	BST	X	NOP	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	Begin Read,Latch CA,Determine AP	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	Begin Write,Latch CA,Determine AP	
	L	L	H	H	ACTV	RA11(BA),RA10	ILLEGAL	
	L	L	H	L	PRE	RA11(BA),RA10	Precharge	
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	Mode Register Set**	
	UNDEFINED			-	-		ILLEGAL	
Read	H	X	X	X	DESEL	X	NOP(Continue Burst, Bank remains Active)	
	L	H	H	H	NOP	X	NOP(Continue Burst, Bank remains Active)	
	L	H	H	L	BST	X	NOP (Bank remains Active) BL≠FP:Continue Burst BL=FP:Term Burst)	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	Term Burst,New Read,Determine AP	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	Term Burst,Start Write,Determine AP	
	L	L	H	H	ACTV	RA11(BA),RA10	ILLEGAL	
	L	L	H	L	PRE	RA11(BA),RA10	Term Burst,Precharge Timing for Read	
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	
Write	H	X	X	X	DESEL	X	NOP(Continue Burst Bank remains Active)	
	L	H	H	H	NOP	X	NOP(Continue Burst Bank remains Active)	
	L	H	H	L	BST	X	NOP(Bank remains Active BL≠FP:Continue Burst BL=FP:Term Burst)	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	Term Burst,Start Read,Determine AP	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	Term Burst,New Write,Determine AP	
	L	L	H	H	ACTV	RA11(BA),RA10	ILLEGAL	
	L	L	H	L	PRE	RA11(BA),RA10	Term Burst,Precharge Timing for Read	
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	

*NOTE : NN5216405 / NN5216805

FUNCTIONAL TRUTH TABLE (cont.)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Address	Action	Note
Read With Auto Precharge	H	X	X	X	DESEL	X	NOP(Continue Burst to End Then Precharge)	
	L	H	H	H	NOP	X	NOP(Continue Burst to End Then Precharge)	
	L	H	H	L	BST	X	ILLEGAL	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	L	H	H	ACTV	RA11(BA),RA10	ILLEGAL	2
	L	L	H	L	PRE	RA11(BA),RA10	ILLEGAL	2
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	
Write With Auto Precharge	H	X	X	X	DESEL	X	NOP(Continue Burst to End Then Precharge)	
	L	H	H	H	NOP	X	NOP(Continue Burst to End Then Precharge)	
	L	H	H	L	BST	X	ILLEGAL	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	L	H	H	ACTV	RA11(BA),RA10	ILLEGAL	2
	L	L	H	L	PRE	RA11(BA),RA10	ILLEGAL	2
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	
Precharging	H	X	X	X	DESEL	X	NOP, Idle after t_{PR}	
	L	H	H	H	NOP	X	NOP, Idle after t_{PR}	
	L	H	H	L	BST	X	ILLEGAL	2
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	2
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	2
	L	L	H	H	ACT	RA11(BA),RA10	ILLEGAL	2
	L	L	H	L	PRE	RA11(BA),RA10	NOP	
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	
Row Activating	H	X	X	X	DESEL	X	NOP Bank Active After t_{RCD}	
	L	H	H	H	NOP	X	NOP Bank Active After t_{RCD}	
	L	H	H	L	BST	X	ILLEGAL	2
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	2
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	2
	L	L	H	H	ACT	RA11(BA),RA10	ILLEGAL	2
	L	L	H	L	PRE	RA11(BA),RA810	ILLEGAL	2
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	

*NOTE : NN5216405 / NN5216805

FUNCTIONAL TRUTH TABLE (cont.)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Address	Action	Note
Write	H	X	X	X	DESEL	X	NOP,Row Active After t_{WR}/t_{BWR}	
Recovering	L	H	H	H	NOP	X	NOP ,Row Active After t_{WR}/t_{BWR}	
	L	H	H	L	BST	X	ILLEGAL	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	Start Read, Determine AP	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	Start Read, Determine AP	
	L	L	H	H	ACT	RA11(BA),RA10	ILLEGAL	2
	L	L	H	L	PRE	RA11(BA),RA10	ILLEGAL	2
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	
Refreshing	H	X	X	X	DESEL	X	NOP, Idle After t_{RC}	
	L	H	H	H	NOP	X	NOP, Idle After t_{RC}	
	L	H	H	L	BST	X	ILLEGAL	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	L	H	H	ACT	RA11(BA),RA10	ILLEGAL	
	L	L	H	L	PRE	RA11(BA),RA10	ILLEGAL	
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	
Mode Register	H	X	X	X	DESEL	X	NOP	
Accessing	L	H	H	H	NOP	X	NOP	
	L	H	H	L	BST	X	ILLEGAL	
	L	H	L	H	READ/READA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	H	L	L	WRITE/WRITEA	CA11(BA),CA10,*CA9/8-CA0	ILLEGAL	
	L	L	H	H	ACT	RA11(BA),RA10	ILLEGAL	
	L	L	H	L	PRE	RA11(BA),RA10	ILLEGAL	
	L	L	L	H	REF	X	ILLEGAL	
	L	L	L	L	MRS	OP-code	ILLEGAL	
	UNDEFINED			-	-		ILLEGAL	

*NOTE : NN5216405 / NN5216805

Notes :

1. All entries assume that CKE was active (High) during the preceding clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Device dose not require "2n-rule" , but minimum timing between commands are specified.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (A11) and RA10.
5. If illegal states are executed, the device operation and data-integrity are not guaranteed.

MODE REGISTER CONFIGURATION

Mode register has 5 fields.

A11 - A8: Write Type
A7: (Must be a " 0 ")
A6 - A4: CAS Latency
A3: Burst Type
A2 - A0: Burst Length

Mode Register Options

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Function
WT				0	LTMODE			BT	BL			Mode Register Set

WT: Write

WT	Write Type
0000	Burst Read and Burst Write
XX01	Reserved
XX10	Burst Read and Single Write
XX11	Reserved

BT: Burst Type

BT	Burst Type
0	Sequential
1	Interleave

LTMODE: Latency Mode

LTMODE	CAS Latency
000	Reserved
001	1
010	2
011	3
100	Reserved
101	Reserved
110	Reserved
111	Reserved

BL: Burst Length

BL	Burst Length	
	BT=0	BT=1
000	1	1
001	2 (Modulo-2)	2
010	4 (Modulo-4)	4
011	8 (Modulo-8)	8
100	Reserved	Reserved
101	Reserved	Reserved
110	Reserved	Reserved
111	Full Page [1]	Reserved

Notes :
1. Length of full page burst is *1024/512 (*1024 4 - bit words / 512 8 - bit words). When the burst pointer reaches column address = *1023/511, then the pointer wraps around to column address = 0. Auto-precharge is disabled when full page burst is enabled.
2. BL values of 100, 101, and 110 for Sequential and 100, 101, 110, and 111 for Interleave are defined as "Reserved" in JEDEC specification.

*NOTE : NN5216405 / NN5216805

BURST SEQUENCE

Burst Length	Wrap Type	
	Sequential (Modulo-N) (JEDEC Standard)	Interleave (JEDEC Standard)
2	Sequential, Modulo - 2	Interleave
	0 - 1	0 - 1
	1 - 0	1 - 0
4	Sequential, Modulo - 4	Interleave
	0 - 1 - 2 - 3	0 - 1 - 2 - 3
	1 - 2 - 3 - 0	1 - 0 - 3 - 2
	2 - 3 - 0 - 1	2 - 3 - 0 - 1
	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8	Sequential, Modulo - 8	Interleave
	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
Full Page	Sequential, Modulo -*1024/512	Interleave
	CA(s),CA(s+1),..,CA(s+*1022/510)	Reserved
	CA(*1023/511),CA(0),....	Not Presently Defined

CA: Column Address

OPERATION

Read / Write

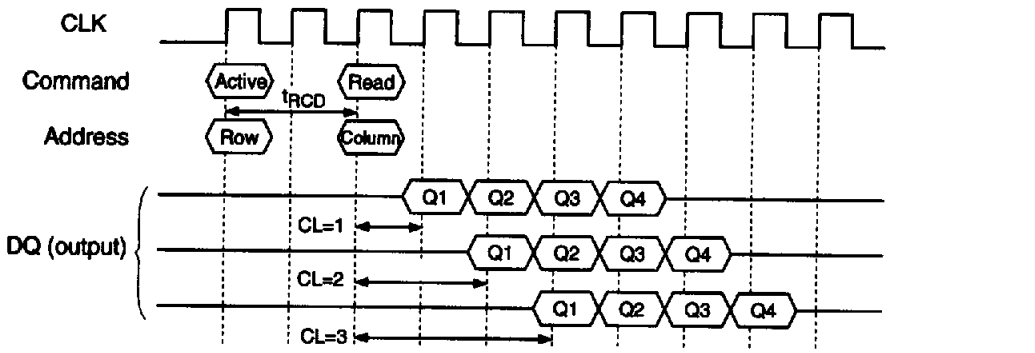
Bank Active

Before executing a read or write operation, Bank Active command must be issued. In a bank Active command cycle, either bank 0 or bank 1 is selected by BA(A11), and the row address is selected by A0 to A10.
An interval of t_{RCD} is required between Bank Active command and Read or Write command.

Read

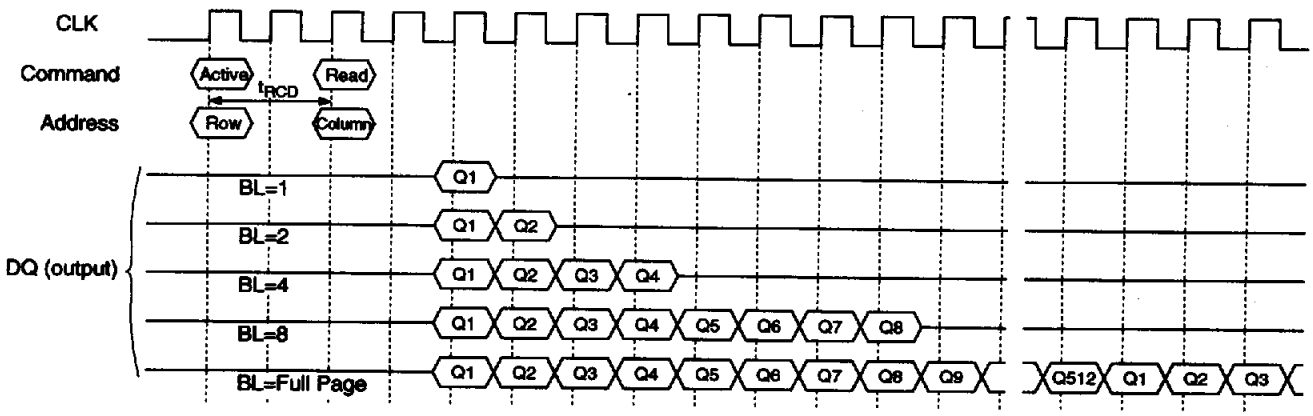
When Read command is issued, a burst read operation is performed. In a Read command cycle, the bank select address and the column address is asserted by A11 and A0 to A8. Data output starts after the number of cycles specified by the CAS latency. The CAS latency can be set to 1, 2 or 3. The burst length can be set to 1, 2, 4, 8 or full page. The start address for a burst read is specified by A0 to A8. When the burst length is 1, 2, 4 or 8, the output buffers automatically become High-Z after the completion of a read burst operation. When the burst length is full page, a read operation continues until Burst Stop command is issued.

CAS Latency for Reads



CL : CAS Latency
Burst Length = 4

Burst Length for Reads



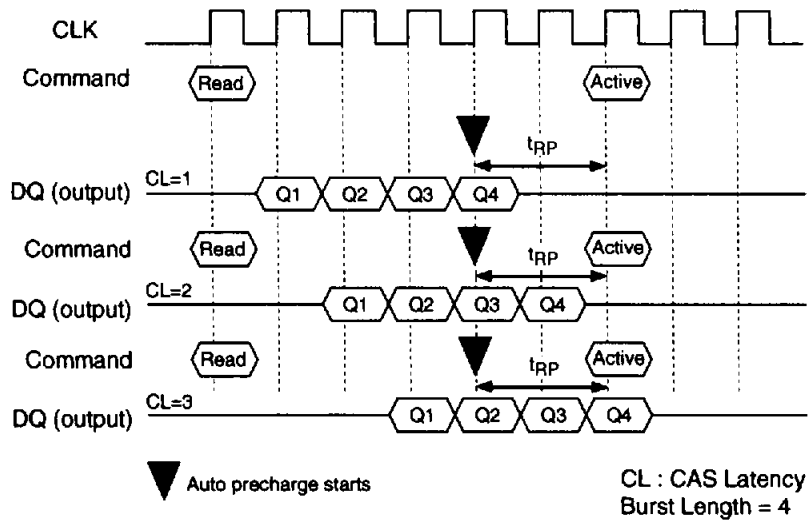
BL : Burst Length
CAS Latency = 2

Read / Write (cont.)

Read with Auto-Precharge

Read with auto-precharge operation is a function to execute automatic precharge operation after the completion of a read burst operation. An interval of t_{RP} is required between the start point of Auto-Precharge and next Bank Active command of the same bank. When the burst length is full page, this operation cannot be used.

Read with Auto-Precharge



Read / Write (cont.)

Write

When Write command is issued, a burst write or single write operation is performed. Burst write or single write mode is selected by WT (A11-A8) of the mode register. When WT is 0000, a burst write operation is enabled. When WT is XX01, a single write operation is enabled. In Write command cycle, the bank select address and the column addresses are asserted by A11 and A0 to A8.

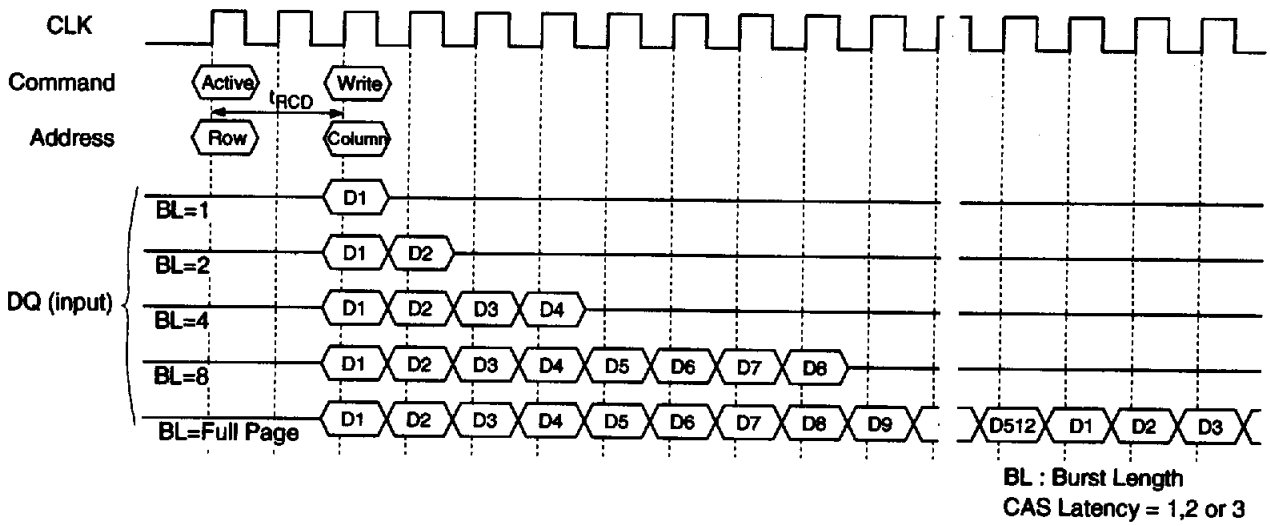
Burst Write

A burst write operation starts in the same cycle of Write command for all CAS latency . The burst length can be set to 1,2,4,8 and full page. A11 and A0 to A8 is also used as a start address of a burst write operation.

Single Write

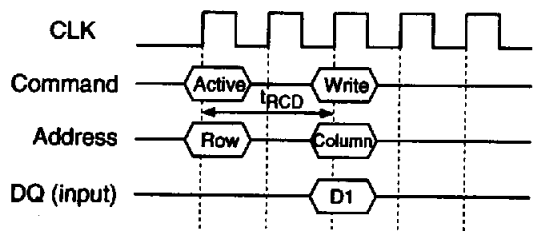
In a single write operation, data is only written to the column address of the selected bank at the Write command cycle without regard to the burst length setting.

Burst Write



BL : Burst Length
CAS Latency = 1,2 or 3

Single Write



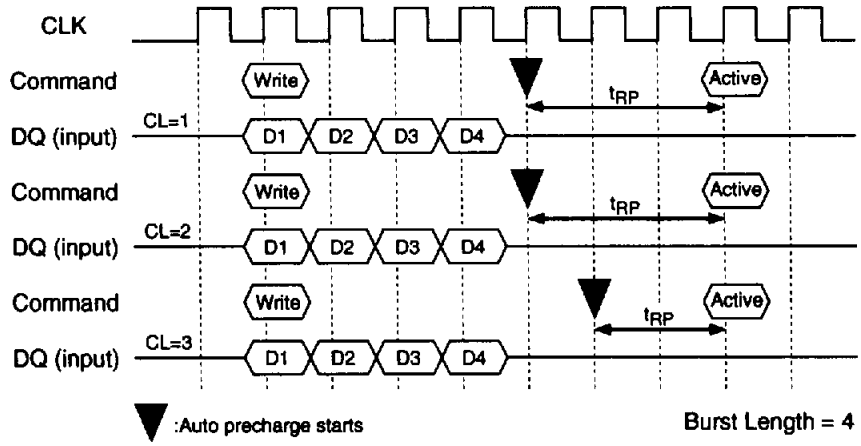
Burst Length = 1,2,4,8 or Full Page
CAS Latency = 1,2 or 3

Read / Write (cont.)

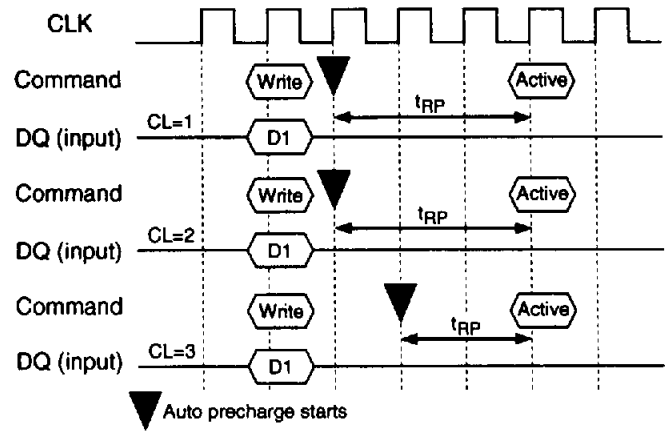
Write with Auto-Precharge

Write with auto-precharge operation is a function to execute automatic precharge operation after a write operation. An interval of t_{RP} is required between the start point of Auto-Precharge and next Bank Active command of the same bank. When the burst length is full page, this operation cannot be used.

Burst Write with Auto-Precharge



Single Write with Auto-Precharge



Precharge

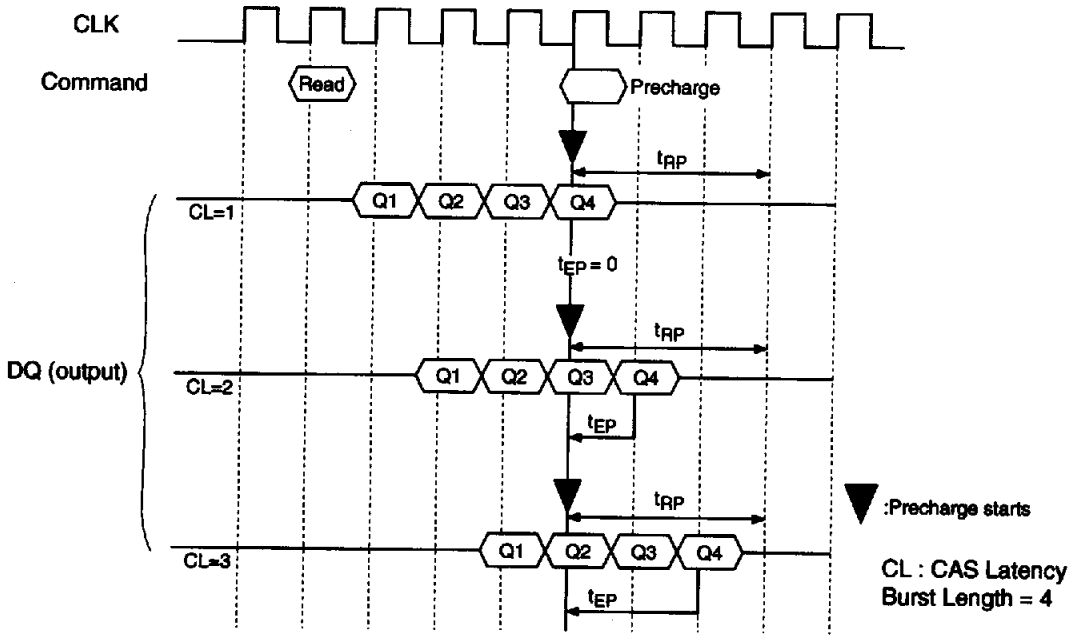
Read to Precharge Command

An interval between Read command and Precharge command is minimum 1clock.

To read all data

Precharge command makes the output buffer High-Z when the precharge bank is the same bank as accessed with the previous Read command. If all of the burst locations are to be read, the Precharge command must not be issued earlier than the t_{EP} interval. The t_{EP} is an interval between the final data output and Precharge command to ensure that all data are read.

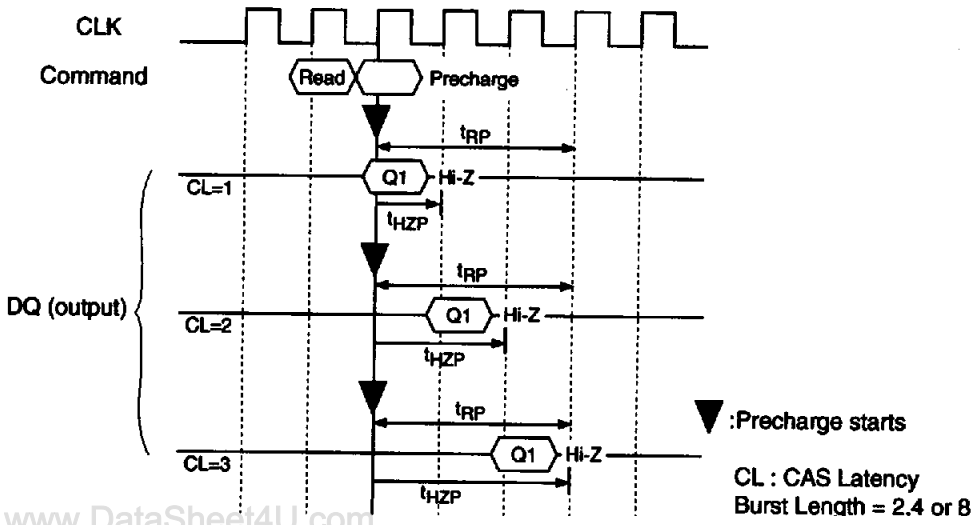
Read to Precharge Command : To read all data in burst sequence



To stop reading data

Precharge command makes output buffer High-Z after the cycles defined t_{HZP}.

Read to Precharge Command : To stop reading data



Precharge (cont.)

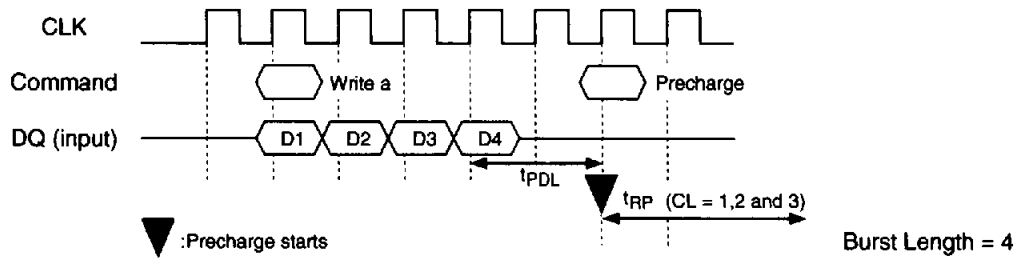
Write to Precharge Command

An interval between Write command and Precharge command is minimum 1clock.

To write all data

If it is necessary to write all of input data, Precharge command must be asserted after the cycle defined by t_{PDL}.
The t_{PDL} is an interval between the final data input and Precharge command to ensure that all data are written.

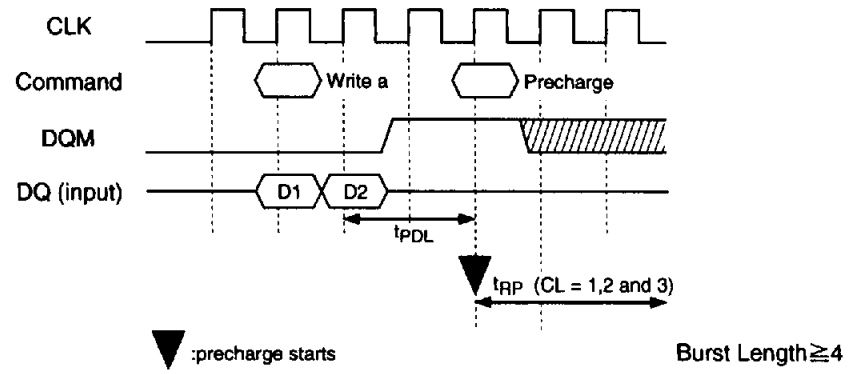
Write to Precharge Command : To write all data



To stop writing data

If Precharge command is asserted during a write operation, the input data must be masked by setting DQM high for assurance of the cycle defined by t_{PDL}.

Write to Precharge Command : To stop writing data



Full Page Burst Stop

A full page burst read or write operation can be terminated by Burst Stop command. Burst Stop command will terminate Full Page and non-wrapped Sequential bursts (Mode Register : BL(MSB)=1 and BT=0). Burst Stop command will not terminate wrapped Sequential (modulo-n; n = 2, 4, or 8) bursts or Interleave bursts (Mode Register : BL(MSB)=0).

Full Page Burst Read

When CAS latency is 1, data remains valid in the same cycle as Burst Stop command, and output buffer goes to High-Z in the next cycle.

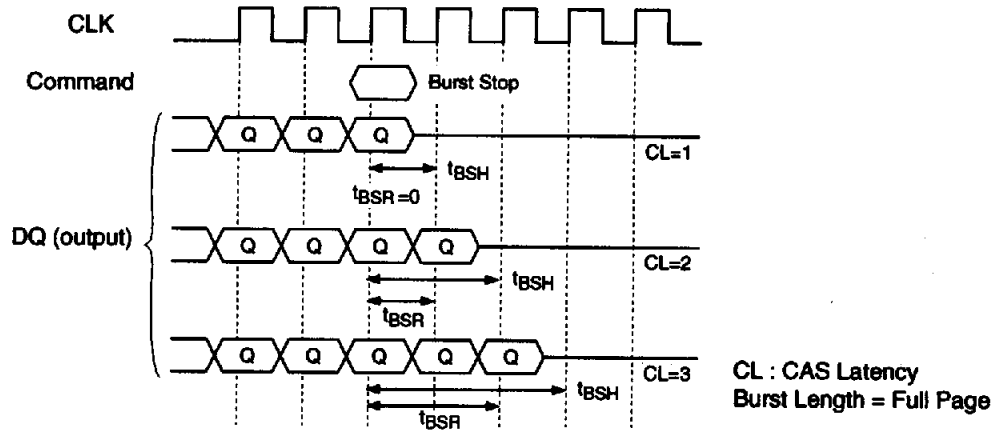
When CAS latency is 2, data remains valid in one clock cycle after Burst Stop command, and output buffer goes to High-Z in the next cycle.

When CAS latency is 3, data remains valid in two clock cycles after Burst Stop command,and output buffer goes to High-Z in the next cycle.

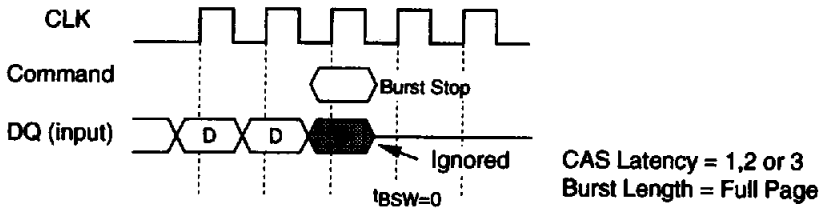
Full Page Burst Write

In all cases of CAS latency, no data is written in same cycle as Burst Stop command.

Full Page Burst Read Stop



Full Page Burst Write Stop

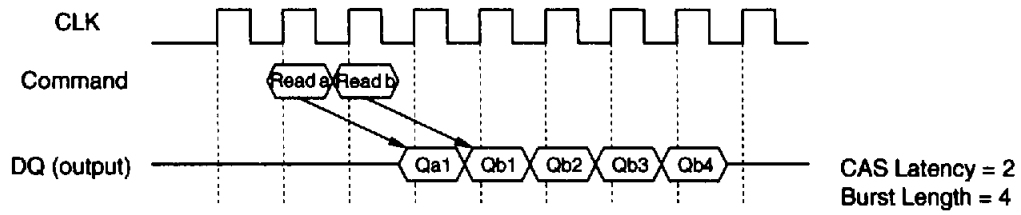


Command Intervals

Read to Read Command Interval

During burst read operation, when new Read command is issued, the previous burst read is interrupted and the new burst read starts after the number of cycles specified by CAS latency. An interval between the commands is minimum 1clock. During burst read operation, next Read command can be issued in every cycle.

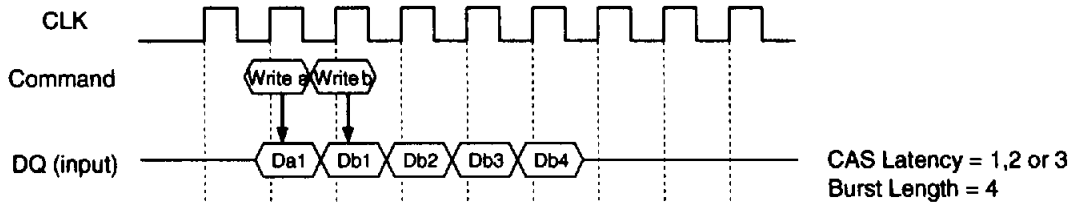
Read to Read Command Interval



Write to Write Command Interval

During burst write operation, when new Write command is issued, the previous burst write is interrupted and the new burst write starts in the same cycle as setting new command. An interval between the commands is minimum 1clock. During burst write operation, next Write command can be issued in every cycle.

Write to Write Command Interval

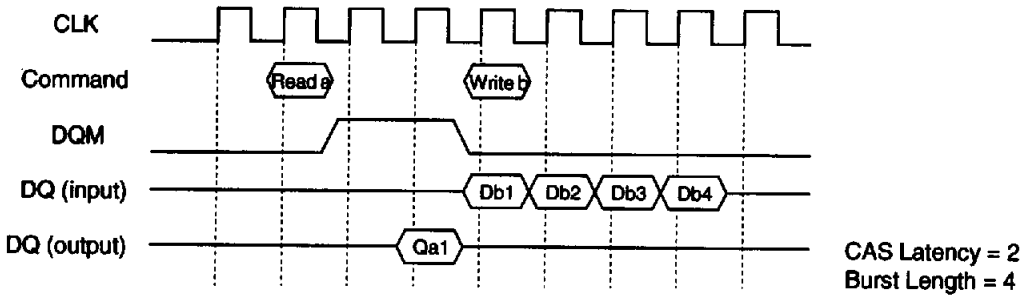


Command Intervals (cont.)

Read to Write Command Interval

During burst read operation, when Write command is issued, the burst read is interrupted and the burst write starts in the same cycle as setting new command. An interval between the commands is minimum 1clock. There is a restriction to avoid data conflict. Before asserting Write command, DQM must be set high so that the output buffer becomes High-Z before data-in is applied.

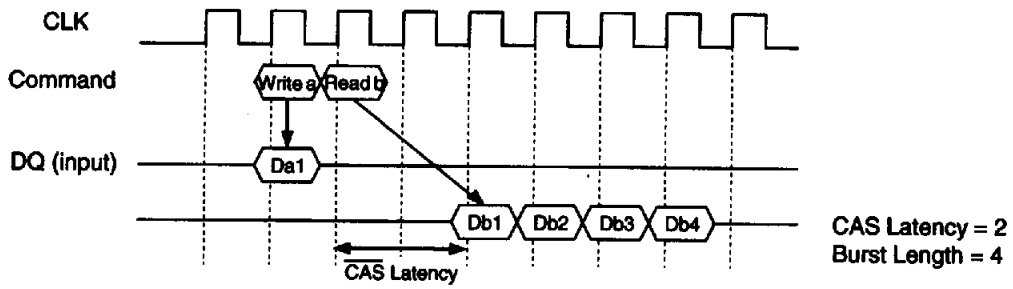
Read to Write Command Interval



Write to Read Command Interval

During burst write operation, when Read command is issued, data is written until one cycle before setting new command and data output starts after the number of cycles specified by CAS latency. An interval between the commands is minimum 1clock. During burst read operation, next Write command can be issued in every cycle without any restriction.

Write to Read Command Interval

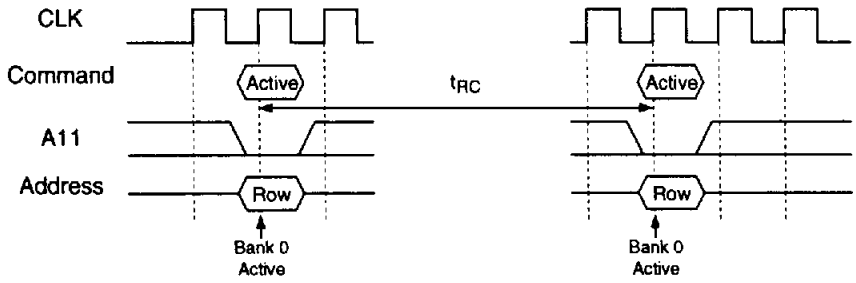


Command Intervals (cont.)

For the same bank

An interval between the two Bank Active Commands for the same bank must be no less than t_{RC}.

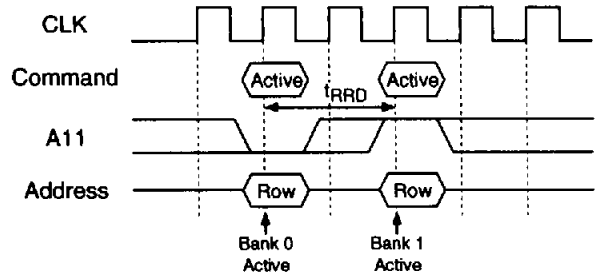
Bank Active to Bank Active Command Interval for same bank



For different bank

An interval between the two Bank Active Commands for different bank must be no less than t_{RRD}

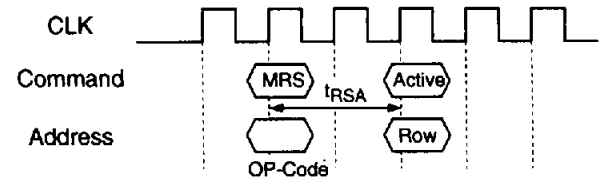
Bank Active to Bank Active Command Interval for different bank



Mode Register Set Command Interval

An interval between Mode Register Set command and Bank Active command must be no less than t_{RSA}.

Mode Register Set to Bank Active Command Interval

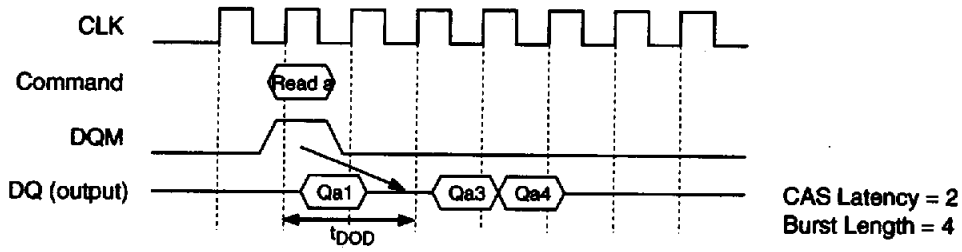


DQM Control

DQM controls output buffer. DQM mask the DQ data.

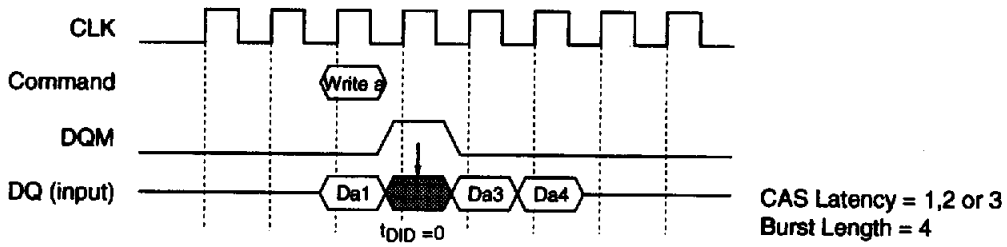
Reading
When DQM is low and data is being read, the output buffer becomes Low-Z and data output is enabled.
When DQM is high, the output buffer becomes High-Z two cycles(t_{DOD}) after. t_{DOD} doesn't depend on CAS latency.

DQM Control : Reading



Writing
When DQM is low, data is written. When DQM is high, data is not written and the previous data is maintained.
In this case, the latency (t_{DID}) is 0. t_{DID} doesn't depend on CAS latency.

DQM Control : Writing



Refresh

Auto-Refresh

Before executing Auto-Refresh command, both banks must be idle. When Auto-Refresh command is executed, the refresh address is generated internally and the refresh is executed. The refresh operation should be performed 4096 times within 64ms. A minimum interval of t_{RC} is required between two Auto-Refresh commands or between an Auto-Refresh command and bank active command.
A precharge is completed automatically after the auto-refresh, therefore, an additional precharge operation is not necessary.

Self-Refresh

After executing Enter Self-Refresh command, the self-refresh operation continues as long as CKE stays low.
In this mode, power consumption is reduced by turning off all input and output buffers. While in self-refresh mode, refresh operation is performed internally, so there is no need to control refresh operation externally. The self-refresh mode is exited by Exit Self-Refresh command. After exiting self refresh mode , NOP command or DESEL command should be asserted within one t_{RC} period. It is recommended to assert an Auto-Refresh command just after the t_{RC} period to avoid the violation of refresh period.

Power Down Mode

Power down mode starts when CKE goes low in the idle state. This mode continues as long as CKE remains low. In this mode, power consumption is reduced by turning off all input and output buffers. However, self-refresh is not performed in this mode. When CKE goes high, the power down mode is terminated, and command input is enabled on the second low-to-high transition of CLK after CKE goes high.

Clock Suspend Mode

Clock suspend mode starts when CKE goes low while a bank is active. This mode continues as long as CKE stays low. In this mode, the internal state is maintained and external input signals are ignored.
When CKE goes high, clock suspend mode is terminated, and command input is enabled on the second low-to high transition of CLK after CKE goes high.

Initialization Sequence

After power-up the following initialize sequence should be used:

(1)CKE,DQM = High and V_{DD} stabilized
↓ (wait more than 100us after power-up.)
(2)Precharge all banks
↓
(3)Mode register set
↓
(4)More than 2 auto refresh cycles (Initialization Complete)

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	VT	−1.0 to 4.6	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to 4.6	V
Short Circuit Output Current	Iout	50	mA
Power Dissipation	PT	1.0	W
Operating Temperature	Topr	0 to + 70	°C
Storage Temperature	Tstg	−55 to +125	°C

Notes : 1.Short circuit output current, Iout, is limited to one output at a time, 1 second maximum duration.

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{DD}	Supply Voltage: V_{DD}, V_{DDQ}	3.0	3.6	V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage: DQ	2.0	V_{DDQ}+1.0	V	V_{IH}(MAX.)=5.5V for Pulse Width ≤5ns
	Input High Voltage: All Except DQ	2.0	V_{DD}+1.0	V	V_{IH}(MAX.)=5.5V for Pulse Width ≤5ns
V_{IL}	Input Low Voltage	−0.3	0.8	V	V_{IL}(MAX.)=-1.0V for Pulse Width ≤5ns

CAPACITANCE (Ta = 25 °C, f = 1MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance, All Control Signals & Addresses	CI	-	5	pF
Output Capacitance (DQ)[1]	CO	-	7	pF

Notes : 1. DQM = V_{IH} to disable Dout.

DC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Speed Version		-10		-12		Unit	Test condition	Note
Frequency		100MHz		83MHz				
Parameter	Symbol	Min.	Max.	Min.	Max.			
Operating Current	I_{CC1}	-	100	-	85	mA	Burst Length = 1 t_{RC} = min.	1
Standby Current	I_{CC2}	-	3	-	3	mA	CKE = V_{IL},t_{CK} = min.	
		-	2	-	2	mA	CKE = V_{IL} CLK = V_{IL} or V_{IH} (fix)	
		-	35	-	25	mA	CKE = V_{IH} , NOP t_{CK} = min.	
Active Standby Current (One Bank Active , One Bank Idle)	I_{CC3}	-	7	-	7	mA	CKE = V_{IL},t_{CK} = min. I/O = High-Z	1
		-	35	-	30	mA	CKE = V_{IH} , NOP t_{CK} = min., I/O = High-Z	
Burst Operating Current	I_{CC4}	-	75	-	65	mA	CL = 1,t_{CK} = min.	1
		-	120	-	100	mA	CL = 2,t_{CK} = min.	
		-	165	-	145	mA	CL = 3,t_{CK} = min.	
Refresh Current	I_{CC5}	-	95	-	80	mA	t_{RC} = min.	
Self-Refresh Current	I_{CC6}	-	2	-	2	mA	$V_{IH} \geqq V_{DD}$-0.2V $V_{IL} \leqq$0.2V	
Input Leakage Current	ILi		±1.0	-	±1.0	μA	$0 \leqq Vin \leqq V_{DD}$	
Output Leakage Current	ILo		±1.0	-	±1.0	μA	$0 \leqq Vin \leqq V_{DD}$ I/O = Disable	
Output High Voltage	V_{OH}	2.4		2.4		V	I_{OH} = -2mA	
Output Low Voltage	V_{OL}		0.4		0.4	V	I_{OH} = 2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Input signal transition is once per two CLK cycles.

AC Characteristics (Ta = 0 to 70 °C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

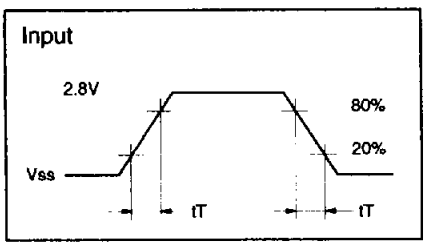
SPEED VERSION				-10		-12		UNIT	NOTE
FREQUENCY				100MHz		83MHz			
NO.	SYMBOL	PARAMETER		MIN.	MAX.	MIN.	MAX.		
1	t_{CK}	System Clock	(CL=3)	10	-	12	-	ns	1
			(CL=2)	15	-	18	-	ns	
			(CL=1)	30	-	36	-	ns	
2	t_{CKH}	CLK High Pulse Width		3	-	4	-	ns	1
3	t_{CKL}	CLK Low Pulse Width		3	-	4	-	ns	1
4	t_{AC}	Access Time from CLK	(CL=3)	-	7	-	9	ns	1,2
			(CL=2)	-	9	-	12	ns	
			(CL=1)	-	25	-	30	ns	
5	t_{ACK}	Read Command	(CL=3)	-	2CLK+7	-	2CLK+9	ns	1,2
		to Data Valid	(CL=2)	-	1CLK+9	-	1CLK+12	ns	
			(CL=1)	-	25	-	30	ns	
6	t_{OH}	Data Out Hold Time		3	-	3	-	ns	1,2
7	t_{LZ}	CLK to Data Out Low Impedance		0	-	0	-	ns	1,2
8	t_{HZ}	CLK to Data Out	(CL=3)	4	7	4	8	ns	1,3
		High Impedance	(CL=2)	4	7	4	8	ns	
			(CL=1)	4	13	4	15	ns	
9	t_{DS}	Data in Setup Time		2	-	3	-	ns	1
10	t_{DH}	Data in Hold Time		1	-	1	-	ns	1
11	t_{AS}	Address Setup Time		2	-	3	-	ns	1
12	t_{AH}	Address Hold Time		1	-	1	-	ns	1
13	t_{CES}	CKE Setup Time		2	-	3	-	ns	1
14	t_{CESP}	CKE Setup Time for Power Down Exit		2	-	3	-	ns	1
15	t_{CEH}	CKE Hold Time		1	-	1	-	ns	1
16	t_{RASC}	Active to Precharge on Full Page Mode		-	12000	-	12000	ns	1
17	t_{RCD}	Active Command to Column Command (same bank)		30	-	30	-	ns	1
18	t_{RP}	Precharge to Active Command Period		30	-	30	-	ns	1
19	t_{PDL}	The Last Data in to	(CL=3)	10	-	12	-	ns	1
		Precharge Lead Time	(CL=2)	15	-	15	-	ns	
			(CL=1)	15	-	15	-	ns	

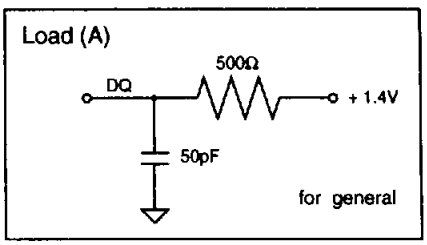
AC Characteristics (Ta = 0 to 70 °C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V) (cont.)

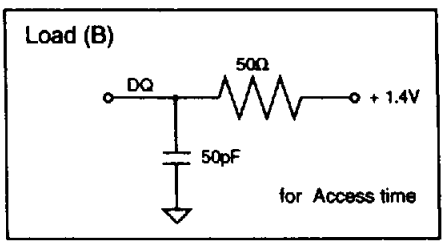
SPEED VERSION			-10		-12		UNIT	NOTE
FREQUENCY			100MHz		83MHz			
NO.	SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.		
20	t_{DAL}	The Last Data in to (CL=3)	40	-	42	-	ns	1
		Active/Ref Lead Time (CL=2)	45	-	45	-	ns	
		(Auto Precharge) (CL=1)	45	-	45	-	ns	
21	t_{RRD}	Active to Active Command Period	20	-	24	-	ns	1
22	t_{RSA}	Mode Register Set to Active Command	14	-	18	-	ns	1
23	t_{RSC}	Mode Register Set to Column Command	14	-	18	-	ns	1
24	t_T	Transition Time (Rise to Fall)	1	5	1	5	ns	
25	t_{REF}	Refresh Period	-	64	-	64	ms	
26	t_{CS}	Command ($\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DQM) Setup Time	2	-	3	-	ns	1
27	t_{CH}	Command ($\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DQM) Hold Time	1	-	1	-	ns	1
28	t_{RC}	Ref/Active to Ref/Active Command Period	90	-	108	-	ns	1
29	t_{RAS}	Active to Precharge Command Period	60	120000	72	120000	ns	1

Notes :

1. AC measurement assume VIL = VSS,VIH = 2.8V and t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load conditions as shown below.
3. t_{HZ}(max) defines the time at which the outputs are neither sinking nor source current, and is not reference to an output voltage.
4. An initial pause of 100us is required after power up followed by a mode register set cycle and minimum of two initialization cycles. (auto refresh cycles)
5. If tT is longer than 1ns, input timing reference level should be VIH(min)/VIL(max).
6. t_{CES} defines CKE setup time to CKE rising edge except for power down exit command.



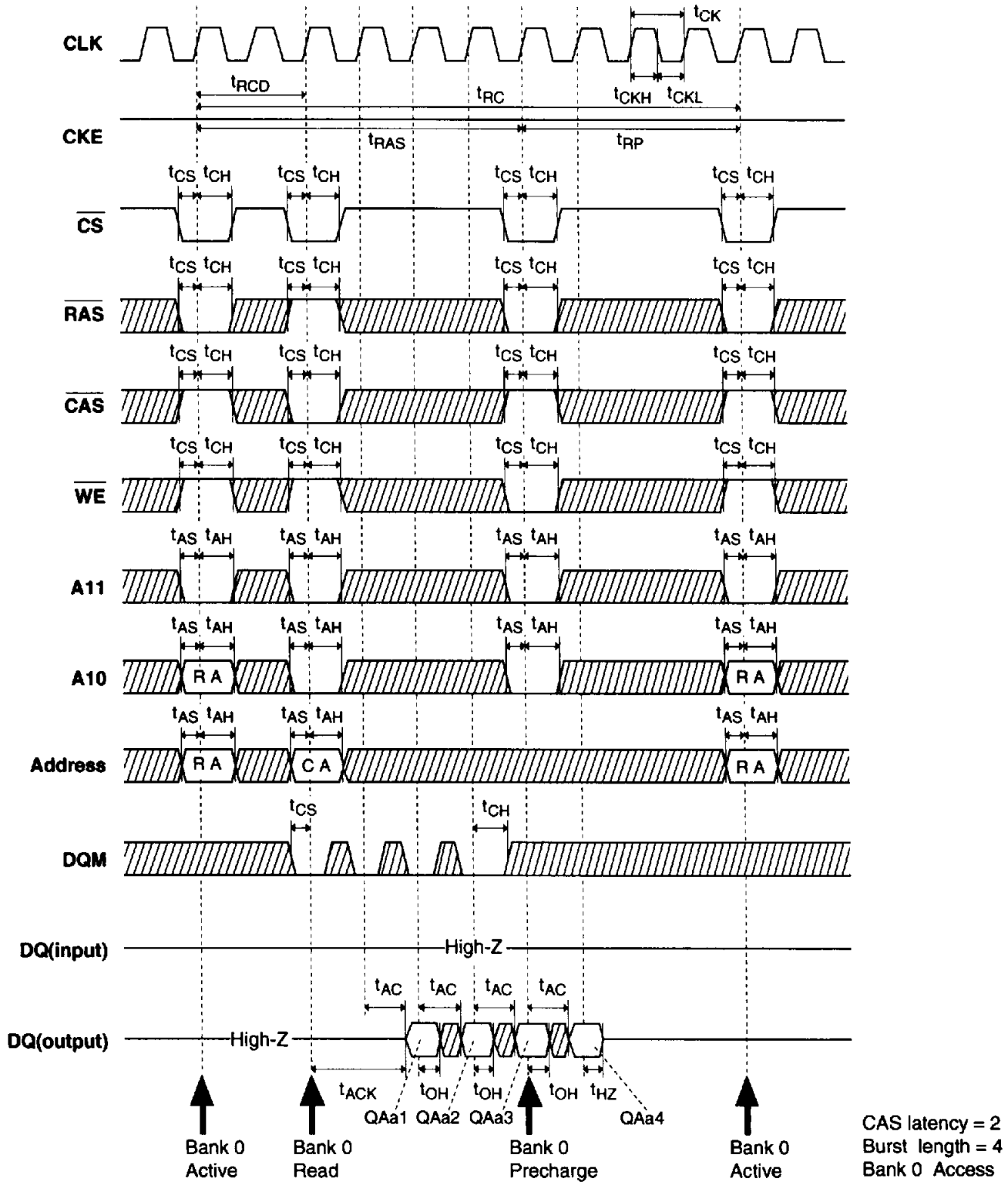




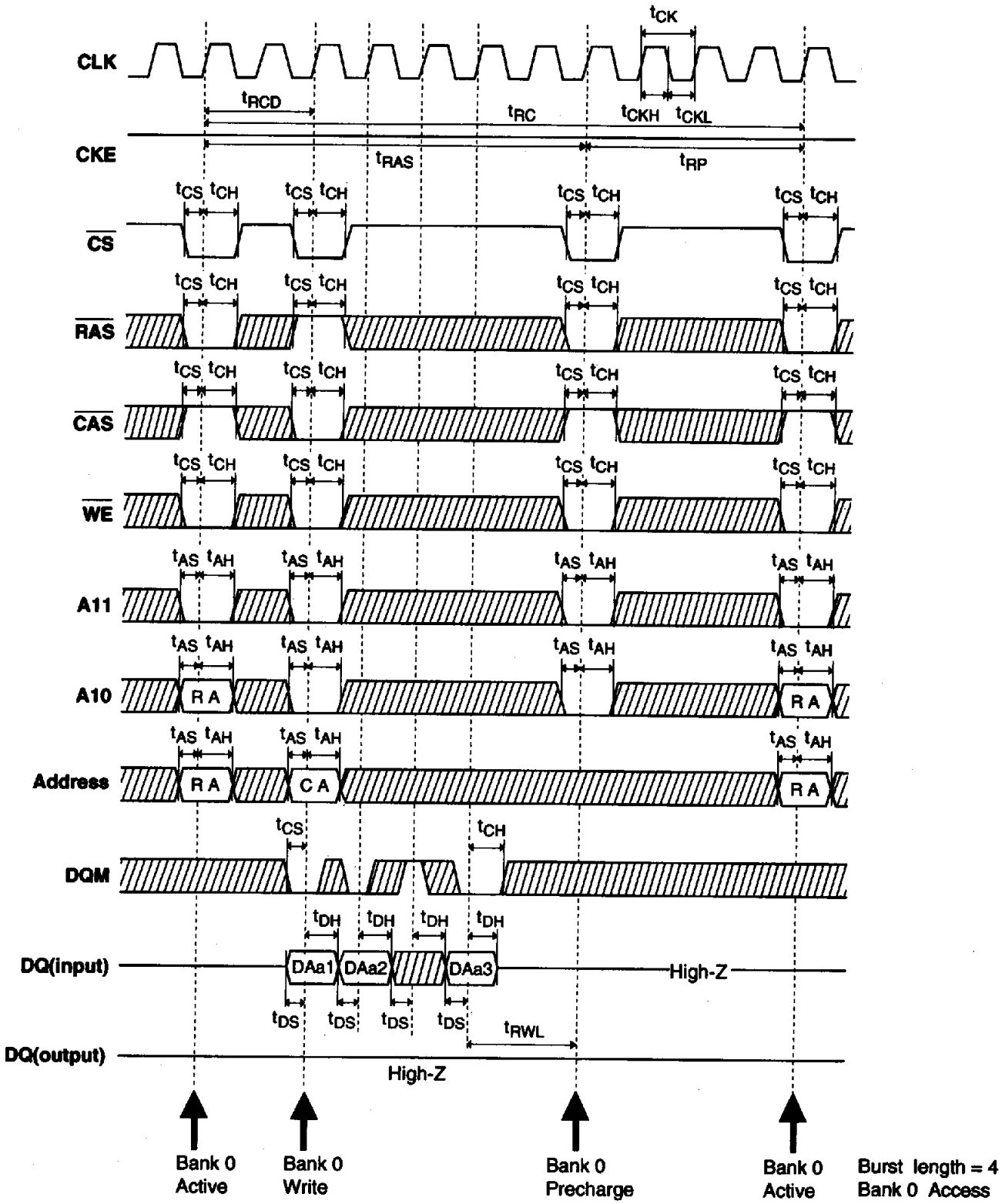
Clock Latency

SPEED VERSION			-10	-12	
FREQUENCY			100MHz	83MHz	
NO.	SYMBOL	PARAMETER			UNIT
1	t_{CLE}	CKE to CLK Disable	1	1	CLK Cycles
2	t_{CDD}	$\overline{CS}$ to Command Disable	0	0	CLK Cycles
3	t_{PEC}	Power Down Exit to Command Input	1	1	CLK Cycles
4	t_{BSR}	Burst Stop to (CL=3)	2	2	CLK Cycles
		Output Valid Data Hold (CL=2)	1	1	CLK Cycles
		(CL=1)	0	0	CLK Cycles
5	t_{BSH}	Burst Stop to (CL=3)	3	3	CLK Cycles
		Output High Impedance (CL=2)	2	2	CLK Cycles
		(CL=1)	1	1	CLK Cycles
6	t_{BSW}	Burst Stop to Write Data Ignore	0	0	CLK Cycles
7	t_{HZP}	Precharge Command to (CL=3)	3	3	CLK Cycles
		High Impedance (CL=2)	2	2	CLK Cycles
		(CL=1)	1	1	CLK Cycles
8	t_{EP}	Last Data Out to (CL=3)	-2	-2	CLK Cycles
		Precharge (CL=2)	-1	-1	CLK Cycles
		(Early Precharge) (CL=1)	0	0	CLK Cycles
9	t_{CCD}	Column Command to Column Command	1	1	CLK Cycles
10	t_{WCD}	Write Command to Data in Latency	0	0	CLK Cycles
11	t_{DID}	DQM to Data in	0	0	CLK Cycles
12	t_{DOD}	DQM to Data out	2	2	CLK Cycles

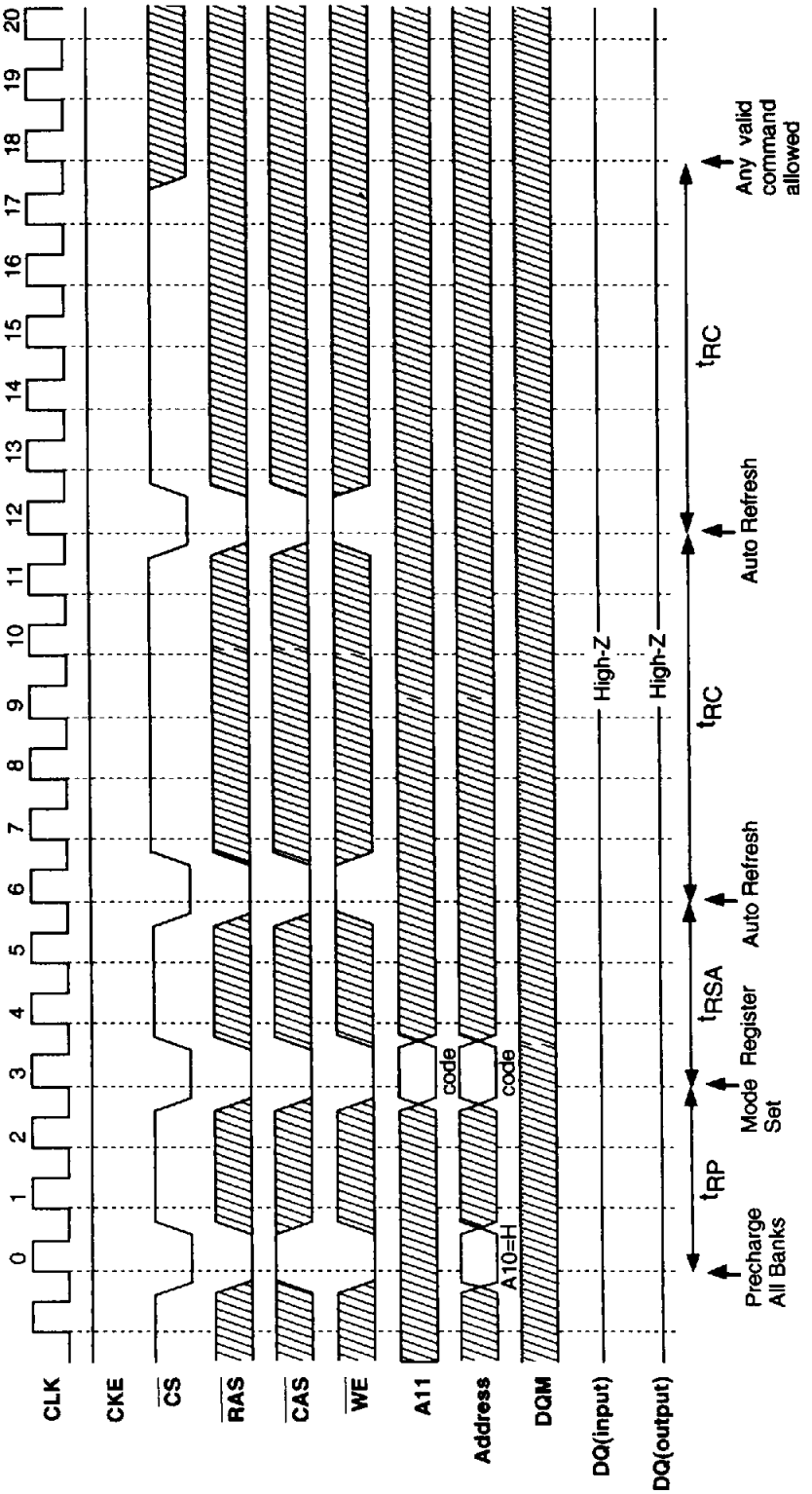
Read cycle



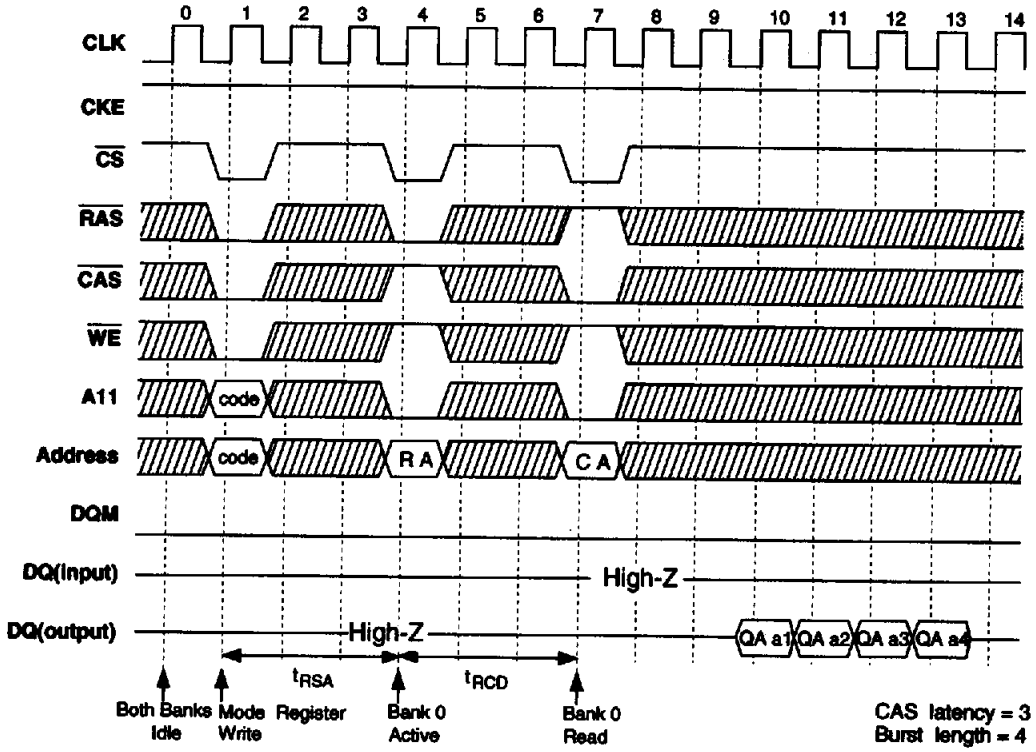
Write cycle



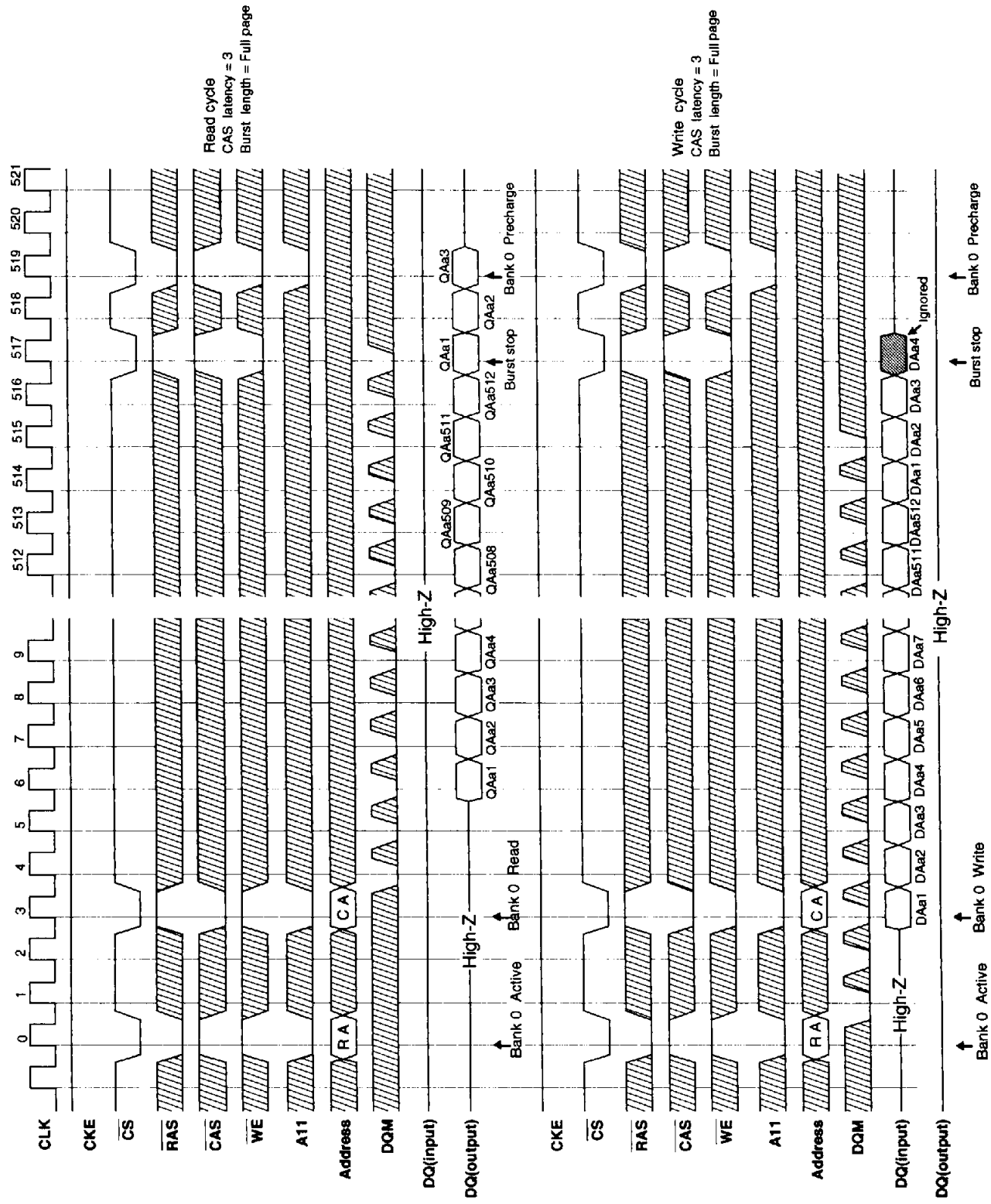
Initialization Sequence



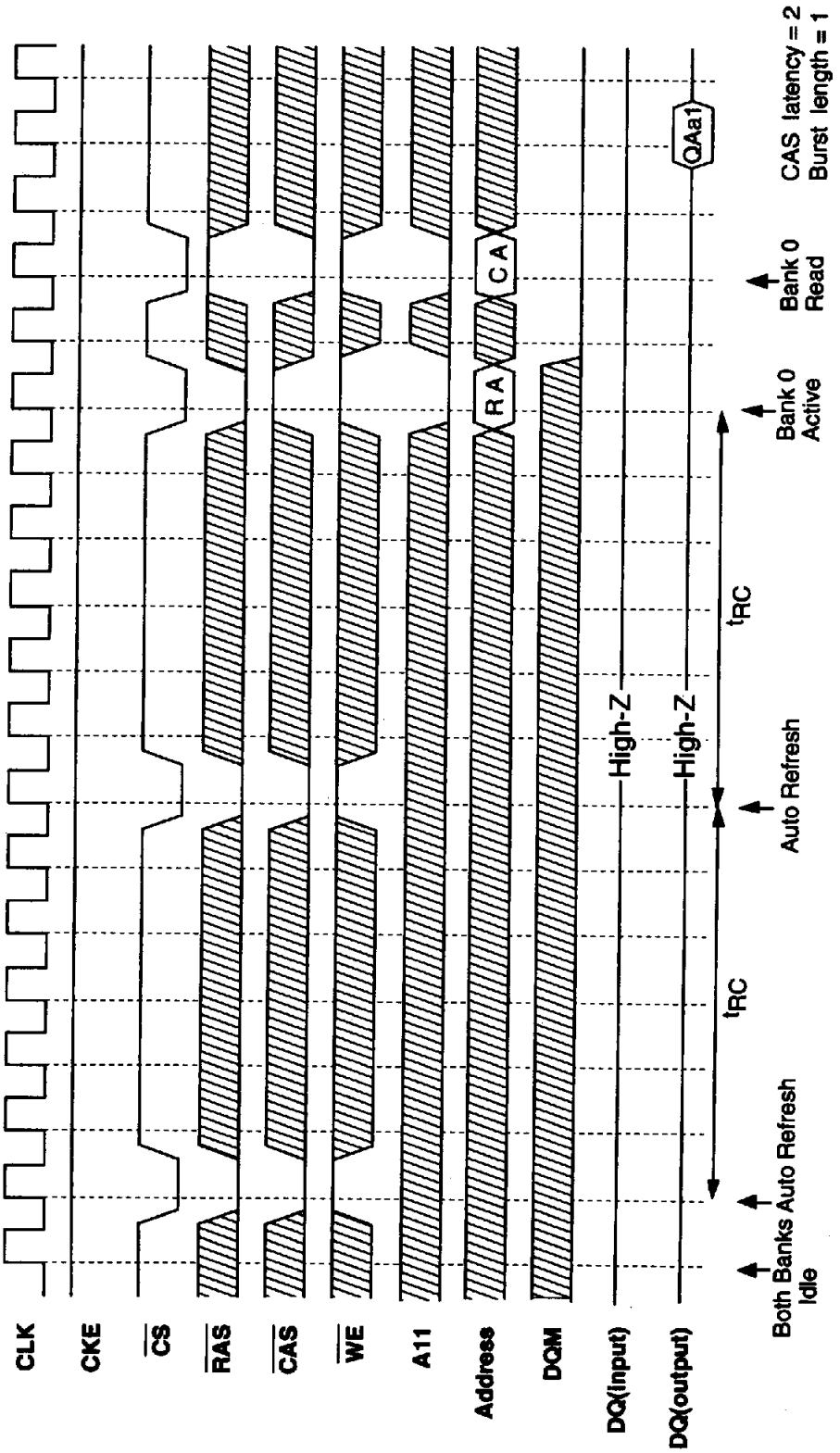
Mode Register Set Cycle



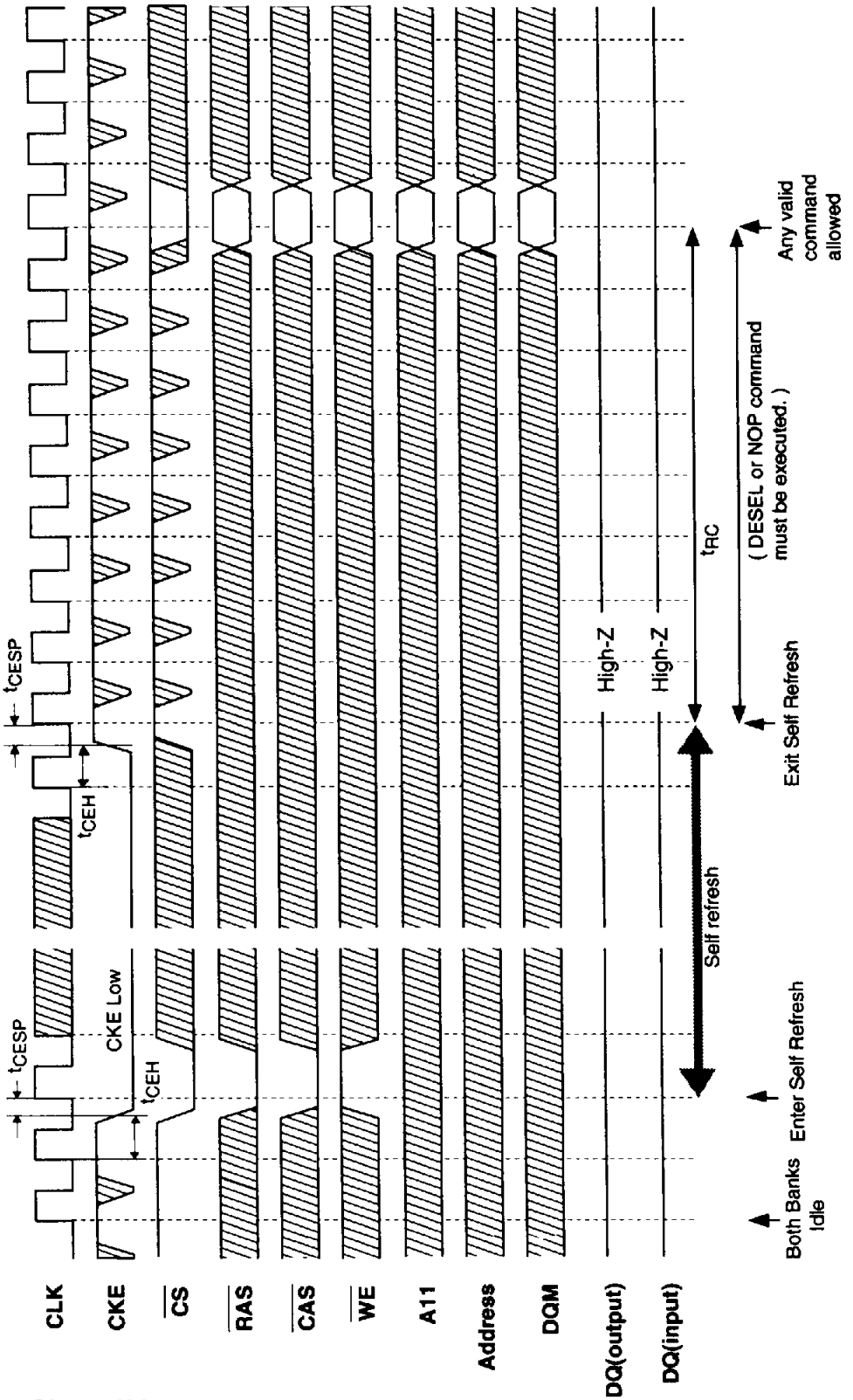
Full Page Read / Write Cycle



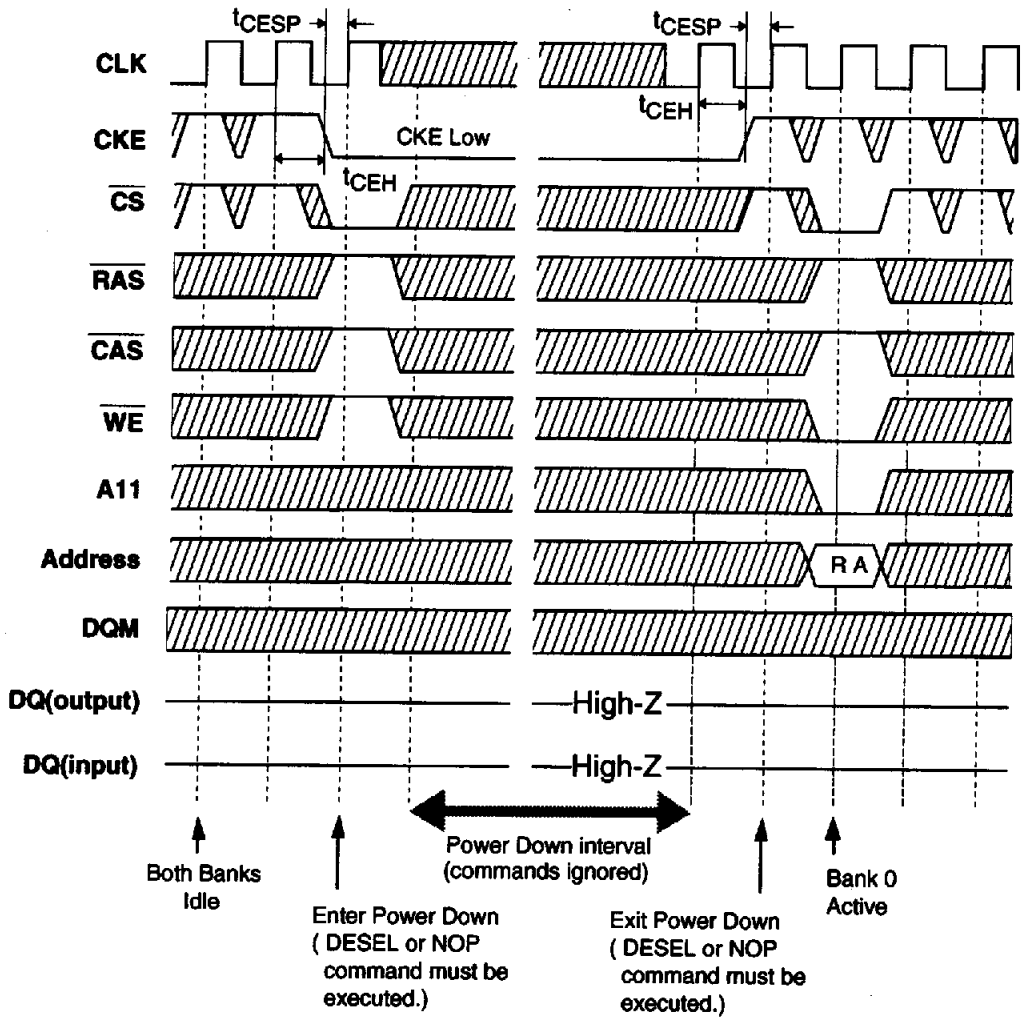
Auto Refresh Cycle



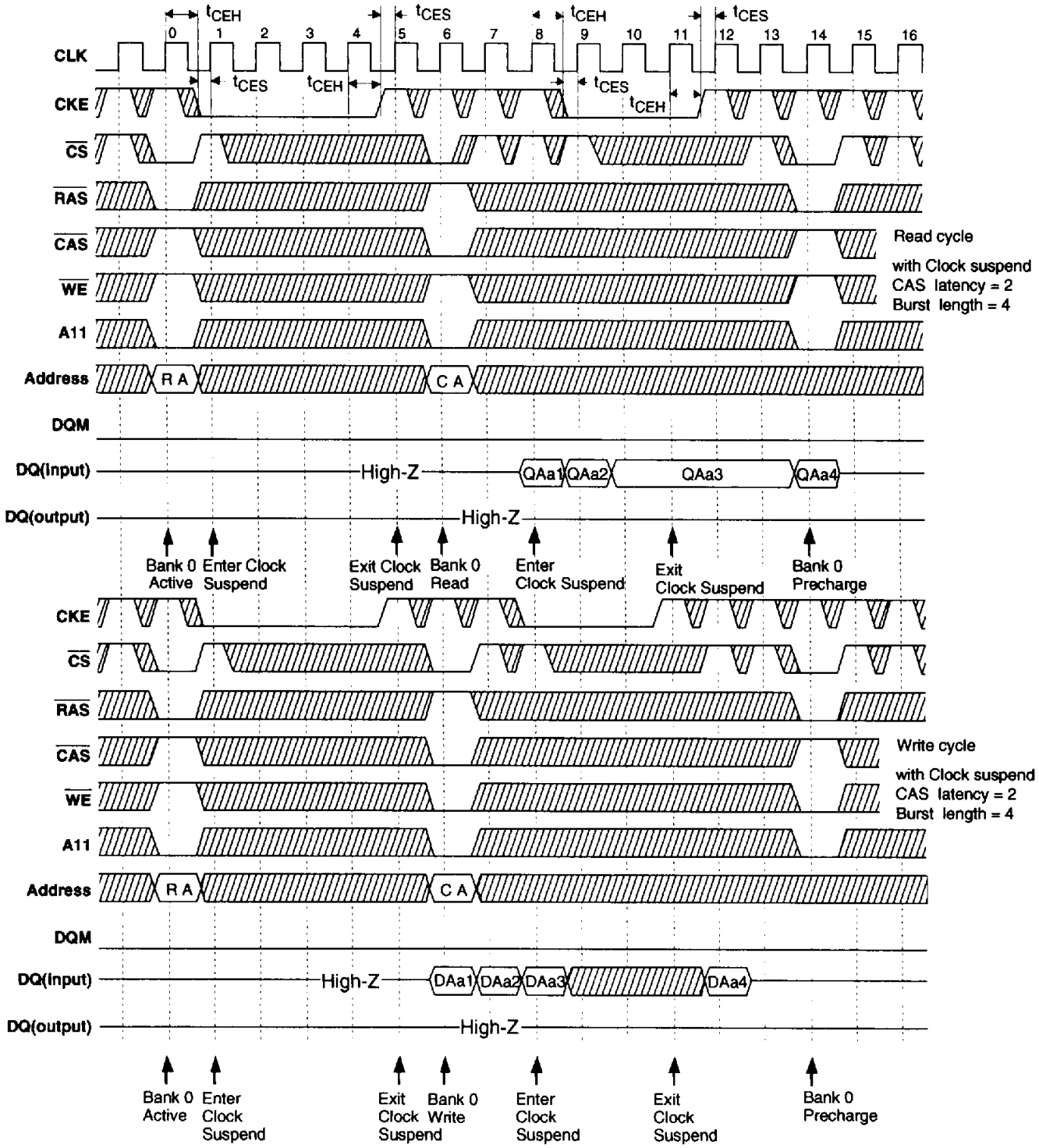
Self Refresh Cycle



Power Down Cycle



Clock Suspend Cycle



ORDERING INFORMATION

NN5216405XX - XX

SPEED (clock cycle time)	10	:	10ns
	12	:	12ns
PACKAGE	TT	:	44pin Plastic TSOP Type II
MODE	16405	:	Synchronous mode 16Mbits (2M X4bits X2banks) 4096 Refresh Cycle / 64ms
PRODUCT	52	:	Synchronous DRAM

NN5216805XX - XX

SPEED (clock cycle time)	10	:	10ns
	12	:	12ns
PACKAGE	TT	:	44pin Plastic TSOP Type II
MODE	16805	:	Synchronous mode 16Mbits (1M X8bits X2banks) 4096 Refresh Cycle / 64ms
PRODUCT	52	:	Synchronous DRAM