

January 13, 2000

APPLICATION NOTE FOR SC1101/03

INTRODUCTION

DESCRIPTION

The SC1101/03 is a versatile, low-cost, voltage-mode PWM controller designed for use in single ended DC/DC power supply applications. A simple, fixed-voltage buck regulator can be implemented using the SC1101/03 with a minimum of external components. Internal level shift and drive circuitry eliminates the need for an expensive p-channel, high-side switch. The small device footprint allows for compact circuit design.

SC1101/03 features include a temperature compensated voltage reference, triangle wave oscillator, current limit comparator, frequency shift over-current protection, and an internally compensated error amplifier. Pulse by pulse current limiting is implemented by sensing the differential voltage across an external resistor, or an appropriately sized PC board trace.

The SC1101/03 operates at a fixed frequency of 200kHz, providing an optimum compromise between efficiency, external component size, and cost.

The SC1103's manufacturing process has been optimized for 12V operation and is capable of handling up to 26V at it's BST pin.

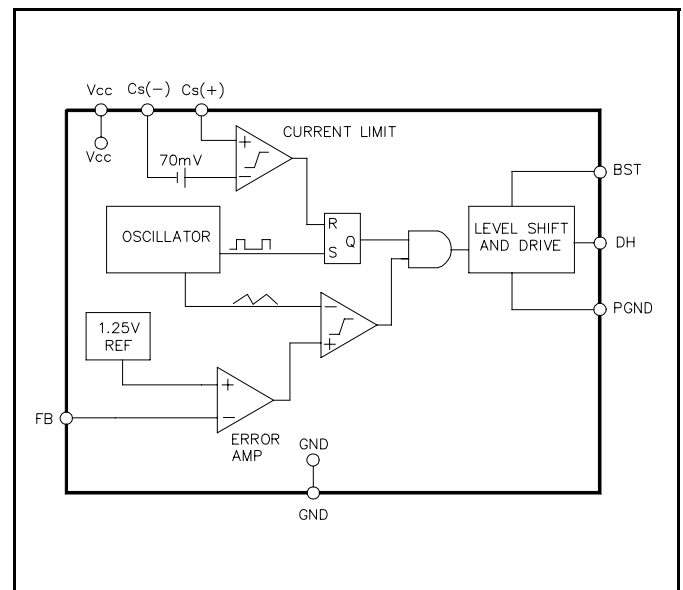
APPLICATIONS

- Pentium® P55 Core Supply
- Low Cost Microprocessor Supplies
- Peripheral Card Supplies
- Industrial Power Supplies
- High Density DC/DC Conversion

FEATURES

- Low cost / small size
- Switch mode efficiency (90%)
- 1% reference voltage accuracy
- Over current protection
- 500mA output drive
- 5V to 12V Input power source

BLOCK DIAGRAM



January 13, 2000

LAYOUT GUIDELINES

Careful attention to layout requirements are necessary for successful implementation of the SC1101/03 PWM controller. High currents switching at 200kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

- 1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom Schottky ground.
- 2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Schottky (D1) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will reduce EMI, lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and minimize source ringing, resulting in more reliable gate switching signals.
- 3). The connection between the junction of Q1, D1 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so impor-

tant, however adding unnecessary impedance will reduce efficiency.

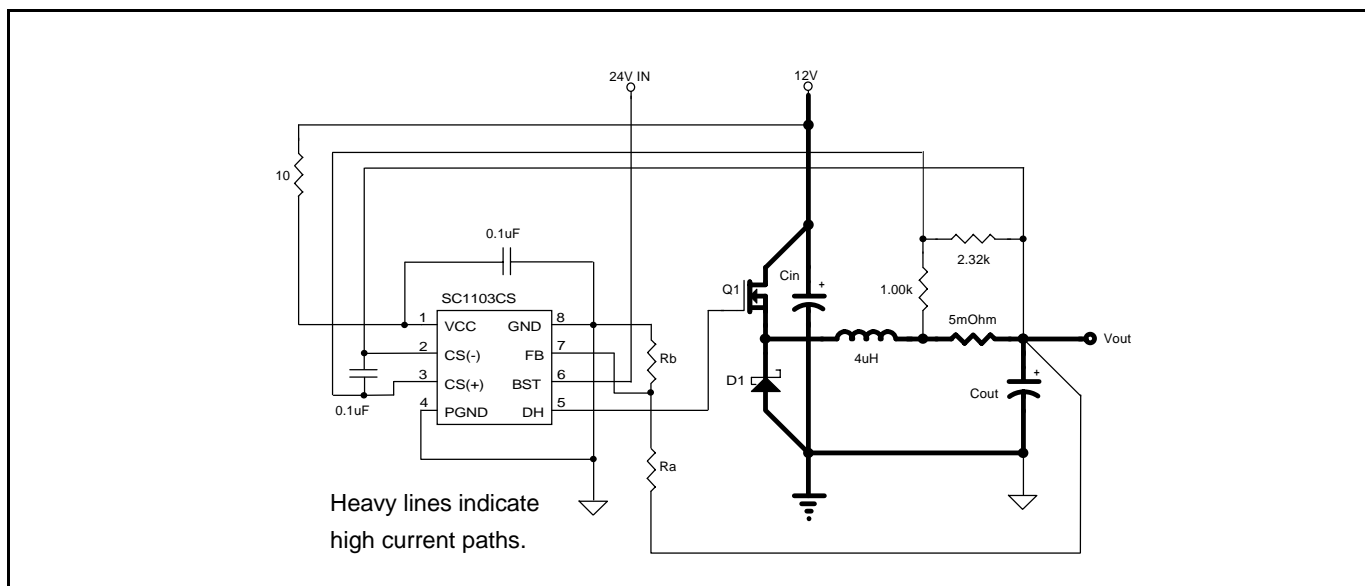
4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1101/03 is best placed over an isolated ground plane area. GND and PGND should be returned to this isolated ground. This isolated ground area should be connected to the main ground by a trace that runs from the GND pin to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, D1 loop. Under no circumstances should GND be returned to a ground inside the Cin, Q1, D1 loop.

6) Vcc for the SC1101/03 should be supplied from the VIN supply through a 10Ω resistor, the Vcc pin should be decoupled directly to GND by a 0.1mF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS(+) and CS(-) on the SC1101/03 should run parallel and close to each other. The 0.1μF capacitor should be mounted as close to the CS(+) and CS(-) pins as possible.

8) To minimize noise pickup at the sensitive FB pin, the feedback resistors should both be close to the SC1101/03 with the bottom resistor (Rb) returned to ground at the GND pin.

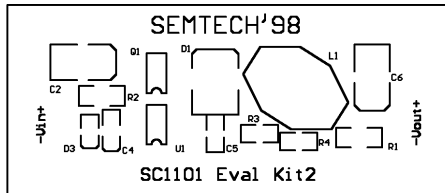


January 13, 2000

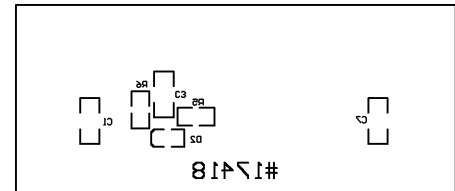
TYPICAL APPLICATIONS
1. Small footprint - Low power

This circuit utilizes SO-8 MOSFET and SMC Schottky Diode. The area is 1 sq. in.

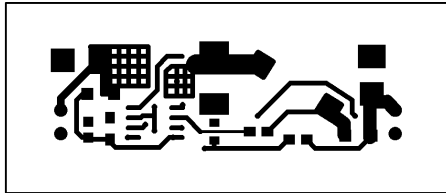
Top - Component View



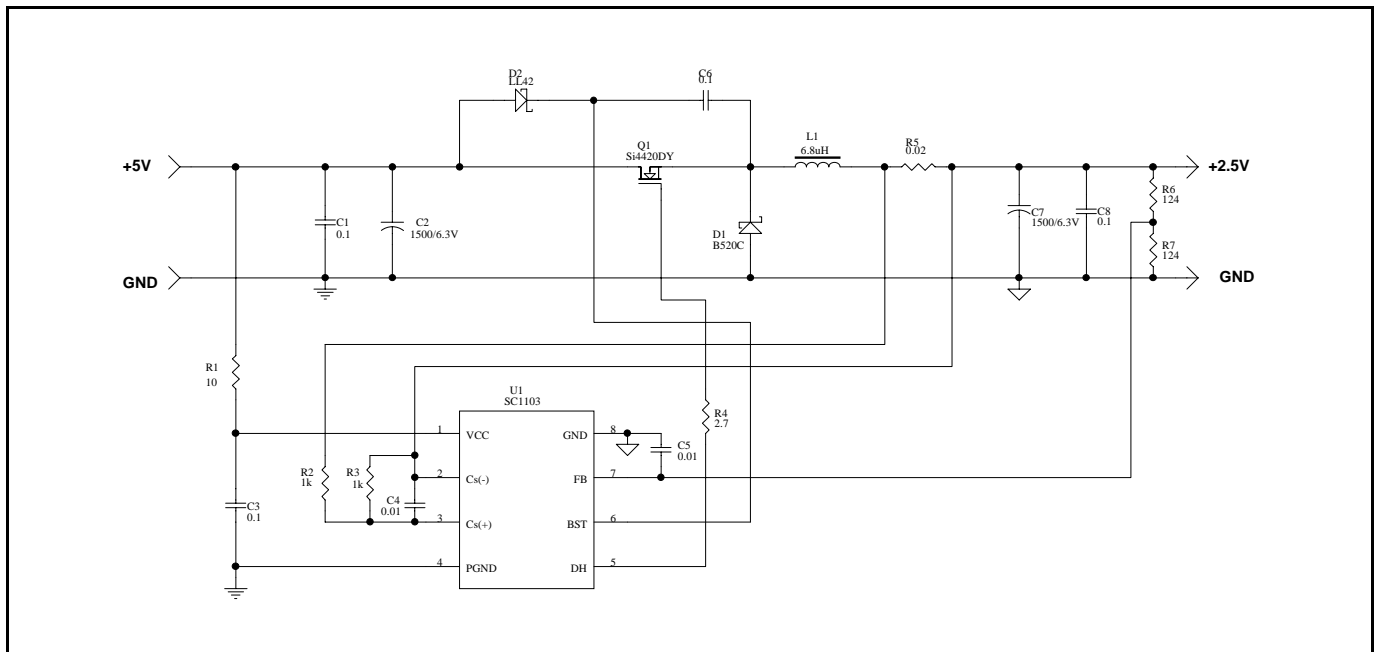
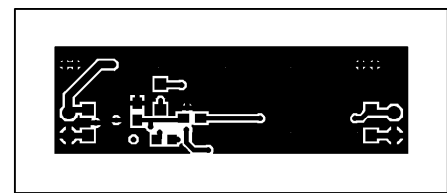
Bottom - Component View



Top - Copper



Bottom - Copper



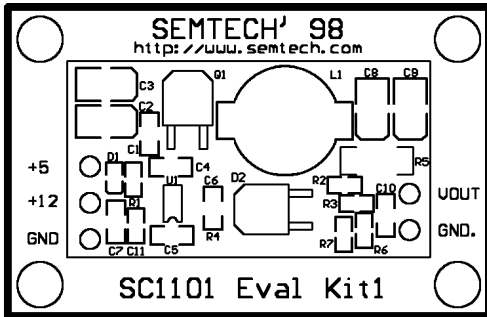
5V to 2.5V @ 4A with "flying capacitor" boost voltage.

January 13, 2000

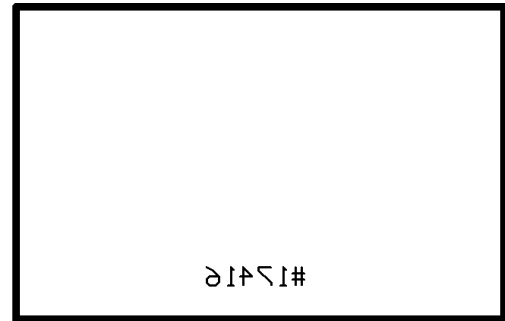
TYPICAL APPLICATIONS (Cont.)
2. Small footprint - Medium power

This circuit utilizes DPAK MOSFET and Schottky Diode. The area is 2.2 sq. in.

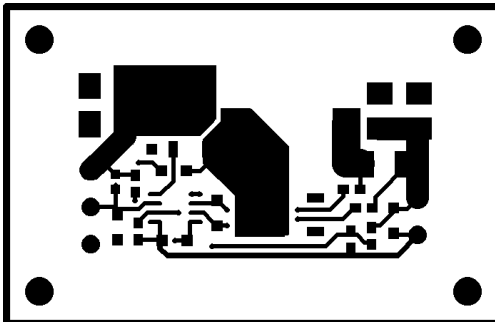
Top - Component View



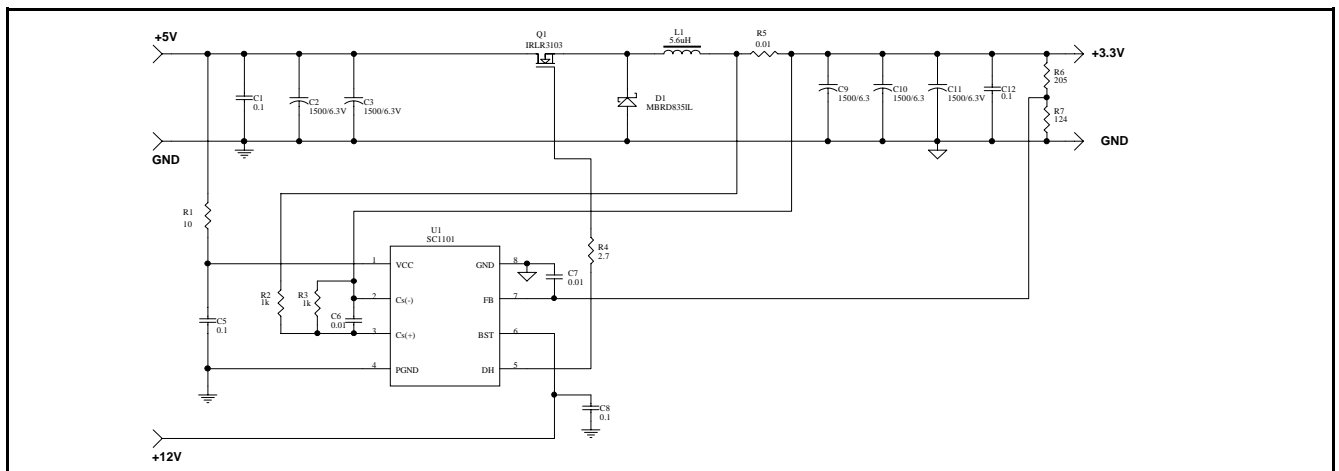
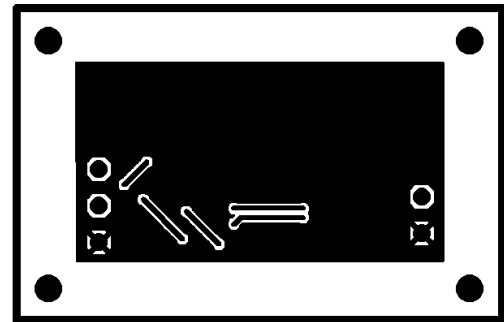
Bottom - Component View



Top - Copper



Bottom - Copper

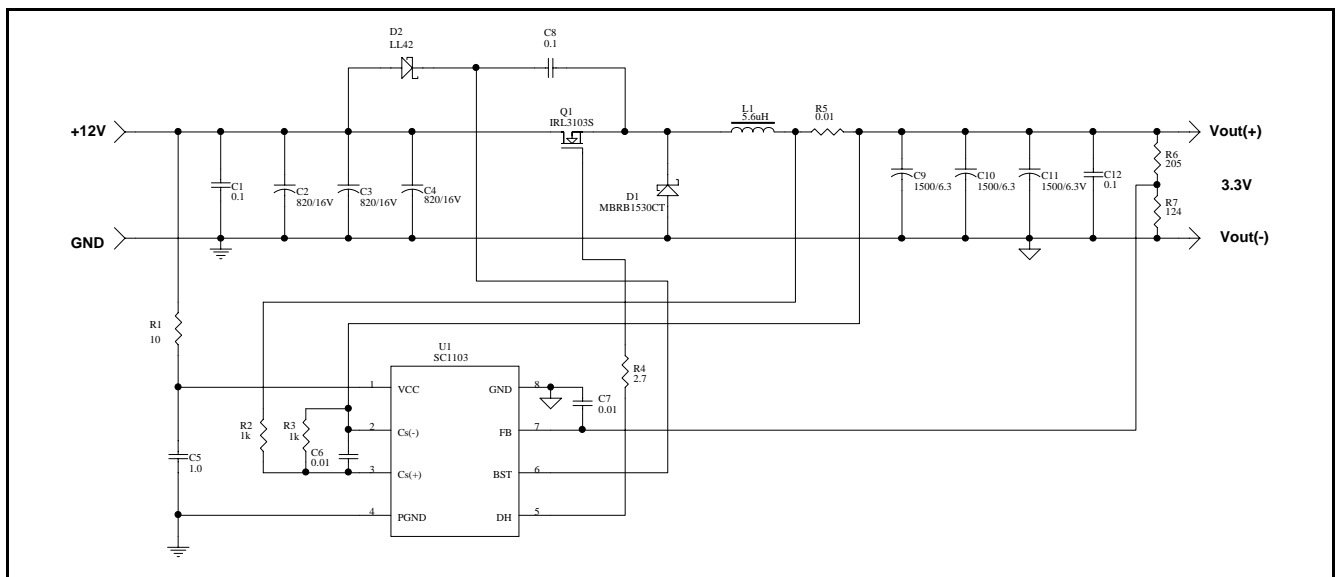
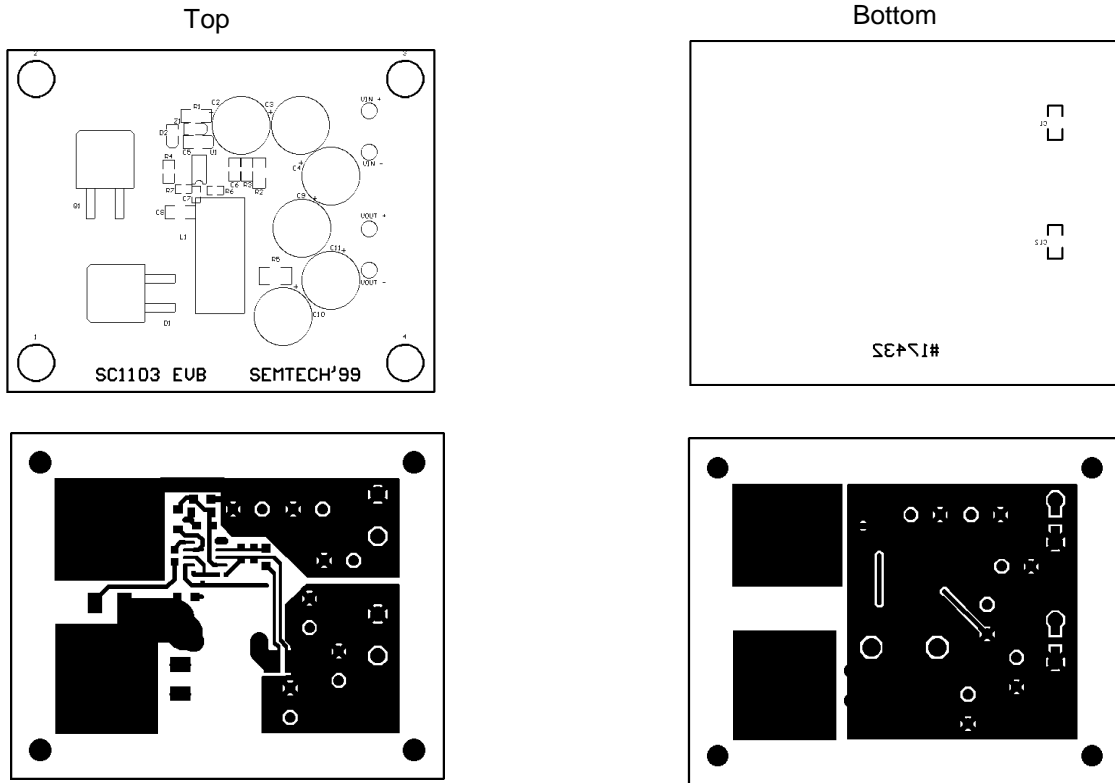


5V to 3.3V @ 8A

January 13, 2000

TYPICAL APPLICATIONS (Cont.)
3. Medium footprint - High power

This circuit utilizes D2PAK MOSFET and Schottky Diode. The area is 4.1 sq. in.



12V to 3.3V @ 10A with "flying capacitor" boost voltage.

January 13, 2000

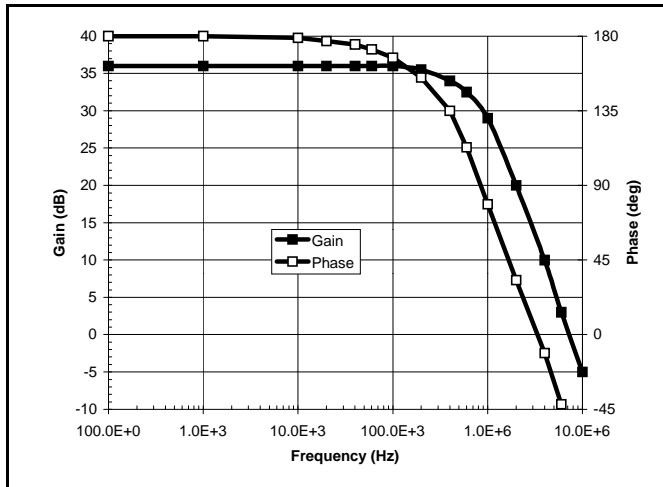
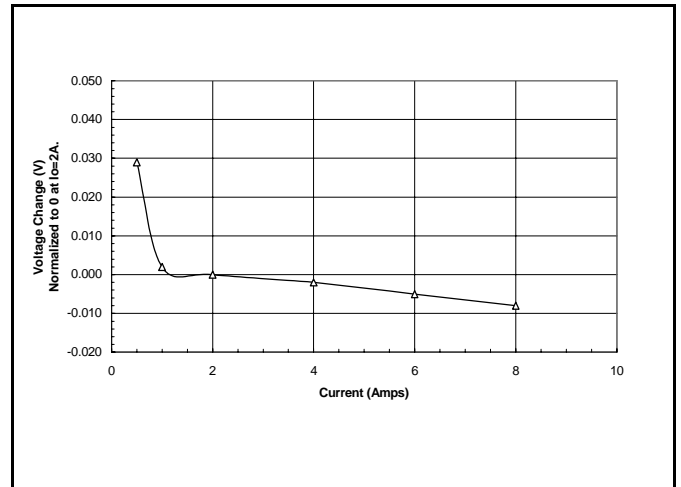
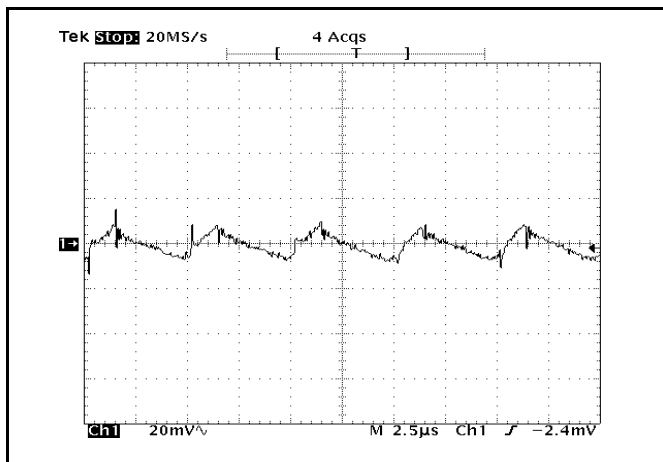
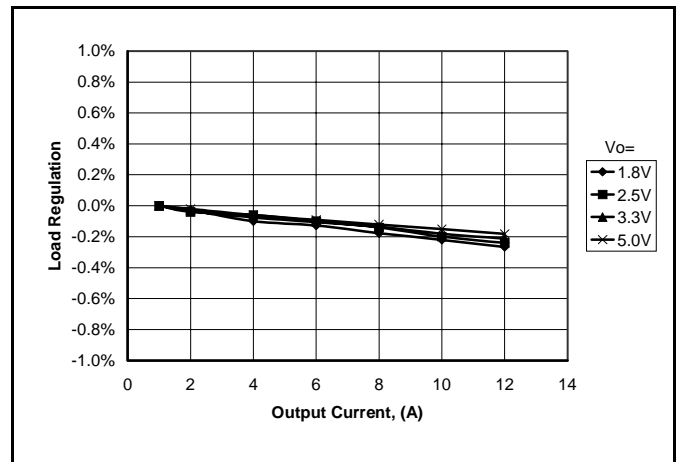
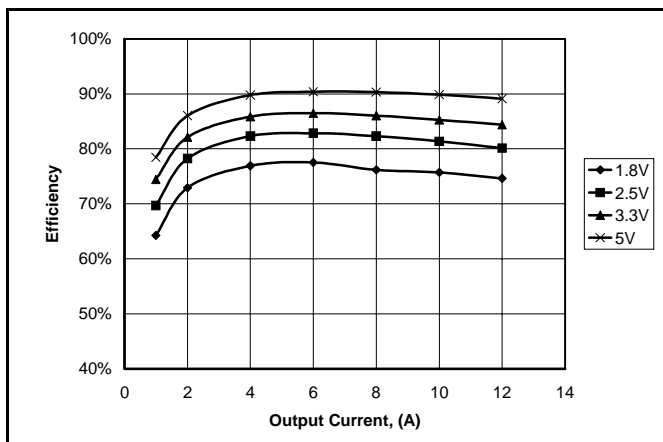
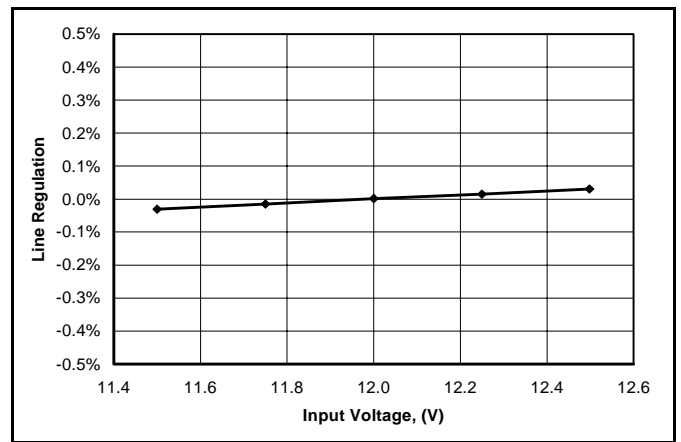
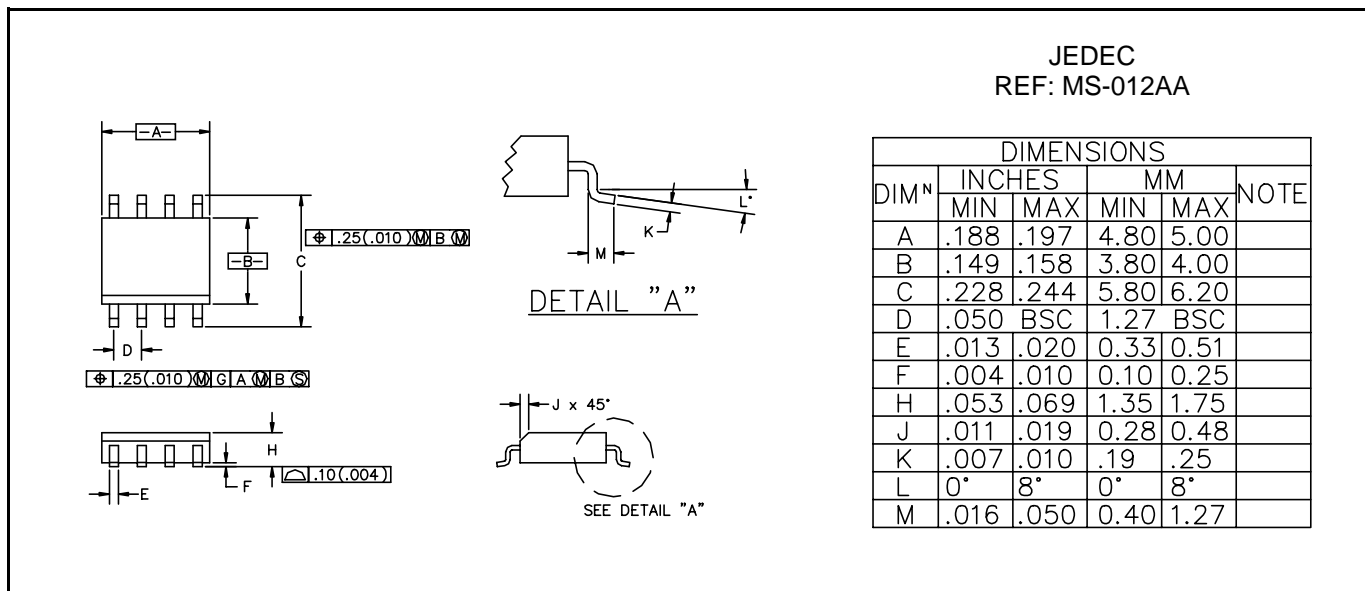
TYPICAL PLOTS & WAVEFORMS


Fig. 1: Error Amplifier, Gain and Phase


 Fig. 2: Load Regulation @ $V_O = 3.3V$, $V_{IN} = 12V$

 Fig. 3: V_{RIPPLE} @ $V_{IN} = 12V$, $V_O = 3.3V$, $I_O = 10A$

 Fig. 4: Load Regulation @ $V_{IN} = 12V$

 Fig. 5: Efficiency @ $V_{IN} = 12V$

 Fig. 6: Line Regulation @ $V_O = 3.3V$, $I_O = 10A$

January 13, 2000

OUTLINE DRAWING

LAND PATTERN SO-8
