FAIRCHILD
A Schlumberger Company

93458/93459
16 x 48 x 8 Field Programmable Logic Array

Bipolar Division

Isoplanar Schottky TTL Logic Array

Description

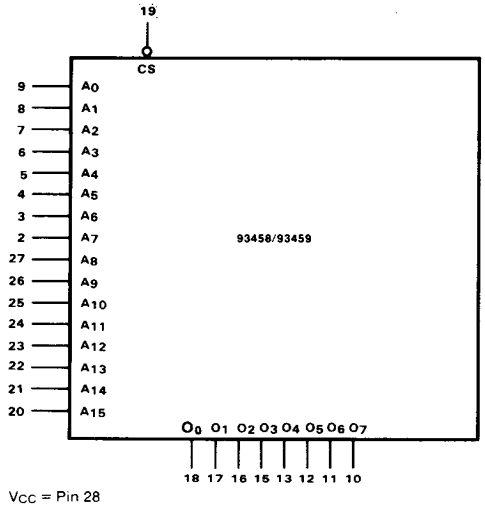
The 93458 and 93459 are bipolar Field Programmable Logic Arrays (FPLAs) organized with 16 inputs, 48 product terms and eight outputs. The 16 inputs and their complements are fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates are fuse linked to eight 48-input OR gates (eight summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93458 has open-collector outputs; the 93459 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}$ is LOW.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 65 ns Max**
- **Fully Programmable Product Array, Summing Array and Output Polarity**
- **Available with Open Collector (93458) or Three State (93459) Outputs**
- **Industry Proven Nichrome Fuses**

Pin Names

A_0–A_{15}	Address Inputs
$\overline{CS}$	Chip Select Inputs
O_0–O_7	Data Outputs
V_P	Programming Pin

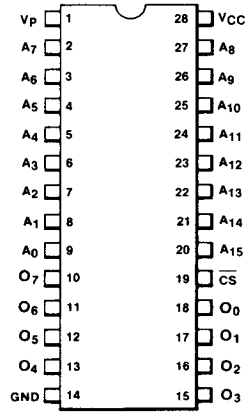
Logic Symbol



V_{CC} = Pin 28
GND = Pin 14

Connection Diagram

28-Pin DIP (Top View)

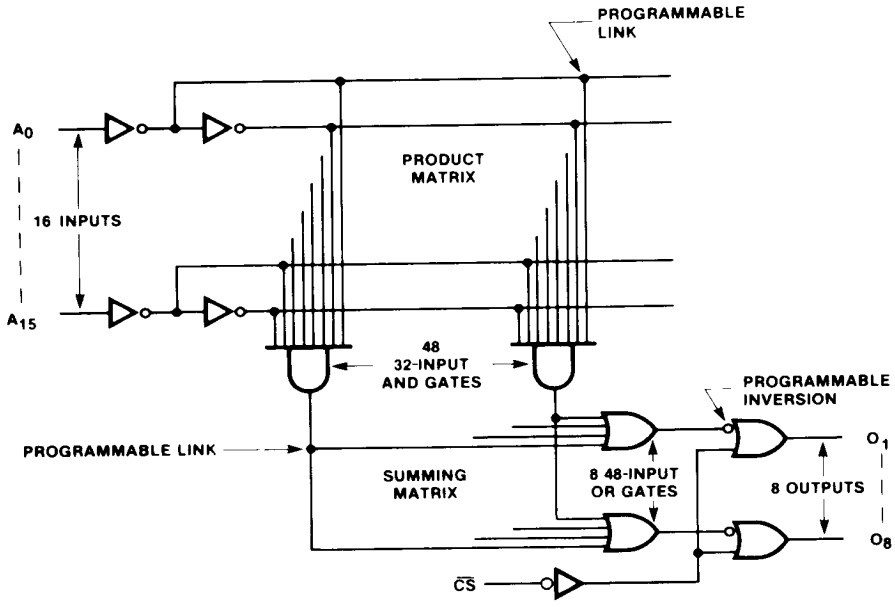


Note

The 28-pin Flatpak and the 28-pin Leadless Chip Carrier have the same pinout (Connection Diagram) as the 28-pin DIP.

8

Logic Diagram



Functional Description

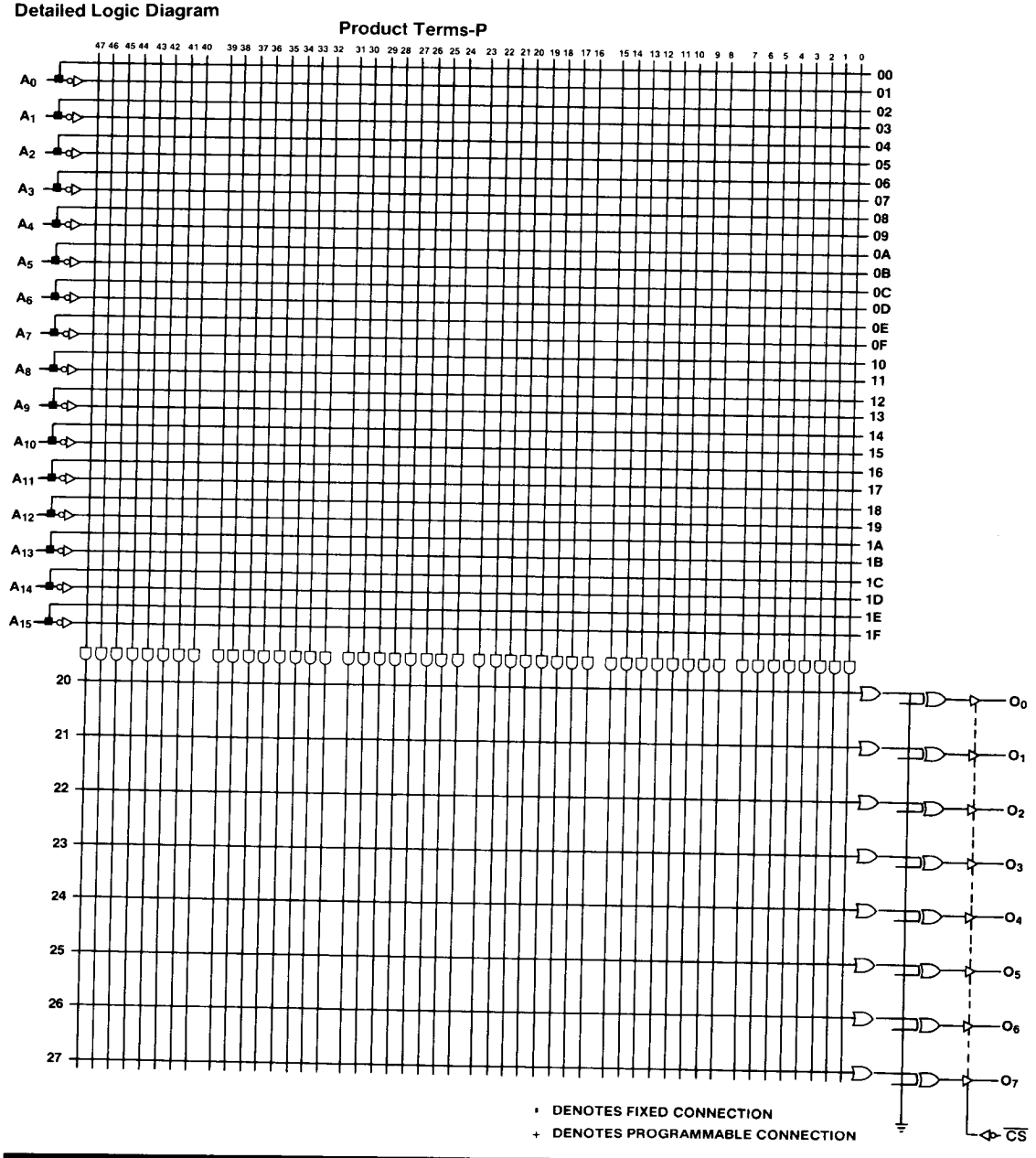
The 93458 and 93459 are bipolar Field Programmable Logic Arrays (FPLAs) organized 16 inputs by 48 product terms by eight outputs. Open-collector outputs are provided on the 93458 for use in wired-OR systems. The 93459 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The 93458 and 93459 both contain a test input line, two test product term lines and a test output line. These test fuses are accessed during both wafer sort and final test and used to assure high programmability and to guarantee DC parameters and AC performance.

The read function is identical to that of a conventional bipolar PLA. That is, a binary address is applied to inputs A_0 through A_{15}, the chip is selected, and data is valid at the outputs after t_{AA}.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined in the *Programming Specifications* table.

Detailed Logic Diagram



8

Logic Relationships

Input Term

A_n — $n = 0, \ldots, 15$, one of 16 inputs

Product Term

$P_m = \pi_0^{15} (i_n A_n + j_n \overline{A_n})$ — $m = 0, \ldots, 47$, one of 48 product terms

where:

a) $i_n = j_n = 0$ for unprogrammed input

b) $i_n \neq j_n$ for programmed input

c) $i_n = j_n = 1$ for Don't Care input

$F_r = \Sigma_0^{47} P_m$ — $r = 0, \ldots, 7$, the OR function of the 48 product terms

Summing Term

$S_r = \Sigma_0^{47} k_m P_m$ — where $k_m = 0$ for product term inactive (programmed)

$k_m = 1$ for product term active (unprogrammed)

				Output	
Mode	$\overline{CS}$	F_r	S_r	**Active HIGH**	**Active LOW**
Read	L	H	L	L	H
	L	H	H	H	L
	L	L	X	L	H
Disable	H	X	X	H (93458) High-Z (93459)	H (93458) High-Z (93459)
	H	X	X		

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Don't Care

By programming, the eight outputs of an FPLA can be made to relate to the 16 inputs as given by the following example:

8 outputs total

$O_1 = A_0 \overline{A_6} A_{14} + \overline{A_2}\,\overline{A_{15}} + \underbrace{\overline{A_0} A_1 \ldots A_{15}}_{\text{One Product Term, 16 input terms max}} + \overline{A_8} A_{10} \overline{A_{13}}$

One Output, 48 product terms max

$O_2 = A_0 \overline{A_6} A_{14} + \overline{A_2}\,\overline{A_{15}}$
(Output polarity programmed, active HIGH)

$O_7 = \overline{(\overline{A_8} A_{10} \overline{A_{13}} + A_4 \overline{A_7}\,\overline{A_9} A_{11} \overline{A_{12}})}$
(Output polarity not programmed, active LOW)

Programming

The 93458 and 93459 are delivered in an unprogrammed state, characterized by:

- All fuses intact
- All 8 output buffers in active LOW state
- All outputs read HIGH

Programming and verifying the Product Matrix, the Summing Matrix, and the Output Polarity are outlined below.

Program Product Matrix

All 48 AND gates of the product matrix are fuse linked to both the true and false lines of every input buffer in the initial unprogrammed state. The initial logic expression for the 48 unprogrammed AND gates is $A_0 \overline{A_0} A_1 \overline{A_1} \ldots A_{15} \overline{A_{15}}$ (where A_n or $\overline{A_n}$ is defined to be an input term). Programming the fuse located by the selection of an input line, A_n, and the mth AND gate replaces the input term A_n with '1' in the logic expression for the mth AND gate.

- Program one input at a time.
- All unused inputs of programmed product terms must be programmed as Don't Care.
- Inputs of unused product lines are not required to be programmed.
- Pin 18 (O_0) is in the read mode (open collector). Care must be taken so that this pin is either left open, grounded, or loaded such that the current flowing into the pin does not exceed 16 mA.

1. Connect pin 28 (V_{CC}) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 10 through 13, 15, and 16 (O_7 through O_2) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed (O_7 = LSB and O_2 = MSB).
5. Apply +12.0 V to all input pins (A_0 through A_{15}).
6. Apply the proper TTL level to an A_n input pin as follows (program one input at a time):
   a. If the product term to be programmed contains the input term A_n (where n = 0 through 15), lower the A_n pin to a TTL HIGH level.
   b. If the product term to be programmed contains the input term $\overline{A_n}$, lower the A_n to a TTL LOW level.
   c. If the product term does not contain the input terms A_n or $\overline{A_n}$ (i.e., A_n is a "Don't Care" input), perform steps 6a, 7, 6b, and 7.
7. Apply a 15.0 V programming pulse to pin 1 (V_P) according to the *Programming Specifications* table.
8. Repeat steps 5 through 7 for each input of the selected product term.
9. Repeat steps 4 through 8 for all other product terms to be programmed.

Verify Product Matrix

1. Connect pin 28 (V_{CC}) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 10 through 13, 15, and 16 (O_7 through O_2) to address an on-chip 1-of-48 decoder to select the AND gate to be verified (O_7 = LSB and O_2 = MSB).
5. Apply +12.0 V to all input pins (A_0 through A_{15}).
6. Test the state of the A_n input as follows:
   a. Lower the A_n pin to a TTL HIGH level and sense the voltage on pin 18 (O_0).
   b. Lower the A_n pin to a TTL LOW level and sense the voltage on pin 18 (O_0).
7. The state of the A_n input is determined as follows:

	A_n = TTL HIGH	A_n = TTL LOW	Condition of A_n for Selected Product Term
Level at Output 0 (Notes 1, 2, 3)	H	H	Don't Care
	H	L	A_n in P-Term
	L	H	$\overline{A_n}$ in P-Term
	L	L	Unprogrammed

8. Repeat steps 5 through 7 for each input of the selected product term.
9. Repeat steps 4 through 8 for all other product terms.
10. Repeat steps 4 through 9 with V_{CC} at the Low V_{CC} Read recommended value.

Notes

1. O_0 in this mode functions as an open-collector output.
2. The table above is valid regardless of the polarity (active HIGH or active LOW) of O_0.
3. Pin 1 (V_P) should be either floating or grounded.

Programming Summing Matrix

All eight OR gates of the summing matrix are fuse linked to the outputs of the AND gates in the initial unprogrammed state. The initial logic expression (sum of products) of the eight unprogrammed OR gates is $P_0 + P_1 + P_2 + \ldots + P_{47}$ where Pm is the product term programmed into the mth AND gate. Programming the fuse located by the selection of the mth AND gate and the nth summing line replaces the product term Pm with '0' in the logic expression of the nth OR gate. The nth summing line is selected by the selection of the nth output buffer where n = 0 through seven.

- Program one input at a time.
- All unused product lines are not required to be programmed.

1. Connect pin 28 (V_{CC}) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 4 through 9 (A_5 through A_0) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed (A_0 = LSB and A_5 = MSB).
5. Apply a TTL HIGH level to pins 20 and 21 (A_{15} and A_{14}).
6. Connect the remaining input pins to +12.0 V.
7. Apply an 18 V programming pulse (see *Programming Specifications* table) at the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

Verify Summing Matrix

1. Connect pin 28 (V_{CC}) to 5 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL LOW level.
4. Apply TTL levels to pins 4 through 9 (A_5 through A_0) to address an on-chip 1-of-48 decoder to select the AND gate to be verified (A_0 = LSB and A_5 = MSB).
5. Apply a TTL HIGH level to pins 20 and 22 (A_{15} and A_{13}).
6. Connect the remaining input pins to +12.0 V.
7. Sense the voltage on the output pin to be verified. The programming of the selected product line to the output line can be determined as follows:

Output Reads (Note)	Fuse Link
L	Blown (Inactive)
H	Unblown (Active)

Note
The condition of the fuse link can be determined from the table above regardless of the polarity (active HIGH or active LOW) of the output buffer being verified.

8. Repeat steps 4 through 7 with V_{CC} at the Low V_{CC} Read recommended value.

Program Output Polarity

The initial unprogrammed state of all eight output buffers is active LOW or inverting. To program an output buffer into the active HIGH or non-inverting state follow the steps shown below:

- Program one output at a time.

1. Connect pin 28 (V_{CC}) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply a TTL level to pins 4 through 9 (A_5 through A_0).
5. Apply a TTL HIGH level to pin 20 (A_{15}).
6. Connect the remaining input pins to +12.0 V.
7. Apply an 18 V programming pulse (see *Programming Specifications* table) to the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

Verify Output Polarity

1. Connect pin 28 (V_{CC}) to 5 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL LOW level.
4. Apply a TTL level to pins 4 through 9 (A_5 through A_0).
5. Apply a TTL HIGH level to pins 21 and 22 (A_{14} and A_{13}).
6. Connect the remaining input pins to +12.0 V.
7. Sense the voltage on the pin of the output buffer to be verified. The condition of the output can be determined as follows:

Output Reads	Output State
H	Active LOW
L	Active HIGH

8. Repeat step 7 with V_{CC} at the Low V_{CC} Read recommended value.

The table given below summarizes the full programming and verifying procedures.

Summary of Pin Voltages (Volts)

	Read	Program Product Matrix	Verify Product Matrix	Program Summing Matrix	Verify Summing Matrix	Program Output Polarity	Verify Output Polarity
Pin 1 (V_P)	***	15.0	***	***	***	***	***
Pin 2 (A_7)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 3 (A_6)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 4 (A_5)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 5 (A_4)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 6 (A_3)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 7 (A_2)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 8 (A_1)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 9 (A_0)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 10 (O_7)	READ	TTL	TTL	****	READ	****	READ
Pin 11 (O_6)	READ	TTL	TTL	****	READ	****	READ
Pin 12 (O_5)	READ	TTL	TTL	****	READ	****	READ
Pin 13 (O_4)	READ	TTL	TTL	****	READ	****	READ
Pin 14 (GND)	GND	GND	GND	GND	GND	GND	GND
Pin 15 (O_3)	READ	TTL	TTL	****	READ	****	READ
Pin 16 (O_2)	READ	TTL	TTL	****	READ	****	READ
Pin 17 (O_1)	READ	**	**	****	READ	****	READ
Pin 18 (O_0)	READ	READ	READ	****	READ	****	READ
Pin 19 ($\overline{CS}$)	TTL LOW	TTL HIGH	TTL HIGH	TTL HIGH	TTL LOW	TTL HIGH	TTL LOW
Pin 20 (A_{15})	TTL	12.0*	12.0*	TTL HIGH	TTL HIGH	TTL HIGH	12.0
Pin 21 (A_{14})	TTL	12.0*	12.0*	TTL HIGH	12.0	12.0	TTL HIGH
Pin 22 (A_{13})	TTL	12.0*	12.0*	12.0	TTL HIGH	12.0	TTL HIGH
Pin 23 (A_{12})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 24 (A_{11})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 25 (A_{10})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 26 (A_9)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 27 (A_8)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 28 (V_{CC})	5.0	5.0	5.0	5.0	5.0	5.0	5.0

*For selection of input apply TTL HIGH or TTL LOW
**Left open or TTL HIGH
***Left open or grounded
****Left open, TTL HIGH, or programming pulse

Programming Specifications

Symbol	Characteristic	Min	Recommended Value	Max	Unit	Comment
V_{IH}	TTL Levels	2.4	5.0	5.0	V	Apply to appropriate address and output pins. Do not leave pins open
V_{IL}		0	0	0.4	V	
$\overline{CS}$	Chip Select	2.4	5.0	5.0	V	
V_{OP}	Programming Voltage Pulse	17.5	18.0	18.5	V	Applied to appropriate output pin
V_P	Programming Voltage Pulse	14.5	15.0	15.5	V	Apply to V_P pin
t_{pw}	Programming Pulse Width		0.18	50	ms	
	Duty Cycle, Programming Pulse		20	*	%	*Maximum duty cycle to maintain $T_C < 85°C$
t_r	Programming Pulse Rise Time	0.5	1.0	3.0	μs	
	Number of Pulses Required	1	4	8		
V_{CC}	Power Supply Voltage	4.9	5.0	5.1	V	
T_C	Case Temperature		25	85	°C	
I_{VP}	Programming Pulse Current Limit (V_P Pin)			200	mA	If pulse generator is used, set current limit to this maximum value
I_{OP}	Programming Pulse Current Limit (Any Output Pin)			100	mA	If pulse generator is used, set current limit to this maximum value
LV_{CC}	Low V_{CC} Read	4.2	4.2 or 4.4	4.4	V	Programming Read Verify**

**4.2 V simulates −55°C operation, 4.4 V simulates 0°C operation.

16 x 48 x 8 FPLA Program Table

This Portion to be Completed by Fairchild

CF (XXXX) _____
Customer Symbolized Part # _____
Date Received _____
Comments _____

Customer Name _____
Purchase Order # _____
Fairchild Device # _____
Total Number of Parts _____
Program Table # _____ Rev _____ Date _____

Program Table Entries						
Input Variable			Output Function		Output Active Level	
A_n	$\overline{A}_n$	Immaterial	Product Term Present in F_r	Product Term Not Present in F_r	Active HIGH	Active LOW
H	L	- (dash)	A	· (period)	H	L
Note Enter (—) for *unused* inputs of *used* P terms			**Notes** 1) Entries independent of output polarity 2) Enter (A) for *unused* outputs of *used* P terms		**Notes** 1) Polarity programmed once only 2) Enter (L) for all *unused* outputs.	

Product Term*																	Active Level							
	Input Variable																							
No.	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Output Function*							
																	7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
4																								
5																								
6																								
7																								
8																								
9																								
10																								
11																								
12																								
13																								
14																								
15																								
16																								
17																								
18																								
19																								
20																								
21																								
22																								
23																								
24																								
25																								
26																								
27																								
28																								
29																								
30																								
31																								
32																								
33																								
34																								
35																								
36																								
37																								
38																								
39																								
40																								
41																								
42																								
43																								
44																								
45																								
46																								
47																								

*Input and Output fields of *unused* P terms can be left blank

8

DC Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93459 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA	
I_{IL}	Input LOW Current		−160	−250	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93459 only)			50 −50	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93459 only)			100 −100	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93458 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, −0°C to +75°C Chip Deselected	
I_{CEX}	Output Leakage Current (93458 only)			150	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93459 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2	
I_{CC}	Power Supply Current		105	170	mA	V_{CC} = Max, Chip Selected, Note 3	
C_{IN}	Input Pin Capacitance		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 4.0 V, f = 1.0 MHz	
C_O	Output Pin Capacitance		7.0		pF	V_{CC} 5.0 = V, V_O = 4.0 V, f = 1.0 MHz	

Commercial
AC Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_A = 0°C to +75°C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	45	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	30	ns	See AC Output Load

Military

AC Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_A = 55°C to +125°C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	65	ns	See AC Test Output Load
t_{ACS}	Chip Select to Output Access Time	30	ns	See AC Test Output Load

1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.
3. For programmed part, add 0.45 mA typical, 0.60 mA maximum per selected programmed product terms and add 2.9 mA typical, 3.9 mA maximum per enabled low output or 33 mA typical, 44 mA maximum for disabled states.

Fig. 1 AC Test Loads

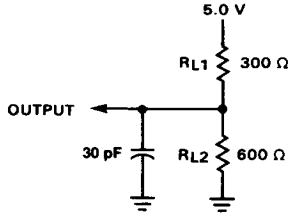


Fig. 3 Read Mode Timing

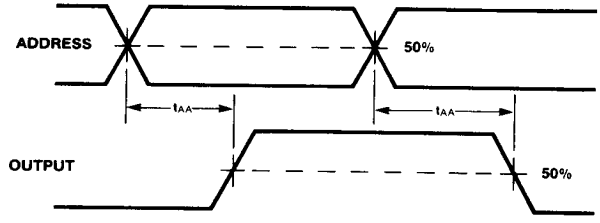
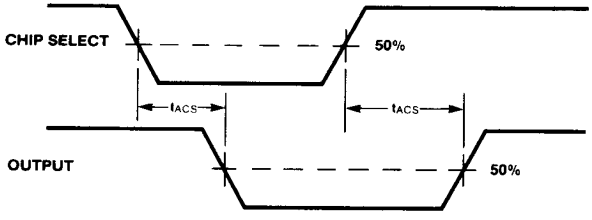
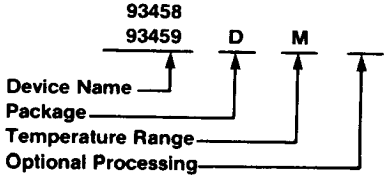


Fig. 2 Input Levels



8

Ordering Information



Packages
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

Temperature Ranges
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 & 5005, Level B
QC = Mil Std 883
Method 5004 & 5005, Level C
QR = Commercial Device with
160 Hour Burn In