REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thomas M. Hess	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 93-09-16 REVISION LEVEL	MICROCIRCUIT, DIGITAL, CMOS, 8-16 BIT PARALLEL INTERFACE/TIMER MONOLITHIC SILICON SIZE A | CAGE CODE 67268 | 5962-93170 SHEET 1 OF 26

DESC FORM 193
JUL 91

5962-E356-93

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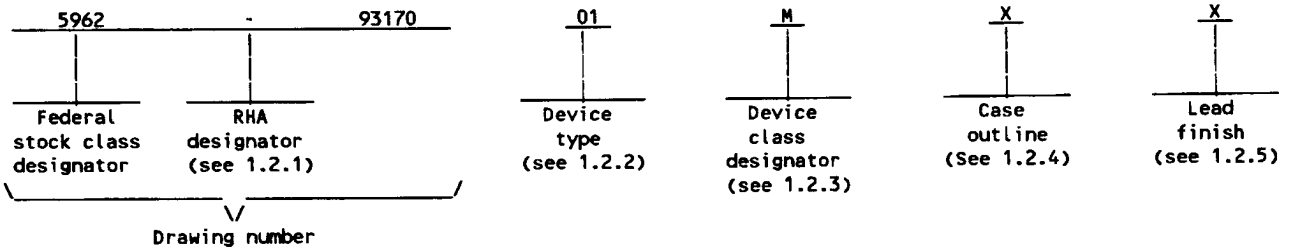
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68230-8	8-16 Bit Parallel Interface/Timer
02	68230-10	8-16 Bit Parallel Interface/Timer

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T48 or CDIP2-T48	48	Dual in line
Y	CQCC1-N52	52	Square Leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/

Supply voltage range with respect to GND (V_{CC})	-0.3 V dc to +7.0 V dc
Storage temperature range	-55°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+170°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.75 V dc minimum to 5.25 V dc maximum
High level input voltage range (V_{IH}):	
All inputs	2.0 V dc to 5.25 V dc
Low level input voltage range (V_{IL}):	
All inputs	GND -0.3 V dc to 0.8 V dc
Minimum high level output voltage (V_{OH})	2.4 V dc
Maximum low level output voltage (V_{OL})	0.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Static characteristics							
High level input voltage (all inputs)	V_{IH}		1,2,3	01, 02	2.0	V_{CC} +0.3	V
Low level input voltage (all inputs)	V_{IL}		1,2,3	01, 02	-0.3	0.8	V
Low level output PC3/TOUT, PC5/$\overline{PIRQ}$	V_{OL}	I_{OL} = 8.8 mA V_{CC} = 4.75 V	1,2,3	01, 02		0.5	V
Low level output voltage D0/D7, $\overline{DTACK}$	V_{OL}	I_{OL} = 5.3 mA V_{CC} = 4.75 V	1,2,3	01, 02		0.5	V
Low level output voltage PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	V_{OL}	I_{OL} = 2.4 mA V_{CC} = 4.75 V	1,2,3	01, 02		0.5	V
High level output D0-D7, $\overline{DTACK}$	V_{OH}	I_{OH} = -400 µA V_{CC} = 4.75 V	1,2,3	01, 02	2.4		V
High level output voltage H2, H4, PB0-PB7, PA0-PA7	V_{OH}	I_{OH} = -150 µA V_{CC} = 4.75 V	1,2,3	01, 02	2.4		V
High level output voltage PC0-PC7	V_{OH}	I_{OH} = -100 µA V_{CC} = 4.75 V	1,2,3	01, 02	2.4		V
Supply current	I_{CC}	V_{CC} = 5.25 V	1,2,3	01, 02		133	mA
High level input current H1, H3, RESET, CLK, RS1-RS5, $\overline{CS}$	I_{IH}	V_{IN} = 5.25 V	1,2,3	01, 02		10	µA
Low level input current H1, H3, RESET CLK, RS1-RS5, $\overline{CS}$	I_{IL}	V_{IN} = 0 V	1,2,3	01, 02	-10		µA
Power off leakage	I_{LO}		1,2,3	01, 02	-10	+10	µA
Tristate input high leakage $\overline{DTACK}$, PC0-PC7, D0-D7	I_{OZH1}	V = 2.4 V V_{CC} = 5.25 V	1,2,3	01, 02	-20	+20	µA
Tristate input high leakage H2, H4, PA0-PA7, PB0-PB7	I_{OZH2}	V = 2.4 V V_{CC} = 5.25 V	1,2,3	01, 02	-0.1	+0.1	mA
Tristate input low leakage $\overline{DTACK}$, PC0-PC7, D0-D7	I_{OZL1}	V = 0.4 V V_{CC} = 5.25 V	1,2,3	01, 02	-20	+20	µA
Tristate input low leakage H2, H4, PA0-PA7, PB0-PB7	I_{OZL2}	V = 0.4 V V_{CC} = 5.25 V	1,2,3	01, 02	-0.1	+0.1	mA

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Static characteristics (continued)							
Input capacitance (all inputs)	C_{IN}	Reverse voltage = 0 V f = 1.0 MHz, See 4.4.1c	4	01, 02		25	pF
Functional testing		See 4.4.1b	7,8	01, 02			
Dynamic (switching) characteristics Read write cycle timings							
R/$\overline{W}$, RS1-RS5 valid to $\overline{CS}$ low	t_{su} (TRVSL)	F = 8 MHz	9,10,11	01	0		ns
		F = 10 MHz		02	0		
$\overline{CS}$ low to R/$\overline{W}$ and RS1-RS5 invalid 2/	t_h (TSRI)	F = 8 MHz	9,10,11	01	100		ns
		F = 10 MHz		02	65		
$\overline{CS}$ low to CLK low 3/	t_{su} (TSLCL)	F = 8 MHz	9,10,11	01	30		ns
		F = 10 MHz		02	20		
$\overline{CS}$ low to data out valid 4/	t_{phl} t_{plh} (TSLDV)	F = 8 MHz, Load B	9,10,11	01		75	ns
		F = 10 MHz, Load B		02		60	
RS1-RS5 valid to data out valid	t_{phl} t_{plh} (TRLDV)	F = 8 MHz, Load B	9,10,11	01		140	ns
		F = 10 MHz, Load B		02		105	
CLK low to $\overline{DTACK}$ low (read-write cycle time)	t_{phl} (TCLDL)	F = 8 MHz, Load E	9,10,11	01	0	70	ns
		F = 10 MHz, Load E		02	0	60	
$\overline{DTACK}$ low to $\overline{CS}$ high 5/	t_h (TDTLSH)	F = 8 MHz	9,10,11	01	0		ns
		F = 10 MHz		02	0		
$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	t_{plh} t_{phl} (TSHDI)	F = 8 MHz, Load B	9,10,11	01	0		ns
		F = 10 MHz, Load B		02	0		
$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	t_{plz} t_{phz} (TSHDZ)	F = 8 MHz, Load B	9,10,11	01		50	ns
		F = 10 MHz, Load B		02		45	
$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high	t_{plh} (TSHDH)	F = 8 MHz, Load E	9,10,11	01	0	50	ns
		F = 10 MHz, Load E		02		45	
$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high (to $\overline{DTACK}$ high Z)	t_{phz} (TSHDTZ)	F = 8 MHz, Load E	9,10,11	01	0	100	ns
		F = 10 MHz, Load E		02		55	
Data in valid to $\overline{CS}$ low	t_{su} (TDVSL)	F = 8 MHz	9,10,11	01	0		ns
		F = 10 MHz		02	0		

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic (switching) characteristics Read and write cycle timings (continued)							
$\overline{CS}$ low to data in invalid	t_h (TSLDI)	F = 8 MHz, Load B	9,10,11	01	100		ns
		F = 10 MHz, Load B		02	65		
CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	t_{phl} (TCDAM-ACDMN)	F = 8 MHz, Load T	9,10,11	01	2.5	3	CLK. per
		F = 10 MHz, Load T		02	2.5	3	
Synchronized $\overline{CS}$ to CLK low on which $\overline{DMAREQ}$ is asserted 6/	t_{phl} (TSSC-LDMA)	F = 8 MHz, Load T	9,10,11	01	3	3	CLK. per
		F = 10 MHz, Load T		02	3	3	
CLK low to $\overline{DMAREQ}$ low	t_{phl} (TCLDML)	F = 8 MHz, Load T	9,10,11	01	0	120	ns
		F = 10 MHz, Load T		02	0	100	
CLK low to $\overline{DMAREQ}$ low	t_{plh} (TCLDMH)	F = 8 MHz, Load T	9,10,11	01	0	120	ns
		F = 10 MHz, Load T		02	0	100	
Synchronized H1(H3) to CLK low on which PIRQ is asserted	t_{phl} (TSHC-LPIA)	F = 8 MHz, Load U	9,10,11	01	3	3	CLK. per
		F = 10 MHz, Load U		02	3	3	
Synchronized H1(H3) to CLK low on which PIRQ is high Z 6/	t_{phl} (TSHC-LPIZ)	F = 8 MHz, Load U	9,10,11	01	3	3	CLK. per
		F = 10 MHz, Load U		02	3	3	
CLK low to $\overline{PIRQ}$ low or high Z	t_{plz} t_{phl} (TCLPLZ)	F = 8 MHz, Load U	9,10,11	01	0	250	ns
		F = 10 MHz, Load U		02	0	225	
TIN frequency (external CLK) prescaler used 7/	t_{cy} (TINPU)	F = 8 MHz	9,10,11	01	0	1	f clk (HZ) 8/
		F = 10 MHz		02	0	1	
TIN frequency (external CLK) prescaler not used	t_{cy} (TINPN)	F = 8 MHz	9,10,11	01	0	1/8	f clk (HZ) 8/
		F = 10 MHz		02	0	1/8	
TIN pulse width high or low (external CLK)	t_w (TIWEC)	F = 8 MHz	9,10,11	01	55		ns
		F = 10 MHz		02	45		
TIN pulse width low (RUN/halt control)	t_w (TIWRH)	F = 8 MHz	9,10,11	01	1		CLK. per
		F = 10 MHz		02	1		

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic (switching) characteristics Read and write cycle timings (continued)							
CLK low to tout high, low or H-Z	t_{plh} t_{plz} (TCTHZ)	F = 8 MHz, Load U	9,10,11	01	0	250	ns
		F = 10 MHz, Load U		02	0	225	
$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ low	t_{phl} (SHSL)	F = 8 MHz, Load T	9,10,11	01	50		ns
		F = 10 MHz, Load T		02	30		
Dynamic (switching) characteristics Peripheral input timings							
Port input data valid to H1 (H3) asserted	t_{su} (TDVHA)	F = 8 MHz	9,10,11	01	100		ns
		F = 10 MHz		02	60		
H1 (H3) asserted to port data invalid	t_h (THADI)	F = 8 MHz, Load B	9,10,11	01	20		ns
		F = 10 MHz, Load B		02	20		
Handshake input H2 (H4) pulse width asserted	t_w (THWA)	F = 8 MHz	9,10,11	01	40		ns
		F = 10 MHz		02	40		
Handshake input H2 (H4) pulse width negated	t_w (THWN)	F = 8 MHz	9,10,11	01	40		ns
		F = 10 MHz		02	40		
H1 (H3) asserted to H2 (H4) negated	t_{plh} (THAHN)	F = 8 MHz, Load S	9,10,11	01		150	ns
		F = 10 MHz, Load S		02		120	
CLK low to H2 (H4) asserted	t_{phl} (TCLHA)	F = 8 MHz, Load S	9,10,11	01		100	ns
		F = 10 MHz, Load S		02		100	
H1 (H3) asserted to H2 (H4) asserted 9/	t_{phl} (THAHA)	F = 8 MHz, Load S	9,10,11	01	0		ns
		F = 10 MHz, Load S		02	0		
CLK low to H2 (H4) pulse negated 10/	t_{plh} (TCLHN)	F = 8 MHz, Load S	9,10,11	01		125	ns
		F = 10 MHz, Load S		02		125	
Synchronized H1(H3) to CLK low on which DMAREQ is asserted 11/ 12/	t_{plh} (TSHC-LDMA)	F = 8 MHz, Load T	9,10,11	01	2.5	3.5	ns
		F = 10 MHz, Load T		02	2.5	3.5	
CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which DMAREQ is negated	t_{phl} (TCDAMA-CDMN)	F = 8 MHz, Load T	9,10,11	01	2.5	3	CLK. per
		F = 10 MHz, Load T		02	2.5	3	

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic (switching) characteristics Peripheral input timings (continued)							
H1 (H3) asserted to CLK high 13/	t_{su} (THACH)	F = 8 MHz	9,10,11	01	50		ns
		F = 10 MHz		02	40		
Synchronized H1(H3) to CLK low on which H2 (H4) asserted 11/ 12/	t_{plh} (TSHC-LHA)	F = 8 MHz, Load S	9,10,11	01	3.5	4.5	ns
		F = 10 MHz, Load S		02	3.5	4.5	
CLK low to $\overline{\text{DMAREQ}}$ low	t_{plh} (TCLDML)	F = 8 MHz, Load T	9,10,11	01	0	120	ns
		F = 10 MHz, Load T		02	0	100	
CLK low to $\overline{\text{DMAREQ}}$ high	t_{plh} (TCLDMH)	F = 8 MHz, Load T	9,10,11	01	0	120	ns
		F = 10 MHz, Load T		02	0	100	
Dynamic (switching) characteristics Peripheral output timings							
Handshake input H2 (H4) pulse width asserted	t_w (THWA)	F = 8 MHz	9,10,11	01	40		ns
		F = 10 MHz		02	40		
Handshake input H2 (H4) pulse width negated	t_w (THWN)	F = 8 MHz	9,10,11	01	40		ns
		F = 10 MHz		02	40		
H1 (H3) asserted to H2 (H4) negated	t_{plh} (THAHN)	F = 8 MHz, Load S	9,10,11	01		150	ns
		F = 10 MHz, Load S		02		120	
CLK low to H2 (H4) asserted	t_{phl} (TCLHA)	F = 8 MHz, Load S	9,10,11	01		100	ns
		F = 10 MHz, Load S		02		100	
H1 (H3) asserted to H2 (H4) asserted 9/	t_{phl} (THAHA)	F = 8 MHz, Load S	9,10,11	01	0		ns
		F = 10 MHz, Load S		02	0		
CLK low to H2 (H4) pulse negated 10/	t_{plh} (TCLHN)	F = 8 MHz, Load S	9,10,11	01		125	ns
		F = 10 MHz, Load S		02		125	
Synchronized H1 (H3) to CLK low on which $\overline{\text{DMAREQ}}$ is asserted 11/ 12/	t_{plh} (TSHC-LDMA)	F = 8 MHz, Load T	9,10,11	01	2.5	3.5	ns
		F = 10 MHz, Load T		02	2.5	3.5	
CLK low on which $\overline{\text{DMAREQ}}$ is asserted to CLK low on which $\overline{\text{DMAREQ}}$ is negated	t_{plh} (TCDMA-CDMN)	F = 8 MHz, Load T	9,10,11	01	2.5	3	CLK. per
		F = 10 MHz, Load T		02	2.5	3	

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Units
					Min	Max	
Dynamic (switching) characteristics Peripheral output timings (continued)							
CLK low to port output data valid (Modes 0 or 1)	t_{plh} t_{phl} (TCLPOD)	F = 8 MHz, Load B	9,10,11	01		150	ns
		F = 10 MHz, Load B		02		120	
Synchronized H1 (H3) to port output data invalid (Mode 0 and 1) 11/ 12/	t_{phl} t_{plh} (TSHDI)	F = 8 MHz, Load B	9,10,11	01	1.5	2.5	CLK per
		F = 10 MHz, Load B		02	1.5	2.5	
H1 negated to port output data valid (Mode 2 and 3)	t_{phl} t_{plh} (THNDV)	F = 8 MHz, Load B	9,10,11	01		70	ns
		F = 10 MHz, Load B		02		60	
H1 asserted to port output data high Z (Mode 2 and 3)	t_{phz} t_{plz} (THADZ)	F = 8 MHz, Load B	9,10,11	01		70	ns
		F = 10 MHz, Load B		02	0	70	
H1 (H3) asserted to CLK high 13/	t_{su} (THACH)	F = 8 MHz, Load T	9,10,11	01	50		ns
		F = 10 MHz, Load T		02	40		
CLK low to $\overline{\text{DMAREQ}}$ low	t_{plh} (TCLDML)	F = 8 MHz, Load T	9,10,11	01	0	120	ns
		F = 10 MHz, Load T		02	0	100	
CLK low to $\overline{\text{DMAREQ}}$ high	t_{plh} (TCLDMH)	F = 8 MHz, Load T	9,10,11	01	0	120	ns
		F = 10 MHz, Load T		02	0	100	
Dynamic (switching) characteristics IACK timings							
$\overline{\text{CS}}$ or $\overline{\text{PIACK}}$ or $\overline{\text{TIACK}}$ high to data out invalid	t_{plh} t_{phl} (TSHDI)	F = 8 MHz, Load B	9,10,11	01	0		ns
		F = 10 MHz, Load B		02	0		
$\overline{\text{CS}}$ or $\overline{\text{PIACK}}$ or $\overline{\text{TIACK}}$ high to D0-D7 high Z	t_{plz} t_{phz} (TSDHZ)	F = 8 MHz, Load B	9,10,11	01		50	ns
		F = 10 MHz, Load B		02		45	
$\overline{\text{CS}}$ or $\overline{\text{PIACK}}$ or $\overline{\text{TIACK}}$ high to $\overline{\text{DTACK}}$ high Z	t_{plh} (TSHDH)	F = 8 MHz, Load E	9,10,11	01		50	ns
		F = 10 MHz, Load E		02		45	
$\overline{\text{CS}}$ or $\overline{\text{PIACK}}$ or $\overline{\text{TIACK}}$ high to $\overline{\text{DTACK}}$ high Z	t_{phz} (TSHDTZ)	F = 8 MHz, Load E	9,10,11	01		100	ns
		F = 10 MHz, Load E		02		55	
CLK low to data output valid interrupt acknowledge	t_{plh} t_{phl} (TCLDV-IAC)	F = 8 MHz, Load B	9,10,11	01		120	ns
		F = 10 MHz, Load B		02		105	

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic (switching) characteristics IACK timings (continued)							
$\overline{PIACK}$ to $\overline{TIACK}$ low to CLK low	t_{su} (TILCL)	F = 8 MHz	9,10,11	01	50		ns
		F = 10 MHz		02	40		
CLK low to $\overline{DTACK}$ low interrupt acknowledge	t_{phl} (TCLDL-IAC)	F = 8 MHz, Load E	9,10,11	01		100	ns
		F = 10 MHz, Load E		02		100	

NOTES:

1/ All testing to be performed using worst-case test conditions unless otherwise specified. Supply voltage range to be $4.75\ V \le V_{CC} \le 5.25\ V$. AC testing shall be at $V_{CC} = 4.5\ V$, see figure 3 for timing waveforms.

2/ See bus interface operation for exception.

3/ This parameter only applies if the PI/T had completed all operations initiated by previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted if $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this parameter is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

4/ Assuming the RS1-RS5 to data valid time has also expired.

5/ This parameter imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.

6/ Synchronized means that the input signal has been by the PI/T on the appropriate edge of the clock (rising edge for H1 (H3) and falling edge for $\overline{CS}$). (Refer to the 1.4 Bus Interface Operation for the exception concerning $\overline{CS}$).

7/ This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80% to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an "AND" function of the clock and a control signal.

8/ CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.

9/ This parameter assures recognition of the asserted edge to H1 (H3).

10/ This parameter applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

11/ The maximum value is caused by a peripheral access (H1)(H3) asserted and bus access ($\overline{CS}$ asserted) occurring at the same time.

12/ Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$). (Refer to the 1.4 Bus Interface Operation for the exception concerning $\overline{CS}$).

13/ If the setup time on the rising edge of the clock is not met, H1 (H3) may not be recognized until the next rising of the clock.

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Device Type	01, 02	Device Type	01, 02
Case Outline	X	Case Outline	X
Terminal Number	Terminal Connection	Terminal Number	Terminal Connection
1	D5	25	RS5
2	D6	26	RS4
3	D7	27	RS3
4	PA0	28	RS2
5	PA1	29	RS1
6	PA2	30	PC0
7	PA3	31	PC1
8	PA4	32	PC2/TIN
9	PA5	33	PC3/TOUT
10	PA6	34	PC4/$\overline{\text{DMAREQ}}$
11	PA7	35	PC5/$\overline{\text{PIRQ}}$
12	V_{CC}	36	PC6/$\overline{\text{PIACK}}$
13	H1	37	PC7/$\overline{\text{TIACK}}$
14	H2	38	V_{SS}
15	H3	39	$\overline{\text{RESET}}$
16	H4	40	CLK
17	PB0	41	$\overline{\text{CS}}$
18	PB1	42	$\overline{\text{DTACK}}$
19	PB2	43	R/$\overline{\text{W}}$
20	PB3	44	D0
21	PB4	45	D1
22	PB5	46	D2
23	PB6	47	D3
24	PB7	48	D4

FIGURE 1. Terminal connections.

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Device Type	01, 02	Device Type	01, 02
Case Outline	Y	Case Outline	Y
Terminal Number	Terminal Connection	Terminal Number	Terminal Connection
1	D5	27	PB7
2	D6	28	RS5
3	D7	29	RS4
4	PA0	30	RS3
5	PA1	31	RS2
6	PA2	32	RS1
7	PA3	33	NC
8	NC	34	PC0
9	PA4	35	PC1
10	PA5	36	PC2
11	PA6	37	PC3
12	PA7	38	PC4
13	V_{CC}	39	PC5
14	H1	40	PC6
15	H2	41	PC7
16	H3	42	V_{SS}
17	H4	43	$\overline{RESET}$
18	PB0	44	CLK
19	PB1	45	$\overline{CS}$
20	NC	46	$\overline{DTACK}$
21	NC	47	$R/\overline{W}$
22	PB2	48	D0
23	PB3	49	D1
24	PB4	50	D2
25	PB5	51	D3
26	PB6	52	D4

FIGURE 1. Terminal connections. - Continued

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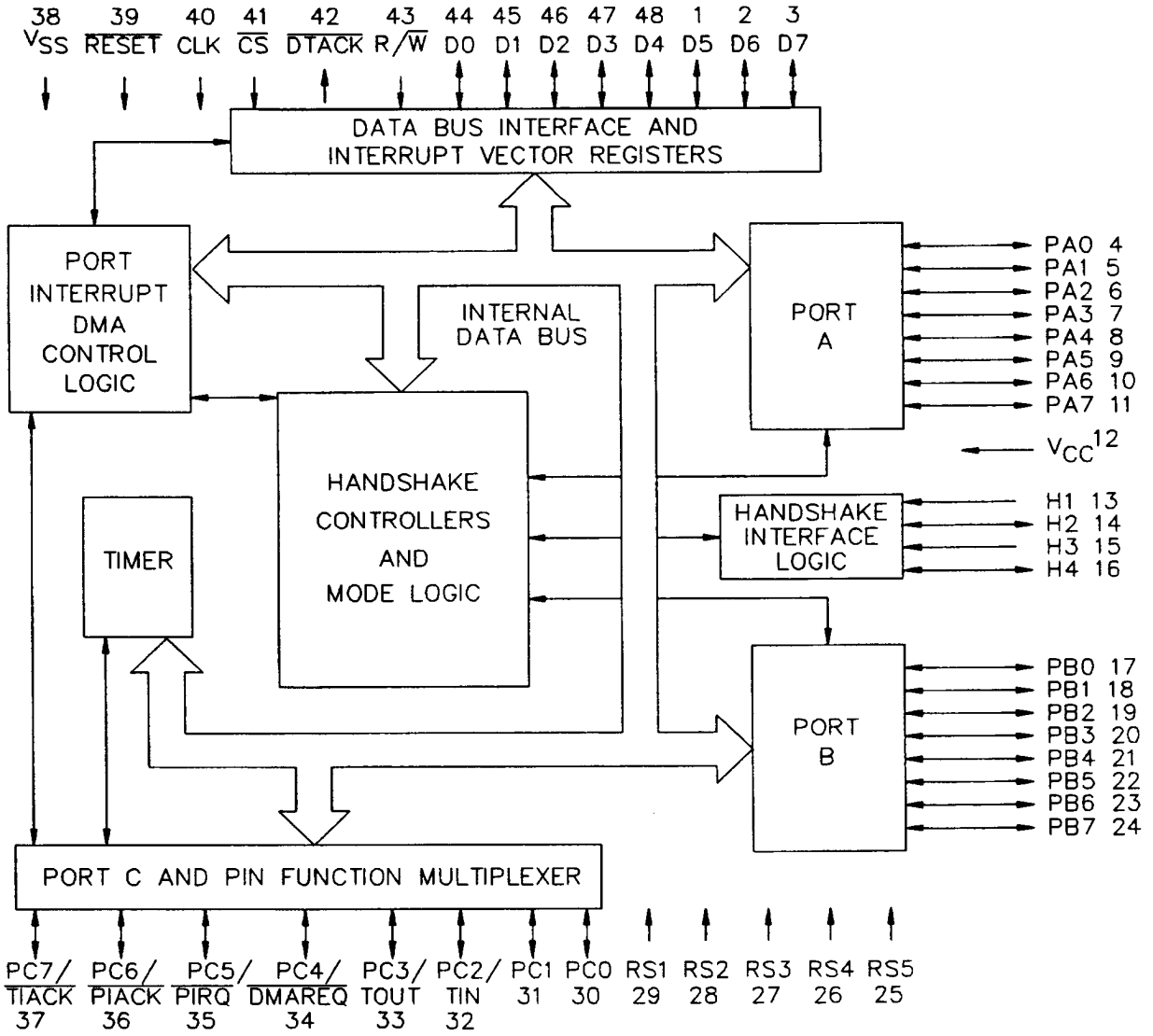

Note:
1. Pinouts refer to case outline "X".

FIGURE 2. Functional block diagram.

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Load NBR	Figure	R1	R2	C1	Output application
B	A	750	19 K	82 pF	D0-D7
T	B	1.62 K	24.3 K	---	PC0,PC1,PC2,PC4,PC6,PC7
S	C	1.62 K	16.2 K	---	PA0-PA7, H2, H4, PB0-PB7
U	D	475	---	---	PC5,PC3
E	E	750	---	82 pF	DTACK

TYPE B

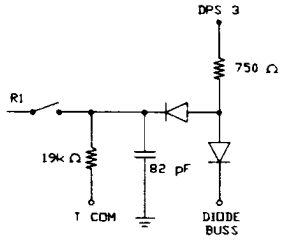

FIGURE A

TYPE T

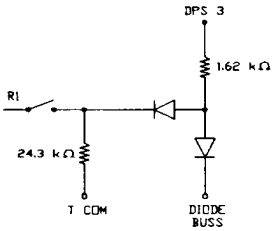

FIGURE B

TYPE S

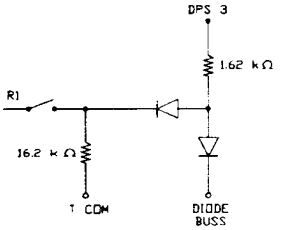

FIGURE C

TYPE U

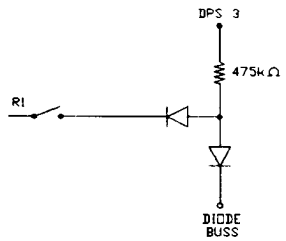

FIGURE D

TYPE E

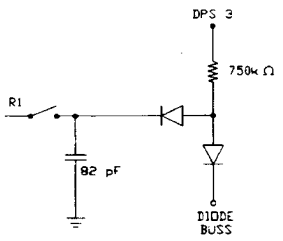

FIGURE E

FIGURE 3. Timing waveforms.

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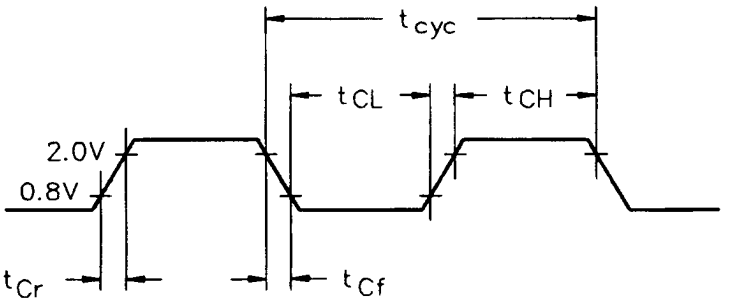
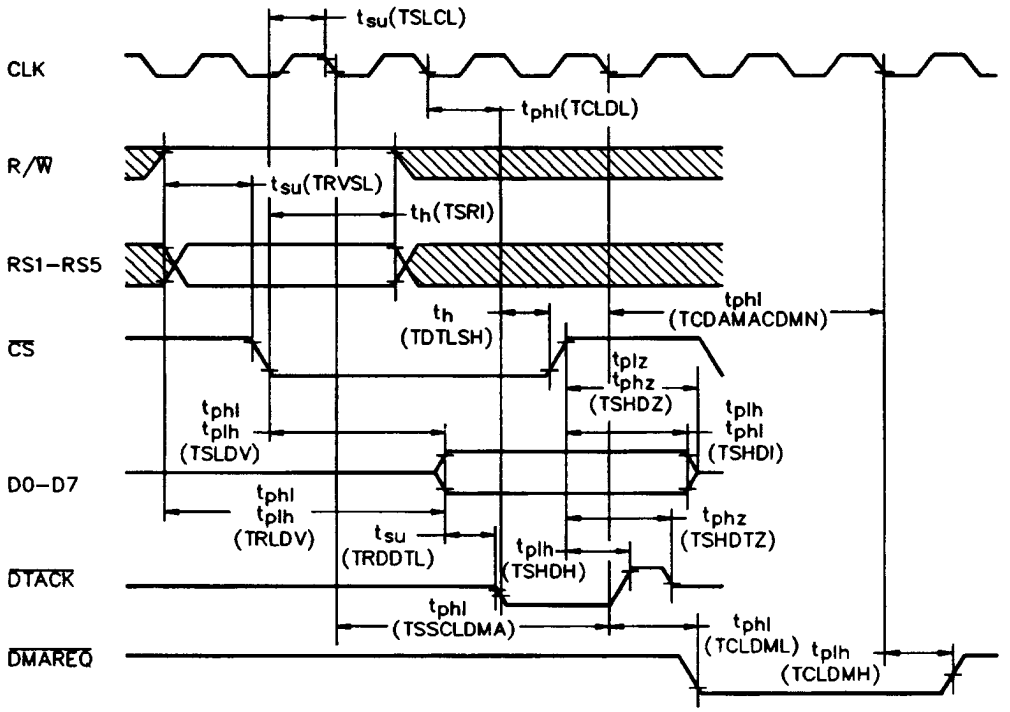


Clock input timing diagram



Read cycle timing diagram

FIGURE 3. Timing waveforms. - Continued

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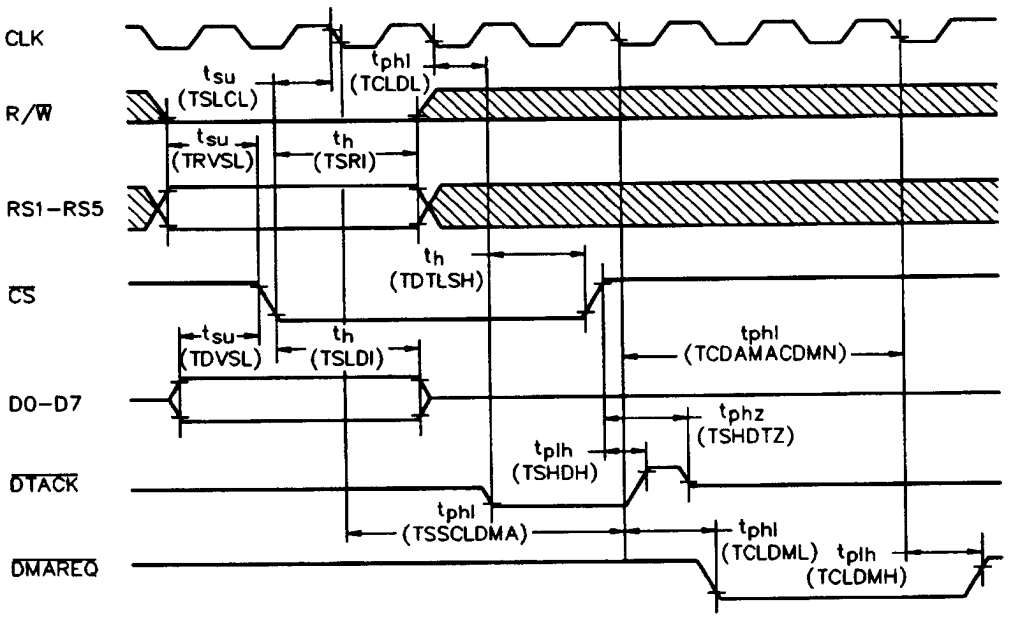

Write cycle timing diagram.

NOTE: 1. Timing requirements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. Timing waveforms. - Continued

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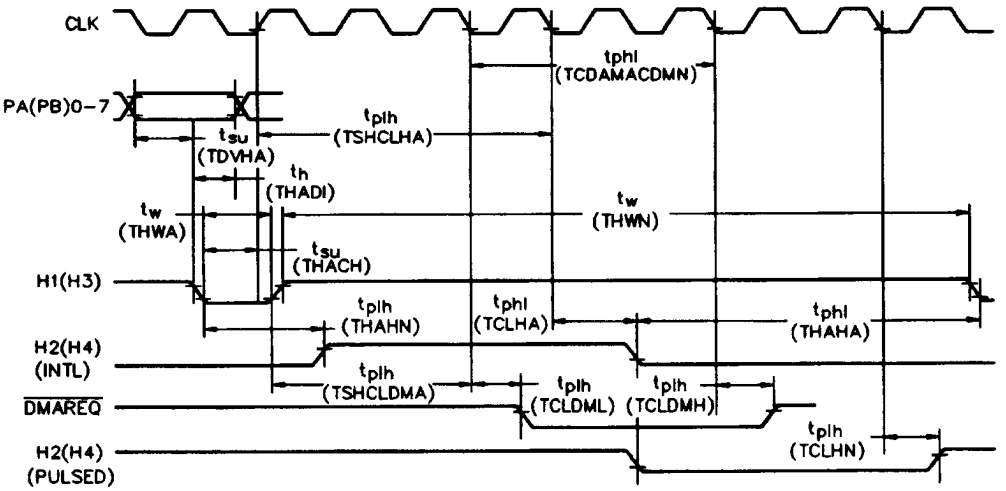

NOTES: 1. Timing diagram shows H1, H2, H3 and H4 asserted low.
2. Timing requirements are referenced to and from a low voltage of 0.8 volt and from a high voltage of 2.0 volts, unless otherwise noted.

Peripheral input timing diagram.

FIGURE 3. Timing waveforms. - Continued

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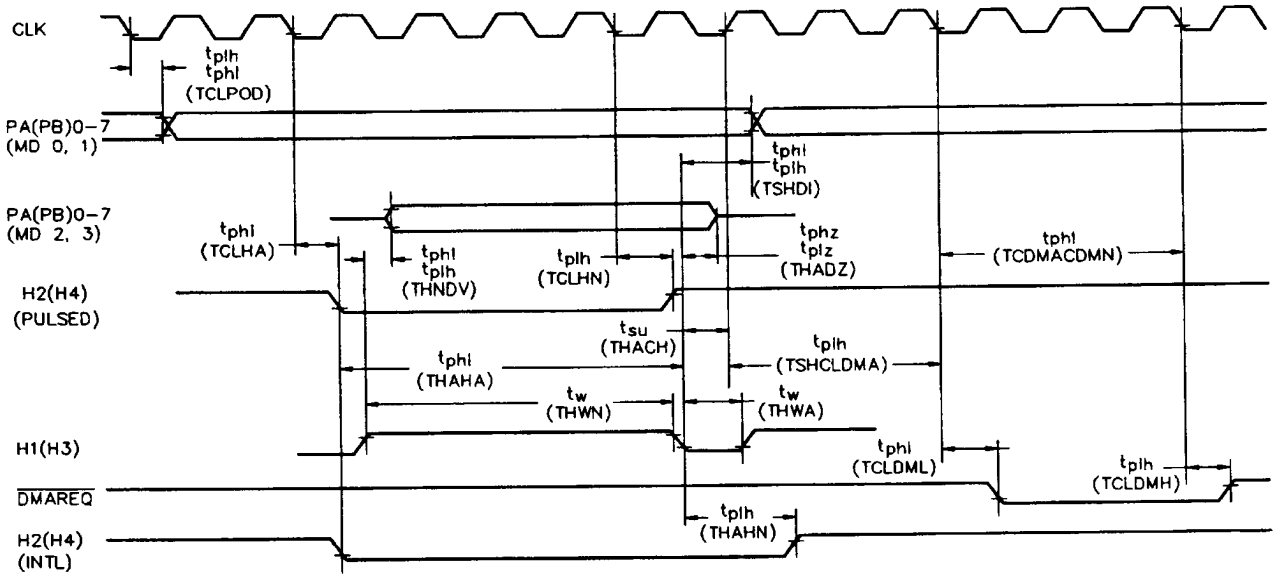

NOTES:

1. TIMING DIAGRAM SHOWS H1, H2, H3 AND H4 ASSERTED LOW.
2. TIMING REQUIREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLT AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

PERIPHERAL OUTPUT TIMING DIAGRAM.

FIGURE 3. Timing waveforms. - Continued

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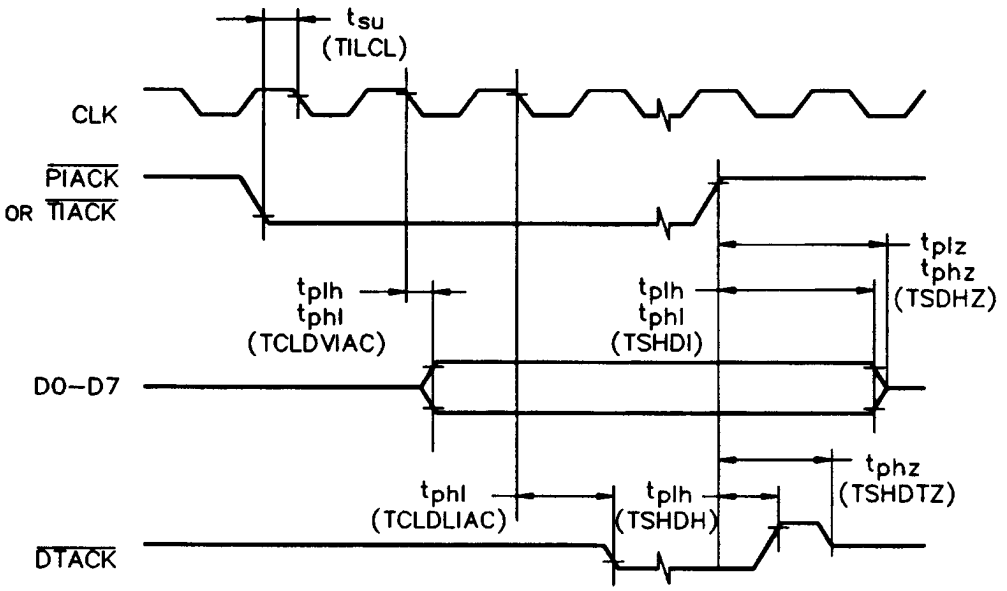

NOTES: 1. Timing requirements are referenced to and from a low voltage of 0.8 volt and from a high voltage of 2.0 volts, unless otherwise noted.

IACK timing

FIGURE 3. Timing waveforms. - Continued

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4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4(C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7, 8, 9,10,11	1,2,3,4,7, 8, 9,10,11	1,2,3,4,7 8, 9,10,11	1,2,3,4,7, 8, 9,10,11	1,2,3,4,7, 8, 9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	2,7,8a,9, 10	---	---
Group C end-point electrical parameters (see 4.4)	2,7, 8a, 9,10	2,7, 8a, 9,10	---	2,7, 8a, 9,10	2,7, 8a, 9,10
Group D end-point electrical parameters (see 4.4)	2,7, 8a, 9,10	2,7, 8a, 9,10	2,7, 8a, 9,10	2,7, 8a, 9,10	2,7, 8a, 9,10
Group E end-point electrical parameters (see 4.4)	---	---	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

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b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331 and as in table III.

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Table III. Pin descriptions.

Symbol	Function	Category
V_{CC}	Power supply	Supply terminal
V_{SS}	Power supply	Supply terminal
D0-D7	Bidirectional data bus	Bi-directional
RS1-RS5	Register select	Input
R/W	Read/Write	Input
CS	Chip select	Input
DTACK	Data transfer acknowledge	Output
RESET	Reset	Input
CLK	Clock	Input
PA0-PA7 PB0-PB7	Port A and Port B	Input/Output
H1-H3	Handshake Pins	Input
H2-H4	Handshake Pins	Input or Output
PC0-PC7	Port C	Input or Output

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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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