T-52-33-45

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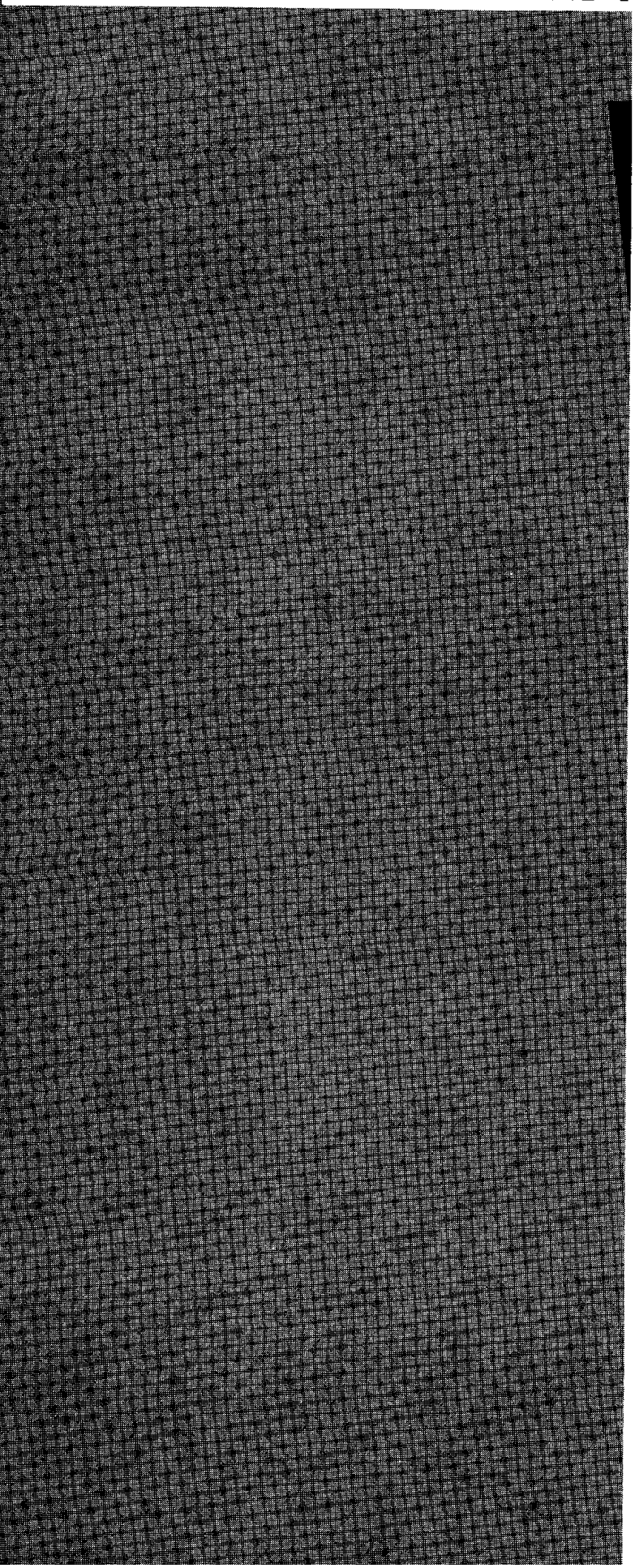
WD90C31A

High Performance Video Controller with Windows Accelerator



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ADDITIONAL REFERENCES

IBM Personal Computer Hardware User Guide (IBM # 6322510)
IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
IBM Personal System 2 Model 30 Hardware User Guide (IBM # 63x2230)
IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 63x2201)
IBM PC Options And Adapters Technical Reference Manual (IBM # 6322509)
IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)

1.0 INTRODUCTION

The WD90C31A VGA Controller is a 0.9 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with either the AT bus or the IBM Micro Channel bus, while maintaining backward compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. A major advantage of the WD90C31A is that designs implementing this graphics controller are able to run applications requiring VGA hardware and BIOS compatibility and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C31A supports high resolution graphics with 1024 by 768 dot resolution and 256 colors. The WD90C31A also supports 132-column text mode and 6-16 pixel fonts.

This document supplies a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information and associated references.

1.1 FEATURES

- A full-function VGA controller optimized for windows.
- Hardware Cursor.
  - Up to 64 by 64 pixels.
  - Inversion and transparency.
  - Two color and three color modes.
  - Pattern fill.
- Hardware BITBLT.
  - Raster operations.
  - Transparency.
  - Color expansion for text support.
  - Rectangular and linear addressing.
  - Filled rectangles.
  - Transfers to and from the Host.
- Provides single chip video graphics solution for IBM AT and PS/2 compatible systems.
- Supports two, four or eight 64K by 16 DRAMs; four or eight 256K by 4 DRAMs; and one or two 256K by 16 DRAMs. ①
- Pin compatible with the WD90C30.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics and AT&T Model 6300 compatible.
- Supports all IBM VGA modes with two 64K by 16 DRAMs or only one 256K by 16 DRAM. ①
- With more DRAMS installed it can support 256 colors at the following resolutions: 640 by 400, 640 by 480, 800 by 600 and 1024 by 768. ②
- Supports 132-column text.
- Write buffer for zero wait state CPU write performance.
- 8-bit or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Provides 16-bit or 32-bit memory interface with fast page operations.
- Up to 80 MHz maximum video clock rate. ②
- Up to 50 MHz maximum memory clock rate. ②
- Up to four simultaneous displayable fonts.
- 6-16 pixel-wide fonts.
- A maximum of 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Eleven-bit vertical counter to support scan resolution of up to 2048 scan lines.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC and overscan registers.
- Special CRTC shadow registers for support of non-standard monitors.
- Special register locking for flat panel applications.

- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- Low power 0.9 micron CMOS technology.
- 132-pin PQFP (Plastic Quad Flat Package) or 144-pin MQFP (Metric Quad Flat Package).
- Integrated Feature connector interface and external RAMDAC support.
- Integrated bus interface for AT and Micro Channel with minimum external component support.
- Programmable memory mapping register to map WD90C31A into any CPU memory address space.
- Eight-bit CPU address offset register to support 1 Mbyte memory segmentation.

① 256 by 16 DRAMs must have nine address lines, one $\overline{CAS}$ line and two $\overline{WE}$ lines.

② Refer to Section 13.9 for high resolution mode considerations.

1.2 GENERAL DESCRIPTION

This document describes the WD90C31A VGA controller specifically designed for the Microsoft Windows marketplace. The WD90C31A incorporates numerous advanced features that Windows drivers may take advantage of for increased performance.

Although the WD90C31A replaces the WD90C31 it is identical to the WD90C31 in pinout and functionality. The WD90C31A provides substantial performance improvement over the WD90C31 when used with the Western Digital BIOS version 521 and Western Digital utilities version 4.2 or newer.

The WD90C31A is fully compatible with the WD90C30, making it possible to utilize the additional features of the WD90C31A by upgrading only the BIOS and software drivers.

1.2.1 Hardware Cursor

The WD90C31A supports a hardware cursor with a user-defined pattern of up to 64 by 64 pixels at two bits per pixel. The cursor pattern is stored in off-screen display memory. A programmable origin is provided and cursors may be displayed with any two or three desired colors.

1.2.2 Hardware BITBLT

The WD90C31A provides hardware accelerated Bit Block Transfers (BITBLT) of data between regions of display memory, or between display memory and a fixed I/O port. Display memory regions may be rectangular or linear.

The BITBLT hardware supports text modes as well as monochrome, 4-bit (16-color) and 8-bit (256 color) modes.

A full complement of raster operations and transparencies are available, as well as 8 by 8 color patterns. Color expansion, useful for accelerating text modes is supported. Plane masking is also supported.

2.0 WD90C31A ARCHITECTURE

The WD90C31A contains six major internal modules, the CRT Controller, the Sequencer, the Graphics Controller, Hardware Cursor Controller, BITBLT Controller and the Attribute Controller. The WD90C31A also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface and the Clock interface.

An internal four-level write buffer is used to achieve fast memory write. A zero wait state may be achieved with a 32-bit video memory interface for most memory write operations.

An internal FIFO is used to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates a horizontal sync (HSYNC), vertical sync (VSYNC) and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the display memory cycles. It provides the character clock in the alphanumeric mode and the dot clock in the graphics mode. The sequencer arbitrates between video display refresh, memory refresh and CPU access of the video memory. The sequencer also provides write buffer control.

The Graphics Controller manipulates the data flow between the CPU and the video memory for both CPU write and CPU read cycles.

The Attribute Controller serializes the video memory data into video data stream according to different display formats. It controls blinking, underlining, cursor, pixel panning, reverse video and background or foreground color in all display modes.

The Hardware Cursor Controller reads in each line of the cursor pattern during the horizontal retrace immediately preceding the scan line on which that line of the cursor pattern is to be displayed. It then merges the cursor pattern into the video stream for the scan line.

The BITBLT Controller generates addresses and data for BITBLT operations, including pattern, rectangle and system-to-display memory operation.

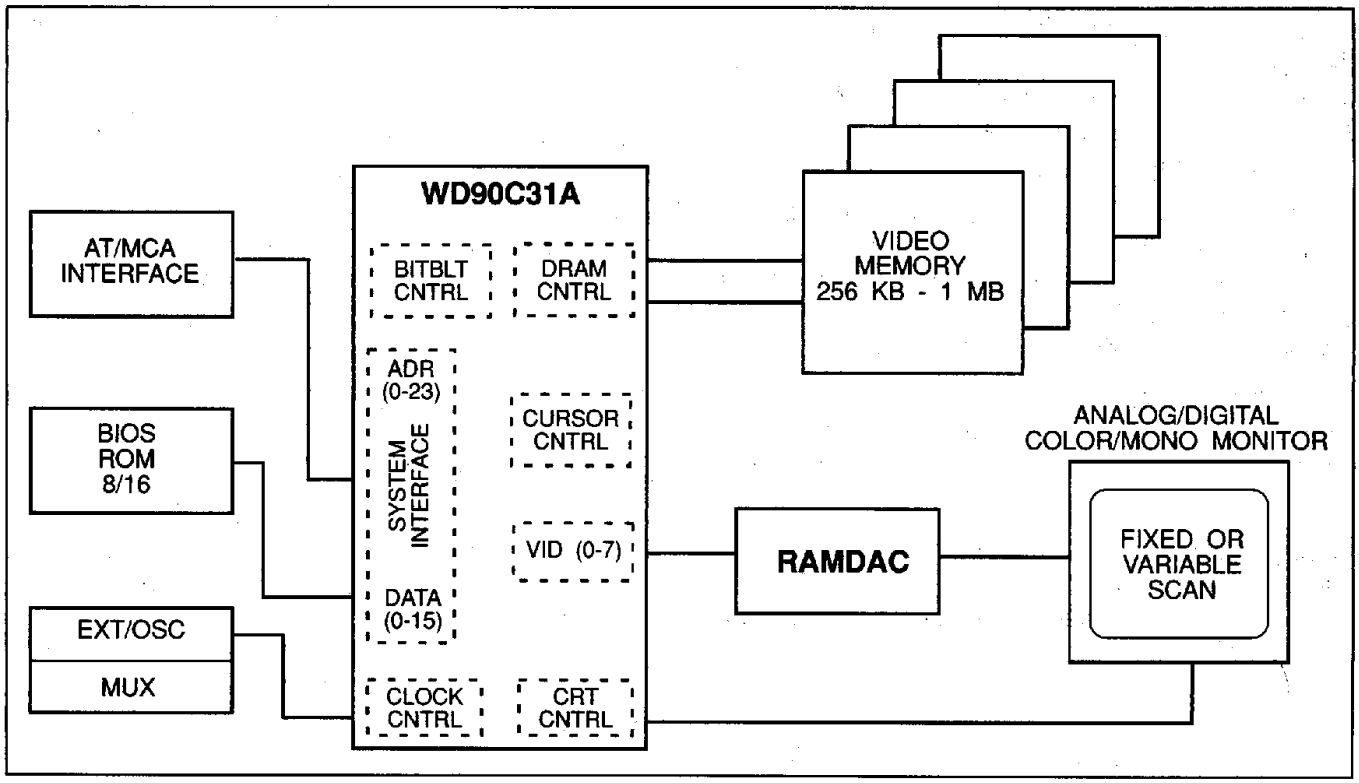

FIGURE 2-1. SYSTEM BLOCK DIAGRAM

3.0 WD90C31A INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C31A is designed to operate in both the AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of the Configuration Register bit CNF(2), which is determined upon power-up/reset and is described in Section 9, WD90C31A Configuration Register Bits CNF(18:0).

Whether configured for AT or Micro Channel operation, the WD90C31A operates functionally in a manner conducive to AT or Micro Channel interfacing. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C31A provides all the signals and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus in 8-bit or 16-bit data path modes. WD90C31A also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, it is possible to implement designs which operate in 8-bit or 16-bit mode and control an 8-bit or 16-bit BIOS ROM.

The I/O data path can be programmed to be either 16-bit or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C31A to indicate a 16-bit operation.

The WD90C31A has a display memory write buffer which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C31A provides the necessary wait states for CPU accesses to the video memory if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT (or 03C3H for Micro Channel) for setup and 102H for VGA enable, have been implemented internally in the WD90C31A.

3.2 DRAM INTERFACE

The WD90C31A has a very flexible DRAM interface. It can work with two, four, or eight 64K by 16 DRAMs with a 32-bit memory interface. It can also work with four 256 Kbyte by 4 DRAMs and one 256 Kbyte by 16 DRAM with a 16-bit memory interface. Other possible configurations are eight 256 Kbyte by 4 DRAMS or two 256 Kbyte by 16 DRAMS with a 32-bit memory interface. In all cases the WD90C31A uses the DRAM fast page mode to optimize performance.

The WD90C31A can support all standard IBM VGA modes with only two 64K by 16 DRAMs. Because it uses a 32-bit memory interface and has internal write buffer, the WD90C31A can update the video memory without inserting wait states to the AT bus for most standard IBM VGA modes.

When additional DRAMs are installed the WD90C31A is capable of supporting high resolution color video modes (1024 by 768 with 256 colors, non-interlaced at 72 Hz vertical refresh rate).

The WD90C31A is designed to support 60 ns, 70 ns, 80 ns and 100 ns DRAMs with the dedicated MCLOCK which can operate from 32 MHz to 50 MHz maximum.

The WD90C31A generates fast page DRAM timing for all BITBLT, cursor and CPU accesses, graphics display and text display. A choice of page mode and non-page mode operation is provided to access fonts in text modes.

The WD90C31A also generates CAS before RAS DRAM refresh for the display memory.

3.3 VIDEO INTERFACE

The WD90C31A is optimized to connect to an analog CRT monitor through a RAMDAC but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C31A provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C31A can be programmed to directly generate all the CRT signals for up to eight bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C31A. The WD90C31A also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C31A has four clock input signals, Memory Clock, MCLK, which drives the DRAM and bus interface timing, and the three Video Clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCLK1 and VCLK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. MCLK can also be selected as a memory clock or video clock.

3.5 WD90C31A POWER-UP CONFIGURATION

The WD90C31A uses the memory data pins to configure an internal configuration register upon power-up-reset. CNF(2) determines whether the WD90C31A will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C31A at power-up-reset are used as status bits or for clock source control. For more information on WD90C31A power-up configuration, refer to Section 9, Configuration Bits.

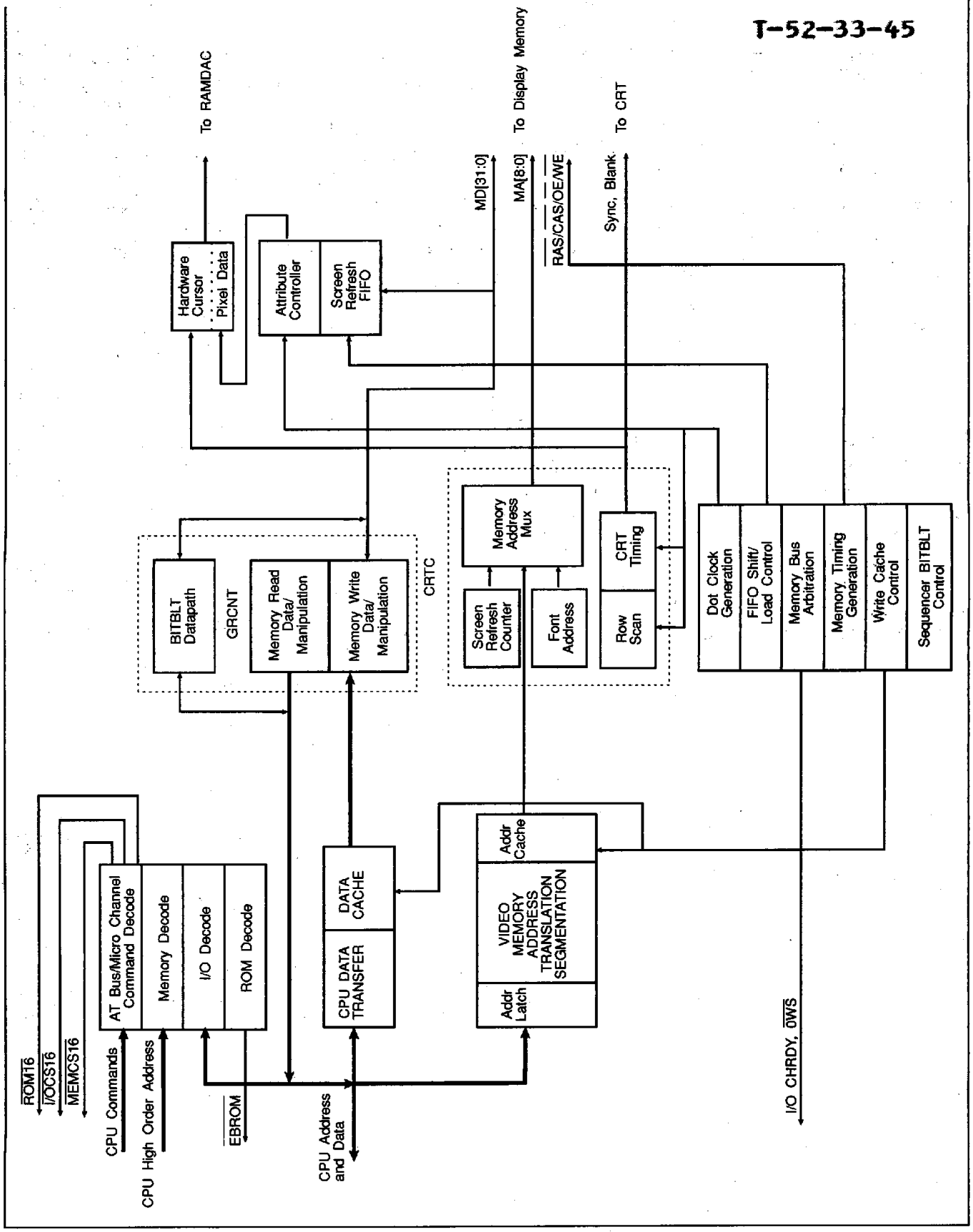

FIGURE 3-1. WD90C31A BLOCK DIAGRAM

4.0 SIGNAL DESCRIPTION

Table 4-1 provides a list of pin assignments for the 132-pin PQFP package. Table 4-2 provides a list of pin assignments for the 144-pin MQFP package. Table 4-3 provides a description of the signals controlled by the WD90C31A, and both the PQFP and MQFP pins are identified. The WD90C31A mnemonics are used.

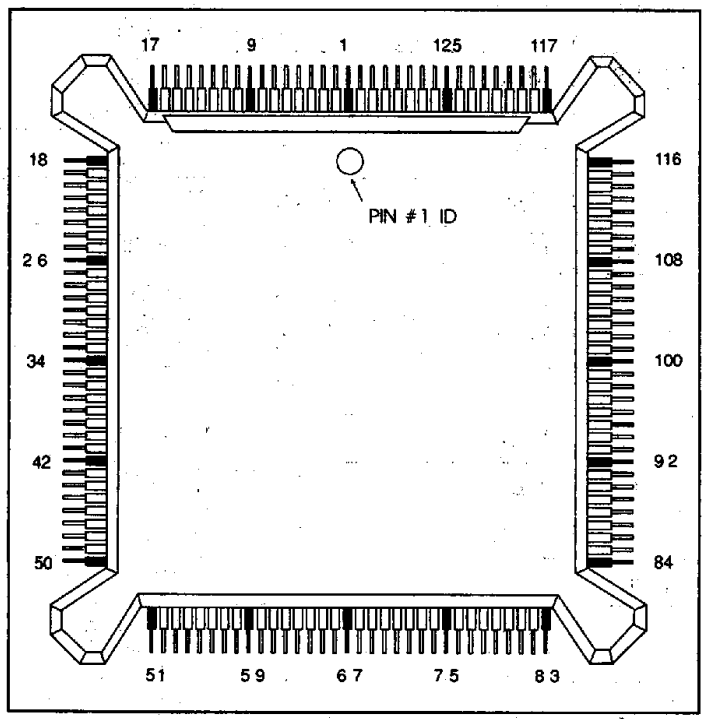

FIGURE 4-1. 132-PIN PQFP PACKAGE

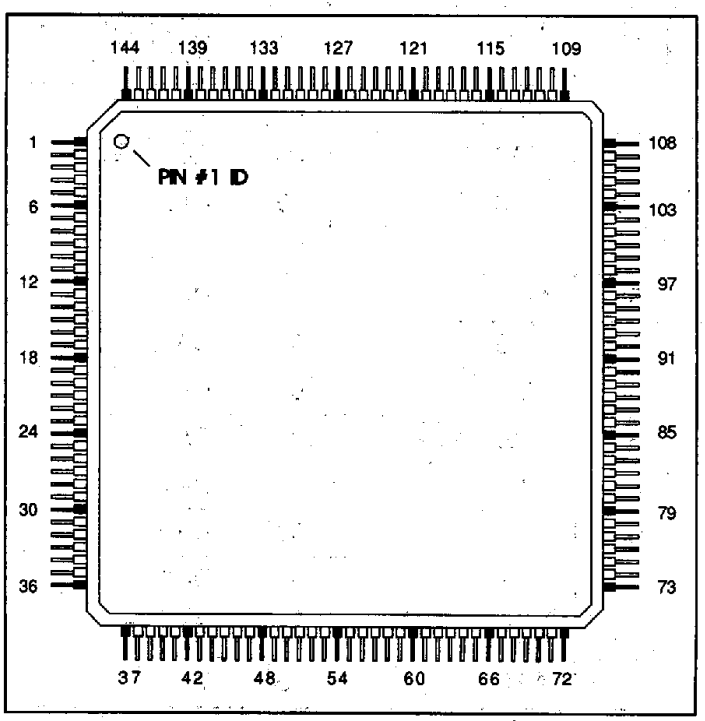

FIGURE 4-2. 144-PIN MQFP PACKAGE

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	MDET	34	MD12	67	VSS	100	DIR
2	USR1	35	MD11	68	A22	101	DA7
3	USR0	36	MD10	69	A23	102	DA6
4	MCLK	37	MD9	70	$\overline{\text{IOCS16}}$ (CDSETUP)	103	DA5
5	VSS	38	MD8	71	$\overline{\text{MEMCS16}}$ (CDDS16)	104	DA4
6	$\overline{\text{OE}}$	39	$\overline{\text{RAS}}$	72	$\overline{\text{BHE}}$	105	DA3
7	$\overline{\text{WE3}}$	40	VSS	73	ALE	106	DA2
8	MD31	41	$\overline{\text{CAS}}$	74	IRQ($\overline{\text{IRQ}}$)	107	DA1
9	MD30	42	MD7	75	EMEM	108	DA0
10	MD29	43	MD6	76	$\overline{\text{IOR}}$($\overline{\text{S1}}$)	109	$\overline{\text{EDBUFL}}$
11	MD28	44	MD5	77	$\overline{\text{IOW}}$($\overline{\text{CMD}}$)	110	VSYNC
12	MD27	45	MD4	78	$\overline{\text{MRD}}$(M/$\overline{\text{IO}}$)	111	HSYNC
13	MD26	46	MD3	79	$\overline{\text{MWR}}$($\overline{\text{S0}}$)	112	$\overline{\text{BLANK}}$
14	MD25	47	MD2	80	RESET	113	$\overline{\text{HTL}}$
15	MD24	48	MD1	81	$\overline{\text{0WS}}$	114	$\overline{\text{WPLT}}$
16	$\overline{\text{WE2}}$	49	MD0	82	IOCHRDY	115	$\overline{\text{RPLT}}$
17	VSS	50	VCC	83	VSS	116	VCC
18	VCC	51	VSS	84	VCC	117	VSS
19	MD23	52	$\overline{\text{WE0}}$	85	$\overline{\text{EIO}}$(3C3B0)	118	PCLK
20	MD22	53	MA0	86	$\overline{\text{ROM16}}$($\overline{\text{CSFB}}$) $\overline{\text{EXBLANK}}$	119	VID0
21	MD21	54	MA1	87	$\overline{\text{EBROM}}$	120	VID1
22	MD20	55	MA2	88	$\overline{\text{EDBUFH}}$	121	VID2
23	MD19	56	MA3	89	A16	122	VID3
24	MD18	57	MA4	90	DA15	123	VID4
25	MD17	58	MA5	91	DA14	124	VID5
26	MD16	59	MA6	92	DA13	125	VID6
27	$\overline{\text{RAS4}}$	60	MA7	93	DA12	126	VID7
28	$\overline{\text{RAS3}}$	61	MA8/$\overline{\text{RAS2}}$	94	DA11	127	VSS
29	VSS	62	A17	95	DA10	128	VCLK0
30	$\overline{\text{WE1}}$	63	A18	96	DA9	129	VCLK1
31	MD15	64	A19	97	DA8	130	VCLK2
32	MD14	65	A20	98	$\overline{\text{EABUF}}$	131	$\overline{\text{EXPCLK}}$
33	MD13	66	A21	99	VSS	132	$\overline{\text{EXVID}}$

TABLE 4-1. WD90C31A 132-PIN PQFP ASSIGNMENTS

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	N.C.	37	N.C.	73	N.C.	109	N.C.
2	VCC	38	VSS	74	VCC	110	VSS
3	MD23	39	WE0	75	EIO(3C3B0)	111	PCLK
4	MD22	40	MA0	76	ROM16(CSFB) EXBLANK	112	VID0
5	MD21	41	MA1	77	EBROM	113	VID1
6	MD20	42	MA2	78	EDBUFH	114	VID2
7	MD19	43	MA3	79	A16	115	VID3
8	MD18	44	MA4	80	DA15	116	VID4
9	MD17	45	MA5	81	DA14	117	VID5
10	MD16	46	MA6	82	DA13	118	VID6
11	RAS4	47	MA7	83	DA12	119	VID7
12	RAS3	48	MA8/RAS2	84	DA11	120	VSS
13	VSS	49	A17	85	DA10	121	VCLK0
14	WE1	50	A18	86	DA9	122	VCLK1
15	MD15	51	A19	87	DA8	123	VCLK2
16	MD14	52	A20	88	EABUF	124	EXPCLK
17	MD13	53	A21	89	VSS	125	EXVID
18	N.C.	54	N.C.	90	N.C.	126	N.C.
19	MD12	55	VSS	91	DIR	127	MDET
20	MD11	56	A22	92	DA7	128	USR1
21	MD10	57	A23	93	DA6	129	USR0
22	MD9	58	IOCS16 (CDSETUP)	94	DA5	130	MCLK
23	MD8	59	MEMCS16 (CDDS16)	95	DA4	131	VSS
24	RAS	60	BHE	96	DA3	132	OE
25	VSS	61	ALE	97	DA2	133	WE3
26	CAS	62	IRQ	98	DA1	134	MD31
27	MD7	63	EMEM	99	DA0	135	MD30
28	MD6	64	IOR(S1)	100	EDBUFL	136	MD29
29	MD5	65	IOW(CMD)	101	VSYNC	137	MD28
30	MD4	66	MRD(M/IO)	102	HSYNC	138	MD27
31	MD3	67	MWR(S0)	103	BLANK	139	MD26
32	MD2	68	RESET	104	HTL	140	MD25
33	MD1	69	OWS	105	WPLT	141	MD24
34	MD0	70	IOCHRDY	106	RPLT	142	WE2
35	VCC	71	VSS	107	VCC	143	VSS
36	N.C.	72	N.C.	108	N.C.	144	N.C.

TABLE 4-2. WD90C31A 144-PIN MQFP ASSIGNMENTS

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION T-52-33-45
			POWER ON
80 - 68	RESET	I	**RESET** This signal resets the WD90C31A. To initialize the WD90C31A during reset, MCLK and VCLK0 must be connected to the WD90C31A. Western Digital configuration bits are initialized at power-up reset, based on the logic level on the MD(15:0) bus, as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
			CLOCK SELECTION
4 - 130	MCLK	I	**MEMORY CLOCK** This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
128 - 121	VCLK0	I	**VIDEO CLOCK 0** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. VCLK0 is selected as clock when VCLK1 and VCLK2 are used as inputs and both Miscellaneous Output Register bits 2 and 3 set to 0.
129 - 122	VCLK1	I/O	**VIDEO CLOCK 1** VCLK1 can be a second video display clock input or an output to an external clock selection module. The direction is determined at Reset by a pull-up/down resistor on MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. As an output, VCLK1 is an active low pulse during I/O writes to port 3C2H, or reflects the contents of 03C2H, Miscellaneous Register Bit 2. Refer to the Configuration Register and PR15 Register, Bit 5 description.
130 - 123	VCLK2	I/O	**VIDEO CLOCK 2** VCLK2 is a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. VCLK2 performs as a user-defined external clock input, an output reflecting the state of Bit PR2(1) or represents the state of 03C2H, Miscellaneous Register, Bit 3, when CNF(3) is set to 1. See the Configuration Register and PR15 Register, Bit 5 description.

TABLE 4-3. SIGNAL DESCRIPTION

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE
69 - 57 68 - 56 66 - 53 65 - 52 64 - 51 63 - 50 62 - 49	A23 A22 A21 A20 A19 A18 A17	I I I I I I I	**ADDRESS BUS (A23 - A17)** In Micro Channel mode, A(23:17) should be connected to address bus SA(23:17). In AT mode, A(23:17) should be connected to LA(23:17) of the AT address bus.
89 - 79	A16	I	**ADDRESS BUS (A16)** Bit SA16 of CPU address bus.
73 - 61	ALE	I	**ADDRESS LATCH ENABLE** In AT mode, A(23:17) are latched internally at the falling edge of the ALE. In Micro Channel mode, ALE is not used and should be connected to VSS.
90 - 80 91 - 81 92 - 82 93 - 83 94 - 84 95 - 85 96 - 86 97 - 87 101 - 92 102 - 93 103 - 94 104 - 95 105 - 96 106 - 97 107 - 98 108 - 99	DA15 DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**DATA/ADDRESS BUS** This is the multiplexed CPU data and address bus. $\overline{\text{EABUF}}$ = 0: Enables the external address buffer. $\overline{\text{EDBUFL}}$ = 0 or $\overline{\text{EDBUFH}}$ = 0: Enables the external bidirectional data buffers. DIR controls the data flow for the data buffer.
82 - 70	IOCHRDY	O	**IO CHANNEL READY** When low, IOCHRDY indicates to the system processor that the Video Controller is not able to immediately complete the requested memory or I/O access, and causes the system processor to wait until IOCHRDY is de-asserted, indicating completion of the transfer. This signal is not generated on I/O cycles and accesses to the BIOS ROM.

TABLE 4-3. SIGNAL DESCRIPTION (Continued)

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
74 - 62	IRQ/(IRQ)	O	**INTERRUPT REQUEST** This programmable processor interrupt request is enabled via Bit 5 in the Vertical Retrace End register. When the end of Vertical Display occurs, this signal is active, causing the interrupt. It stays active until cleared by CRTC11 Bit 4. An AT system uses IRQ as an active high signal. Although an AT system does not usually use IRQ it may be connected if desired. The Micro Channel mode uses $\overline{IRQ}$ as an active low to generate interrupts.
71 - 59	$\overline{MEMCS16}$/ ($\overline{CDDS16}$)	O	**MEMORY CHIP SELECT 16 BITS** In AT mode, $\overline{MEMCS16}$ is used to inform the host that the WD90C31A is capable of performing the requested 16-bit video memory data transfer. In Micro Channel mode, $\overline{CDDS16}$ is used to indicate 16-bit video memory or I/O access.
85 - 75	$\overline{EIO}$/ (3C3B0)	I	**ENABLE I/O** In AT mode, $\overline{EIO}$ is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, $\overline{EIO}$ is enabled by I/O port 3C3 bit 0 = 1, and is used to enable video subsystem memory and I/O address decoding.
87 - 77	$\overline{EBROM}$	O	**ENABLE BIOS ROM** This is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A write to WD90C31A internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
113 - 104	$\overline{HTL}$	O	**ENABLE HIGH-TO-LOW** (for 16-bit BIOS) If only an eight-bit CPU interface is used, this output enables a data buffer to allow reading of the upper byte of ROM data on the lower data bus when two ROMs (16-bit) are supported.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Signals enclosed in parentheses are Micro Channel only.

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
75 - 63	EMEM	I	**ENABLE MEMORY** When asserted, EMEM enables memory decoding. It is normally connected to the Refresh signal.
72 - 60	$\overline{BHE}$	I	**BYTE HIGH ENABLE:** $\overline{BHE}$ should be connected to $\overline{BHE}$ of the AT or Micro Channel bus. $\overline{BHE}$, SA0 = 00 - Word transfer = 01 - High byte transfer = 10 - Low byte transfer = 11 - Illegal
81 - 69	$\overline{0WS}$	O	**ZERO WAIT STATE** $\overline{0WS}$ is asserted to generate a zero wait state to the AT bus. $\overline{0WS}$ is controlled by the PR33 register, bits 7 and 6. See section 7.25 for programming.
78 - 66	$\overline{MRD}$/(M/$\overline{IO}$)	I	**MEMORY READ** In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
79 - 67	$\overline{MWR}$/($\overline{S0}$)	I	**MEMORY WRITE** In AT mode $\overline{MWR}$ is the memory write strobe. In Micro Channel mode, $\overline{S0}$ is the channel status signal and indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$ and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
76 - 64	$\overline{IOR}$/($\overline{S1}$)	I	**I/O READ** In AT mode $\overline{IOR}$ is the I/O read strobe. In Micro Channel mode, $\overline{S1}$ is the channel status signal that indicates the start and type of a channel cycle.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Signals enclosed in parentheses are Micro Channel only.

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
77 - 65	$\overline{IOW}$/($\overline{CMD}$)	I	**I/O WRITE** In AT mode, $\overline{IOW}$ strobe signals an I/O write. In Micro Channel mode $\overline{CMD}$ is the bus data strobe. Address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
70 - 58	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	**I/O CHIP SELECT 16 BITS** In AT mode, $\overline{IOCS16}$ is an output, and is used to inform the host that the WD90C31A is capable of performing the requested 16-bit I/O accesses. In Micro Channel mode, this signal is an input driven by the host to individually select channel connector slots during system configuration.
100 - 91	DIR	O	**DIRECTION CONTROL** DIR is the Direction Control for external bus buffers in both AT and Micro Channel implementation. The default state is low until a read cycle occurs. The WD90C31A then drives DIR high to change the direction of the data buffers.
88 - 78	$\overline{EDBUFH}$	O	**ENABLE DATA BUFFER HIGH** $\overline{EDBUFH}$ may be used to enable an external data buffer for data bits D15 through D8.
109 - 100	$\overline{EDBUFL}$	O	**ENABLE DATA BUFFER LOW** $\overline{EDBUFL}$ may be used to enable an external data buffer for data bits D7 through D0.
98 - 88	$\overline{EABUF}$	O	**ENABLE ADDRESS BUFFER** $\overline{EABUF}$ may be used to enable an external address buffer.

TABLE 4-3. SIGNAL DESCRIPTION (Continued)

NOTE:
( ) Signals enclosed in parentheses are Micro Channel only.

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
86 - 76	ROM16/ (CSFB)/ EXBLANK	I/O	**BIOS ROM SELECT 16 BITS** In AT Mode, ROM16 is an output and decodes the ROM address LA(23:17) for space 0C0000 - 0DFFFF. It may be combined with SA16 and SA15 externally to control MEMCS16 for the address space C0000 - C7FFF. If CNF(17) is set to 0 at power up reset, the ROM16 address decoding is disabled. ROM16 then reflects the status of PR1 bit 1. **CARD SELECT FEEDBACK** In Micro Channel mode, CSFB is an output and is used as Card Selected Feedback to provide positive acknowledgement of its presence at the specified host's addresses. **EXTERNAL BLANK** In AT or Micro Channel Mode, EXBLANK becomes an input If CNF(18) is set to zero (MD18 = 0 at power-up reset). EXBLANK = 1: Enables BLANK, VSYNC and HSYNC outputs. EXBLANK = 0: Tristate BLANK, VSYNC and HSYNC outputs.
			DISPLAY MEMORY INTERFACE
41 - 26	CAS	O	**COLUMN ADDRESS STROBE** CAS is the Column Address Strobe for two, four and eight DRAM configurations.
39 - 24	RAS	O	**ROW ADDRESS STROBE** RAS is the Row Address Strobe for the 256K by 4, or 256K by 16 DRAM interface. If 64K by 16 DRAMS are used, RAS is the strobe for the first 256 Kbyte memory bank. *For RAS2 see pin 61 in Video Memory Address section.*
28 - 12	RAS3	O	**ROW ADDRESS STROBE 3** RAS3 is used only if eight 64K by 16 DRAMs are used. It controls the third 256 Kbyte memory bank.
27 - 11	RAS4	O	**ROW ADDRESS STROBE 4** RAS4 is used only if eight 64K by 16 DRAMs are used. It controls the fourth 256 Kbyte memory bank.
6 - 132	OE	O	**OUTPUT ENABLE** OE is the Output Enable signal for two, four and eight DRAM configurations.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			DISPLAY MEMORY INTERFACE (Cont.)
52 - 39	$\overline{WE0}$	O	**WRITE ENABLE** $\overline{WE0}$ is the write enable signal for MD7 through MD0.
30 - 14	$\overline{WE1}$	O	**WRITE ENABLE** $\overline{WE1}$ is the write enable signal for MD15 through MD8.
16 - 142	$\overline{WE2}$	O	**WRITE ENABLE** $\overline{WE2}$ is the write enable signal for MD23 through MD16.
7 - 133	$\overline{WE3}$	O	**WRITE ENABLE** $\overline{WE3}$ is the write enable signal for MD31 through MD24.
			PROGRAMMABLE OUTPUTS
3 - 129	USR0	O	May be used to control special card or system features (see PR32 register).
2 - 128	USR1	O	May be used to control special card or system features (see PR32 register).

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			VIDEO MEMORY DATA
8 - 134	MD31	I/O	**DISPLAY MEMORY DATA (MD31 through MD0)**
9 - 135	MD30	I/O	These lines are the data bus to the video display
10 - 136	MD29	I/O	DRAMS. The MD(18:0) data lines are pulled up by inter-
11 - 137	MD28	I/O	nal 50 Kohm resistors, but may be pulled down by exter-
12 - 138	MD27	I/O	nal 4.7 Kohm resistors to provide setup information on
13 - 139	MD26	I/O	power-up reset as follows:
14 - 140	MD25	I/O	
15 - 141	MD24	I/O	**MD** **POWER-UP FUNCTION** **REGISTER (BIT)**
19 - 3	MD23	I/O	18 Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ CNF(18) +
20 - 4	MD22	I/O	16 64K by 16 or 256K by 4 DRAM Select CNF(16) +
21 - 5	MD21	I/O	15 EGA SW4/General Purpose PR11(7) +
22 - 6	MD20	I/O	14 EGA SW3/General Purpose PR11(6) +
23 - 7	MD19	I/O	13 EGA SW2/General Purpose PR11(5) +
24 - 8	MD18	I/O	12 EGA SW1/General Purpose PR11(4) +
25 - 9	MD17	I/O	11 ANALOG/TTL Display CNF(8) *
26 - 10	MD16	I/O	10 Set 16-bit ROM CNF(10) *
31 - 15	MD15	I/O	9 3C3H or 46E8H I/O port for wake up CNF(9) +
32 - 16	MD14	I/O	8 Reserved CNF(11) +
33 - 17	MD13	I/O	7 General Purpose CNF(7) *
34 - 19	MD12	I/O	6 General Purpose CNF(6) *
35 - 20	MD11	I/O	5 General Purpose CNF(5) *
36 - 21	MD10	I/O	4 General Purpose CNF(4) *
37 - 22	MD9	I/O	3 VCLK1,2 I/O CNF(3) +
38 - 23	MD8	I/O	2 AT/Micro Channel Mode CNF(2) +
42 - 27	MD7	I/O	1 1 or 2 ROMs CNF(1) *
43 - 28	MD6	I/O	0 BIOS ROM Mapping PR1(0) *
44 - 29	MD5	I/O	
45 - 30	MD4	I/O	NOTES:
46 - 31	MD3	I/O	"*" Pulldown resistor sets these bits to logic 1.
47 - 32	MD2	I/O	"+" Pulldown resistor sets these bits to logic 0.
48 - 33	MD1	I/O	For more details refer to PR and Configuration Registers.
49 - 34	MD0	I/O	

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

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PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			VIDEO MEMORY ADDRESS
61 - 48	MA8/$\overline{RAS2}$	O	**MEMORY ADDRESS (MA8 through MA0)**
60 - 47	MA7	O	Display memory DRAM address. For testing purposes,
59 - 46	MA6	O	these pins can be tristated by setting Register PR4(4)=1.
58 - 45	MA5	O	MA8/$\overline{RAS2}$ is an active low RAS strobe for the second
57 - 44	MA4	O	256 Kbyte memory bank if four 64K by 16 DRAMs are
56 - 43	MA3	O	used.
55 - 42	MA2	O	
54 - 41	MA1	O	
53 - 40	MA0	O	
			RAMDAC INTERFACE
126 - 119	VID7	O	**VIDEO (VD7 through VD0)**
125 - 118	VID6	O	Pixel video data output to DAC and to Feature Connector.
124 - 117	VID5	O	These lines can drive up to a 8 mA load.
123 - 116	VID4	O	
122 - 115	VID3	O	
121 - 114	VID2	O	
120 - 113	VID1	O	
119 - 112	VID0	O	
115 - 106	$\overline{RPLT}$	O	**READ PALETTE** Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H and 3C9H.
114 - 105	$\overline{WPLT}$	O	**WRITE PALETTE** Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H through 3C9H.
118 - 111	PCLK	O	**PIXEL CLOCK** Video pixel clock output used by the DAC to latch video signals VID7 through VID0. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output Register.
			CRT CONTROL
112 - 103	$\overline{BLANK}$	O	**BLANK** Active low display monitor blank pulse to external RAMDAC.
111 - 102	HSYNC/ $\overline{HSYNC}$	O	**HORIZONTAL SYNC** Display monitor horizontal synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER PQFP - MQFP	MNEMONIC	I/O	DESCRIPTION
			CRT CONTROL (Cont.)
110 - 101	VSYNC/ $\overline{\text{VSYNC}}$	O	**VERTICAL SYNC** Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
1 - 127	MDET	I	**MONITOR DETECT** When the RAMDAC is external, MDET is used to determine the monitor type and can be read at port 3C2H Bit 4.
			FEATURE CONNECTOR SUPPORT
132 - 125	$\overline{\text{EXVID}}$	I	**ENABLE EXTERNAL VIDEO DATA** A Feature Connector input. A low tristates the video data lines VID7:0. An internal pullup resistor is provided.
131 - 124	$\overline{\text{EXPCLK}}$	I	**ENABLE EXTERNAL PIXEL CLOCK** A Feature Connector input. A low tristates the PCLK output. An internal pullup resistor is provided.
			POWER AND GROUND
18 - 2	VCC	-----	+5VDC
50 - 35	VCC	-----	+5VDC
84 - 74	VCC	-----	+5VDC
116 - 107	VCC	-----	+5VDC
5 - 13	VSS	-----	Ground
17 - 25	VSS	-----	Ground
29 - 38	VSS	-----	Ground
40 - 55	VSS	-----	Ground
51 - 71	VSS	-----	Ground
67 - 89	VSS	-----	Ground
83 - 110	VSS	-----	Ground
99 - 120	VSS	-----	Ground
117 - 131	VSS	-----	Ground
127 - 143	VSS	-----	Ground
- 1 - 18 - 36 - 37 - 54 - 72 - 73 - 90 - 108 - 109 - 126 - 144			These pins are not connected in the 144-pin MQFP package

TABLE 4-3. SIGNAL DESCRIPTION (Continued)

5 .0 VGA/EGA REGISTERS

All the standard IBM registers incorporated inside the WD90C31A are functionally equivalent to the VGA implementation, while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA/EGA registers. For more information, refer to the additional reference literature listed in the Table Of Contents.

5.1 EGA MODE ENTRY

A brief description of the procedure for entering EGA mode of operation is provided here. The actual software implementation details are not covered in this procedure.

- Load Configuration Register Bit 8. Select logic 0 for a VGA-compatible PS/2 display or logic 1 for an EGA-compatible TTL monitor by using the appropriate pull-up or pull-down resistor on MD11. A pull-up resistor on MD11 causes CNF(8) to be latched with logic 0 for analog PS/2 compatible displays. This status information signifies the type of monitor attached to the system and is available to the BIOS or application.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 Bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on Pins MD(15:12). (A pull-up resistor causes logic 1 to be latched after power-on-reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O Port 3C2H Bit 4.
- If EGA mode is to be emulated on an IBM PS/2 analog display, follow the suggested steps listed below:

  Initialize all the registers.
  Lock CRT controller registers.
  Force clock control rate of the CRT controller.

  - Set EGA emulation mode by programming:
    PR11(3) = 1; Set EGA emulation on PS/2 type display
    PR14(6) = 1; Vertical double scan
    PR11(2) = 1; Lock clock select
    PR11(0) = 1; Lock 8/9 dot timing.
    PR14(7) = 1; Enable IRQ (optional).
  - Lock the PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    PR11(3) = 0; EGA TTL
    PR14(7) = 1; Enable IRQ
    PR15(6) = 1; Set Low Clock
    PR14(7) = 1; Enable IRQ
  - Lock PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.

For more details on the PR registers, refer to the PR registers Section 7. The EGA register summary shown in Table 5-2 highlights all the EGA mode registers.

① REGISTERS	② RW	MONO	COLOR	INDEX
GENERAL REGISTERS		*Section 5.2*		
Miscellaneous Output Register	W	3C2	3C2	
	R	3CC	3CC	
Input Status Register 0	RO	3C2	3C2	
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	W	3BA	3DA	
	R	3CA	3CA	
* Video Subsystem Enable Register.	RW	3C3	3C3	
* I/O Port 3C3H can be used to replace 46E8H [if CNF(9) = 0] for setup in AT mode. In Micro Channel mode, writes to 3C3H, Bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS		*Section 5.3*		
Sequencer Index Register	RW	3C4	3C4	
Sequencer Data Register	RW	3C5	3C5	00H:04H
CRT CONTROLLER REGISTERS		*Section 5.4*		
Index Register	RW	3B4	3D4	
CRT Controller Data Register	RW	3B5	3D5	00H:18H
GRAPHICS CONTROLLER REGISTERS		*Section 5.5*		
Index Register	RW	3CE	3CE	
Other Graphics Registers	RW	3CF	3CF	00H:08H
ATTRIBUTE CONTROLLER REGISTERS		*Section 5.6*		
Index Register	RW	3C0	3C0	
Attribute Controller Data Register	W	3C0	3C0	00H:14H
	R	3C1	3C1	
VIDEO DAC PALETTE REGISTERS ③		*Section 5.7*		
Write Address	RW	3C8	3C8	
Read Address	W	3C7	3C7	
DAC State	R	3C7	3C7	
Data	RW	3C9	3C9	
Pel Mask	RW	3C6	3C6	
WINDOWS ACCELERATOR REGISTERS		*Section 10.0, 12.0*		
Index Controller	RW	23C0/23C1	23C0/23C1	
Register Access Block Port	RW	23C2/23C3	23C2/23C3	
BITBLT I/O Port	RW	23C4/23C5	23C4/23C5	
① All Register addresses are in hexadecimal. ② RO = Read-Only, RW = Read/Write, W = Write, and R = Read. ③ PR16(0) = 1 locks these registers.				

TABLE 5-1. VGA REGISTERS SUMMARY

① REGISTERS	② RW	MONO	COLOR	INDEX
GENERAL REGISTERS *Section 5.2*				
Miscellaneous Output Register	WO	3C2	3C2	
Input Status Register 0	RO	3C2	3C2	
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	WO	3BA	3DA	
SEQUENCER REGISTERS *Section 5.3*				
Sequencer Index Register	WO	3C4	3C4	
Sequencer Data Register	RW	3C5	3C5	01H, 03H, 04H
CRT CONTROLLER REGISTERS *Section 5.4*				
Index Register	RW	3B4	3D4	
CRT Controller Data Register	RW	3B5 ③	3D5 ③	00H, 03H, 05H:07H 09H: 0BH, 10H, 11H, 14H, 16H, 17H
GRAPHICS CONTROLLER REGISTERS *Section 5.5*				
Index Register	RW	3CE	3CE	
Other Graphics Register	RW	3CF	3CF	04H, 05H
ATTRIBUTE CONTROLLER REGISTERS *Section 5.6*				
Index Register	RW	3C0	3C0	
Attribute Controller Data Register	W	3C0	3C0	00H:13H
	R	3C1	3C1	

① All Register addresses are in hexadecimal.
② RO = Read Only, WO = Write Only, and RW = Read/Write.
③ Miscellaneous Output Register bit 0 = 0, "B" in Monochrome modes
Miscellaneous Output Register bit 0 = 1, "D" in Color modes.

TABLE 5-2. EGA REGISTERS SUMMARY

5.2 GENERAL REGISTERS

REGISTER NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES

1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as follows:

   0 = B in Monochrome Modes
   1 = D in Color Modes
3. Unless specifically identified, the descriptions apply to both VGA and EGA.

5.2.1 Miscellaneous Output Register, VGA - Read Port = 3CCH, VGA/EGA - Write Port = 3C2H

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3:2	Video Clock Select
1	Enable Video RAM
0	I/O Address Select

Bit 7 - Vertical Sync Polarity Selection.

This bit is locked if PR3(7) = 1

0 = Positive vertical sync polarity.

1 = Negative vertical sync polarity.

Bit 6 - Horizontal Sync Polarity Selection.

This bit is locked if PR3(6) = 1

0 = Positive horizontal sync polarity.

1 = Negative horizontal sync polarity.

The vertical and horizontal sync polarity bits (bits 7:6) should be set to conform with the vertical size of the frame used by the monitor.

VERTICAL FRAME SIZE

00 = Reserved

01 = 400 lines/scan

10 = 350 lines/scan

11 = 480 lines/scan

Bit 5 - Odd or Even Memory Page Select.

When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.

0 = Lower page is selected.

1 = Upper page is selected.

Bit 4

Reserved.

Bits (3:2) - Video Clock Select.

These bits are locked if PR11(2) = 1 or if PR2(1) = 1 and CNF(3) = 0.

00 = Selects VCLK0 for VGA/EGA applications. For VGA, can be connected to allow 640 dots/line (25.175 MHz). For EGA, 14.318 MHz is selected.

01 = Selects VCLK1 for VGA/EGA applications if Configuration Register Bit 3 = 0. For VGA, can be connected to allow 720 dots/line (28.322 MHz). For EGA, 16.257 MHz clock is selected.

10 = Selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

11 = Reserved. Also selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

Bit 1 - VGA - System Processor Video RAM Access Enable.

0 = CPU access disabled.

1 = CPU access enabled.

- EGA - Reserved.

Bit 0 - CRT Controller I/O Address Range Selection.

Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).

1 = CRTC and status addresses for CGA mode (3DX).

5.2.2 Input Status Register 0, Read Only Port = 3C2H

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3:0	Reserved

Bit 7 - CRT Vertical Retrace Interrupt Pending or Cleared.

0 = Vertical retrace interrupt cleared.

1 = Vertical retrace interrupt pending.

Bits (6:5)

Reserved.

Bit 4 - VGA Mode - Monitor Detection.

MDET monitor status is sampled and can be read from this bit.

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0 = Monochrome.

1 = Color.

- EGA Mode - Configuration Switches SW4-SW1

The information stored in the four configuration switches in PR11 can be read at this bit if the EGA compatibility bit PR4(1) has been set to 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H as follows:

WRITE 3C2H Bit 3	WRITE 3C2H Bit 2	READ 3C2H Bit 4
0	0	PR11(7) = EGA SW4
0	1	PR11(6) = EGA SW3
1	0	PR11(5) = EGA SW2
1	1	PR11(4) = EGA SW1

These bits may be used as general purpose scratch bits.

Bits (3:0)

Reserved. In EGA mode they must be set to 1.

5.2.3 Input Status Register 1, Read Only Port = 3?AH

BIT	FUNCTION
7:6	Reserved
5:4	Diagnostic
3	Vertical Retrace
2:1	Reserved
0	Display Enable

Bits (7:6)

Reserved. In EGA mode, bit 6 must be set to 1.

Bits (5:4) - Color Plane Diagnostics.

These bits return two of the eight video outputs VID7 through VID0, as selected by Color Plane Enable Register Bits 5 and 4. See section 5.6.6.

Bit 3 - Vertical Retrace Status.

0 = Vertical frame is displayed.

1 = Vertical retrace is active.

Bits (2:1)

Reserved. In EGA mode bit 2 must be set to 1.

Bit 0 - Display Enable Status.

0 = CRT screen display in process.

1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.2.4 Feature Control Register, VGA - Read Port = 3CAH, VGA/EGA - Write Port = 3?AH

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits (7:4)

Reserved

Bit 3 - VGA - Vertical Sync Control.

0 = VSYNC output enabled.

1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

- EGA - Reserved

Bits (2:0)

Reserved

5.3 SEQUENCER REGISTERS

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PORT	INDEX	NAME
3C4H	-----	Sequencer Index
3C5H	00	Reset
3C5H	01	Clocking Mode
3C5H	02	Map Mask
3C5H	03	Character Map Select
3C5H	04	Memory Mode

NOTE

Reserved bits should be set to zero.

5.3.1 Sequencer Index Register, Read/Write Port = 3C4H - VGA/EGA

BIT	FUNCTION
7:5	Reserved
4:0	Sequencer Address/ Index Bits

Bits (7:5)

Reserved.

Bits (4:0) - Sequencer Address/Index.

The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer Register to be accessed. Sequencer extension registers are also indexed by this register.

5.3.2 Reset Register, Read/Write Port = 3C5H, Index = 00H - VGA/EGA

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits (7:2)

Reserved.

Bit 1 - Synchronous Reset. ☆

0 = Sequencer is cleared and halted synchronously.

1 = Operational mode (Bit 0 = 1).

Bit 0 - Asynchronous Reset. ☆

0 = Sequencer is cleared and halted asynchronously.

1 = Operational mode (Bit 1 = 1).

☆ Both bits 1 and 0 must be set to 1 for Operational mode.

5.3.3 Clocking Mode Register, Read/Write Port = 3C5H, Index = 01H

Bits 5:2 are locked if PR11(1) = 1. They appear unlocked during reads.

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits (7:6)

Reserved.

Bit 5 - VGA - Screen Off.

0 = Normal screen operation.

1 = Screen is turned off but SYNC signals remain active. This bit may be used to provide maximum display memory bandwidth for quick full screen updates.

- EGA - Reserved

Bit 4 - VGA - Video Serial Shift Register Loading. T-52-33-45

0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.

1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

- EGA - Reserved

Bit 3 - Dot Clock Selection.

0 = Normal dot clock selected by VCLK input frequency.

1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2 - Shift Load. Effective Only If Bit 4 = 0.

0 = Video serializers are loaded every character clock.

1 = Video serializers are loaded every other character clock.

Bit 1

Reserved. In EGA mode bit 1 must be set to 0.

Bit 0 - 8/9 Dot Clock.

Commands Sequencer to generate an eight or nine dot wide character clock.

This bit is locked if PR11(0) = 1

0 = Nine dot wide character clock.

1 = Eight dot wide character clock.

5.3.4 Map Mask Register, Read/Write Port = 3C5H, Index = 02H - VGA/EGA

BIT	FUNCTION
7:4	Reserved
3:0	Map 3:0 Enable

Bits (7:4)

Reserved.

Bits (3:0) - Enables Writing to Memory Maps 3 Through 0, Respectively.

0 = Writing to respective Memory Map disabled.

1 = Writing to respective Memory Map enabled.

5.3.5 Character Map Select Register, Read/Write Port = 3C5H, Index = 03H

Bits 5:0 are locked if PR11(1) = 1. They appear unlocked during reads.

BIT	FUNCTION
7:6	Reserved
5, 3, 2	Character Map Select A Bits 2:0
4, 1, 0	Character Map Select B Bits 2:0

If Sequencer Register 4, Bit 1 = 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. A "0" selects Character Map B. A "1" selects Character Map A. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and Bit 4 of the attribute code.

Bits (7:6)

Reserved. VGA

Bits (7:4)

Reserved. EGA

Bits 5, 3, 2 - VGA - Character Map A Select.

These bits select the location of Character Map A as shown below.

BITS 5 3 2	MAP	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte Block
0 0 1	1	3rd 8 KByte Block
0 1 0	2	5th 8 KByte Block
0 1 1	3	7th 8 KByte Block
1 0 0	4	2nd 8 KByte Block
1 0 1	5	4th 8 KByte Block
1 1 0	6	6th 8 KByte Block
1 1 1	7	8th 8 KByte Block

Bits (3:2) - EGA - Character Map A Select.

These bits select the location of Character Map A as shown below.

BITS 3 2	MAP	FONT/PLANE 2 LOCATION
0 0	0	1st 8 KByte Block
0 1	1	2nd 8 KByte Block
1 0	2	3rd 8 KByte Block
1 1	3	4th 8 KByte Block

Bits 4, 1, 0 - VGA - Character Map B Select.

These bits select the location of Character Map B as shown below.

BITS 4 1 0	MAP	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte Block
0 0 1	1	3rd 8 KByte Block
0 1 0	2	5th 8 KByte Block
0 1 1	3	7th 8 KByte Block
1 0 0	4	2nd 8 KByte Block
1 0 1	5	4th 8 KByte Block
1 1 0	6	6th 8 KByte Block
1 1 1	7	8th 8 KByte Block

Bits (1:0) - EGA - Character Map B Select.

These bits select the location of Character Map B as shown below.

BITS 1 0	MAP	FONT/PLANE 2 LOCATION
0 0	0	1st 8 KByte Block
0 1	1	2nd 8 KByte Block
1 0	2	3rd 8 KByte Block
1 1	3	4th 8 KByte Block

NOTE
Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

5.3.6 Memory Mode Register, Read/Write Port = 3C5H, Index = 04H

BIT	FUNCTION
7:4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits (7:4)
Reserved.

Bit 3 - VGA - Chains Four Maps.

0 = Processor sequentially accesses data using Map Mask Register.

1 = Directs the two lower order video Memory Address pins (MA1, MA0) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP
0	0	0
0	1	1
1	0	2
1	1	3

- EGA - Reserved

Bit 2 - VGA/EGA - Odd/Even Map Selection.

0 = Even processor addresses to access Maps 0 and 2. Odd processor addresses to access Maps 1 and 3.

1 = Sequential processor access as defined by Map Mask Register.

Bit 1 - VGA/EGA - Extended Video Memory.

0 = 64 KB of video memory.

1 = Greater than 64 KB of memory for VGA/EGA modes.

Bit 0 - VGA - Reserved.
- EGA - Alpha Mode

0 = Disables Alpha modes and enables non-Alpha modes.

1 = Alpha mode is active and character map selection is enabled.

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① PORT	INDEX	VGA/EGA REGISTER NAME	② 6845 REGISTER NAME
3?4	---	CRT Controller Address Register	CRTC Address Register
3?5	00 ④	Horizontal Total	Horizontal Total
3?5	01	Horizontal Display Enable End	Horizontal Display
3?5	02	Start Horizontal Blanking	③
3?5	03 ④	End Horizontal Blanking	③
3?5	04	Start Horizontal Retrace	③
3?5	05 ④	End Horizontal Retrace	③
3?5	06 ④	Vertical Total	+Vert. Display
3?5	07 ④	Overflow	③
3?5	08	Preset Row Scan	③
3?5	09 ④	Maximum Scan Line	Maximum Scan Line Address
3?5	0A ④	Block Cursor Start	Cursor Start
3?5	0B ④	Block Cursor End	Cursor End
3?5	0C	Start Address High	Start Address High
3?5	0D	Start Address Low	Start Address Low
3?5	0E	Block Cursor Location High	Cursor Location High
3?5	0F	Block Cursor Location Low	Cursor Location Low
3?5	10 ④	Vertical Retrace Start	Light Pen High Read
3?5	11 ④	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	③
3?5	13	Offset	③
3?5	14 ④	Underline Location	③
3?5	15	Start Vertical Blank	③
3?5	16 ④	End Vertical Blank	③
3?5	17 ④	CRTC Mode Control	③
3?5	18	Line Compare	③

① ? Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

② 6845 Mode Registers are defined and explained in greater detail in the reference literature listed in the Table Of Contents.

③ This register can be programmed in VGA/EGA mode only. It is not applicable in 6845 mode.

④ The parameters differ between the VGA and EGA modes.

⑤ Reserved bits should be set to zero.

TABLE 5-3. CRT CONTROLLER REGISTERS

5.4.1 CRT Register Index, Read/Write Port = 3?4H

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bits (7:5)

Reserved.

Bits (4:0) - CRT Register Index Bits.

These bits specify the CRT Controller register to be addressed. Its value is programmed in hexadecimal.

5.4.2 Horizontal Total Register, Read/Write Port = 3?5H, Index = 00H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Horizontal Total Period

Bits (7:0) - VGA - Count Plus Retrace Less Five.

- EGA - Count Plus Retrace Less Two.

The total character count is the total number of characters including retrace time per horizontal scan line, less 5 in VGA mode, less 2 in EGA mode.

5.4.3 Horizontal Display Enable End Register, Read/Write Port = 3?5H, Index 01H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Displayed Characters per Scan Line

Bits (7:0) - Number Of Displayed Characters Less One.

This register contains the total number of displayed characters less one.

5.4.4 Start Horizontal Blanking Register, Read/Write Port = 3?5H, Index = 02H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches the value written in this register.

5.4.5 End Horizontal Blanking, Read/Write Port = 3?5H, Index = 03H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

Bit 7

Reserved

Bits (6:5) - Display Enable Signal Skew Control.

These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

SKEW

00 = 0, Character Clock Skews

01 = 1, Character Clock Skews

10 = 2, Character Clock Skews

11 = 3, Character Clock Skews

Bits (4:0) - End Horizontal Blanking.

VGA Mode

These five bits, along with bit 7 of the End Horizontal Retrace Register (Index 05H), determine when horizontal blanking is to end. Bits 4:0 are the least significant bits, bit 7 is the most significant bit.

When the least significant six bits of the Horizontal Character Counter matches these six bits, the horizontal blanking ends.

EGA Mode

These five bits, determine when horizontal blanking is to end. When the least significant five bits of the Horizontal Character Counter matches these five bits, the horizontal blanking ends.

5.4.6 Start Horizontal Retrace Pulse Register, Read/Write Port = 3?5H, Index = 04H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bits (7:0) - Start Horizontal Retrace Character Count.

The character count at which the horizontal retrace output is to become active is programmed in this register as a hexadecimal value.

5.4.7 End Horizontal Retrace Register, Read/Write Port = 3?5H, Index = 05H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7	End Horizontal Blank Bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal Retrace

Bit 7 - VGA - End Horizontal Blank Bit 6.

This is the sixth bit (Bit 5) of the End Horizontal Blanking Value programmed in bits 4:0 of the End Horizontal Blanking Register at Port 3?5H, Index 03H.

- EGA - CRT Counter Memory Address

This bit defines whether the CRT counter memory address starts at an even or odd address following the horizontal retrace.

0 = Even Address

1 = Odd Address

Bits (6:5) - Horizontal Retrace Delay.

These bits define the horizontal retrace signal delay.

00 = 0, Character Clock Delay

01 = 1, Character Clock Delay

10 = 2, Character Clock Delays

11 = 3, Character Clock Delays

Bits (4:0) - End Horizontal Retrace.

The least significant five bits are programmed in this register. When the least significant bits of the Horizontal Character Counter match these five bits, the Horizontal Retrace signal is turned off.

5.4.8 Vertical Total Register, Read/Write Port = 3?5H, Index = 06H

This register is locked if register PR3(0) = 1, or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Raster Scan Line Total Less 2

Bits (7:0) - VGA - Raster Scan Line Total Less 2.

This register contains the least significant eight bits of an eleven bit count of raster scan lines for a display frame. The programmed value includes the total number of vertical scan lines, minus two. Time for vertical retrace and vertical sync are also included. Bit 10 of this count is in register PR18 at Port 3?5H, Index 3EH, Bit 0. Bits 9 and 8 of this count are loaded into the Vertical Overflow Register at Port 3?5H, Index 07H, Bit 5 and Bit 0, respectively.

In 6845 mode, total vertical display time in rows is programmed into Bit 6 through Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (Index 09H Bits 4 through 0).

- EGA - CRT Vertical Frame Time.

This register contains the least significant eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

5.4.9 Overflow Vertical Register, Read/Write Port = 3?5H, Index = 07H

BIT	FUNCTION
7, 2	Start Vertical Retrace Bits 9:8
6, 1	End Vertical Display Enable Bits 9:8
5, 0	Vertical Total Bits 9:8
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8

Bits (7:5) - EGA -

Reserved

② Bits 7, 2 - VGA

Start Vertical Retrace - Bits 9:8. (Bits 7:0 are at Index 10H.)

① Bits 6, 1 - VGA

End Vertical Display Enable - Bits 9:8. (Bits 7:0 are at Index 12H.)

② Bits 5, 0 - VGA

Vertical Total - Bits 9:8. (Bits 7:0 are at Index 06H.)

Bit 4 - VGA/EGA

Line Compare - Bit 8. (Bit 9 is at Bit 6 of index 09H, Bits 7:0 are at Index = 18H.)

② Bit 3 - VGA/EGA

Start Vertical Blank - Bit 8. (Bit 9 is at Bit 5 of index 09H, Bits 7:0 are at Index =15H.)

② Bits 2 - EGA

Start Vertical Retrace - Bit 8. (Bits 7:0 are at Index 10H.)

① Bits 1 - EGA

End Vertical Display Enable - Bit 8. (Bits 7:0 are at Index 12H.)

② Bits 0 - EGA

Vertical Total - Bit 8. (Bits 7:0 are at Index 06H.)

NOTES

① This register is locked if Register PR3(1) = 0 AND the End Vertical Retrace Register Bit 7 = 1.

② This register is locked if Register PR3(0) = 1 OR the End Vertical Retrace Register Bit 7 = 1.

5.4.10 Preset Row Scan Register, Read/Write Port = 3?5H, Index = 08H

BIT	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bits (6:5) - Byte Panning Control.

These bits allow up to three bytes to be panned in modes programmed as multiple shift modes.

OPERATION

0 0 = Normal

0 1 = 1 Byte Left Shift

1 0 = 2 Bytes Left Shift

1 1 = 3 Bytes Left Shift

Bits (4:0) - Preset Row Scan Count.

These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period until the maximum row scan count is reached. When the maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

5.4.11 Maximum Scan Line Register, Read/Write Port = 3?5H, Index = 09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4:0	Maximum Scan Line

In 6845 mode, Bits 7 through 5 are reserved,

Bits (7:5) - EGA -

Reserved

Bit 7 - VGA - 200 to 400 Line Conversion.

0 = Normal operation.

1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes to display 400 scan lines. Each line is double scanned.

Bit 6 - VGA - Line Compare.

This is Bit 9 of the Line Compare Register at Port 3?5H, Index 18H.

Bit 5 - VGA - Start Vertical Blank.

This is Bit 9 of the Start Vertical Blank Register at Port 3?5H, Index 15H. The Vertical Blank Register is locked if register PR3(0) = 1. or the Vertical Retrace End Register Bit 7 = 1.

Bits (4:0) - VGA/EGA - Maximum Scan Line.

These bits are the maximum number of scanned lines for each row of characters. The value programmed is one less than the maximum number of scanned rows per character.

In 6845 mode, the value programmed is one less than the maximum scan line count for non-interlace mode. Interlaced mode is not supported.

5.4.12 Block Cursor Start Register, Read/Write Port = 3?5H, Index = 0AH

BIT	FUNCTION
7:6	Reserved
5	Block Cursor Control
4:0	Block Cursor Start Scan Line

Bits (7:6)
Reserved.

Bit 5 - VGA - Block Cursor Control.

0 = Block Cursor on.

1 = Block Cursor off.

- EGA - Reserved

Bits (4:0) - VGA/EGA - Block Cursor Start Scan Line.

These bits specify the value of the row scan counter within the cursor's starting character box. These bits are programmed with one less than the value of the character row. If these bits are programmed with a value greater than the Block Cursor End Register at Port 3?5H, Index 0BH, no cursor is generated.

For 6845 modes, Bits 7 and 6 are reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value.

5.4.13 Block Cursor End Register, Read/Write Port = 3?5H, Index = 0BH

BIT	FUNCTION
7	Reserved
6:5	Block Cursor Skew
4:0	Block Cursor End Scan Line

In 6845 mode, Bits 7 through 5 are reserved.

Bit 7
Reserved.

Bits (6:5) - Block Cursor Skew Bits.

Moves the displayed cursor to the right by the skew value in character clocks, e.g., one character clock skew moves the cursor right by one position on the screen.

SKEW

0 0 = 0 Character Clocks

0 1 = 1 Character Clocks

1 0 = 2 Character Clocks

1 1 = 3 Character Clocks

Bits (4:0) - VGA - Block Cursor End Scanline.

These bits specify the value of the last row scan counter within the character box in which the cursor is active. If this value is less than the cursor start value, no cursor is displayed.

In 6845 mode Bits 4 through 0 contain the row value of the cursor end.

NOTE

There are three types of cursors generated, depending upon the mode, i.e, VGA, EGA or 6845 (non-VGA). The above description refers to the VGA cursor only.

- EGA - Block Cursor End Scanline.

These bits specify the Cursor End value of the last row scan address counter. The programmed value is equal to N+1 where N is the last row of the cursor to be displayed.

5.4.14 Start Address High Register, Read/Write Port = 3?5H, Index = 0CH

BIT	FUNCTION
7:0	Start Address High Byte

Bits (7:0) - Display Screen Start Address Upper Byte Bits.

These are the high order eight bits of the 16-bit video memory address, used for screen refresh. The low order 8-bit register is at Port 3?5H Index 0DH. Register PR3 Bits 4 and 3 extend this video memory start register to 18 bits.

In 6845 mode, Bits 7 and 6 are forced to 0 regardless of this register's contents. The lower order eight bits are at Port 3?5H Index 0DH.

5.4.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7:0	Start Address Low Byte

Bits (7:0) - Start Address Low Byte.

These are the low order eight bits of the 16-bit video memory address in **VGA/EGA or 6845 modes**.

5.4.16 Block Cursor Location High Register, Read/Write Port = 3?5H, Index = 0EH

BIT	FUNCTION
7:0	Block Cursor Location High Byte

Bits (7:0) - Block Cursor Address Upper Byte Bits.

In VGA mode, these are the eight high order bits of the 16-bit cursor location. For the low order eight bits, see the Block Cursor Location Low Register at Port 3?5H, Index 0FH. Register PR3 Bits 4 and 3 extend the cursor location High Register to 18 bits.

In 6845 mode, Bits 7 and 6 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

5.4.17 Block Cursor Location Low Register, Read/Write Port = 3?5H, Index = 0FH

BIT	FUNCTION
7:0	Block Cursor Location Low Byte

Bits (7:0) - Block Cursor Address Low Byte Bits.

These are the low order eight bits of the 16-bit video memory address in **VGA/EGA or 6845 mode**.

5.4.18 Vertical Retrace Start Register, Read/Write Port = 3?5H, Index = 10H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	Vertical Retrace Start (Lower eight bits)

Bits (7:0) - Vertical Retrace Start Pulse Lower Eight Bits.

In VGA mode, these are the lower eight bits of the 11-bit Vertical Retrace Start Register. Bit 10 is located in 3?5H, Index 3EH, Bit 2. Bits 9 and 8 are located in the Overflow Register at Port 3?5H, Index 07H.

In 6845 compatible mode, Bits 7 and 6 are reserved. Bits 5 through 0 are read back as the high order six bits of the Light Pen Value. The lower order eight bits of the Light Pen Value are read back at Index 11H.

In EGA compatible mode, this register is read back as the low order eight bits of the Light Pen Value.

5.4.19 Vertical Retrace End Register, Read/Write Port = 3?5H, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End.

In 6845 compatible mode, this register reads back the value of the lower eight bits of Light Pen Register.

Bit 7 - VGA - CRTC Registers Write Protect.

0 = Enables writing to CRT index registers 00H-07H.

1 = Write protects CRT Controller index registers in the range of index 00H-07H. Line Compare Bit 4 in the Overflow Register (07H) is not protected.

- EGA - Reserved

Bit 6 - VGA - DRAM Refresh/Horizontal Scan Line.

This bit selects DRAM refresh cycles per horizontal scan line.

0 = Generates three refresh cycles for each horizontal scan line for normal VGA operation.

1 = Generates five DRAM refresh cycles per horizontal scan line.

- EGA - Reserved

Bit 5 - VGA - Enable Vertical Retrace Interrupt.

0 = Enable vertical retrace interrupt.

1 = Disable vertical retrace interrupt.

- EGA - IRQ Output Buffer

0 = The IRQ output buffer control is enabled. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal.

1 = The IRQ output buffer is switched to a high impedance state.

Bit 4 - VGA - Clear Vertical Retrace Interrupt.

0 = Clears the vertical retrace interrupt by writing a 0 to (resetting) an internal flip flop.

1 = Vertical retrace interrupt. This allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

- EGA - IRQ Latch

0 = The IRQ latch is reset if bit 5 = 0.

1 = The IRQ latch is set at the end of the vertical display.

Bits (3:0) - VGA/EGA - Vertical Retrace End.

These bits specify the scan count at which vertical sync becomes inactive. When these four bits match the four low-order bits of the vertical counter, vertical sync becomes inactive.

Bits (3:0) are locked if register PR3(0) = 1.

5.4.20 Vertical Display Enable End Register, Read/Write Port = 3?5H, Index = 12H

BIT	FUNCTION
7:0	Vertical Display Enable End (Lower eight bits)

Bits (7:0) - Vertical Display Enable End Lower Eight Bits.

These bits define where the active display frame ends and are the lower eight bits of an 11-bit register. The programmed count is in scan lines minus one. Bit 10 is in Port 3?5H, Index 3EH, Bit 10. Bits 9 and 8 are in the Overflow Register at Port 3?5H, Index 07H, Bits 6 and 1, respectively.

5.4.21 Offset Register, Read/Write Port = 3?5H, Index = 13H

BIT	FUNCTION
7:0	Logical Line Screen Width

Bits (7:0) - Logical Line Screen Width.

This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address equals the Current Row Scan Start Address, plus the product of the Offset Register multiplied by either 2 in the byte mode or 4 in word mode.

5.4.22 Underline Location Register, Read/Write Port = 3?5H, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7 - VGA/EGA -

Reserved.

Bit 6 - VGA - Doubleword Mode.

0 = Display memory addressed for byte or word access.

1 = Display memory addressed for double word access. This overrides the state of Port 3?5H, Index 17H, Bit 6 (see table at section 5.4.25, Bit 6).

- EGA - Reserved

Bit 5 - VGA - Count by Four for Doubleword Access.

0 = Memory address counter clocked for byte or word access.

1 = Memory address counter is clocked at the character clock rate divided by four.

- EGA - Reserved

Bits (4:0) - VGA/EGA - Underline Location.

These bits specify the row scan counter value within a character matrix where underline is to be displayed. The value programmed should be one less than the desired scan line number.

5.4.23 Start Vertical Blank Register, Read/Write Port = 3?5H, Index =15H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	Start Vertical Blank (Lower eight bits)

Bits (7:0) - Start Vertical Blank Lower Eight Bits.

These are the lower eight bits of the 11-bit Start Vertical Blank Register. Bit 10 is in register PR18 at Port 3?5H, Index 3EH, Bit 3. Bit 9 is in the Maximum Scan Line Register at Port 3?5H, Index 09H. Bit 8 is in the Overflow Register at Port 3?5H, Index 07H.

The eleventh bit value is reduced by one from the desired scan line count where the vertical blanking signal starts.

5.4.24 End Vertical Blank Register, Read/Write Port = 3?5H, Index = 16H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	End Vertical Blank

Bits (7:0) - VGA - Vertical Blank Inactive Count.

End Vertical Blank is an eight-bit value calculated as follows:

Eight-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

Bits (7:5) - EGA -

Reserved

Bits (4:0) - EGA -

End Vertical Blank is a five-bit value calculated as follows:

Five-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

5.4.25 CRT Mode Control Register, Read/Write Port = 3?5H, Index = 17H

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select.
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7 - VGA/EGA - Hardware Reset.

0 = Horizontal and vertical retrace outputs inactive.

1 = Horizontal and vertical retrace outputs enabled.

Bit 6 - VGA/EGA - Word or Byte Mode.

The state of this bit is ignored and Doubleword mode selected when Port 3?5H, Index 14H, Bit 6 is set to 1 (see section 5.4.22 Bit 6).

0 = Word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB.

1 = Byte address mode.

CRT14H Bit 6	CRT17H Bit 6	ADDRESS Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5 - VGA/EGA - Address Wrap.

0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MA0.

1 = Select MA15 for odd/even mode when 256 Kbytes of video memory are used on the system board.

Bit 4 - VGA/EGA -

Reserved.

Bit 3 - VGA/EGA - Count by 2.

0 = Character clock increments memory address counter.

1 = Character clock divided by two increments the address counter.

Bit 2 - VGA/EGA - Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

This bit is locked if register PR3(5) = 1.

0 = Selects horizontal retrace clock rate

1 = Selects horizontal retrace clock rate divided by two.

Bit 1 - VGA/EGA - Select Row Scan Counter.

0 = Row Scan Counter Bit 1 replaces CRTC when MA14 is selected to drive an address pin.

1 = CRTC drives MA14 when MA14 is selected to drive an address pin.

Bit 0 - 6845 CRT Controller Compatibility Mode Support for CGA Operation.

0 = Row Scan Counter Bit 1 replaces CRTC when MA13 is selected to drive an address pin.

1 = CRTC drives MA13 when MA13 is selected to drive an address pin.

5.4.26 Line Compare Register, Read/Write Port = 3?5H, Index = 18H

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bits (7:0) - Line Compare Lower Eight Bits.

These are the lower eight bits of the ten-bit Scan Line Compare Register. Bit 9 is in the Maximum Scan Line Register at Port 3?5H, Index 09H. Bit 8 is in the Overflow Register at Port 3?5H, Index 07H. When the vertical counter reaches the value programmed in the Scan Line Compare Register, the internal start of the line counter is cleared.

5.5 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

TABLE 5-4. GRAPHICS CONTROLLER REGISTERS

NOTE
Reserved bits should be set to zero.

5.5.1 Graphics Index Register, Read/Write Port = 3CEH

BIT	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bits (7:4)

Reserved.

Bits (3:0) - Graphics Controller Register Index Pointer Bits.

NOTE
Some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.5.2 Set/Reset Register, Read/Write Port = 3CFH, Index = 00H

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Set/Reset Map.

When the CPU executes display memory write with Write Mode 0 (see note below) selected, and the Enable Set/Reset Register at Port 3CFH Index 01H activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight-bit fill operation.

0 = Reset.

1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE

The selection of Write Mode 0 is determined by the Graphics Mode Register (Index = 05H) Bit 1 and Bit 0.

5.5.3 Enable Set/Reset Register, Read/Write Port = 3CFH, Index = 01H

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Enable Set/Reset Register Maps 3 through 0 respectively (Index 00H).

0 = In Write Mode 0, each bit (3:0) when set to 0, disables its corresponding Set/Reset Register (Index = 00H) bit and the corresponding memory map is written with the rotated 8-bit data from the system microprocessor, as defined by the Data Rotate Register.

1 = In Write Mode 0, each bit (3:0) when set to 1, enables memory map access defined by the corresponding Set/Reset Register (Index = 00H) bit and the respective memory map is written with the Set/Reset Register value.

5.5.4 Color Compare Register, Read/Write Port = 3CFH, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Color Compare.

The Color Compare bits contain the value to which all eight bits of the corresponding memory map are compared. This comparison also occurs across all four maps and a 1 is returned for the map positions when the bits of all four maps equal the Color Compare Register. If a system read is done with Bit 3 = 0 for the Graphics Mode Register at Port 3CFH, Index 05H, data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.5.5 Data Rotate Register, Read/Write Port = 3CFH, Index = 03H

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bits (7:5)

Reserved.

Bits (4:3) - Function Select.

This is the Function Select for any of the write mode operations defined in the Graphics Mode Register at Port 3CFH, Index 05H as defined below.

00 = Video memory data unmodified.

01 = Video memory data ANDed with system data in the latches.

10 = Video memory data ORed with system data in the latches.

11 = Video memory data XORed with system data in the latches.

NOTE

"Data" refers to CPU data that has gone through data rotation. The latches contain the data from the last memory read operation.

Bits (2:0) - Rotate Count.

These bits specify the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register at Port 3CFH, Index 05H.

5.5.6 Read Map Select Register, Read/Write Port = 3CFH, Index = 04H

BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bits (7:3) - VGA/EGA

Reserved.

Bit 2 - VGA

Reserved.

Bits (2:0) - EGA - Map Select.

These bits select the memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value is defined below.

0 0 0 = Map 0 selected

0 0 1 = Map 1 selected

0 1 0 = Map 2 selected

0 1 1 = Map 3 selected

Bits (1:0) - VGA - Map Select.

These bits select the memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value is defined below.

0 0 = Map 0 selected

0 1 = Map 1 selected

1 0 = Map 2 selected

1 1 = Map 3 selected

5.5.7 Graphics Mode Register, Read/Write Port = 3CFH, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7 - VGA/EGA -

Reserved.

Bit 6 - EGA -

Reserved

Bit 6 - VGA - 256 Color Mode.

This bit is locked if PR11(1) = 1. It appears unlocked during reads.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four-bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID7, VID6) are determined by Bits 3 and 2 of the Color Select Register located at Port 3C1H/3C0H, Index 14H within the Attribute Controller.

1 = Load Video Shift Registers to support 256-color mode.

BIT 1	BIT 0	WRITE MODE
0	0	**Write Mode 0**. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is rotated right by the number of bits defined in the Data Rotate Register (with the old LSB now the new MSB).
0	1	**Write Mode 1**. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2**. Memory maps (3:0) are filled with the eight-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	**Write Mode 3.** Eight bits of the value contained in the Set/Reset Register (Index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (Index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an eight-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2. **In EGA Mode** this configuration is not valid and will default to Write Mode 1.

TABLE 5-5. WRITE MODES

Bit 5 - VGA/EGA - Shift Register.

Shift Register Load controls the way in which memory data is formatted in the four Video Shift Registers. MSB is shifted out in all cases.

This bit is locked if PR11(1) = 1. It appears unlocked during reads.

0 = Map 3 through Map 0 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4 - VGA/EGA - Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the Sequencer Memory Mode Register at Port 3CFH, Index 04H. Even system addresses access Maps 2 or 0 and odd system addresses access Maps 3 or 1.

Bit 3 - VGA/EGA - Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register at Port 3CFH, Index 04H. This setting has no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2 - VGA/EGA -

Reserved.

Bits (1:0) - VGA/EGA - Write Mode.

Table 5-5 defines the four write modes.

5.5.8 Miscellaneous Register, Read/Write Port = 3CFH, Index = 06H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits (7:4)

Reserved.

Bits (3:2) - Memory Map 1, 0.

Display memory map control into the CPU address space is shown below:

	CPU ADDRESS RANGE -	LENGTH
0 0	= A000:0H-BFFF:FH -	128KB
0 1	= A000:0H-AFFF:FH -	64KB
1 0	= B000:0H-B7FF:FH -	32KB
1 1	= B800:0H-BFFF:FH -	32KB

Bit 1 - Odd/Even Mode.

0 = CPU address Bit A0 is the memory address Bit MA0.

1 = CPU address Bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects Map 2 or 0, while A0 = 1 selects Map 3 or 1.

Bit 0 - Graphics/Alphanumeric Mode.

This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register at Port 3C1H/3C0H, Index 10H.

0 = Alphanumeric mode selected.

1 = Graphics mode selected.

5.5.9 Color Don't Care Register, Read/Write Port = 3CFH, Index = 07H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Memory Map Color Compare Operation.

0 = Disable color compare operation.

1 = Enable color compare operation.

5.5.10 Bit Mask Register, Read/Write Port = 3CFH, Index = 08H

BIT	FUNCTION
7:0	Bit Mask

Bits (7:0) - Bit Mask.

Bit Mask operation applies simultaneously to all four maps. In Write Modes 2 and 0, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.

1 = Bit position value is unmasked and can be changed in the corresponding map.

5.6 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3C0	——	Index Register
3C0	00-0F	VGA - Palette Pixel Colors EGA - Dynamic Color Selection
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

TABLE 5-6. ATTRIBUTE CONTROLLER REGISTERS

NOTES

1. The Attribute Index Register has an internal flip-flop rather than an input bit to control the selection of the Address and Data Registers. Reading the Input Status Register 1 (Port 3?AH) clears the flip-flop and selects the Address Register, which is read at address 3C1H and written at address 3C0H. Once the Address Register has been loaded with an index, the next write operation to 3C0H loads the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0H but does not toggle for reads from address 3C1H.
2. Attribute Register data is written at 3C0H and register data is read from address 3C1H.
3. Reserved bits should be set to zero.

5.6.1 Attribute Index Register, Read/Write Port = 3C0H

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BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bits (7:6)

Reserved.

Bit 5 - Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to Color Palette Registers Port 3C0H, Index 00 - 0FH.

1 = Enable internal color palette and normal video translation.

Bits (4:0) - Attribute Controller Index Register Address Bits.

5.6.2 VGA - Palette Registers, Read Port = 3C1H, Write Port = 3C0H, Index 00-0FH

These registers are locked if PR4(2) = 1.

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:6)

Reserved.

Bits (5:0) - Palette Pixel Colors.

Bits 5 through 0 control VID5 through VID0 respectively.

They are defined as follows:

0 = Current pixel color deselected.

1 = Enables the corresponding pixel color.

5.6.3 EGA - Dynamic Color Registers, Read Port = 3C1H, Write Port = 3C0H, Index 00-0FH

These registers are locked if PR4(2) = 1.

Bits (7:6)

Reserved.

Bits (5:0) - Dynamic Color Selection.

Bits 5 through 0 are defined as follows:

0 = Color deselected.

1 = Color selected.

Bit	Color	Pixel
5	Secondary Red	VID5
4	Secondary Green/Inten.	VID4
3	Secondary Blue/Mono	VID3
2	Red	VID2
1	Green	VID1
0	Blue	VID0

5.6.4 Attribute Mode Control Register, Read Port = 3C1H, Write Port = 3C0H, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bits (7:4) - EGA -

Reserved.

Bit 7 - VGA - VID5, VID4 Select.

0 = VID5 and VID4 palette register outputs are selected.

1 = Color Select Register Port 3C1H/3C0H, Index 14H, Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6 - VGA - Pixel Width.

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.

1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5 - VGA - PEL Panning Compatibility.

Line Compare in the CRT Controller.

0 = A Line compare will have no effect on the PEL Panning Register.

1 = Allows a successful line compare to disable the PEL Panning Register and Bits 6 and 5 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4 - VGA

Reserved.

Bit 3 - VGA/EGA - Background Intensity/Blink Selection.

0 = Selects background intensity from the MSB of the attribute byte.

1 = Selects blink attribute.

Bit 2 - VGA/EGA - Enable Line Graphics Character Code.

This bit should be set to zero for character fonts that do not utilize line graphics character codes.

0 = Forces the ninth dot to be the same color as the background in line graphics character codes.

1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1 - VGA/EGA - Mono/Color Emulation.

0 = Color display attributes.

1 = MDA attributes.

Bit 0 - VGA/EGA - Graphics/Alphanumeric Mode Enable.

0 = Alphanumeric mode.

1 = Graphics mode.

5.6.5 Overscan Color Register, Read Port = 3C1H, Write Port = 3C0H, Index = 11H

This register is locked if PR4(2) = 1.

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:0) - VGA - Overscan/Border Color.

These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

Bits (7:6) - EGA -

Reserved.

Bits (5:0) - EGA - Overscan/Border Color.

For a monochrome display, Bits 5:0 = 0.

For the border color, refer to Bits (5:0) in the Dynamic Color Selection in section 5.6.3.

5.6.6 Color Plane Enable Register, Read Port = 3C1H, Write Port = 3C0H, Index = 12H

BIT	FUNCTION
7:6	Reserved
5:4	Video Status Multiplexer
3:0	Color Plane Enable

Bits (7:6) - VGA/EGA -

Reserved.

Bits (5:4) - VGA - Video Status Multilexer

These bits select two out of eight color outputs which can be read by the Input Status Register 1 at Port 3?AH, Bits 5 and 4. See section 5.2.3.

COLOR PLANE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bits (5:4) - EGA - Video Status Multiplexer

These bits select two out of six color outputs which can be read by the Input Status Register 1 at Port 3?AH, Bits 5 and 4. See section 5.2.3.

COLOR PLANE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2 Red	VID0 Blue
0	1	VID5 SRed	VID4 SGreen
1	0	VID3 SBlue	VID1 Green
1	1	VID5 SRed	VID4 SGreen

Bits (3:0) - VGA/EGA - Color Plane Enable.

0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.

1 = Enables the respective display memory color plane.

5.6.7 Horizontal Pel Panning Register, Read Port = 3C1H, Write Port = 3C0H, Index = 13H

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BIT	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bits (7:4) - VGA/EGA -

Reserved.

Bits (3:0) - Horizontal Pixel Panning.

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- VGA -

Horizontal Pixel Panning is available in text or graphics modes. These bits select pixel shift to the left. For nine dots/character modes, up to eight pixels can be shifted. Likewise, for eight dots/character modes, up to seven pixels can be shifted. For 256 color, up to three position pixel shifts can occur. The following table defines the shift in different modes.

- EGA -

These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alphanumeric modes, (nine dots/character) image can be shifted by nine pixels. For all other graphics or alphanumeric modes, a maximum left shift of eight pixels is permitted.

Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

TABLE 5-7. LEFT SHIFT PIXEL VALUE

5.6.8 Color Select Register, Read Port = 3C1H, Write Port = 3COH, Index = 14H

BIT	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bits (7:4)

Reserved.

Bits (3:2) - Color Value MSB.

These are the two most significant bits of the eight-digit color value for the video DAC. They are normally used in all modes except 256 color graphics.

Bit 3 = Set color bit VID7.

Bit 2 = Set color bit VID6.

Bits (1:0) - Substituted Color Value Bits.

These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers, to create eight-bit color value. They are selected by the Attribute Controller Mode Control Register at Port 3C0H, Index 10H.

5.7 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C31A. However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C31A. Setting PR16 Bit 0 to 1 de-asserts $\overline{WPLT}$ disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the I/O ports illustrated in table 5-8 are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL Address Port (Write)	Read/Write Port
3C7H	PEL Address Port (Read)	Read Only Port
*3C7H	*DAC State (Read Only)	* If Bits 1:0 = 1, DAC is in read operation. When Bits 1:0 = 0, DAC is in write operation. Bits 7:2 are reserved.
3C6H	PEL Mask (Read/Write)	Not to be written to by application code. To do so changes the color look-up table.
3C9H	PEL Data Register (Read/Write)	Three successive read/write bytes.
* This port is internal to the WD90C31A.		

TABLE 5-8. VIDEO RAMDAC PORTS

6 .0 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting register PR2(6) = 1.
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting register PR2(7) = 1.
3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register at Port 3CCH/3C2H and is programmed as shown below:
   0 = B in Monochrome Modes
   1 = D in Color Modes.

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Register	WO	3B8	3D8	3D8	3B8
Color Select Register	WO		3D9	3D9	
Status Register	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Register	WO			3DE	
Hercules Register	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.

TABLE 6-1. COMPATIBILITY REGISTERS SUMMARY

6.1 HERCULES/MDA MODE CONTROL REGISTER, MDA OPERATION WRITE ONLY PORT = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7 - Select Display Memory Page Address in Hercules Mode.

Reserved in MDA mode.

In Hercules Graphics mode, this bit selects the Display Memory Page if Bit 1 of this register is 1 and Bit 0 in Port 3BFH is 0.

0 = Display memory page address starts at B000:0H.

1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5 - Enable Blink.

0 = Disable Blinking.

1 = Enable Blinking.

Bit 4

Reserved.

Bit 3 - Video Enable.

0 = Video Disabled.

1 = Video Activated.

Bit 2

Reserved.

Bit 1 - Port 3BFH Enabled.

0 = Prevents setting of Port 3BFH Bits 1:0, thereby forcing the alpha mode operation.

1 = Allows the Port 3BFH Bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0 - High Resolution Mode.

Should be set to "1".

0 = High resolution disabled.

1 = High resolution is enabled.

6.2 HERCULES REGISTERS

The Hercules Mode Register is a two-bit write only register located at I/O port address 3BFH. It affects the device operation only in the 6845 mode. The Enable Mode Register located at address 3B8H overrides the write port 3BFH functions defined by its Bits 1 and 0.

6.3 ENABLE MODE REGISTER PORT 3B8H

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7 - Select Display Memory Page Address in Graphics Mode.

0 = Display memory page address starts at B000:0H.

1 = Display memory page address starts at B800:0H.

Bits (6:2, 0)

Not applicable in Hercules Mode.

Bit 1 - Port 3BFH, Bit 0 Override.

0 = Prevents setting of Port 3BFH, Bit 0, thereby forcing the Alpha Mode operation.

1 = Allows the Port 3BFH, Bit 0 to switch for the Alpha or Graphics Mode selection.

6.4 HERCULES COMPATIBILITY REGISTER, WRITE ONLY PORT = 3BFH

This register is locked if PR17(1) = 1

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1 - Upper Memory Page Address.

In the graphics mode, Bit 7 of the Enable Mode Control Register at Port 3B8H selects the displayed memory page address. When that bit is reset, Bit 1 of this register prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.

0 = Upper memory page is mapped out.

1 = Upper memory page is accessible.

Bit 0 - Enable Graphics.

Bit 1 of Enable Mode Register at Port 3B8H may prevent setting this bit, thereby selecting Alpha Mode display.

0 = Alpha mode display.

1 = Graphics modes may be displayed.

6.5 COLOR CGA OPERATION REGISTER, WRITE ONLY PORT = 3D8H

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	(40 by 25) or (80 by 25) Alpha Mode

Bits (7:6)

Reserved.

Bit 5 - Enable Blink Function.

0 = Disables blinking function.

1 = For normal operation, set this bit to allow blinking.

Bit 4 - B/W Graphics Mode Enable.

0 = Deselect 640 by 200 B/W graphics mode.

1 = Enable 640 by 200 B/W graphics mode.

Bit 3 - Enable Video Signal.

0 = Deactivates video signal. This is done during mode changes.

1 = B/W mode enabled.

Bit 2 - B/W or Color Display Mode.

0 = Color mode selected.

1 = B/W mode selected.

Bit 1 - Graphics or Alpha Mode Selection.

0 = Alpha mode selected.

1 = Graphics mode (320 by 200) selected.

Bit 0 - (40 by 25) or (80 by 25) Alpha Mode Selection.

0 = 40 by 25 alpha mode selected.

1 = 80 by 25 alpha mode selected.

6.6 CGA COLOR SELECT REGISTER, WRITE ONLY PORT = 3D9H

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	High Intensity Component
2	Red Component
1	Green Component
0	Blue Component

Bits (7:6)

Reserved.

Bit 5 - 320 by 200 Color Set Select for the CGA (two bits per pixel).

0 = Background, green, red, brown colors.

1 = Background, cyan, magenta, white colors.

Bit 4 - Alternate Color Set Enable.

0 = Background color in alpha mode.

1 = Enable alternate color set in graphics mode.

Bit 3 - High Intensity Component.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.

0 = No selection.

1 = Selects intensified border color.

320 by 200 Graphics Mode.

0 = No selection.

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1 = Selects intensified background and border color.

640 by 200 Graphics Mode.

0 = No selection.

1 = Selects red foreground color.

Bit 2 - Red Component.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

0 = No component added.

1 = Red component added to border color.

320 by 200 Graphics Mode.

0 = No component added.

1 = Red component added to background and border color.

640 by 200 Graphics Mode.

0 = No component added.

1 = Red component added to foreground color.

Bit 1 - Green Component.

Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

0 = No component added.

1 = Green component added to border color.

320 by 200 Graphics Mode.

0 = No component added.

1 = Green component added to background and border color.

640 by 200 Graphics Mode.

0 = No component added.

1 = Green component added to foreground color.

Bit 0 - Blue Component.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

0 = No component added.

1 = Blue component added to border color.

320 by 200 Graphics Mode.

0 = No component added.

1 = Blue component added to background and border color.

640 by 200 Graphics Mode.

0 = No component added.

1 = Blue component added to foreground color.

6.7 CRT STATUS REGISTER, MDA OPERATION, READ ONLY PORT = 3BAH

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7 - Vertical Retrace.

0 = Indicates that the raster is in vertical retrace mode.

1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bits (6:4)

Reserved.

Bit 3 - B/W Video Status.

0 = B/W Video disabled.

1 = B/W Video enabled.

Bits (2:1)

Reserved.

Bit 0 - Display Enable.

0 = Display Enable is active.

1 = Indicates that the screen border or blanking is active, Display Enable is inactive.

6.8 CRT STATUS REGISTER, CGA OPERATION, READ ONLY PORT = 3DAH

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bits (7:4)

Reserved.

Bit 3 - Vertical Retrace.

0 = Indicates that vertical retrace is inactive.

1 = Indicates that the raster is in vertical retrace mode.

Bit 2 - Light Pen Switch Status.

0 = Light pen switch closed.

1 = Light pen switch open

Bit 1 - Light Pen Latch.

0 = Light pen latch cleared.

1 = Light pen latch set.

Bit 0 - Display Enable.

0 = Display Enable is active.

1 = Indicates that the screen border or blanking is active, Display Enable is inactive.

6.9 AT&T/M24 REGISTER, WRITE ONLY PORT = 3DEH

This is a write only, eight-bit register located at address 3DEH. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting Bit 7 in register PR2.

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5:4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bits (7, 5, 4, 1)

Reserved.

Bit 6 - White/Blue Underline.

Defines underline attribute according to the MDA display requirements.

0 = Underline attribute selects blue foreground in color text modes.

1 = Underline attribute selects white underlined foreground.

Bit 3 - Page Select.

Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.

0 = Display memory address starts at B800:0H (16 Kbyte length).

1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2 - Character Set Select.

Selects between two character font planes.

0 = Standard character font from plane 2.

1 = Alternate character font from plane 3.

Bit 0 - M24 or Non-IBM Graphics Mode, 400-line Mode.

A 400-line monitor is required for this mode.

0 = 200-line graphics mode active, using paired lines.

1 = AT&T mode enabled for 400-line graphics.

7.0 PR REGISTERS

The WD90C31A has additional features that enhance the performance and function of the earlier Western Digital Imaging video controllers and the basic VGA subsystem. To accomplish this, the WD90C31A architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES

1. The designation 3?5H means that the register is mapped into either 3B5H in monochrome mode or 3D5H in color modes.
2. PR Register notation - XXX.YY when XXX is the data port address and YY is the register index, e.g., 3CF.0F implies 0F → 3CEH (Select Index register) followed by (Data byte) → 3CFH (Data Port). Registers PR(0:4) and PR(11:1A) are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101. A register remains unlocked until another value is written to the unlocked register. Registers PR(0:5) are readable only if PR4 Bit 1 = 0. Registers PR(10:17) are read protected at power up by hardware reset. In order to read registers PR(10:17), load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR(10:17) are read protected, reading them would show data to be FFH. Setting PR4 Bit 1 to "1" does not read protect registers PR(10:17). PR(21:23) and PR(30:35) are R/W protected by PR20. PR20 must be loaded with 48H to make it possible to read or write to PR(21:23) and PR(30:35). All PR registers are set to "0" at power on reset except where noted.

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3?5.31- 3?5.3C	RW	3B5.31 - 3B5.3C	3D5.31 - 3D5.3C
PR18 CRTC Vertical Timing Overflow	RW	3B5.3E	3D5.3E
PR19 Signature Analyzer Control	RW	3B5.3F	3D5.3F
PR1A CRTC Shadow Register Control	RW	3B5.3D	3D5.3D
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad	RW	3C5.08	3C5.08
PR23 Scratch Pad	RW	3C5.09	3C5.09
PR30 Memory Interface write buffer and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12
PR33 DRAM Timing and Zero Wait State Control	RW	3C5.13	3C5.13
PR34 Video Memory Mapping	RW	3C5.14	3C5.14
PR35 Reserved	RW	3C5.15	3C5.15

NOTE:
All of the PR Registers may be read/write protected. Refer to the PR Registers description for more details.

A register description from locations such as 3CF.09 is the value read from or written to location 3CFH, after a value of 09 has been written to the corresponding Index register 3CEH.

"?" Value is controlled by Bit 0 of the Miscellaneous Output Register at Port 3CCH/3C2H and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes.

TABLE 7-1. PR REGISTERS SUMMARY

7.1 ADDRESS OFFSET REGISTERS PROA AND PROB

PROA - Address Offset Register A, Read/Write Port = 3CFH, Index = 09H

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7:0	Primary Address Offset Bits

PROB - Address Offset Register B, Read/Write Port = 3CFH, Index = 0AH

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7:0	Alternate Address Offset Bits

The WD90C31A can control up to 1 Mbyte of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA reach the memory beyond this range, the WD90C31A has two CPU address offset registers, PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PROA (Bits 7:0) or PROB (Bits 7:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture. PROA and PROB will then provide four Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a four Kbyte segment to another four Kbyte segment of the display memory.)

PROA and PROB are all set to zero at power-on-reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 0.**

  When PR1-3 = 0, PR0A is always selected as the CPU address offset register.

  When PR1-3 = 1 and the display memory is mapped into A000 - BFFFF (128 Kbytes), PR0A offset CPU address range is B0000 - BFFFF, the PR0B offset CPU address range is A0000 - AFFFF. (If CPU address bit A16 = 1, select PR0A. Otherwise PR0B is selected.)

  When PR1-3 = 1 and the display memory is mapped into A0000 - AFFFF (64 Kbytes) or B0000 - B7FFF or B800 - BFFFF (32 Kbytes), then PR0B offset CPU address range is A0000 - A7FFF or B0000 - B7FFF. PR0A offset CPU address range is A8000 - AFFFF or B8000 - BFFFF. (If CPU address bit A15 = 1, select PR0A. Otherwise PR0B is selected.)

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 1.**

  Both PR0A and PR0B are enabled. A CPU memory write selects PR0B as the offset register. Otherwise, PR0A is selected as the offset register.

7.2 PR1 - MEMORY SIZE, READ/WRITE PORT = 3CFH, INDEX = 0BH

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate Address Offset Register PR0B
2	16-Bit System Interface
1	16-bit BIOS ROM
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1(1:0) are latched internally at power on reset from the corresponding memory data bus pins MD10, MD0, using either pull-up or pull-down external resistors. Pull-up resistors on MD10, MD0 cause PR1(1:0) bits to be latched low.

Bits (7:6) - Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits, in conjunction with PR0A, PR0B, PR16(1), select the way memory is mapped into the CPU address space. IF PR16(1) is set to 1, the memory mapping will be set identical to the IBM VGA, regardless of PR1(7), PR1(6).

Tables 7-2 through 7-5 list the different settings on these two bits for different memory organizations.

PR1(7) = 0 PR1(6) = 0		256K TOTAL,		IBM VGA MEMORY ORGANIZATION		
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
PA ⑤	PA	PA	PA	PA	PA	MA(17)
0	0	0	0	0	0	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)	MA(1)
A(0)	CA(0)	A(14) or ③ XRN(5)	CA(15) or ④ CA(13)	A(14)	CA(12)	MA(0)

TABLE 7-2. IBM COMPATIBLE MEMORY ORGANIZATION

PR1(7) = 0 PR1(6) = 1 256K TOTAL, 64K/PLANE, WD90C31A MEMORY ORGANIZATION						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
PA ⑤	PA	PA	PA	PA	PA	MA(17)
0	0	0	0	0	0	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	MA(1)
A(0)	CA(0)	A(16) or ③ XRN(5)	CA(15)	A(16)	CA(14)	MA(0)

TABLE 7-3. WD90C31A MEMORY ORGANIZATION - 256 KBYTES

PR1(7) = 1 PR1(6) = 0 512K TOTAL, 128K/PLANE, WD90C31A MEMORY ORGANIZATION						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
PA ⑤	PA	PA	PA	PA	PA	MA(17)
A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	MA(1)
A(0)	CA(0)	A(16) or ③ XRN(5)	CA(15)	A(16)	CA(14)	MA(0)

TABLE 7-4. WD90C31A MEMORY ORGANIZATION - 512 KBYTES

PR1(7) = 1 PR1(6) = 1		1M TOTAL, 256K/PLANE, WD90C31A MEMORY ORGANIZATION				
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)	MA(17)
A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)	MA(13)
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)	MA(1)
A(0)	CA(0)	A(16) or ③ XRN(5)	CA(15)	A(18)	CA(16)	MA(0)

TABLE 7-5. WD90C31A MEMORY ORGANIZATION - 1 MBYTES

NOTES:

1. A(19:0) are WD90C31A internally modified system Addresses (CPU address + offset address).
2. CA(17:0) are either CRT Character Address Counter Bits or bitblit generated counter bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted Bit 5. XRN(5) can be used to replace CPU address bits in order to select memory pages in word mode. In IBM compatible memory mapping, 3C5.4, Bit 1 = 1 will select XRN(5) to replace CPU address bits. In other memory mapping schemes PR1(7,6) ≠ 00, 3C5.4, Bit 1 = 1 and PR16_2 = 1 will select XRN(5) to replace address bits.
4. CA(15) is selected as MA(0) if CRTC Mode Register 17, Bit 5 = 1 in word addressing modes.
5. PA is the memory plane select bit when DRAM interface is set for 16 bits.
   PA = 0 selects Plane 1,0
   PA = 1 selects Plane 3, 2
6. MA(17:0) are divided into $\overline{RAS}$, $\overline{CAS}$ addresses as follows:

For 256K by 4 DRAM or 256K by 16 DRAM	MA(16) - MA(8) ⇒ MA(17), MA(7) - MA(0) ⇒	$\overline{RAS}$(8) - $\overline{RAS}$(0) $\overline{CAS}$(8) - $\overline{CAS}$(0)
For 64K by 16 DRAM	MA(15) - MA(8) ⇒ MA(7) - MA(0) ⇒	$\overline{RAS}$(7) - $\overline{RAS}$(0) $\overline{CAS}$(7) - $\overline{CAS}$(0)
MA(17, 16) = 00 = 01 = 10 = 11	Select 1st 64K bank Select 2nd 64K bank Select 3rd 64K bank Select 4th 64K bank	

Bits (5:4) - PR1(5,4) Memory Map Select.

0 0 = IBM VGA mapping. CPU addresses are decoded from 0A0000H - 0BFFFFH from the lowest 1 Mbyte CPU address space (depending on 3CF.06 bits 2 and 3).

0 1 = First 256 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X3FFFFH)

1 0 = First 512 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X7FFFFH)

1 1 = In any 1Mbyte CPU address space (X00000H - XFFFFFH)

NOTE

PR34(3C5.14) Bits (3:0) control which 1 Mbyte of CPU address space the WD90C31A maps. See section 7.26.

Bit 3 - Enable Alternate Address Offset Register PROB.

Bit 2 - Enable 16 bit system interface bus.

0 = System interface is 8 bits.

1 = System interface is 16 bits.

Bit 1 - 16-bit BIOS ROM.

0 = BIOS ROM access is 8 bits.

1 = BIOS ROM access is 16 bits.

A pull-down resistor on MD10 sets this bit to 1 after power-on reset. This bit can also be set to 1 by an I/O write cycle only if the CNF(1) = 1.

Bit 0 - BIOS ROM Map Out.

0 = The BIOS ROM is available.

1 = The BIOS ROM is mapped out.

A pull-down resistor on MD0 sets this bit to 1 at power-on-reset.

7.3 PR2 - VIDEO SELECT REGISTER, READ/WRITE PORT = 3CFH, INDEX = 0CH

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This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7 - Enable AT&T/M24 Register and Mode.

0 = Disable.

1 = Enable.

Bit 6 - 6845 Compatibility.

0 = VGA or EGA mode.

1 = Non-VGA (6845) mode.

Bit 5 - Character Map Select.

Bits 5 and 2 of this register, and Bit 4 of the Attribute byte, enables character maps from Planes 2 or 3 to be selected as shown in the table below.

PR15 (2)	3DE (2)	PR2 (5)	PR2 (2)	ATT (4)	PLANE SELECT
0	0	0	X	X	2
0	0	1	0	X	3
0	0	1	1	0	2
0	0	1	1	1	3

The above functions are overridden by setting PR15(2) or 3DE(2) to 1, see section 7.12.

Bits (4:3) - Character clock period control.

0 0 = IBM VGA character clock (8 or 9 dots).

0 1 = 7 dots (used for 132-character text mode only).

1 0 = 9 dots.

1 1 = 6 dots if PR17(5) = 0
10 dots if PR17(5) = 1.

NOTE

The character clock period control functions have no effect in graphics modes (Graphics Mode always uses eight dots).

Bit 2 - Underline and character map select.

Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., programming 1 gives blue underline. It overrides the background color function of the Attribute Code Bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See the table in PR2(5) for details.

Bit 1 - Third Clock Select Line.

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) = 1. When CNF(3) = 0, it locks the internal video clock select multiplexer.

Bit 0 - Force VCLK.

This bit forces horizontal sync timing clock of the CRT Control Register to VCLK.

Uses VCLK when Sequencer Register 1, Bit 3, is set for VCLK/2. This is for compatibility modes that require locking the CRT Control Register timing parameters.

7.4 PR3 - CRT LOCK CONTROL REGISTER, READ/WRITE PORT = 3CFH, INDEX = 0DH

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7 - Lock VSYNC Polarity.

This bit locks VSYNC polarity as programmed at Port 3C2H, Bit 7.

Bit 6 - Lock HSYNC Polarity.

This bit locks HSYNC polarity as programmed at Port 3C2H, Bit 6.

Bit 5 - Lock Horizontal Timing.

This bit locks CRT Control Registers of Groups 4 and 0. It prevents applications software from unlocking Group 0 registers by setting 3?5.11 Bit 7 = 0.

Bit 4 - Bit 9 Control.

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C and Bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA(17).

Bit 3 - Bit 8 Control.

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C and Bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA(16).

Bit 2 - Cursor Control.

Cursor Start, Stop, Preset Row Scan and Maximum Scan Line Address registers value multiplied by two.

Bit 1 - Lock Prevention.

1 = Prevents attempts by applications software to lock registers of Group 1 by setting 3?5.11, Bit 7 = 1.

Bit 0 - Lock vertical timing.

1 = Locks CRTC registers of Groups 2 and 3. Overrides attempts by applications software to unlock Group 2 registers by setting 3?5.11, Bit 7 = 0.

7.4.1 CRT Controller Register locking

Register locking is controlled by four bits. They are PR3(5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register Bit 7 controlled by Index register 11). When 3?5.11 Bit 7 = 1, CRT controller registers (R0:7) are write-protected per VGA definition. For more information on the five groups and their locking schemes, refer to the following sections.

- **Group 0**

  These registers are locked if PR3(5) = 1 OR 3?5.11(7) = 1.

  3?5 index 00 - Horizontal Total Characters per scan

  3?5 index 01 - Horizontal Display Enable End

  3?5 index 02 - Start Horizontal Blanking

  3?5 index 03 - End Horizontal Blanking

  3?5 index 04 - Start Horizontal Retrace

  3?5 index 05 - End Horizontal Retrace

- **Group 1**

  These registers are locked if PR3(1) = 0 AND 3?5.11(7) = 1.

  3?5 index 07 (Bit 6) - Vertical Display Enable End Bit 9

  3?5 index 07 (Bit 1) - Vertical Display Enable End Bit 8

  3?5 index 3E (Bit 1) - Vertical Display Enable End Bit 10

- **Group 2**

  These registers are locked if PR3(0) = 1 OR 3?5.11(7) = 1.

  3?5 index 06 - Vertical Total

  3?5 index 07 (Bit 7) - Vertical Retrace Start Bit 9

  3?5 index 07 (Bit 5) - Vertical Total Bit 9

  3?5 index 07 (Bit 3) - Start Vertical Blank Bit 8

  3?5 index 07 (Bit 2) - Vertical Retrace Start Bit 8

  3?5 index 07 (Bit 0) - Vertical Total Bit 8

  3?5 index 09 (Bit 5) - Start Vertical Blank Bit 9

  3?5 index 3E (Bit 0) - Vertical Total Bit 10

  3?5 index 3E (Bit 2) - Vertical Retrace Start Bit 10

  3?5 index 3E (Bit 3) - Start Vertical Blank Bit 10

- **Group 3**

  These registers are locked if PR3(0) = 1.

  3?5 index 10 - Vertical Retrace Start

  3?5 index 11 [Bits(3:0)] - Vertical Retrace End

  3?5 index 15 - Start Vertical Blanking

  3?5 index 16 - End Vertical Blanking

- **Group 4**

  This register is locked if PR3(5) = 1.

  CRTC Mode Control Register 17 (Bit 2) - Selects divide-by-two vertical timing.

7.5 PR4 - VIDEO CONTROL REGISTER, READ/WRITE PORT = 3CFH, INDEX = 0EH

The video monitor output control register (PR4) can be programmed to tristate the CRT display control outputs, as well as video data for the RAMDAC and memory control outputs.

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7	$\overline{\text{BLANK}}$/Display Enable
6	PCLK = VCLK
5	Tristate Video Outputs
4	Tristate Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Extended 256-color Shift Register Control

Bit 7 - $\overline{\text{BLANK}}$/Display Enable.

This bit controls the output signal $\overline{\text{BLANK}}$. Normally in the VGA mode, $\overline{\text{BLANK}}$ is used by the external video DAC to generate blanking.

1 = The $\overline{\text{BLANK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected and is determined by PR15(1).

Bit 6 - Select PCLK equal to VCLK.

0 = PCLK is either the inverted internal video dot clock or half the dot clock frequency, depending upon the video mode.

1 = PCLK is always the non-inverted VCLK input clock.

Bit 5 - Tristate Video Outputs.

1 = Video Outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLANK}}$ are tristated.

Bit 4 - Tristate Memory Control Outputs.

1 = The memory address bus, MA(8:0), and all ten DRAM control signals are tristated.

Bit 3 - Override CGA Enable Video Bit.

Overrides the CGA Enable Video Bit 3 of mode register 3D8H, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2 - Lock Internal Palette and Overscan Registers.

1 = Internal palette and overscan registers are locked.

Bit 1 - EGA compatibility.

1 = EGA Compatible Mode. Reads are disabled to all registers which are write-only registers in the IBM EGA mode.

Also, registers at 3COH/3C1H change to write-only mode.

Reading PR5 through PR0 is disabled. In VGA mode [PR(4) Bit 1 = 0] 3C0H register is read/write while 3C1H register is read only, per the Attribute Controller Register's definitions.

Bit 0 - Extended Shift Register Control.

1 = Extended 256-color modes selected (IBM Mode 13 is not included).

7.6 PR5 - GENERAL PURPOSE STATUS BITS, READ/WRITE PORT = 3CFH, INDEX = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR4-PR0 Unlock
1	PR4-PR0 Unlock
0	PR4-PR0 Unlock

Bits (7:3) - CNF Status

Bits (7:3) provide a means of reading the read only Configuration Register (CNF), Status Bits (8:4). CNF(8:4) are described in section 9.0.

Bit 7 - CNF(7) General Purpose Status.

Bit 6 - CNF(6) General Purpose Status.

Bit 5 - CNF(5) General Purpose Status.

Bit 4 - CNF(4) General Purpose Status.

Bit 3 - CNF(8) Analog/TTL Display Status.

Bits (2:0) - PR4-PR0.

These are read/write bits and are cleared by reset. They provide lock and unlock capability for PR registers PR4 through PR0. The PR4 through PR0 registers are unlocked when "X5H" is written to PR5. They remain unlocked until any other value is written to PR5.

Setting PR4 Bit 1 to 1, read protects registers PR5 through PR0.

PR5 2 1 0	PR4-PR0
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected
1 0 1	Write enabled

7.7 PR10 - UNLOCK PR1A, PR(17:11) READ/WRITE PORT = 3?5H, INDEX = 29H

PR10 is a read/write register and is cleared by reset. PR10 controls access to registers PR1A and PR17 through PR11.

Bits (7, 3) enable read operations for PR1A and PR17 through PR11.

Bits (6:4) are reserved, must be set to 0.

Bits (2:0) enable write operations for PR1A and PR17 through PR11.

BIT	FUNCTION
7	PR1A, PR(17:11) - Read Enable Bit 1
6:4	Reserved, must be set to 0
3	PR1A, PR(17:11) - Read Enable Bit 0
2:0	PR1A, PR(17:11) - Write Enable

Bits 7, 3 - PR1A, PR(17:11) Read Enable.

BIT7	BIT3	PR1A, PR(17:11)
0 X	X 1	Read protected, read back data FFH
1	0	Read Enabled

Bits 6:4 -

Reserved, must be set to 0.

Bits 2:0 - PR1A, PR(17:11) Write Enable.

PR10 2 1 0	PR1A, PR(17:11)
0 X X X 1 X X X 0	Write protected
1 0 1	Write enabled

7.8 PR11 - EGA SWITCHES, READ/WRITE PORT = 3?5H, INDEX = 2AH

The EGA switch configuration details are stored in register PR11.

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7	EGASW4/General Purpose
6	EGASW3/General Purpose
5	EGASW2/General Purpose
4	EGASW1/General Purpose
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4) - EGA Configuration Switches SW4-SW1.

These read/write bits from corresponding memory data bus pins MD(15:12) are latched internally at power-on-reset with either pull-up or pull-down external resistors. Pulling-up MD(15:12) causes PR11(7:4) to be latched high. These bits can be read from Bit 4 of the Input Status Register at Port 3C2H if the EGA compatibility bit PR4(1) = 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register at Port 3C2H, as follows.

WRITE 3C2H Bit 3	WRITE 3C2H Bit 2	READ 3C2H Bit 4
0	0	PR11(7) = EGA SW4
0	1	PR11(6) = EGA SW3
1	0	PR11(5) = EGA SW2
1	1	PR11(4) = EGA SW1

These bits may be used as general purpose scratch bits.

Bit 3 - Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

This is a read/write bit and is set to zero at power-on-reset.

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Bit 2 - Lock Clock Select.

This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

This is a read/write bit and is set to zero at power-on-reset.

Bit 1 - Lock Graphics Controller/Sequencer Screen Control.

Setting this bit to 1 prevents modification of the following bits in the Graphics Controller as well as the Sequencer:

Graphics Controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by the graphics controller and sequencer bits are locked by setting PR11 Bit 1 to 1, they appear unlocked to the system processor during read operation.

This is a read/write bit and is set to zero at power-on-reset.

Bit 0 - Lock 8/9 Dots.

Setting this bit to 1 prevents modification of the Clocking Mode Sequencer Register 3C5.01, Bit 0.

1 = Eight and nine dot wide character timing is locked. Register 3C5H.01 Bit 0 still appears unlocked to the system processor during read operations.

This is a read/write bit and is set to zero at power-on-reset.

7.9 PR12 - SCRATCH PAD, READ/WRITE PORT = 3?5H, INDEX = 2BH

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7:0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

7.10 PR13 - INTERLACE H/2 START, READ/WRITE PORT = 3?5H, INDEX = 2CH

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up.

In interlaced operations, this register defines the starting horizontal character count at which vertical timing is clocked on alternate fields. Interlaced operation is enabled by setting PR14(5) to 1.

All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE

In the above expression, HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

7.11 PR14 - INTERLACE H/2 END, READ/WRITE PORT = 3?5H, INDEX = 2DH

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bits 7 through 5 are set to 0 by reset.

Bits 4 through 0 are unaffected by hardware reset and undefined at power-up.

Bit 7 - Enable IRQ.

This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used and this bit should be set to 0. This bit should not be set to 1 in Micro Channel operation.

0 = IRQ disabled. Used in VGA operations with an AT bus and Micro Channel operations.

1 = IRQ enabled.

Bit 6 - Vertical Double Scan.

This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed Line Counter and Row Scan Counter to be clocked by divide-by-two horizontal timing, if vertical sync polarity (3C2H Bit 7 = 0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is: N=2(n+1).

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5 - Interlaced Mode.

The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000. Line compare and double scan are not supported.

0 = Interlaced Mode not enabled.

1 = Interlaced Mode is enabled.

Bits (4:0) - Interlaced H/2 End Bits (4:0).

Add the contents of the Interlaced H/2 Start Register PR13 to the horizontal sync width (same as defined by 3X5.04,05). Program the five LSBs of the sum into these bit locations.

7.12 PR15 - MISCELLANEOUS CONTROL 1, READ/WRITE PORT = 3?5H, INDEX = 2EH

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7	Read 46E8H Enable
6	High VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7- Enable Reading Port 46E8H.

This bit is functional only if AT BUS architecture [CNF(2)=1] is selected.

1 = I/O Port 46E8H may be read, regardless of the state of its own Bits 4 and 3 and of Port 102H, Bit 0 (sleep bit). Only Bits(4:0) of Port 46E8H are readable, Bits (7:5) are 0.

Bit 6 - High VCLK.

This bit should be set to 1 when (MCLK in MHz / VCLK in MHz) equals 1.5, or in an extended 256-color mode.

1 = Memory timing is adjusted to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency.

Bit 5 - Latched VCLK1 and VCLK2.

This bit is used only if CNF(3) = 1, which configures the VCLK1 and VCLK2 pins as outputs.

1 = Outputs VCLK2 and VCLK1 are equal to Bits 3 and 2 of I/O write register (Miscellaneous Output Register) at Port 3C2H, respectively.

Bit 4 - Select MCLK as Video Clock.

1 = MCLK input is selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3 - Interlaced Compatibility.

This bit should be set to 1 only if interlaced mode is selected (see PR14) and exact timing emulation of the IBM 8514/A's interlaced video timing is required.

1 = Vertical sync is generated from the trailing edge of non-skewed horizontal sync instead of the leading edge, as generated for VGA timing. Also, two VCLK delays are removed from the default VGA video dot path delay chain.

Bit 2 - Select Page Mode Addressing.

Graphics Modes automatically use Page Mode addressing.

Alpha modes require this bit to be set to 1 for screen refresh memory read cycles to use Page Mode addressing. Setting this bit to 1 in any Alpha Mode overrides the character map select functions of PR2(2) and PR2(5).

Page Mode addressing requires less time than $\overline{RAS}$-$\overline{CAS}$ addressing, therefore, selecting Page Mode addressing increases the bandwidth for the CPU to access video memory by 30-40%.

PR15(2) should be set to 1 if 132 Character Mode timing is selected (see description of PR2).

When PR15(2) is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight 8K memory segments containing a pair of maps in Plane 3 or Plane 2 is addressed by Bits(2:0) of this register while the map selection is determined by Bits(4:3). A pair of adjacent 8K character maps in Planes 3 and 2, (adjacent in the sense that they have the same addressing) may be selected by Bit 3 of the Attribute Code.

The Character Attribute Bit 3 (see section 5.6.4), in conjunction with Bits 4 and 3 of the Character Map Select Register (3C5.03), determine a character map from either Plane 3 or Plane 2 as shown by the table below.

PR15 (2)	3C5.03 (4)	3C5.03 (3)	ATT (3)	PLANE SELECT
1	0	0	X	2
1	0	1	0	3
1	0	1	1	2
1	1	0	0	2
1	1	0	1	3
1	1	1	X	3

The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1, internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1 - Display Enable Timing Select.

This bit is used to select between two types of display enable timings available at output pin $\overline{BLANK}$ if PR4(7) = 1. If PR4(7) = 0, this bit has no effect.

0 = $\overline{BLANK}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{BLANK}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0 - Disable Border.

Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

7.13 PR16 - MISCELLANEOUS CONTROL 2, READ/WRITE PORT = 3?5H, INDEX = 2FH

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRT Control Address Count Width Bit 1
5	CRT Control Address Count Width Bit 0
4	CRT Control Address Counter Offset Bit 1
3	CRT Control Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7 - Lock External 46E8H Register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to Port 46E8H.

Bits (6:5) - CRT Control Address Counter Width.

Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT Controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory, in which CRT Controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations.

COUNT WIDTH

0 0 = 256KB

0 1 = 128K

1 X = 64K

Bits (4:3) - CRT Control Address Counter Offset.

Bits 4 and 3 are summed with the CRT Controller's Address Counter Bits CA(17) and CA(16), respectively, and the two-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2 - Enable Page Bit for Odd/Even.

This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the Page Bit for Odd/Even [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size Bits PR1(7:6).

Bit 1 - VGA Memory Mapping.

Setting this bit to 1 selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size Bits PR1(7:6).

Bit 0 - Lock RAMDAC Write Strobe (3C6H - 3C9H).

0 = Normal operation.

1 = Output $\overline{\text{WPLT}}$ to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C31A, is also protected from the modification but may still be read at the Port 3C7H.

7.14 PR17 - MISCELLANEOUS CONTROL 3, READ/WRITE PORT = 3?5H, INDEX = 30H

This register is locked if PR10(2:0) ≠ 5.

BIT	FUNCTION
7:6	Reserved
5	Character Clock Period Select
4	PCLK = $^{VCLK}/2$
3	Map Out 4K Of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map Out 2K Of BIOS ROM

Bits (7:6)

Reserved.

Bit 5: - Character Clock Period Select.

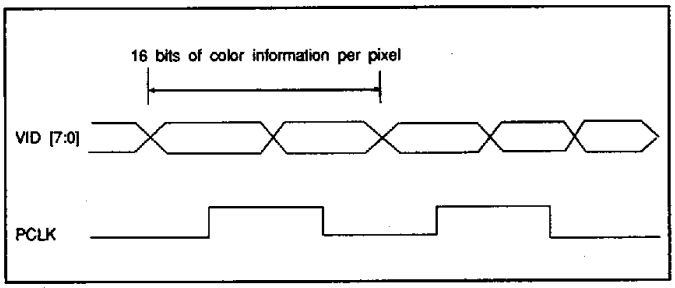
To enable PR17 Bit 5, PR2 (3CF.0C) Bits 4:3 must equal 11. When Bit 5 is not enabled, it has no effect.

0 = Six-dot font is selected.

1 = Ten-dot font is selected.

Bit 4 - PCLK = $^{VCLK}/2$.

1 = Forces PCLK = $^{VCLK}/2$. This control is useful for interface with high color RAM-DAC as follows:



Bit (3) - Map Out 4K of BIOS ROM.

1 = Disables access of the BIOS ROM in the system address range C600:0H through C6FF:FH.

Power-on-reset sets this bit to 0.

Bit 2 - Enable 64K BIOS ROM.

1 = Enables access of the BIOS ROM in the system address range C000:0H through CFFF:FH.

Power-on-reset sets this bit to 0.

Bit 1 - Hercules Compatibility.

1 = Locks Hercules compatibility register (I/O Port 3BFH).

Power-on-reset sets this bit to 0.

Bit 0 - Map Out 2K of BIOS ROM.

1 = Disables access of the BIOS ROM in the system address range C600:0H through C67F:FH.

Power-on-reset sets this bit to 0.

7.15 PR18 - CRTC VERTICAL TIMING OVERFLOW, READ/WRITE PORT = 3?5H, INDEX = 3EH

These bits, combined with other vertical timing overflow bits in CRT Control, constitutes an 11-bit vertical timing control. These bits are set to zero at power-on-reset.

BIT	FUNCTION
7:5	Reserved
4	Line Compare Bit 10
① 3	Start Vertical Blank Bit 10
① 2	Start Vertical Retrace Bit 10
② 1	Vertical Display Enable End Bit 10
① 0	Vertical Total Bit 10

① The bit is locked if PR3(0) = 1 OR the 3?5 Index 11 Bit 7 = 1

② The bit is locked if PR3(1) = 0 AND the 3?5 Index 11 Bit 7 = 1

7.16 PR19 - VIDEO SIGNATURE ANALYZER CONTROL READ/WRITE PORT = 3?5H, INDEX = 3FH

BIT	FUNCTION
7:4	Reserved
3	SIgnature Read Enable
2	Enable Video Input
1	PreLoad Control
0	Enable/Status Bits

Bits (7:4)

Reserved

Bit 3 - Signature Read Enable.

1 = Read signature analyzer results from 3?5H, Index 20 and 21.

Bit 2 - Enable Video Input.

This bit is used for self-test.

0 = Enable video input for signature analyzer.

1 = Self-testing. The video input to the signature analyzer is disabled.

Bit 1 - Preload Control.

0 = The Signature Analyzer Result Register (3?5, Index 20 and 21) is preloaded with 0001H.

1 = Normal operation.

Bit 0 - Enable/Status Bits.

Writing to this bit:

1 = Enables the signature analyzer to collect signature on video input.

Reading this bit:

Indicates the status of the signature analyzer collecting the signature on video input.

0 = Finished (or not enabled).

1 = Busy.

7.17 PR1A - SHADOW REGISTER CONTROL, READ/WRITE PORT = 3?5H, INDEX = 3DH

This register is locked if PR10(2:0) ≠ 5.

Bits (7:4)

Reserved.

Bits 3 - I/O Read Select.

0 = Select actual CRT Control registers for read.

1 = Select shadow CRT Control registers for read.

Bits (2:0) - Shadow Lock.

101 = Locks all the shadowed register bits. This lock overrides any locks. Refer to the Shadow Register description for details.

7.18 PR20 - UNLOCK SEQUENCER EXTENDED REGISTERS, READ/WRITE PORT 3C5H, INDEX = 6H, (RESET STATE = LOCKED)

A value of X1X01XXX must be written to this register to allow Read or Write operations of the Sequencer Extended Registers. When the extended registers are locked, the Sequencer Index is read as three bits. When unlocked, the Sequencer Index reads as six bits.

7.19 PR21 - DISPLAY CONFIGURATION STATUS AND SCRATCH PAD BITS REGISTER, BITS 7:4 READ/WRITE BITS 3:0, READ ONLY PORT 3C5H, INDEX = 7H

This register is locked if PR20(6, 4, 3) ≠ 101.

This register provides a convenient location for determining the current state of the VGA configuration. This information is required for many BIOS calls.

BIT	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2 Bit 0
2	Status of PR2 Bit 6
1	Status of PR4 Bit 1
0	Status of PR5 Bit 3

Bits (7:4) - Scratch Pad Bits.

These read/write bits serve as a scratch pad for any BIOS status data that may need to be saved. These bits are preset to 1111 at reset.

Bit 3 - Status of 3C2H Bit 0.

This read only bit represents the setting of the I/O address select bit in the Miscellaneous Output Register.

0 = MDA (3Bx) addresses have been selected.

1 = CGA (3Dx) addresses have been selected.

Bit 2 - Status of PR2 Bit 6.

This read only bit represents the setting of the VGA/6845 select bit in PR2 (3CFH Index CH).

0 = VGA or EGA compatibility has been selected.

1 = 6845 compatibility has been selected.

Bit 1 - Status of PR4 Bit 1.

This read only bit represents the setting of the VGA/EGA select bit in PR4 (3CFH Index EH).

0 = VGA was selected.

1 = EGA compatibility has been selected.

Bit 0 - Status of PR5 Bit 3.

This read only bit represents the setting of the Analog/TTL status bit in PR5 (3CFH Index FH).

0 = An analog monitor was selected.

1 = A TTL-type monitor was selected.

7.20 PR22 - SCRATCH PAD REGISTER, READ/WRITE PORT = 3C5H, INDEX = 8H

Bits (7:0)

Scratch pad bits.

7.21 PR23 - SCRATCH PAD REGISTER, READ/WRITE PORT = 3C5H, INDEX = 9H

Bits (7:0)

Scratch pad bits.

7.22 PR30 - MEMORY INTERFACE, WRITE BUFFER AND FIFO CONTROL REGISTER, READ/WRITE PORT = 3C5H, INDEX 10H

This register is locked if PR20(6, 4, 3) ≠ 101.

This register controls display memory data width and its bandwidth. All bits are reset to zero at power-on-reset.

BIT	FUNCTION
7:6	Write Buffer Control
5	32-bit or 16-bit Memory Data Path
4	Disable 16-bit CPU Interface for Unchain Mode
3	Two-level FIFO
2	Four or Eight-level FIFO
1:0	Display FIFO control

Bits (7:6) - Write Buffer Control.

Bits 7 and 6 determine the depth of the write buffer.

PR31 Bit 2 must be set to 1 for these two bits to have any effect.

WRITE BUFFER LEVEL

0 0 = One level deep.

0 1 = Two levels deep.

1 0 = Three levels deep.

1 1 = Four levels deep.

Bit 5 - Memory Data Path.

0 = The display memory data path is 32-bits wide.

1 = The display memory data path is 16-bits wide.

Bit 4 - Disable Unchained Mode.

0 = Normal conditions.

1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3 - Two-level FIFO.

0 = The FIFO is four or eight levels deep, depending on Bit 2 of this register.

1 = The FIFO is two levels deep, regardless of Bit 2.

Bit 2 - Four or Eight-Level FIFO.

0 = FIFO set to eight levels deep.

1 = FIFO set to four levels deep.

Bits (1:0) - Display FIFO Control.

These two bits can be used to adjust the display memory bandwidth. In general, to accommodate most applications, it is recommended that these two bits be set to 01. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

FIFO requests for memory cycle when FIFO is:

0 0 = One level empty

0 1 = Two levels empty

1 0 = Three levels empty

1 1 = Four levels empty

7.23 PR31 - SYSTEM INTERFACE CONTROL, READ/WRITE PORT = 3C5H, INDEX = 11H, RESET STATE = 00

This register is locked if PR20(6, 4, 3) ≠ 101.

This register provides the control bits for the system interface. This register should be set during the post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 is used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY Release Control 1
3	CPU Read RDY Release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7 - Read/Write Offset Enable.

0 = Normal (Refer to PR0A and PR0B definitions).

1 = During read cycles, the offset register PR0-A, is added to the CPU address. During write cycles PR0-B is added to the CPU address.

Bit 6 - Turbo Mode for Blanked Lines.

0 = Normal.

1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.

Bit 5 - Turbo Mode for Text.

0 = Normal.

1 = Improved text mode performance.

Bits (4:3) - CPU Read IOCHRDY Release Controls 1,0.

These two bits select the IOCHRDY timing for CPU reads. To improve performance of systems with a slower bus clock, IOCHRDY may be asserted earlier. Data will be ready following IOCHRDY no sooner than the time selected by bits (4:3).

0 0 = 40 ns. (Power-on-reset condition).

0 1 = 40 ns. plus 1 MCLK.

1 0 = 40 ns. plus 2 MCLKs.

1 1 = 40 ns. minus 1MCLK.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2 - Enable Write Buffer.

0 = Write buffer disabled.

1 = Write buffer is enabled. This greatly reduces the number of wait states for CPU writes to display memory.

Bit 1 - Enable 16-bit I/O Attribute Controller.

If Bit 1 and Bit 0 are both set to 1, the Attribute Controller (3C0H/3C1H) is configured for 16-bit access. The index is at 3C0H while the data is at 3C1H and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for eight-bit cycles. $\overline{\text{IOCS16}}$ is asserted for all cycles to 3C0H or 3C1H.

Bit 0 - Enable 16-bit I/O Operations.

0 = The VGA I/O is eight-bits.

1 = Enables 16-bit access to the CRTC (3?4H/3?5H), Sequencer (3C4H/3C5H) and Graphics Controller (3CEH/3CFH). The output $\overline{\text{IOCS16}}$ will be active for any I/O read or write to these addresses.

7.24 PR32 - MISCELLANEOUS CONTROL 4, READ/WRITE PORT = 3C5H, INDEX = 12H, RESET STATE = 00

This register is locked if PR20(6, 4, 3) ≠ 101.

This register provides control for several different features. Some of these features help to support Genlock of the WD90C31A to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow Read Back in Backward compatible Modes
0	Force Standard CPU Addressing in 132-column Mode

Bit 7 - Enable External Sync Mode.

0 = Normal operation mode.

1 = $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external $\overline{\text{HSYNC}}$ signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID7:0 and PCLK output buffers, but they are used to genlock the WD90C31A to another display controller.

Bit 6 - Disable Cursor Blink.

0 = Blink enabled.

1 = The text cursor blink is disabled and the cursor remains on. This option can be used when cursor blink is not desired.

Bit 5 - USR1 Function Select.

0 = The USR1 output represents the state of Bit 4. This can be used to control new features added by the system board designer.

1 = Reserved.

Bit 4 - USR1 Control.

Controls the USR1 output when selected by Bit 5.

Bit 3 - USR0 Function Select.

0 = The USR0 output represents the state of Bit 2. This can be used to control new features added by the system board designer.

1 = Reserved.

Bit 2 - USR0 Control.

Controls the USR0 output when selected by Bit 3.

Bit 1 - Read in Backward Compatible Modes.

0 = Registers that are not normally readable in backward compatibility modes may not be read.

1 = Registers that are not normally readable in backward compatibility modes may be read.

This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0 - 132-Column Mode.

1 = The special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This is used only for special virtual VGA applications.

7.25 PR33 - DRAM TIMING AND ZERO WAIT STATE CONTROL, READ/WRITE PORT = 3C5H, INDEX = 13H

This register is locked if PR20(6, 4, 3) ≠ 101.

Bits (7:6) - $\overline{\text{0WS}}$ Control.

These two bits control the operation of the $\overline{\text{0WS}}$ output pin. $\overline{\text{0WS}}$ is disabled if PR31 bit 2 = 0 (Write Buffer is off).

0 0 = $\overline{\text{0WS}}$ = 0 if the internal write buffer is ready.

0 1 = $\overline{\text{0WS}}$ = 0 if the internal write buffer is ready and the memory address is decoded.

1 0 = $\overline{\text{0WS}}$ = 0 if the internal write buffer is ready and the memory address is decoded and MWR = 0.

1 1 = $\overline{\text{0WS}}$ = 0 if the condition in 10 is true or I/O write to the WD90C31A is occurring.

Bit 5

Reserved

Bits (4:3) - $\overline{CAS}$ Timing.

These two bits control the $\overline{CAS}$ timing.

0 0 = $\overline{CAS}$ cycle is 2 MCLKs.
$\overline{CAS}$ low is 1 MCLK + (4~7) ns.
$\overline{CAS}$ high is 1 MCLK - (4~7) ns.

0 1 = $\overline{CAS}$ cycle is 2 MCLKs.
$\overline{CAS}$ low is 1 MCLK + (8~14) ns.
$\overline{CAS}$ high is 1 MCLK - (8~14) ns.

1 0 = $\overline{CAS}$ cycle is 2 MCLKs.
$\overline{CAS}$ low is 1.5 MCLKs.
$\overline{CAS}$ high is 0.5 MCLKs.

1 1 = Reserved.

Bit 2 - $\overline{CAS}$ After $\overline{RAS}$ Timing.

0 = $\overline{CAS}$ cycle starts 2.5 MCLKs after $\overline{RAS}$ low.

1 = $\overline{CAS}$ cycle starts 1.5 MCLKs after $\overline{RAS}$ low.

Bits (1:0) - $\overline{RAS}$ Precharge.

These two bits control $\overline{RAS}$ precharge. Refer to DRAM timing adjustments in Section 19.0.

0 0 = $\overline{RAS}$ high is 2-1/2 MCLKs plus a 4:7 ns. delay.

0 1 = $\overline{RAS}$ high is 3 MCLKs wide.

1 0 = $\overline{RAS}$ high is 2 MCLKs wide.

1 1 = $\overline{RAS}$ high is 2-1/2 MCLKs.

7.26 PR34 - VIDEO MEMORY MAPPING, READ/WRITE PORT = 3C5H, INDEX = 14H

This register is locked if PR20(6, 4, 3) ≠ 101.

Bits (7:4)

7:6 Reserved, 5:4 reserved for Driver usage.

Bits (3:0) - Video Memory Mapping.

These four bits are compared with the CPU address A(23:20) as part of the video memory address decoding. This allows the VGA to be mapped into any 1 Mbyte CPU memory space. This register does not affect the $\overline{EBROM}$ and $\overline{ROM16}$ decoding. $\overline{EBROM}$ and $\overline{ROM16}$ are still decoded at A(23:20) = 0H. Used with the correct setting of PR1, Bits 5 and 4, this register supports virtual VGA applications.

These four bits are set to 0 at power-on-reset.

7.27 PR35 - RESERVED, READ/WRITE PORT = 3C5H, INDEX = 15H

This register is locked if PR20(6, 4, 3) ≠ 101.

Bits (7:0)

Reserved.

8.0 INTERNAL I/O PORTS

8.1 AT MODE SETUP, ENABLE, WRITE ONLY PORT 46E8H (ALSO AT PORT 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7:5	Reserved
4	Setup
3	Enable I/O and Memory
2:0	External BIOS ROM Page Select

Bits (7:5)

Unused.

Bit 4 - Setup.

This bit puts the WD90C31A into Setup mode where only I/O Port 102H is accessible.

Bit 3 - Enable I/O and Memory Accesses.

This bit enables I/O and memory accesses.

Bits (2:0) - BIOS ROM Page Select.

On I/O accesses to Port 46E8H, $\overline{\text{EBROM}}$ becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits and define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM therefore, appears to consist of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using these bits (D2:D0). The WD90C31A also provides Port 3C3H as an alternative to Port 46E8H. If a pull-down resistor is connected to MD9 during power-on-reset [CNF(9) = 0], Port 3C3H is decoded instead of Port 46E8H to support the same functions as described above. Otherwise, Port 46E8H is selected and decoded.

8.2 SETUP MODE VIDEO ENABLE (AT AND MICRO CHANNEL MODES) READ/WRITE PORT = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7:1	Reserved
0	Wakeup VGA

Bits (7:1)

Unused.

Bit 0 - Wakeup VGA.

Wakeup VGA for I/O and Memory Accesses. Only the lower three address bits are decoded for this port and the WD90C31A must be in Setup mode. VGA Enable Sleep bit or Programmable Option Select (POS) Register 102H Bit 0 is used to awaken the WD90C31A after power on in the MCA and AT mode. To enter the Setup mode in AT bus applications, Bit 4 of the partially decoded internal I/O Port 46E8H is set to 1 before accessing the I/O Port 102H. In MCA mode, the WD90C31A is in Setup mode and Port 102H can be accessed when the VGA setup ($\overline{\text{EIO}}$) signal pin is active low.

9.0 CONFIGURATION REGISTER BITS CNF(18:0)

Memory Data Lines (18:0) [MD(18:0)] are used to input configuration data [CNF(18:0)] at power-on-reset (RST) by pull-up or pull-down resistors. This configuration data sets the bits in internal registers. CNF(15:12), CNF(10) and CNF(0) can also be changed by software, while all others are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on. All MD(18:0) are internally pulled up by 50 ohm resistors.

CNF	FUNCTION
18	Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ input
17	
16	64K by 16 or 256K by 4 DRAM select
15:12	EGA Switches
11	A23 - A20 Connection Select
10	Disable $\overline{\text{ROM16}}$ address decode
9	46E8H/3C3H Select
8	Display Status
7:4	General Purpose Status
3	Video Clock Source Control
2	AT/MCA Bus Select
1	ROM Configuration
0	BIOS ROM Mapping

CNF(18) - $\overline{\text{ROM16}}$ As $\overline{\text{EXBLANK}}$ input.

0 = A 4.7K pull-down resistor on Pin MD18. $\overline{\text{ROM16}}$ is configured as $\overline{\text{EXBLANK}}$ input.

1 = No pull-down resistor, the internal pull-up sets CNF(18) to 1. Normal $\overline{\text{ROM16}}$ operation. $\overline{\text{ROM16}}$ is an output.

CNF(16) - 64K By 16 Or 256K By 4 DRAM Select.

0 = A 4.7K pull-down resistor on pin MD16 sets the WD90C31A to interface with a 64K by 16 DRAM.

1 = No pull-down resistor. The internal pull-up sets WD90C31A to interface with a 256K by 4 or 256K by 16 DRAM.

CNF(15:12) - EGA Configuration Switches SW4-SW1.

No external pull-down resistors on MD(15:12) causes PR11(7:4) to be latched high. Pulling down MD(15:12) causes these bits to be latched low.

PR11(7:4) are writable bits. These bits can be read as Bit 4 of Port 3C2H (as on a standard EGA) if the EGA compatibility bit [PR4(1)] has been set to 1. Selection of which bit to read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows.

WRITE		READ
3C2 Bit 3	3C2 Bit 2	3C2 Bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF(11) -

Reserved. Pin has an internal pull-up resistor. Do not use an external pull-down resistor.

CNF(10) - Disable $\overline{\text{ROM16}}$ Address Decode.

0 = The internal pull-up sets CNF(10) = PR1(1) = 0. To enable the 16-bit BIOS, PR1(1) must be set to 1 by writing to Port 3CFH, Index 0BH Bit 1 and, at the same time, CNF(1) must be 1.

1 = A 4.7K pull-down on Pin MD10 sets CNF(10) = PR1(1) = 1. Upon power-up, the pin $\overline{\text{ROM16}}$ is enabled for 16-bit BIOS ROM decoding.

This bit is read/write at PR1(1).

CNF(9) - 46E8H/3C3H Select.

This bit has no effect in Micro Channel applications.

0 = A 4.7K pull-down on Pin MD9. Port 03C3H is selected as the VGA setup and enable register instead of Port 46E8H in the AT interface.

1 = No pull-down resistor. The internal pull-up sets CNF(9) = 1. Port 46E8H is selected as VGA setup and enable register.

CNF(8) - Analog/TTL Display Status Bit.

Whether provided with either a pull-up or pull-down external resistor, CNF(8) is latched internally at power-on-reset from memory data bus Pin MD11.

Pulling up MD11 causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached.

1 = TTL (EGA - compatible) display is attached.

CNF(7:4) - General Purpose Status Bits.

Bits CNF(7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD(7:4), provided with either pull-up or pull-down external resistors.

Pulling down MD(7:4) causes CNF(7:4) to be latched high.

These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F).

CNF(3) - Video Clock Source Control.

This bit cannot be written or read as I/O port.

Pulling up MD3 causes CNF(3) to be latched high. It configures WD90C31A pins VCLK1 and VCLK2 as inputs or outputs.

0 = Inputs.

1 = Outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer.

When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to Port 3C2H. This load pulse may be inhibited by setting PR11(2) = 1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK2 and VCLK1 outputs are equal to Bits 3 and 2 of the Miscellaneous Output Register at 3C2H when PR15 Bit 5 = 1.

CNF (2) - AT/MCA Bus Architecture Select.

This bit cannot be written or read as I/O. Pulling down MD2 causes CNF(2) to be latched low.

0 = Micro Channel architecture.

1 = AT BUS architecture.

Selecting CNF(2) changes the pinout definition between AT BUS and Micro Channel bus. (See Signal Description.)

PC-AT BUS	I/O	MICRO CHANNEL	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF(1) - ROM Configuration.

With an 8-bit system interface [CNF(1) = 0]:

Address bit A0 = 0, selects the even ROM.
A0 = 1, selects the odd ROM.

With a 16-bit system interface, [CNF(1) and PR1 = 1] enables $\overline{\text{ROM16}}$.

This bit can not be written or read.

0 = No pull-down resistor on MD1. The internal pull-up sets CNF(1) = 0 at power-on-reset. The WD90C31A's data bus buffer controls are configured for one ROM (eight bits). PR1(1) can not be set high.

1 = The WD90C31A's data bus buffer controls are configured for 16-bits (as with two ROMs). Setting CNF(1) to 1 enables the $\overline{\text{HTL}}$ output pin.

CNF (0) - BIOS ROM Mapping.

This bit may read or written at PR1(0).

0 = No pull-down resistor on MD0. The internal pullup resistor sets this bit to 0 at power-on-reset.

1 = The BIOS ROM is mapped out. An external 4.7 Kohm pull-down resistor sets CNF(0) = 1 on power-on-reset.

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10.0 HARDWARE CURSOR

The Hardware Cursor supports a user-defined pattern of up to 64 by 64 pixels, defined at 2 bits per pixel. The cursor pattern should be stored in a non-visible part of display memory. The cursor operates in all packed and planar VGA graphics modes, as well as VGA text modes.

The Hardware Cursor is accessed at Port 23C2H/23C3H when the register block pointer at Port 23C0H has been set to 02H.

INDEX	FUNCTION
Index 0	Cursor Control
Index 1	Cursor Pattern Address Low
Index 2	Cursor Pattern Address High
Index 3	Cursor Primary Color
Index 4	Cursor Secondary Color
Index 5	Cursor Origin
Index 6	Cursor Display Position X
Index 7	Cursor Display Position Y
Index 8	Cursor Auxiliary Color

TABLE 10-1. CURSOR REGISTERS

10.1 CURSOR CONTROL REGISTER, INDEX 0

The Cursor Control register controls operation of the hardware cursor.

BIT	FUNCTION
15:12	0000 (Index)
11	Cursor Enable
10:9	Cursor Pattern Type
8	Cursor Plane Protection
7:5	Cursor Color Mode
4:0	Reserved

NOTE

A write to either the Cursor Enable or the Cursor Pattern Type fields does not take effect until the beginning of a video frame following the next write to the Cursor Control Register. (In interlaced mode, it's the next video field.)

Bits (15:12) - Index 0.

Bit 11 - Cursor enable.

0 = Cursor is not displayed.

1 = Cursor is displayed.

Bits (10:9) - Cursor pattern type.

00 = Cursor is 2 bits per pixel, 32x32 pixels.

01 = Cursor is 2 bits per pixel, 64x64 pixels.

10 = Reserved.

11 = Reserved.

Bit 8 - Cursor plane protection.

0 = Cursor plane protection disabled.

1 = Cursor plane protection enabled.

Bits (7:5) - Cursor color mode.

000 = Software compatible cursor.

001 = Two-color cursor with inversion.

010 = Two-color cursor with special inversion.

011 = Three-color cursor.

100 = Reserved.

101 = Reserved.

110 = Reserved.

111 = Reserved.

Bits (4:0)

Reserved.

10.2 CURSOR PATTERN ADDRESS

The two Cursor Pattern Address registers form a 21-bit address, specifying the location in the display memory where the first byte of the cursor pattern is stored. This value is independent of the cursor origin. The cursor pattern may be stored anywhere in the display memory but is generally stored in a non-visible location.

Generally, this address represents the CPU address at which the pattern begins, minus the CPU address of the top-left corner of the screen, in whichever current VGA mode is in use. Not all addresses are valid in all modes. See the section on "Cursor Address Mapping."

NOTE

A write to either of the Cursor Pattern Address Registers or the Cursor Origin Register does not take effect until the beginning of a video frame following the next write to the Cursor Control Register. (In interlaced mode, it's the next video field.)

10.2.1 Cursor Pattern Address Low, Index 1

BIT	FUNCTION
15:12	0001 (Index)
11:0	Cursor Pattern Address Bits 11:0. Bits 1 and 0 must be set to 0.

10.2.2 Cursor Pattern Address High, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:9	Reserved
8:0	Cursor Pattern Address Bits 20:12

10.3 CURSOR ORIGIN, INDEX 5

The Cursor Origin register specifies the offset in pixels from the top-left corner of the pattern which will be displayed at the cursor display position. This value is often referred to as the cursor's "hot spot".

NOTE

For 32 by 32 cursor patterns each field is restricted to the values 31:0.

BIT	FUNCTION
15:12	0101 (Index)
11:6	Cursor Origin Y (63:0)
5:0	Cursor Origin X (63:0)

10.4 CURSOR DISPLAY POSITION

The Cursor Display Position X and Y registers specify the location on the screen at which the cursor origin is displayed. These values represent a position in pixels, referenced to the top-left corner of the screen, regardless of the display mode.

In text modes, the cursor position still represents pixels not characters. The cursor can be displayed at any position on the screen, including between characters.

NOTE

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. (In interlaced mode, it's the next video field.)

10.4.1 Cursor Display Position X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11	Reserved
10:0	Cursor Display Position X

10.4.2 Cursor Display Position Y, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11:10	Reserved
9:0	Cursor Display Position Y

10.5 CURSOR COLOR REGISTERS

The cursor color registers control the display of 2-bit per pixel cursor patterns.

The Cursor Primary Color, Cursor Secondary Color and Cursor Auxiliary Color registers specify eight-bit colors to be displayed for different parts of the cursor pattern.

NOTE

Even in planar mode, in which pixels are four bits each, these colors are eight bits per pixel.

10.5.1 Cursor Primary Color, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:8	Reserved
7:0	Cursor Primary Color

10.5.2 Cursor Secondary Color, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:8	Reserved
7:0	Cursor Secondary Color

10.5.3 Cursor Auxiliary Color, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:8	Reserved
7:0	Cursor Auxiliary Color

10.6 CURSOR REGISTER UPDATES

When a new cursor pattern is selected, up to four different registers must be updated. If a new video frame were to begin before all registers were updated, a single frame could be displayed with incorrect cursor data. While the display would recover within one video frame, the results would be visually annoying. Therefore, the WD90C31A holds off use of updated register data until all of the associated registers have been updated.

Writing to either the Cursor Pattern Address register or the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the Cursor Control register. Therefore, the Cursor Control register must be written to after updating either of these registers, even if the data in the Cursor Control register is to remain unchanged. However, reading any of these registers always returns the data last written to the register, whether or not such data has already taken effect.

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. In interlaced mode, updates occur at the beginning of the next video field.

10.6.1 Cursor Address Mapping

Cursor patterns are always stored in contiguous locations in display memory, usually in a non-visible portion, and always across all four maps. The definition of contiguous locations differs slightly by mode, as defined in Tables 10-2, 3 and 4.

Each mode has restrictions on where a cursor pattern may begin and how such a pattern must be stored. The location where the currently required cursor pattern is stored in display memory is loaded by the host into the Cursor Pattern Address registers, as defined in Tables 10-2, 3 and 4.

The Cursor Pattern Address registers point to the doubleword starting region of the cursor pattern. They are not byte addresses and consecutive register values generally do not point to consecutive memory bytes. However, the cursor pattern must use all of the consecutive memory bytes (1K or 256 bytes) assigned to it starting from the byte pointed to.

CPU Address	Cursor Pattern Address
Bank 0	
A0000 ①	
Map 0	0 If pattern starts here . . .
Map 1	② then next byte is here . . .
Map 2	② then here . . .
Map 3	② then here . . .
A0001	
Map 0	1 and fifth byte is here
⇓	
AFFFF	
Map 0	FFFF
Bank 1	
A0000	
Map 0	10000
⇓	
AFFFF ③	
⇓	
Map 3	1FFFF (Theoretical maximum for 1K X 1K display memory.)

TABLE 10-2. PLANAR MODES

CPU Address	Cursor Pattern Address
Bank 0	
A0000 ①	0 If pattern starts here . . .
A0001	② then next byte is here . . .
A0002	② then here . . .
A0003	② then here . . .
A0004	1 and fifth byte is here
⇓	
AFFFC	3FFF
Bank 1	
A0000	4000
⇓	
Bank 0F	
⇓	
AFFFC ③	3FFFF (Theoretical maximum for 1K X 1K display memory.)

TABLE 10-3. PACKED MODES

CPU Address ④	Cursor Pattern Address
Maps 0:1	
B8000 ①	0 If pattern starts here . . .
B8001	② then next byte is here . . .
Maps 2:3	
B8000	② then here . . .
B8001	② then here . . .
Maps 0:1	
B8002	1 and fifth byte is here
B8003	
⇓	
BFFFE	3FFF
BFFFF	
	See the following notes.

TABLE 10-4. TEXT MODES

NOTES

① These locations are usually visible. In practice, cursor pattern is usually stored in non-visible memory.

② Cursor pattern must start in map 0 but pattern is stored on all maps.

③ Some modes and/or boards may not support CPU addresses up to this level. Since up to 1K consecutive locations are required for the pattern, the pattern cannot actually start at the highest locations.

④ In mode 7, CPU addresses are B0000-B7FFE.

10.6.2 Two-Bit Cursor Pattern Format

The cursor pattern pointed to by the Cursor Pattern Address registers for two-bit cursor patterns is stored in either 1K or 256 consecutive memory byte locations. The cursor pattern data is stored for 64 by 64 and 32 by 32 cursors as follows:

10.6.2.1 Cursor Pattern - 2-Bit, 64 x 64 Cursors

Offset ①	Map ②	Cursor Pattern ③ ④
0	0	AND plane, row 0, col. 0-7
	1	XOR plane, row 0, col. 0-7
	2	AND plane, row 0, col. 8-15
	3	XOR plane, row 0, col. 8-15
1	0	AND plane, row 0, col. 16-23
	1	XOR plane, row 0, col. 16-23
	2	AND plane, row 0, col. 24-31
	3	XOR plane, row 0, col. 24-31
2	0	AND plane, row 0, col. 32-39
	1	XOR plane, row 0, col. 32-39
	2	AND plane, row 0, col. 40-47
	3	XOR plane, row 0, col. 40-47
3	0	AND plane, row 0, col. 48-55
	1	XOR plane, row 0, col. 48-55
	2	AND plane, row 0, col. 56-63
	3	XOR plane, row 0, col. 56-63
4	0	AND plane, row 1, col. 0-7
	1	XOR plane, row 1, col. 0-7
	2	AND plane, row 1, col. 8-15
	3	XOR plane, row 1, col. 8-15
⇓		
255	0	AND plane, row 63, col. 48-55
	1	XOR plane, row 63, col. 48-55
	2	AND plane, row 63, col. 56-63
	3	XOR plane, row 63, col. 56-63

NOTES

① Offset is relative to the value in the Cursor Pattern Address register.

② In packed mode, Map is selected by the two low-order CPU address bits.

③ Cursor pattern must start in map 0 but pattern is stored on all maps.

④ Within each byte, the high-order bit represents the left most column.

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10.6.2.2 Cursor Pattern - 2-Bit, 32 x 32 Cursors

Offset	Map	Cursor Pattern
0	0	AND plane, row 0, col. 0-7
	1	XOR plane, row 0, col. 0-7
	2	AND plane, row 0, col. 8-15
	3	XOR plane, row 0, col. 8-15
1	0	AND plane, row 0, col. 16-23
	1	XOR plane, row 0, col. 16-23
	2	AND plane, row 0, col. 24-31
	3	XOR plane, row 0, col. 24-31
2	0	AND plane, row 1, col. 0-7
	1	XOR plane, row 1, col. 0-7
	2	AND plane, row 1, col. 8-15
	3	XOR plane, row 1, col. 8-15
3	0	AND plane, row 1, col. 16-23
	1	XOR plane, row 1, col. 16-23
	2	AND plane, row 1, col. 24-31
	3	XOR plane, row 1, col. 24-31
⇓		
63	0	AND plane, row 31, col. 16-23
	1	XOR plane, row 31, col. 16-23
	2	AND plane, row 31, col. 24-31
	3	XOR plane, row 31, col. 24-31

10.6.3 Loading the Cursor Pattern

Loading a cursor pattern requires writing the pattern to a non-visible portion of display memory, then pointing to the pattern with the Cursor Pattern Address registers (Index 1, 2). A cursor pattern already in display memory can be selected simply by loading these registers.

In some VGA modes, certain maps are not defined but the physical RAM connected to those maps appears at higher memory locations in the maps that are defined. For instance, the first byte of map 2 may appear as the 64th Kbyte in map 0. Therefore a cursor pattern that occupies contiguous locations in one mode may appear fragmented in other modes. It is the responsibility of the software to track these fragments and assure that no part of the pattern will be accidentally overwritten.

10.6.4 Cursor Color Modes

A cursor may be displayed using any of four color modes selected by the Cursor Color Mode field of the Cursor Control Register (Index 0). Depending on the color mode selected, each 2-bit pixel of the cursor pattern will be displayed against the background as described in Table 10-5.

The "special" color generates the exclusive-NOR (XNOR) of the background and the Auxiliary Color Register (Index 8). This retains the "different from background" color property of inversion while adding the ability to specify one preferred "special inversion" from a background color to any desired color.

To use this feature, the Cursor Color Mode field must be set to "special", and the Cursor Auxiliary Color should be loaded with the exclusive NOR (XNOR) of the background color to be translated and the desired color to be displayed. When set in this manner, any screen pixel of the former color covered by an inverting cursor pattern pixel will be "inverted" into the auxiliary color.

10.6.5 Compatibility Differences Between Hardware and Software Cursor

Some cursor colors may display differently using the hardware cursor than when using a software cursor. This can happen in Planar Modes, because a software cursor modifies memory data that is then passed through the Attribute Controller's Palette registers, while the hardware cursor operates on data at the output of the Attribute Controller's Palette registers. The section on "Cursor Plane Protection" explains how to minimize these incompatibilities.

10.6.6 Cursor Plane Protection

In 256-color modes, a background pixel covered by the cursor is either replaced by a specified 8-bit color or is inverted. For other modes, cursor plane protection is available.

When the Cursor Plane Protection bit of the Cursor Control register is set, some bits of the background are handled differently. In these cases the two or four high-order bits of the background are replaced with the corresponding bits of the Cursor Auxiliary Color register (Index 8).

When bit 7 of the VGA Attribute Mode Control register (Port 3C0H/3C1H, Index 10H) is reset, cursor plane protection applies to the two high-order bits of the background. When this bit is set, protection applies to the four high-order bits.

This feature is designed to provide as much flexibility and compatibility with a software cursor as possible, due to the processing done by the VGA attribute controller.

CURSOR PATTERN ①	COLOR MODE 0	COLOR MODE 1	COLOR MODE 2	COLOR MODE 3
00	All 0s	Secondary	Secondary	Secondary
01	All 1s	Primary	Primary	Primary
10	Transparent	Transparent	Transparent	Transparent
11	Inverted	Inverted	Special ②	Auxiliary

TABLE 10-5. CURSOR COLOR MODES

NOTES

① The high-order bit of each 2-bit pattern is the AND mask, the low-order bit is the XOR mask.

② Result is Background XNOR'd with the auxiliary color.

11.0 HARDWARE BITBLT

The BITBLT hardware supports accelerated data transfers between regions of display memory. Display memory regions may be rectangular or linear.

A full complement of raster operations are available. Color expansion and transparency, useful for accelerating text modes as well as plane masking, are also supported.

This same hardware can be used to rapidly copy 8 by 8 patterns and fill rectangles.

The BITBLT hardware supports text modes and monochrome, 4-bit and 8-bit color modes, as well as the 16-bit color mode.

Index 0	BITBLT Control - part 1*
Index 1	BITBLT Control - part 2
Index 2	BITBLT Source Low
Index 3	BITBLT Source High
Index 4	BITBLT Destination Low*
Index 5	BITBLT Destination High*
Index 6	BITBLT Dimension X
Index 7	BITBLT Dimension Y
Index 8	BITBLT Row Pitch
Index 9	BITBLT Raster Operation
Index A	BITBLT Foreground Color
Index B	BITBLT Background Color
Index C	BITBLT Transparency Color
Index D	BITBLT Transparency Mask
Index E	BITBLT Map And Plane Mask
* All or part of these registers can change automatically.	

TABLE 11-1. BITBLT REGISTERS INDEX

11.1 CONTROL AND STATUS

BITBLT Control - Part 1, Index 0

BIT	FUNCTION
15:12	0000 (Index)
11	BITBLT Activation/Status*
10	BITBLT Direction
9:8	BITBLT Addressing Mode
7:6	BITBLT Destination/ Source Linearity
5:4	BITBLT Destination Select
3:2	BITBLT Source Format
1:0	BITBLT Source Select
* This bit is automatically reset when BITBLT is completed.	

Bits (15:12) - Index 0.

Bit 11 - BITBLT Activation/Status.

Writing a 1 to this bit starts a BITBLT operation using the currently loaded register values. This bit is reset automatically when the BITBLT operation is completed. Therefore, reading a 1 from this bit indicates that a BITBLT operation is in progress.

Writing a 0 to this bit will not start a BITBLT operation but may be useful in "quick start" mode to set the other bits in the register for the coming series of quick-start operations.

CAUTION

Writing a 0 to this bit while a BITBLT operation is in progress may cause unexpected and unrecoverable results.

0 = Do not start BITBLT (write), BITBLT completed (read).

1 = Start BITBLT (write), BITBLT in progress (read).

Bit 10 - BITBLT Direction.

0 = BITBLT direction is top to bottom, left to right.

1 = BITBLT direction is bottom to top, right to left.

Bits (9:8) - BITBLT Address Mode.

00 = Planar Mode (includes monochrome modes).

01 = Packed Mode, includes text and 256-color modes.

1X = Reserved for future expansion.

Bits (7:6) - BITBLT Destination/Source Linearity.

When the Destination or Source region of a BITBLT operation is specified as linear, each row of that region is considered to begin at the doubleword immediately following the doubleword containing the last pixel of the preceding row. The alignment of the first pixel in each line is the same. No doubleword will straddle two lines and there may be gaps at unused pixels between adjacent lines.

Bit 7 controls the destination area, Bit 6 controls the source area.

0 = Area is rectangular.

1 = Area is linear.

Bits (5:4) - BITBLT Destination Select.

00 = Destination is screen memory.

10 = Destination is system I/O location.

X1 = Reserved for future expansion.

Bits (3:2) - BITBLT Source Format.

00 = Source format is color.

01 = Source format is monochrome from color comparators.

10 = Source format is fixed color (filled rectangle).

11 = Source format is monochrome from host.

Bits (1:0) - BITBLT Source Select.

00 = Source is screen memory.

10 = Source is system I/O location, 32 bits.

X1 = Reserved for future expansion.

BITBLT Control - Part 2, Index 1

BIT	FUNCTION
15:12	0001 (Index)
11	Reserved
10	BITBLT Interrupt Enable
9:8	Reserved
7	BITBLT Quick Start
6	BITBLT Update Destination
5:4	BITBLT Pattern Select
3	BITBLT Monochrome Transparency
2	BITBLT Transparency Polarity
1	Reserved, must be 0
0	BITBLT Transparency Enable

Bits (15:12) - Index 1.

Bit 11

Reserved.

Bit 10 - BITBLT Interrupt Enable.

0 = Do not interrupt on completion of BITBLT.

1 = Interrupt on completion of BITBLT.

Bits (9:8)

Reserved.

Bit 7 - BITBLT Quick Start.

Quick Start Mode

When BIT 7 is set, BITBLT starts automatically as soon as the BITBLT Destination Low register (Index 4) is written, unless automatic destination update is enabled for BITBLT, in which case the BITBLT starts automatically when the BITBLT Source Low register (Index 2) is written.

This mode permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bits in the BITBLT Control register operate as they were last written, and the BITBLT Activation bit is physically set and can be read back normally.

0 = BITBLT starts only when explicitly enabled.

1 = BITBLT starts automatically when destination register is written, or source register if destination update is enabled.

BIT 6 - BITBLT Update Destination.

Automatic Destination Update

A host doing multiple BITBLTs need only update those registers that change from one BITBLT to the next. Most BITBLT registers never change unless written by the host. The exceptions to this are the two BITBLT Destination registers (Index 4, 5) and the status bit in the BITBLT Control register (Index 0).

When bit 6 of this register is set, the BITBLT Destination registers are automatically updated at the end of each BITBLT operation to point to the rectangular region immediately to the right of the previous destination region. This is specifically aimed at improving text output operations. When the destination area is specified as linear rather than rectangular, the destination registers point to the location immediately past the previous destination area.

0 = Do not update destination on completion of BITBLT.

1 = Update destination on completion of BITBLT.

Bits (5:4) - BITBLT Pattern Select.

00 = Patterns are not used.

01 = 8X8 patterns are used for source.

1X = reserved for future expansion.

Bit 3 - BITBLT Monochrome Transparency.

0 = Monochrome transparency is not enabled.

1 = Monochrome transparency is enabled.

Bit 2 - BITBLT Transparency Polarity.

0 = Matching pixels are transparent.

1 = Matching pixels are opaque.

Bit 1

Reserved, must be set to 0.

Bit 0 - BITBLT Transparency Enable.

0 = Destination transparency is not enabled.

1 = Destination transparency is enabled.

11.2 SOURCE AND DESTINATION

The BITBLT Source Low and BITBLT Source High registers specify the source address for BITBLT operations. The BITBLT Destination Low and BITBLT Destination High registers specify the destination address. The high and low fields of each register pair are concatenated to form a 21-bit address pointing to the starting corner of the source or destination area.

The starting corner for source and destination will be either the top-left or bottom-right corner. The corner specified must be coordinated with the BITBLT Direction bit of the BITBLT Control register.

When the source and destination areas do not overlap, BITBLT can be started in either corner. When these areas overlap, the corner and direction must be selected to prevent parts of the source area from being overwritten by the destination array before they are copied.

When the BITBLT Update Destination bit in the BITBLT Control register is set, the host should not read the BITBLT Destination registers while a BITBLT is in progress, since these registers change just before the end of the operation.

When the BITBLT Quick Start bit in the BITBLT Control Register is set, writing these registers may automatically start BITBLT operations.

11.2.1 BITBLT Source Low, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:0	BITBLT Source Position Bits 11:0

11.2.2 BITBLT Source High, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:9	Reserved (Must Be 0)
8:0	BITBLT Source Position - Bits 20:12

11.2.3 BITBLT Destination Low, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:0	BITBLT Destination Position - Bits 11:0

11.2.4 BITBLT Destination High, Index 5

BIT	FUNCTION
15:12	0101 (Index)
11:9	Reserved (Must Be 0)
8:0	BITBLT Destination Position - Bits 20:12

11.3 ADDRESS MAPPING

The source and destination addresses are partially mode dependent. Addresses represent the character or pixel at the starting corner of the move, which may be the top left or bottom right corner.

11.3.1 Monochrome and Planar Modes

CPU ADDRESS	BITBLT REGISTER ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Location 0, bit 7 (left most pixel).
	1	Location 0, bit 6.
⇓	⇓	⇓
	7	Location 1, bit 0 (right most pixel).
A0001	8	Location 1, bit 7.
⇓	⇓	⇓
AFFFF ②	2M-1	Location 256K-1, bit 0 ①.

① Last location in a 1 MB system. Smaller memory configurations have fewer display memory locations.

② Not in the same memory page as A0001 above.

11.3.2 Packed Modes

CPU ADDRESS	BITBLT REGISTER ADDRESS	DISPLAY MEMORY LOCATION (ENTIRE BYTE)
A0000	0	Map 0, location 0, (left most pixel).
A0001	1	Map 1, location 0.
A0002	2	Map 2, location 0.
A0003	3	Map 3, location 0, (right most pixel).
A0004	4	Map 0, location 1, (left most pixel).
⇓	⇓	⇓
A0007	7	Map 3, location 1, (right most pixel).
⇓	⇓	⇓
AFFFF ②	1M-1	Map 3, location 256K-1. ①

① Last location in a 1 MB system. Smaller memory configurations have fewer display memory locations.

② Not in the same memory page as A0007 above.

The location referred to in sections 9.2.1 and 9.2.2 is the CPU address offset in bytes from the top of the display memory for any given mode. For example, where display memory starts at CPU address A0000H, location 123H would correspond to CPU address A0123H. Where display memory is divided into pages, the location is calculated as if all pages were consecutive. For example, with display memory pages of 64 Kbytes, location 10123H would correspond to CPU address A0123H in the second page of the display memory.

When the source or destination of a BITBLT operation is not a memory location, the corresponding pair of position registers are unused and may contain any value, except that the two or three low-order bits of the BITBLT Source Low register are still used to specify a source alignment of the data.

11.4 DIMENSIONS AND ROW PITCH

11.4.1 BITBLT Dimension X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11:0	BITBLT Dimension X *
* legal range is 1 to 2K pixels	

The BITBLT Dimension X register specifies the width of the rectangular region to be copied.

In Graphic Modes, this value is expressed in pixels.

In Text Modes, this value is expressed in the number of characters multiplied by eight (even though each character is stored using only two bytes).

11.4.2 BITBLT Dimension Y, Index 7

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BIT	FUNCTION
15:12	0111 (Index)
11:0	BITBLT Dimension Y *
* legal range is 1 to 2K pixels	

The BITBLT Dimension Y register specifies the height of the rectangular region to be copied.

In Graphic Modes, this value is the height of the region in pixels.

In Text Modes, this value is the height of the region in character rows.

11.4.3 BITBLT Row Pitch, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:0	BITBLT Row Pitch *
* In Packed Mode, the two low order bits of this field must be zero. In Planar Mode, the three low order bits must be zero.	

The BITBLT Row Pitch register specifies the linear offset from any location in a given row to the same location in the next row. This offset is in the same units as the source and destination fields to which it applies.

When both source and destination are rectangular areas, the BITBLT Row Pitch applies to both areas. When either or both are non-rectangular, the offset does not apply to that range.

11.5 FOREGROUND AND BACKGROUND COLORS

The BITBLT Foreground and Background Color registers specify 8-bit or 4-bit digital colors to be used when expanding monochrome source areas. The foreground color can also be specified as the source of a BITBLT to produce a filled rectangle.

BITBLT Foreground Color, Index A

BIT	FUNCTION
15:12	1010 (Index)
11:8	Reserved
7:0	BITBLT Foreground Color *
* In Planar modes, only bits 3:0 are used to specify a color.	

BITBLT Background Color, Index B

BIT	FUNCTION
15:12	1011 (Index)
11:8	Reserved
7:0	BITBLT Background Color *
* In Planar modes, only bits 3:0 are used to specify a color.	

11.6 MAP AND PLANE MASK

The BITBLT Mask register controls both Plane and Map Masks used in BITBLT.

The BITBLT Map Mask field specifies a four-bit mask that prevents data in the specified maps from being updated. This map is needed for BITBLT in all text modes to prevent font data from being overwritten in a character-attribute move and vice versa, and VGA mode F. It can also be used in VGA modes 4, 5 and 6 for partial hardware support. Additionally, it can be used in VGA modes D, E, 10, 11 and 12 and extended Planar modes as a Plane Mask if desired.

The BITBLT Plane Mask field specifies an eight-bit mask that prevents data in the specified planes from being updated. It is useful in VGA Mode 13 and extended Packed modes when Plane Masking is desired.

BITBLT Mask - VGA, Index E

BIT	FUNCTION
15:12	1110 (Index)
11:8	Reserved
7:0	BITBLT Plane Map Mask Mode *
* In Planar Modes, only bits 3:0 are used.	

BITS 7:0	BITBLT PLANE MASK
XXXX XXX0	Plane 0 Disabled
XXXX XXX1	Plane 0 Enabled
⇓	
0XXX XXXX	Plane 7 Disabled
1XXX XXXX	Plane 7 Enabled

BITS 3:0	BITBLT MAP MASK
XXX0	Map 0 Disabled
XXX1	Map 0 Enabled
⇓	
0XXX	Map 3 Disabled
1XXX	Map 3 Enabled

11.7 RASTER OPERATIONS

The BITBLT Raster Operation register specifies a bitwise logical operation to be performed on the source and destination fields. This field is always active and must be loaded with the appropriate value even when a simple source copy is to be performed.

BITBLT Raster Operation, Index 9

BIT	FUNCTION
15:12	1001 (Index)
11:8	BITBLT Raster Operation, abcd in Table 11-3.
7:0	Reserved

All BITBLT operations apply a source color, pattern or area to a destination area. The result written to the destination is a logical function of the source and destination pixels for each location.

The Raster Operation code is defined as follows:

The Source (S) and Destination (D) form a 2-bit value. The Truth Table (Table 11-2) defines the results of the two operands, Source and Destination, for the desired function.

The four 1-bit results of the Truth Table for the desired operation in the form "abcd" form the Raster Operation code (Table 11-3). The "a" is defined as the high-order bit of the code.

While the Raster Operation code represents a 2-input operation, both inputs are not always relevant in the operation. For example, codes 0011 (source copy) and 1100 (inverted source copy) are independent of the destination field.

Arithmetic operations are not supported.

S D	Result
0 0	a
0 1	b
1 0	c
1 1	d

TABLE 11-2.
BITBLT TRUTH TABLE

abcd	Function	abcd	Function
0000	Zero	1000	NOR
0001	AND	1001	XNOR
0010	S•$\overline{D}$	1010	Inv Dest
0011	Src	1011	S+$\overline{D}$
0100	$\overline{S}$•D	1100	Inv Src
0101	Dest	1101	$\overline{S}$+D
0110	XOR	1110	NAND
0111	OR	1111	One

TABLE 11-3.
RASTER OPERATION CODE

11.8 PATTERNS

The WD90C31A has a special mode to accelerate the copying of 8 by 8 source patterns. In this mode, an 8 by 8 full-color or monochrome pattern can be repetitively applied to a large destination area in an efficient manner.

To perform a pattern copy, the host first writes the 8 by 8 pattern to display memory in a linear fashion, usually to a non-visible location, depending on the current addressing mode, as described in Sections 11.7.1 and 11.7.2. The host then loads the BITBLT Source registers, with the location of the pixel within the pattern corresponding to the top-left corner of the destination region. The BITBLT Pattern Select field of the BITBLT Control register must be set to 8 by 8 patterns.

To specify a monochrome pattern, the host must write a color pattern in the current mode, planar or packed, and then use the control registers to specify a single plane of the source to be used.

11.8.1 BITBLT Pattern Storage - Monochrome and Planar Modes

In planar mode, the 8 by 8 source pattern must be stored in display memory in a 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

REGISTER ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data.
n* to n + 7	All maps, top row of 8X8 pattern.
n + 8 to n + 15	All maps, second row of 8X8 pattern.
⇓	
n + 56 to n + 63	All maps, bottom row of 8X8 pattern.
n + 64 to ..	Any data.
* 'n' must be a multiple of 64	

11.8.2 BITBLT Pattern Storage - Packed Modes

In packed mode, the 8 by 8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region and the pattern wraps to the right and down from that point.

REGISTER ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data.
n*	Top row of 8X8 pattern, left most pixel.
n + 1	Top row of 8X8 pattern, second pixel.
⇓	
n + 7	Top row of 8X8 pattern, right most pixel.
n + 8	Second row of 8X8 pattern, left most pixel.
⇓	
n + 63	Bottom row 8X8 pattern, right most pixel.
n + 64	Any data.
* 'n' must be a multiple of 64	

11.9 MONOCHROME TO COLOR EXPANSION

When the source of a BITBLT operation is monochrome, each 0 in the source region is replaced with the specified background color, while each 1 is replaced with the foreground color. All other processing options, including masks and raster operations, remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination will be filled with the foreground color, subject to masks, raster operations and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available since the transparency color registers are in use.

11.10 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data extracted in this manner is replicated to each plane or map as if it had been read from the memory.

Monochrome data can also be extracted from host data when the BITBLT source is the I/O port. In this case, each 32-bit word written to the I/O port is treated in the same manner as if it had been read from display memory. Alternately, the host may send monochrome data through the I/O port that does not require extraction (see section 11.14).

To extract a single plane from a color source field, the BITBLT Transparency Color register should be loaded with FFH (all ones), while the BITBLT Transparency Mask register should be loaded with a 0 in the map or plane position to be extracted, and a 1 in all other positions.

Monochrome data is usually extracted as a specific bit of each 4-bit or 8-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color 1, with all other colors returning a monochrome 0.

When the Monochrome Transparency bit is set in the BITBLT Control register, monochrome source pixels of 0 do not modify the destination, regardless of any selected raster operation.

The Transparency Enable and Polarity bits in this register have no effect on monochrome data extraction.

11.11 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually transparent, with the rest being opaque. Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of source and destination, in which a source field of zero is effectively a transparent color, since when OR'ed with the destination, it does not change.

Color destination transparency is supported by the WD90C31A, in addition to the more limited monochrome transparency described elsewhere.

11.11.1 BITBLT Transparency Color, Index C

BIT	FUNCTION
15:12	1100 (Index)
11:8	Reserved
7:0	BITBLT Transparency Color *
* In Planar Modes, only the four low-order bits are used.	

The BITBLT Transparency Color register specifies an 8-bit or 4-bit color to be used as the transparency color.

11.11.2 BITBLT Transparency Mask, Index D

BIT	FUNCTION
15:12	1101 (Index)
11:8	Reserved
7:0	BITBLT Transparency Mask *
* In Planar Modes, only the four low-order bits are used.	

The BITBLT Transparency Mask register specifies an 8-bit or 4-bit mask for use in comparison against the transparency color.

The pixels of the destination are compared against the Transparency Color under control of the Transparency Mask. Each bit of the Transparency Mask that is a 1 makes the corresponding bit of the Transparency Color a "don't care".

The BITBLT Transparency Enable bit of the BITBLT Control register (Index 1) specifies whether Color Transparency is enabled or disabled. The BITBLT Transparency Polarity bit specifies whether pixels matching the Transparency Color are considered transparent. In this case, only destination pixels matching the transparent color can be overwritten, or transparent, and only non-matching pixels can be overwritten.

11.12 FILLED RECTANGLES

Filled rectangles can be drawn very efficiently by the BITBLT hardware. A filled rectangle is simply a BITBLT with a source of a fixed color. To draw a filled rectangle, the host sets the Source Format field in the BITBLT Control register (Index 0) to "fixed color" and the Foreground Color register (Index A) to the desired fill color. A source address is not required. All other BITBLT options are available in a normal manner.

11.13 SYSTEM MEMORY TO DISPLAY MEMORY OPERATIONS

To copy data from system memory to display memory, the host may specify the source of a BITBLT as a system I/O location rather than display memory. In this case, display memory reads come from the 32-bit readback latch written by the host.

After starting the BITBLT operation, the host writes a series of doublewords to the readback latch. This 32-bit register is accessed by two consecutive writes to the 16-bit BITBLT I/O port, with the low-order word of this register written first. This port may also be accessed by two 8-bit writes as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a source read is required and data from the host is unavailable, the WD90C31A suspends the BITBLT operation until data becomes available. Similarly, when the host attempts to write the register before previous data in it has been processed, the WD90C31A holds off the host.

Conceptually, the 32 bits written by the host exactly replace the 32 bits that would have been read from the display memory. Just like the destination, the source may have any alignment. The two or three low-order bits (Packed or Planar Mode) of the BITBLT Source Low register (Index 2) specify the alignment of the source region. The other bits of the BITBLT Source Low register may have any value. That is, the pixel of the source word pointed to by those low-order bits corresponds to the first pixel of the destination.

NOTE

Source writes from the host are always performed in 32-bit groups, however the data is written to a 16-bit port. Therefore the host must always perform two 16-bit I/O writes at a time to the port, even when the remaining width is less than four or eight pixels.

Just like display memory, no source doubleword from the host may straddle two lines of the destination.

11.14 DISPLAY MEMORY TO SYSTEM MEMORY OPERATIONS

To copy data from display memory to system memory, the host may specify the destination of a BITBLT as a system I/O location rather than display memory. In this case, display memory writes are replaced by writes to a 32-bit register read by the host.

This 32-bit register is accessed by two consecutive reads of the 16-bit BITBLT I/O port. The low-order word of this register is read first. This port may also be accessed by two 8-bit reads, as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a destination write is required and the host has not read data from the previous write, the WD90C31A suspends the BITBLT operation until the host catches up. Similarly, when the host attempts to read the register before data is available, the WD90C31A holds off the host.

Conceptually, the 32 bits read by the host exactly match the 32 bits that would have been written to the display memory. Unlike outputting to display memory, the destination is always doubleword aligned, that is, the first pixel of the source corresponds to the first pixel of the destination.

NOTE

Source reads by the host are always performed in 32-bit groups, however the data is read from a 16-bit port. Therefore the host must always perform two 16-bit I/O reads at a time from the port, even when less than 32 bits remain in the current line.

Just like display memory, no destination doubleword to the host may straddle two lines of the source.

11.15 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION

The host may transfer monochrome data from system memory to display memory and, in the process, expand it to any two colors or any one color plus transparent.

To accomplish this, the host sets the BITBLT Source Select field in the BITBLT Control register (Index 0) to "System I/O Location" and the BITBLT Source Format field to "Monochrome From Host". If transparency is desired, the Monochrome Transparency bit is also set. The BITBLT Foreground and Background Color registers (Index A and B) may also be set.

The host then issues a series of 16-bit I/O writes to the BITBLT I/O port which are expanded to eight 4-bit pixels. The remaining eight high-order bits are ignored. In Packed Mode, the four low-order bits are expanded to four 8-bit pixels and the remaining 12 bits are ignored.

The low-order bits of the BITBLT Source register (Index 2) work as in other system-to-video memory transfers.

No source word may straddle two lines of the destination. All other BITBLT options work normally in this mode.

12.0 EXTENDED REGISTER ACCESS

All of the WD90C31A enhanced functions are controlled by one or more extended registers, most of which are above and beyond standard VGA registers.

Enhanced functions are controlled by indexed register blocks. Each indexed register block can contain up to sixteen 12-bit indexed registers. The 4-bit register index is written, along with the 12-bit data field, to form a 16-bit word.

Access to VGA-type registers is described in section 5. This section only describes the access to indexed register blocks.

12.1 ACCESSING INDEXED REGISTERS

To write to one or more indexed registers within any register block, that register block must first be selected by loading its address into the Register Block Pointer field of the Index Control register. This causes the selected register block to appear at the Register Access port.

A 16-bit word is then written to the Register Access port. The four high-order bits specify the Index of the individual register being written, while the 12 low-order bits are the data to be written. Additional registers within the same register block may then be written without re-selecting that register block.

To read one or more indexed registers within a register block, the address of that register block is written to the Register Block Pointer Field, bits 7:0 of the Index Control Register at Port 23C0H/23C1H and the desired starting register to be read within the block is written to the Register Index Field, bits 11:8 of this register. Both fields are set with the same 16-bit write. This causes the selected register to appear at the Register Access port located at 23C2H/23C3H.

A 16-bit word is then read from the Register Access port. When reading an indexed register, the value returned contains the index of the register in the four high-order bits.

If the Auto-Increment Disable bit in the Index Control register is reset, consecutive reads to the Register Access port will return consecutively indexed registers within the same register block. Registers are read in ascending order through register F (the 16th register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Addressing a non-existant register results in zeros being returned in the 12-bit data field.

If the Auto-Increment Disable bit is set, consecutive reads return the same indexed register.

GLOBAL PORT MAP	
Port 23C0H	Index Control register (low byte)
Port 23C1H	Index Control register (high byte)
Port 23C2H	Register Access Port (low byte)
Port 23C3H	Register Access Port (high byte)
Port 23C4H	BITBLT I/O Port
Port 23C5H	BITBLT I/O Port
Port 23C6H	Reserved
Port 23C7H	Reserved

12.2 INDEX CONTROL REGISTER PORT 23C0H/23C1H

Except for bit 13 which is a read only, the Index Control register is a read/write register which controls reads and writes to indexed registers blocks.

BIT	FUNCTION
15:14	Reserved
13	Invalid register block. This bit is read only
12	Auto-increment disable
11:8	Register Index.
7:0	Register Block Pointer

Bits (15:14)

Reserved

Bit 13 - Invalid Register Block (read only).

0 = Currently addressed register block exists on this device.

1 = Currently addressed register block does not exist on this device.

Bit 12 - Auto-increment Disable.

0 = Consecutive reads return consecutive indexed registers.

1 = Consecutive reads return the same indexed register.

Bits (11:8) - Register Index

The index of the desired starting register to be read within a block is written to these bits. When read, these bits return the index of the next register to be read.

Bits (7:0) - Register Block Pointer

To read one or more indexed registers within a register block, the address of that register block is written to this field.

REGISTER BLOCK MAP	
Pointer	**Register Access Port Accesses**
00	System Control registers
01	BITBLT registers
02	Hardware Cursor registers

12.3 INTERRUPT STATUS REGISTER, SYSTEM CONTROL REGISTERS BLOCK - INDEX 0 T-52-33-45

Interrupt status information is provided by the Interrupt Status register in the System Control Register block. This register returns information as to which part of the WD90C31A caused an interrupt.

Reading this register does not reset any interrupts. Resetting of each interrupt is handled independently.

Unassigned interrupts are returned as zeroes.

BIT	FUNCTION
15:12	0000 (Index)
11	Interrupt 10 active
⇓	
8	Interrupt 7 active
7	High when at least one of the interrupts 10 through 7 is active
6	Interrupt 6 active
⇓	
1	Interrupt 1 active
0	Any interrupt is active

12.3.1 Global Interrupt Map

Interrupt	Meaning
1	VGA interrupt
2	BITBLT interrupt

13.0 APPLICATION AND PROGRAMMING NOTES

13.1 USE OF THE HARDWARE CURSOR IN 16-BIT PER COLOR MODE

The hardware cursor, while not specifically designed for hi-color mode operation, can still be used with certain limitations in that mode.

The hardware cursor is unaware of the existence of hi-color mode but can still be used by specifying two adjacent 2-bit pixel codes for each high-color cursor pixel. A transparent hi-color pixel would be specified using two adjacent transparency codes (1010), while a "color" hi-color pixel would usually be specified using adjacent primary and secondary color codes, such as 0100. The desired 16-bit cursor color would then be split between the 8-bit primary and 8-bit secondary color registers. Inversion is also available as 1111 but the results might not be visually desirable.

This limits the effective maximum cursor width in hi-color mode to 32 pixels. Further, the cursor origin and position are defined in terms of 8-bit, not the displayed 16-bit, pixels. Therefore, these values should be horizontal multiples of two.

Secondary and auxiliary color registers may be used to create additional cursor colors by mixing cursor codes within a 16-bit pixel region. It is important to keep in mind the effects of inversion in systems that use one bit to switch between false color and hi-color modes on a pixel-by-pixel basis.

13.2 BITBLT IN VGA MODES 4, 5, AND 6

VGA modes 4, 5 and 6 are partially supported by the WD90C31A. Since these modes are not commonly used in Windows, the additional hardware required to support the even/odd scan line offset technique employed in these modes is not supported.

However, a BITBLT operation in these VGA modes can often be broken up into two or three BLT operations, each of which operates on a contiguous area of memory.

When the vertical offset between source and destination is an even number of rows, the desired operation can be broken into two BITBLTs, one for the even rows and one for the odd rows. This requires careful consideration of the register parameters, especially the BITBLT Dimension Y register.

Where the offset is an odd number of rows, it may still be possible to break up the operation into only two BITBLTs, provided there is no overlap between the source and destination regions. This is because information is being swapped between the even and odd scan line regions.

Where source and destination do overlap, it may be possible to use a scratch space in off-screen memory and break up the operation into three BITBLTs.

Another possibility is to break up a BITBLT into a series of one-line high operations that can be referred to as Line-BLTs. In this manner, a BITBLT may be simulated by the driver as a series of Line-BLTs.

13.3 BITBLT OPERATIONS IN TEXT MODE

BITBLT acceleration is available in VGA Text Modes. Text Mode BITBLTs generally consist of moving only character and attribute data (in maps 0 and 1), while leaving the font data (in maps 2 and 3) alone. The BITBLT mask is set to prevent update to those maps. For this reason, Planar (not Packed) Mode must be used. Similarly, the BITBLT mask can be set to move only character data, or only font data.

Each display memory location consists of four bytes: one character, one attribute and two font plane bytes that are not part of the character but happen to fall in the same location as the character, but on maps 2 and 3. In planar mode, this is a space of eight pixels. Therefore, the source and destination of a character BLT must be multiples of eight. The X dimension is the number of character columns to be copied times eight but the Y dimension is simply the unmultiplied number of character rows. The row pitch is set to the number of characters per row times eight.

13.4 USE OF BITBLT IN 16-BIT PER COLOR MODE

The BITBLT hardware can be used in 16-bit per color hi-color mode with a few changes and a few limitations.

Hi-color BITBLTs should be performed in packed mode, remembering that each hi-color pixel takes up two adjacent normal packed pixels. The BITBLT Source and Destination registers should point to the first byte of the respective regions. Generally, the values in these register pairs are double the corresponding values for 256-color mode.

In a right-to-left BITBLT in hi-color mode, the source and destination values must point to the second byte of each pixel.

The BITBLT dimensions are twice the number of pixel columns, but the correct number of pixel rows. The Row Pitch register contains eight times the number of bytes between rows on the screen. Linear source and destination operate normally.

Monochrome to color expansion or plane masking is not generally useable. Raster operations are available, but often produce undesired results. Similarly, color transparency is seldom useable.

Pattern fills are available, however, the effective pattern is only 4 by 8 pixels. This may be useable where an 8 by 8 pattern is identical in the left and right halves.

Filled rectangles are available in two ways. First, where the desired fill color is the same in the high and low bytes (generally meaning all black or all white), rectangle fill can be used normally.

In the more general case of filling a rectangle with an arbitrary 16-bit color, the host should create a 4 by 8 pattern of the fill color and use pattern fills to create the rectangle.

Host I/O BITBLTs can operate normally be treating each 16-bit hi-color pixel as two adjacent, aligned 8-bit packed mode pixels.

Care should be used when implementing the use of one of the 16 bits in a hi-color pixel as a switch between false color and hi-color, since no mask exists to protect this flag bit during operations.

13.5 USE OF BITBLT FOR ARBITRARY SIZED PATTERNS

While the BITBLT hardware specifically accelerates 8 by 8 patterns, patterns of arbitrary size can be accelerated by use of the BITBLT, although to a lesser degree.

To copy an arbitrary size pattern to a destination region, the pattern should be stored in non-visible memory as a rectangular region, not a linear strip. With destination update enabled, one copy of the pattern should be BITBLT'ed to the top-left corner of the destination. The BITBLT source is then set to point to the pattern now in the destination region.

A series of BITBLTs are then performed, each doubling the width of the patterned area, simply by adjusting the X Dimensions register. (The last of this series of BITBLTs just fill out the destination region.)

A new series of BITBLTs is then performed, taking the horizontally complete pattern and doubling it in height each time. The destination update should be turned off, and the destination must be set for each new BITBLT. The final BITBLT will probably not be a double of the previous one since it just fills out the region.

13.6 PATTERNS BUILT ON-SCREEN

Normally, a pattern to be used in BITBLT is stored in a non-visible portion of display memory. This requires an aligned strip of 32 or 64 bytes to be available.

When this is not available, it may still be possible to perform a pattern BITBLT by placing the pattern in the last line of the destination region. This can be done if the raster operation is a source copy or source inversion, and if the destination region can accommodate the specified aligned strip on a single line. This technique is possible because each row of the pattern is read at the beginning of the row in which it is used, and the pattern is not overwritten until it after it has been read for the last time.

Where a full strip is unavailable, the destination can be broken up into a series of line-BLTs, with a one line pattern, requiring only 4 or 8 aligned bytes, placed on each destination line before the

BITBLT is started for that line. This method is substantially slower than other pattern BITBLTs.

A possible alternative is to write the pattern in a visible portion of memory, first saving the underlying area and restoring it after the BITBLT. This temporary usage of a visible region might be visible to the user. This might be reduced by using the last line of the destination and saving and restoring only those regions that overhang the destination.

13.7 USE OF PATTERNS IN TEXT MODE

Patterns may be in text mode to quickly set character and/or attribute bytes in a rectangular area to a common value. A pattern space must be created containing eight consecutive copies of the four-byte area consisting of the character, the attribute and two Font Map bytes, all aligned to a 64-pixel boundary. The BITBLT map mask is then used to protect the font maps. This pattern should be created in off-screen memory.

If an off-screen pattern space is not available, one may be created on screen by loading an aligned group of eight character/attribute pairs within the destination area, then pointing to that as the pattern source.

If the first character of the destination space happens to be on an 8-byte boundary (such as the conventional top of screen) then, as long as the destination is at least eight characters wide, only the first character/attribute pair must be loaded, and the BITBLT operation creates its own pattern as it goes along. This also works if the destination is less than eight characters wide, but is still wider than it is high.

If this is not possible, then the operation can be performed one character row at a time, loading the first character of each row to be used as an on-screen pattern.

Filled rectangles have a very limited application in text mode, but could be used to clear out a section of a font map or to set a section of a character or attribute map to all zeroes or all ones. Different values are not easily set in this manner because, in order to protect the font maps, planar mode, rather than packed mode, must be used.

13.8 SUPPORT FOR KANJI CHARACTERS

The BITBLT hardware can efficiently support generation of Kanji characters. The common implementation of Kanji characters calls for a character box of 28 by 28 pixels, with five possible scoring lines for each character box. T-52-33-45

Kanji characters are best drawn in two passes. The first pass draws the characters while erasing any old ones. The second pass adds the score lines.

The Kanji font should be stored in non-visible display memory. Since the font is monochrome, multiple characters can be stored one per plane, one under the other. The color compare registers are used to switch between banks of characters stored on different planes.

A group of 32 special characters is generated along with the font, consisting of all possible combinations of scoring lines.

The dimension registers are loaded with the size of the character box. Foreground and background colors are set as desired. Destination update and quick BITBLTs are enabled.

For each character row, the source and destination registers are set to the beginning of the row, and monochrome expansion is enabled. A series of quick BITBLTs is performed, one per character, by loading the source address of each desired character. If a font-plane change is required before any character, it is done before loading the source registers, since these start the BITBLT automatically.

After the character row is complete, the destination registers are reset to the beginning of the row. Monochrome transparency is enabled, and a second pass is done over the character drawn to add score lines as needed, one special score-line character per Kanji character.

Where a Kanji character requires no score lines, either a BITBLT of a special "blank" score-line character is performed, or the destination registers may be updated to skip the position. The driver may add additional intelligence to skip entire character rows or parts where score lines are not required.

13.9 VCLK AND MCLK RATIO FOR HIGH RESOLUTION MODES

Support of the high resolution modes such as 800X600X32K or 1024X768X256 at 70 or 72 Hz refresh rates is one of the strong features of the WD90C31A. However, careful attention needs to be paid to the MCLK and VCLK frequencies used in supporting these modes.

As described earlier, an internal FIFO interleaves CPU accesses and display refresh cycles. The FIFO is filled with data from the memory using the MCLK, and is emptied with a VCLK to produce the screen refresh. In high resolution modes, the video data output rate is very high due to the high VCLK frequencies involved. The MCLK for such modes must be appropriately high to keep the memory data fetch rate in balance with the output rates. If a slower MCLK is used, a FIFO underflow will occur and will appear on the screen as white dashes in random places or as a shimmer.

The WD90C31A is designed so that a ratio of 1.6 or less must be maintained between the VCLK and MCLK. When the VCLK is 65 MHz or less, MCLK of 45 MHz or more can be used. However, MCLK of 50 MHz must be used for the high resolution modes with high refresh rates. Note that the DRAM rated at 60 ns or faster must also be used for the MCLK of 50 MHz so that the worst case memory timing specs are met.

	800X600X32K NON-INTERLACED 70 Hz	1024X768X256 NON-INTERLACED 60 Hz	1024X768X256 NON-INTERLACED 70 Hz	1024X768X256 NON-INTERLACED 72 Hz
VCLK MHz	75	65	75	77.25
MCLK MHz	50	45	50	50
VCLK/MCLK RATIO	1.5	1.44	1.5	1.55
DRAM SPEED	60 ns	70 ns	60 ns	60 ns

TABLE 13-1. VCLK AND MCLK RATIO FOR HIGH RESOLUTION MODES

14.0 WD90C31A INTERFACES

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The WD90C31A applications section is divided into various interfaces: processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes and technical briefs at the end of this document will supplement the information provided in this section.

Figure 14-1 highlights the WD90C31A interfaces.

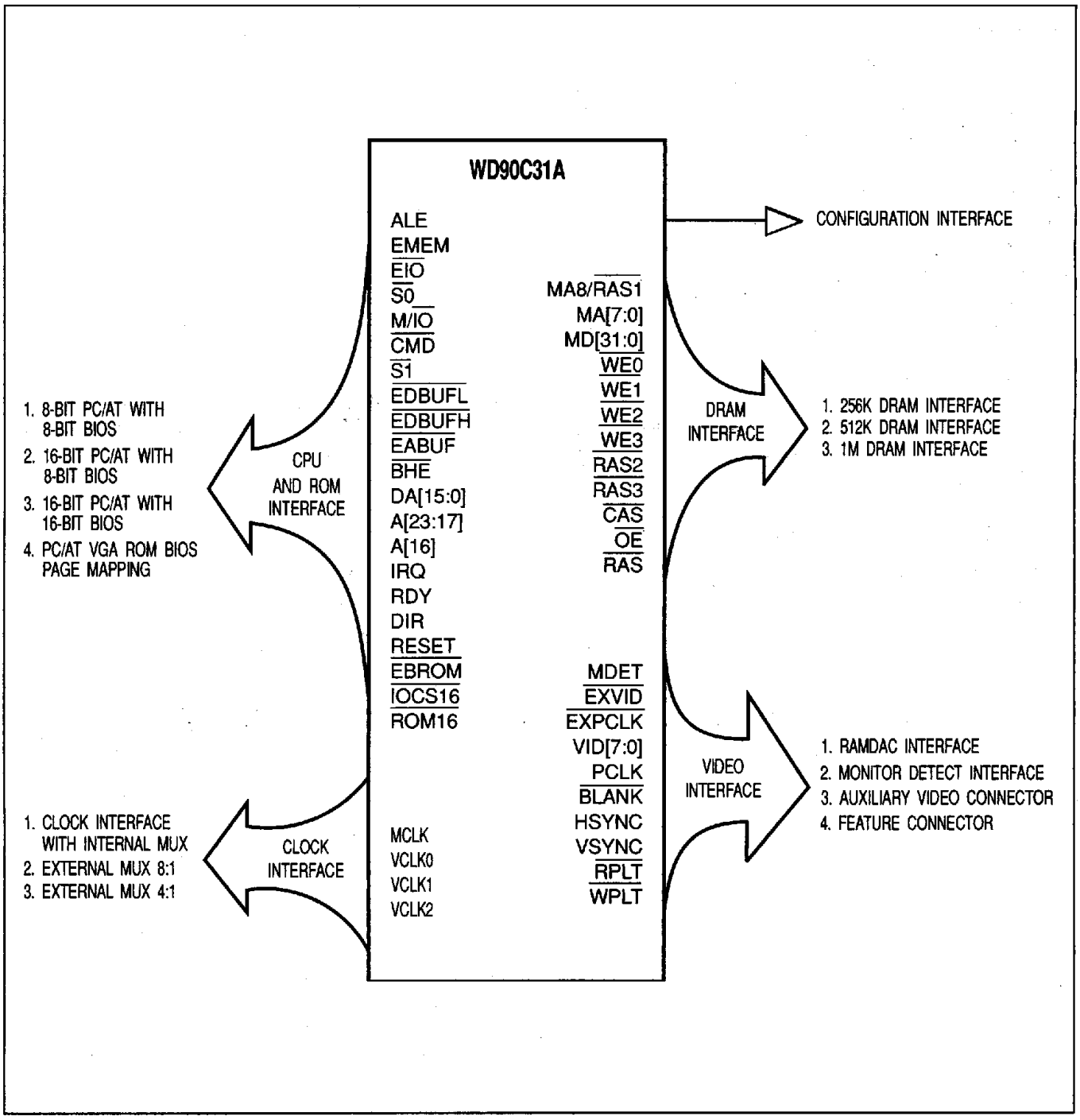

FIGURE 14-1. WD90C31A INTERFACES

14.1. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 14-2 shows a block diagram of the WD90C31A with eight-bit PC/AT interface using eight-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

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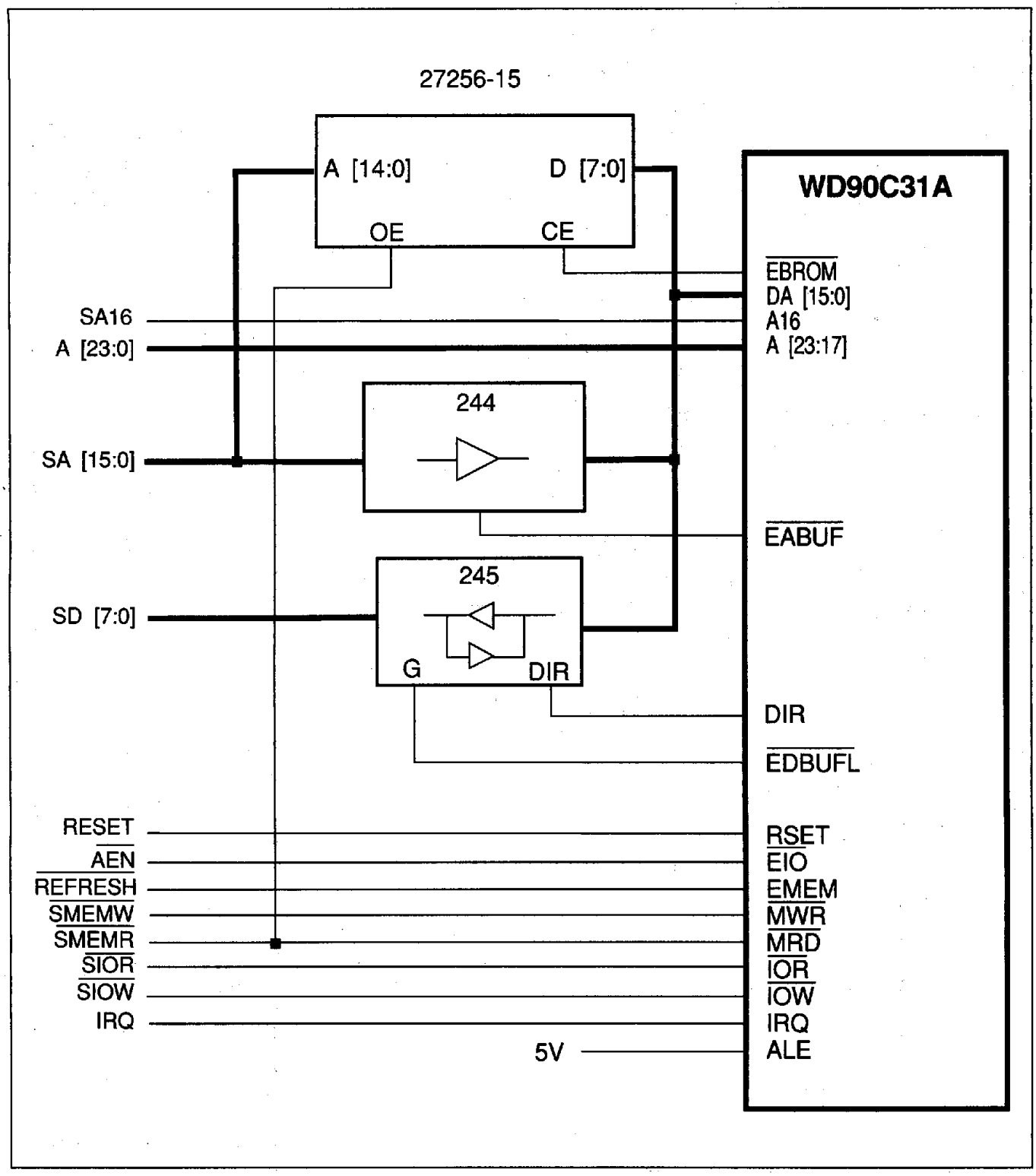

FIGURE 14-2. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

14.2 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 14-3 illustrates 16-bit PC/AT interface with an eight-bit BIOS using WD90C31A. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown.

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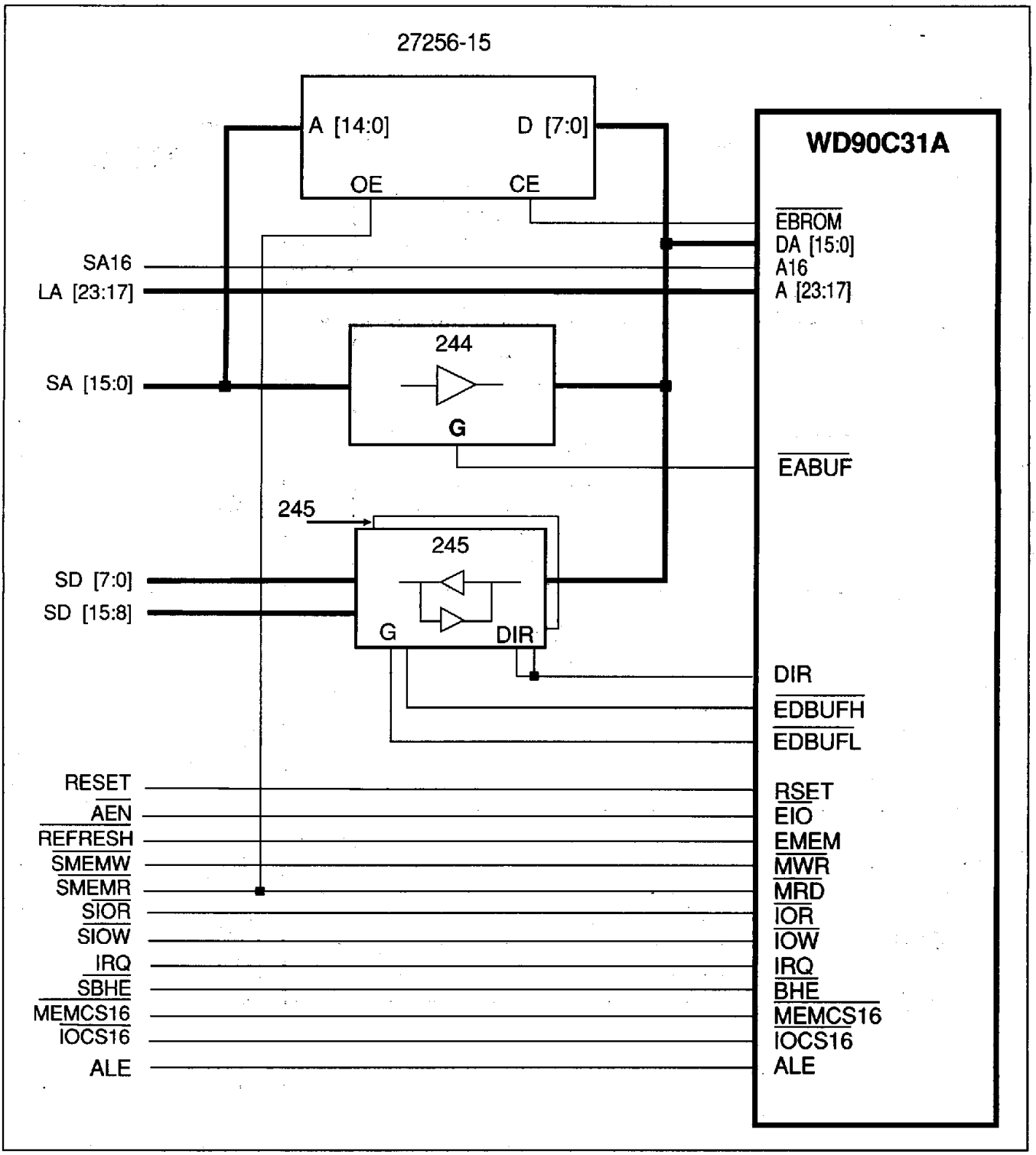

FIGURE 14-3. 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

14.3 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

Figure 14-4 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C31A. The system data bus SD(15:0), address and data bus buffers are presented. Also, MEMCS16 implementation is limited to certain bus speeds since SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 14-6 for 286-based systems.

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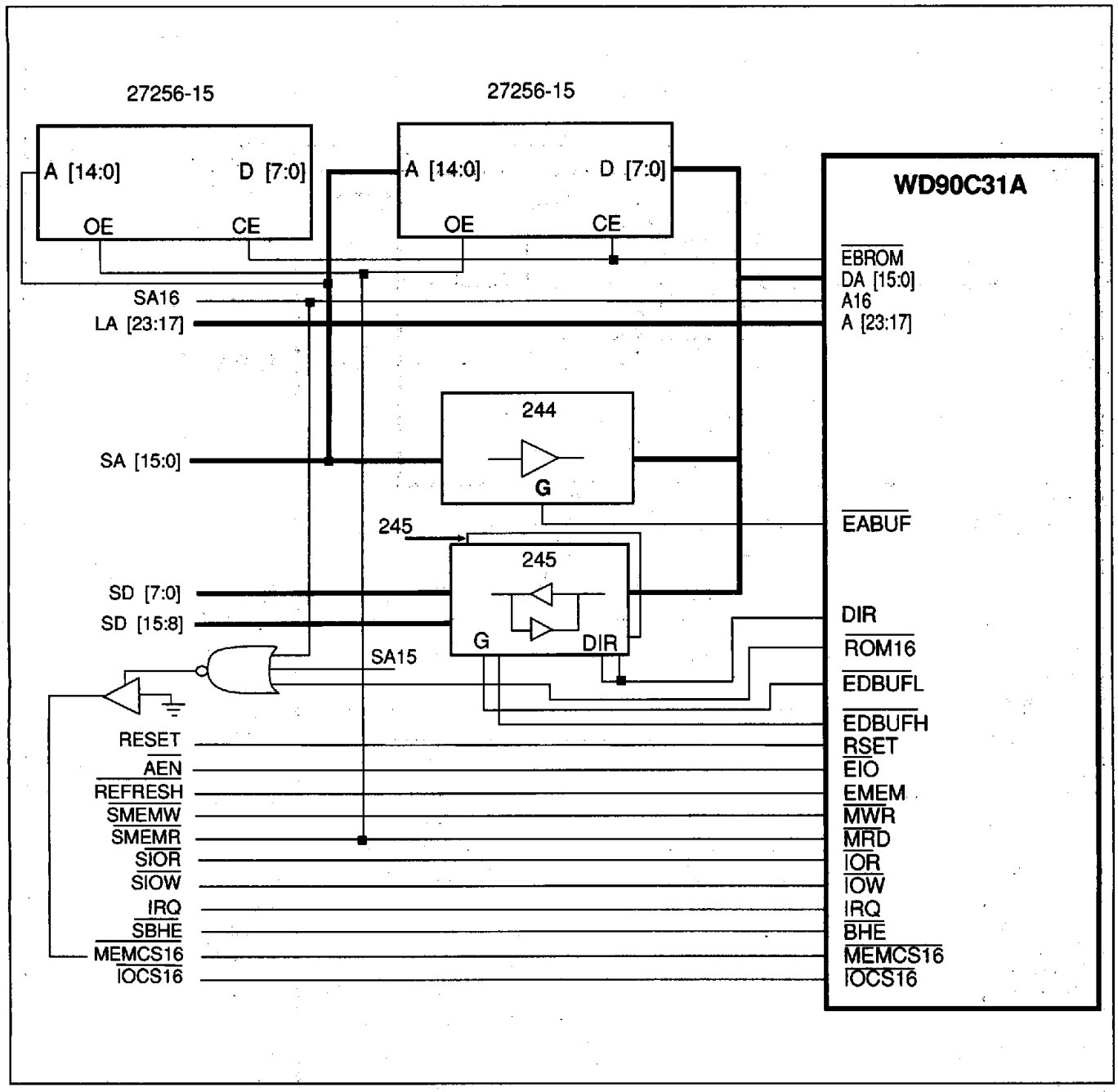

FIGURE 14-4. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

14.4 16-BIT MICRO CHANNEL

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Figure 14-5 illustrates the WD90C31A and 16-bit Micro Channel interface. 3C3.D0 is output of Port 3C3H Bit 0 VGA Subsystem Enable Register.

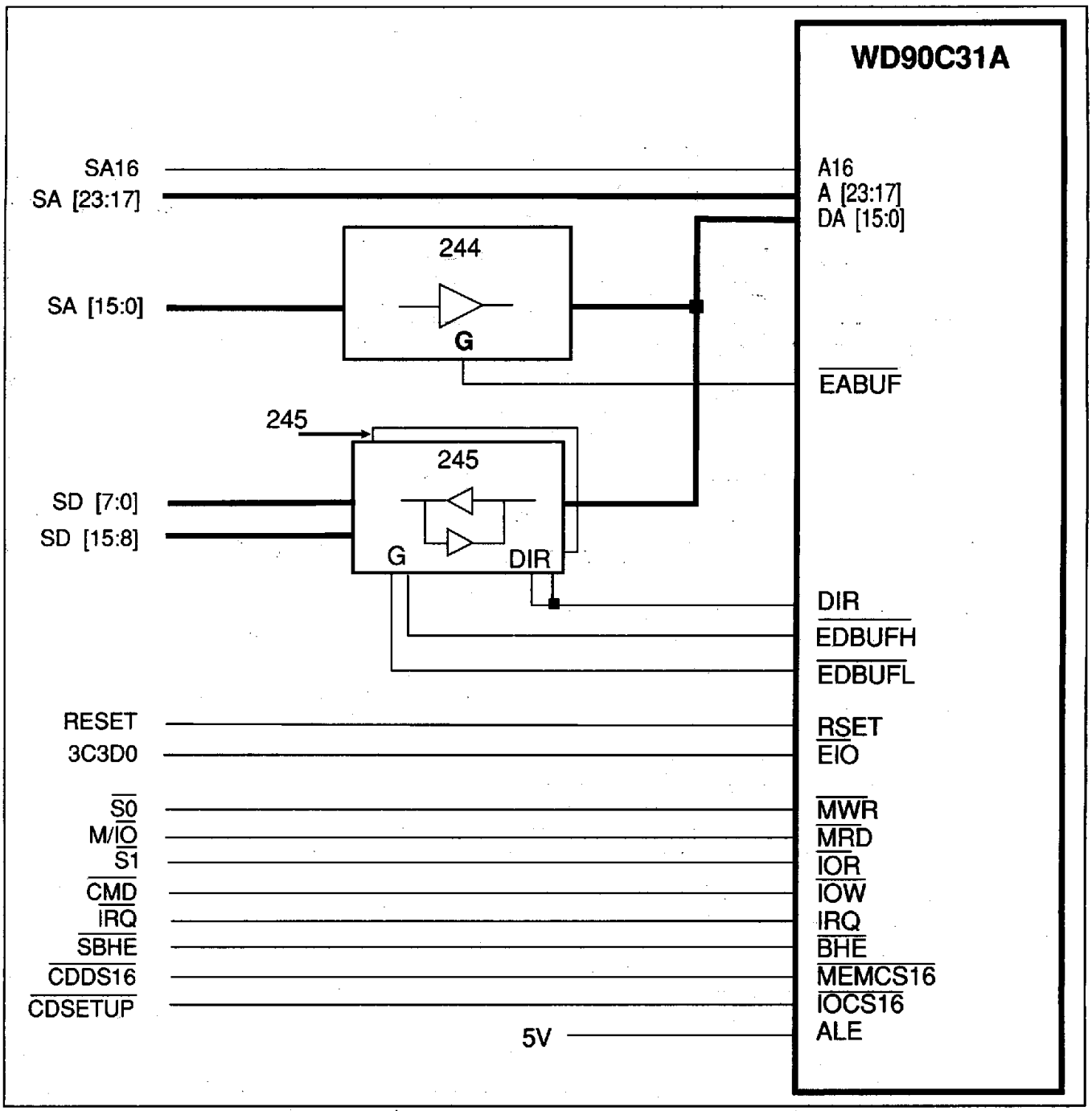

FIGURE 14-5. 16-BIT MICRO CHANNEL INTERFACE

14.5 WD90C31A INTERFACE FOR 286 OR 386 BASED SYSTEMS

To interface the WD90C31A with an 8-bit and 16-bit AT bus, additional external logic is required as shown in the upper half of Figure 14-6. To interface the WD90C31A with only a 16-bit AT bus, the implementation illustrated in the lower half of Figure 14-6 is recommended.

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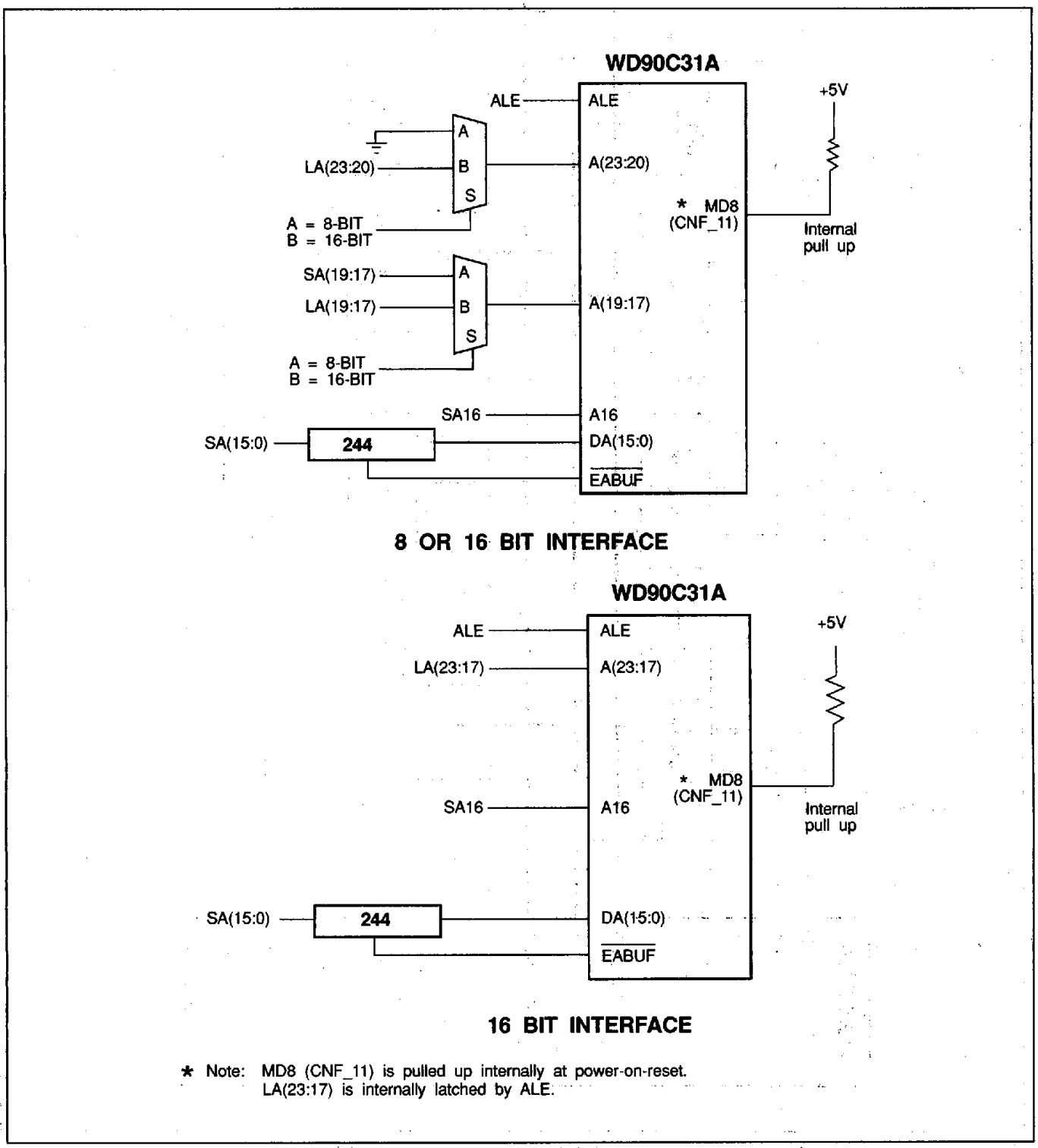


FIGURE 14-6. WD90C31A INTERFACE FOR 286 OR 386-BASED SYSTEMS

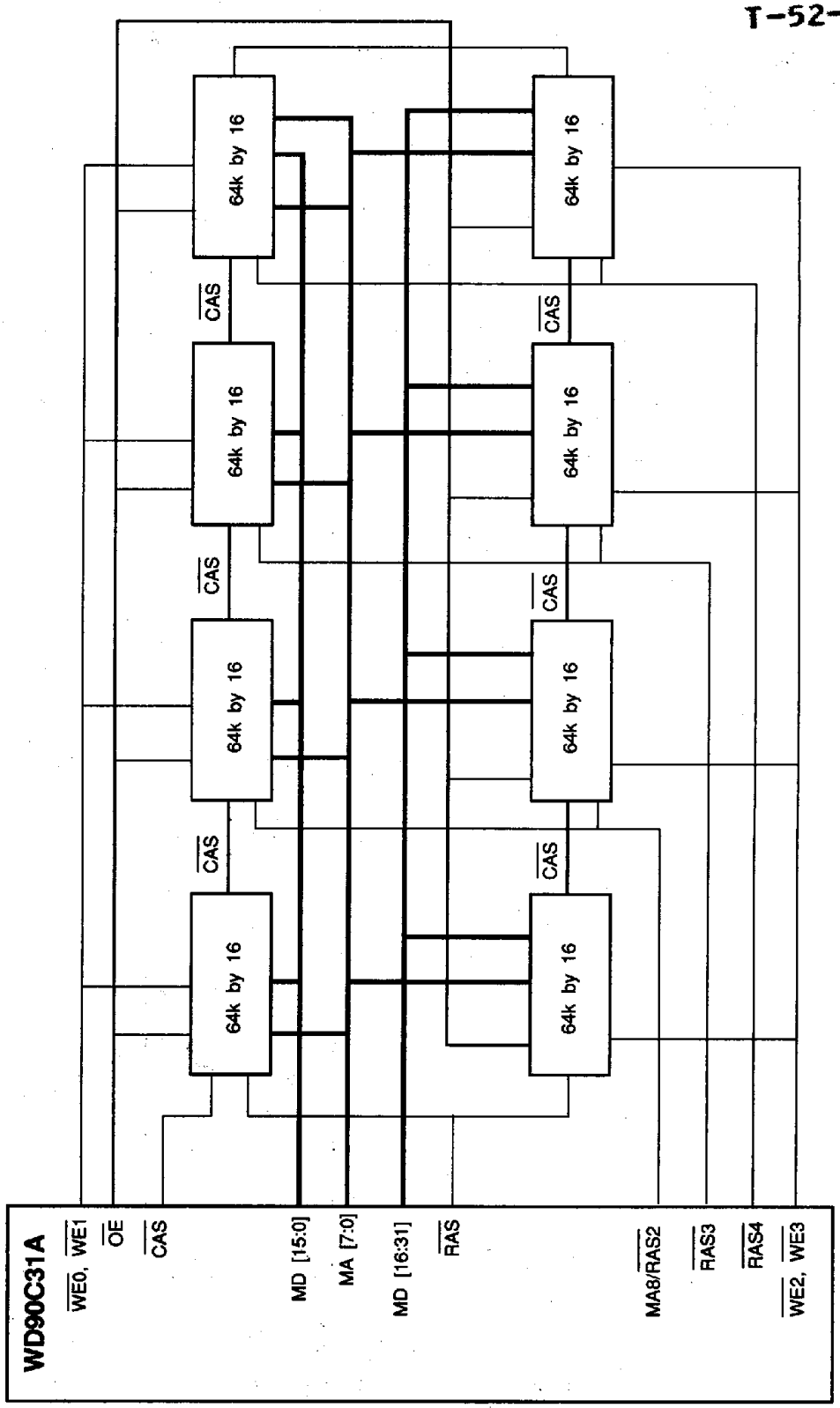
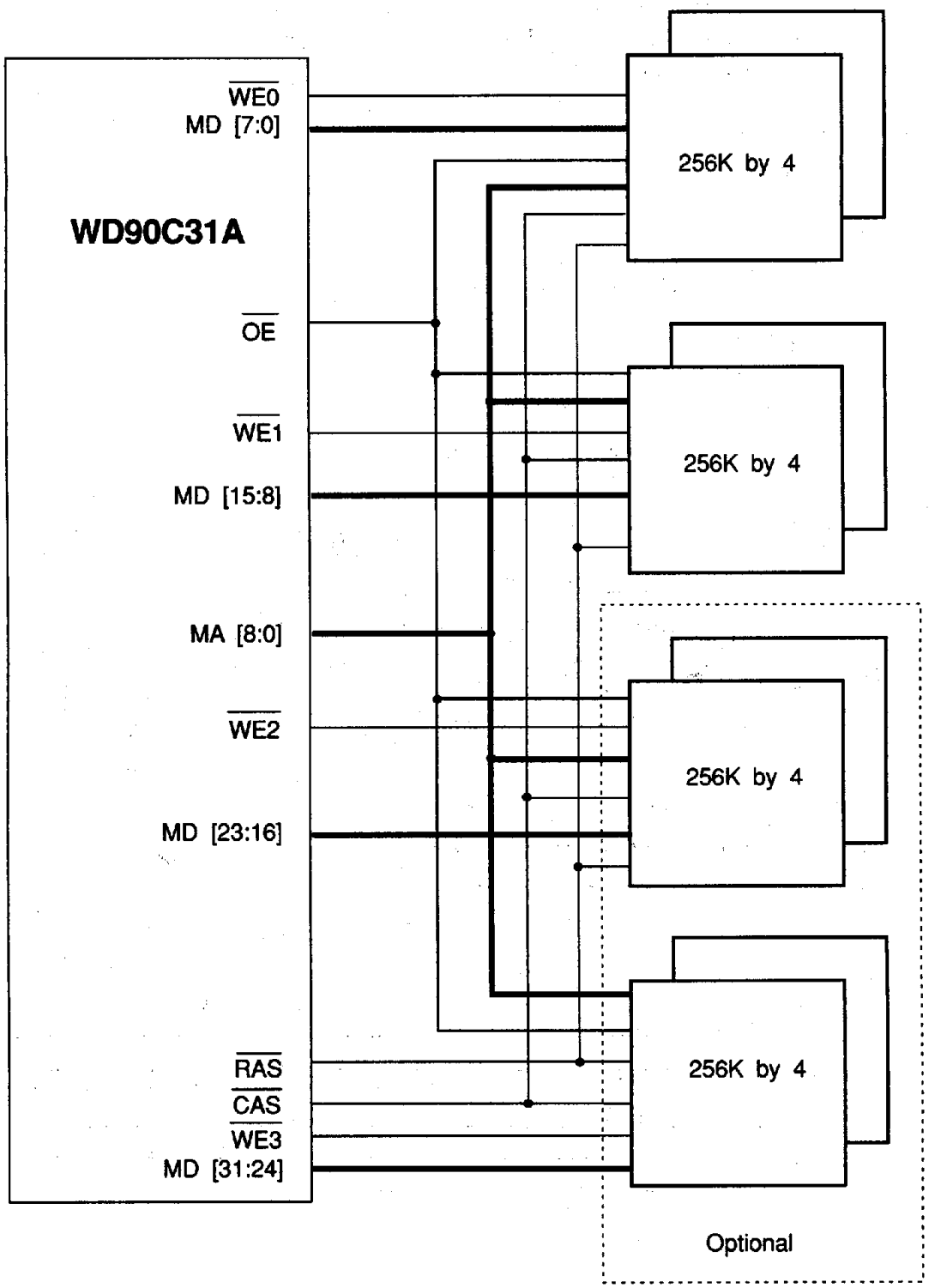


FIGURE 14-7. TWO, FOUR OR EIGHT 64K BY 16 DRAM INTERFACE



Note: Only MD [15:0] will be used if four 25K by 4 DRAMs are installed.

FIGURE 14-8. FOUR OR EIGHT 256K BY 4 DRAM INTERFACE

14.6 WD90C31A WITH RAMDAC INTERFACE

Figure 14-9 illustrates the WD90C31A and RAMDAC (WD90C50) interface block diagram for analog monitors.

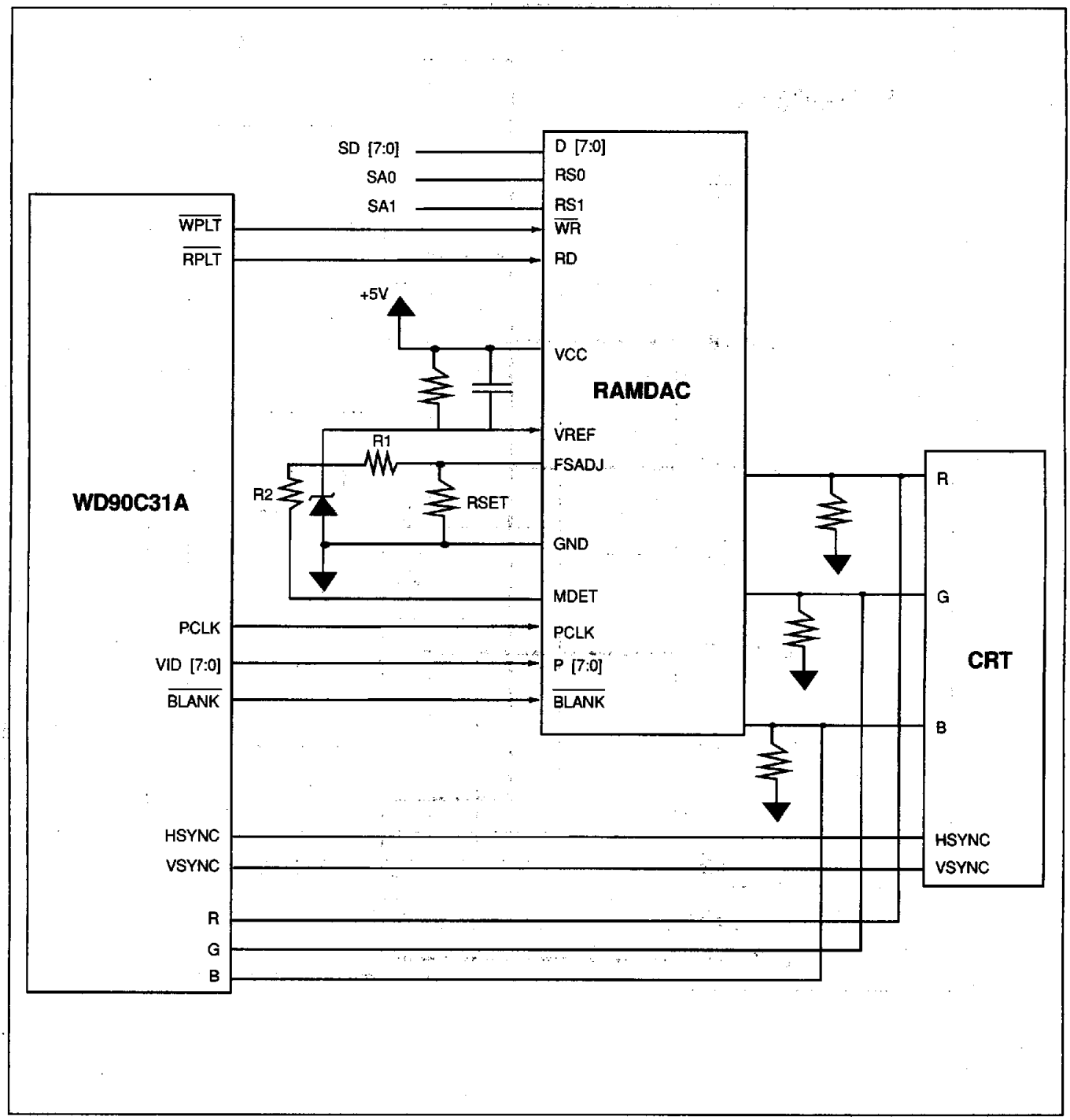


FIGURE 14-9. WD90C31A WITH RAMDAC INTERFACE

14.7 WD90C31A AND TTL MONITOR CONNECTIONS

Figure 14-10 illustrates the WD90C31A and TTL monitor connections

NOTE

- VGA/TTL switch may be used to disable HSYNC and VSYNC for analog or TTL Video connector.
- MD(15:12) may also be connected as the EGA switches if desired. See PR Register and Pinout sections for more detail.
- For AT applications using the WD90C31A, install the IRQ9 resistor.
- Transistor 2N2222A is used to emulate a monochrome and color display connection.

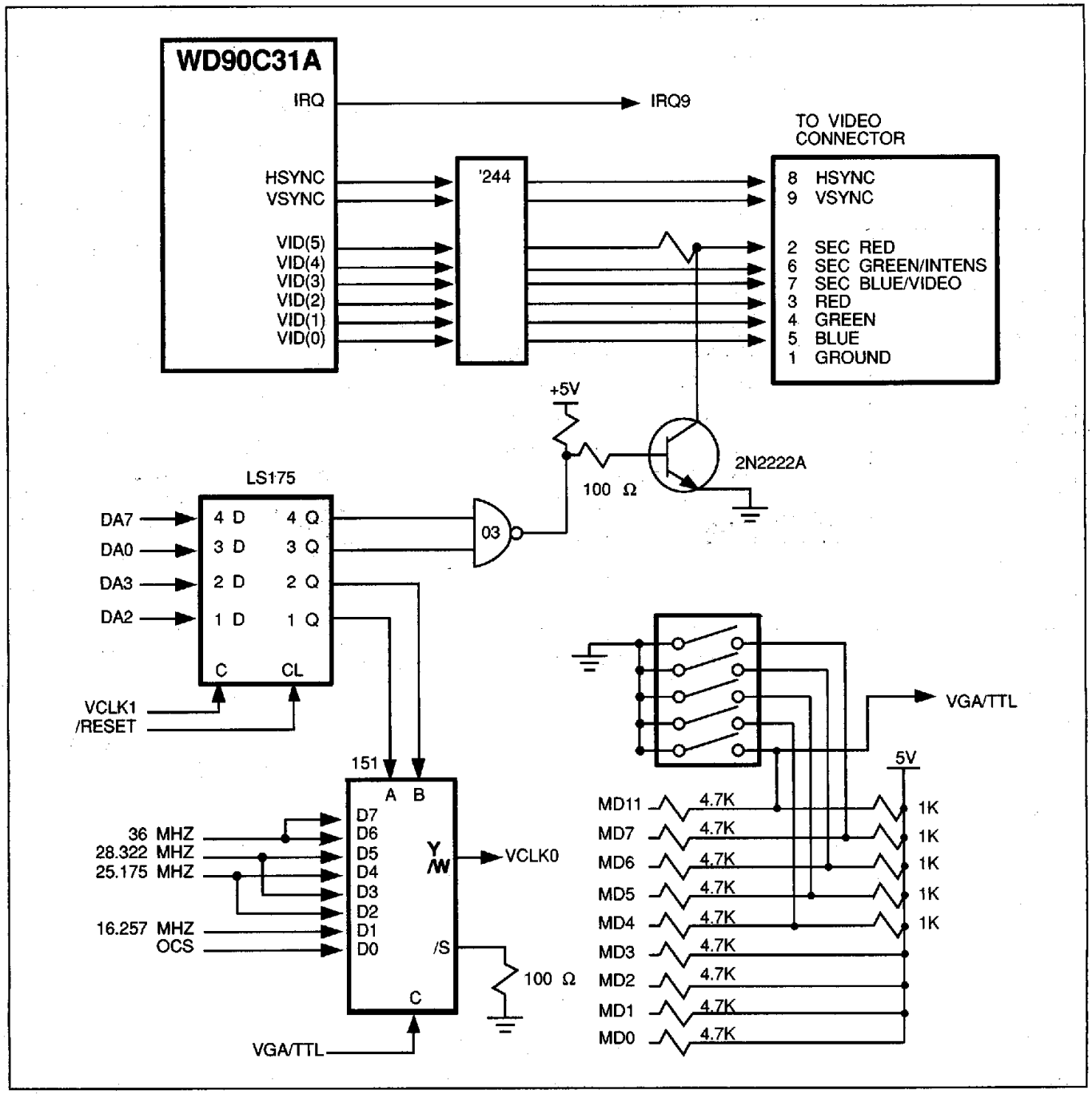


FIGURE 14-10. WD90C31A AND TTL MONITOR CONNECTIONS

14.8 CLOCK INTERFACE

Figure 14-11 illustrates the WD90C31A with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H Bit 3 and Bit 2 and is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C31A signal pins (VCLK1, VCLK2) inputs.

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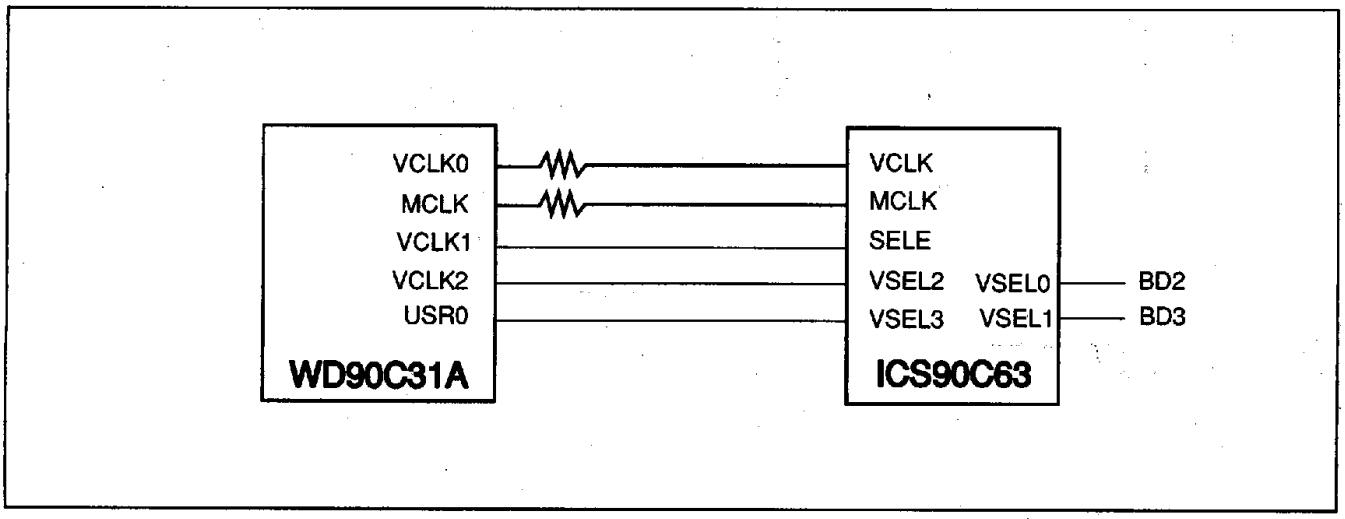

FIGURE 14-11. CLOCK INTERFACE

15.0 SHADOW REGISTER IMPLEMENTATION

The Shadow register has been implemented for some of the CRT Controller registers. The Shadow register makes it possible to have one CRT Controller register that may be written to and read from at all times by application programs without changing CRT Controller timing. The actual CRT Controller timing registers are initialized and locked while using the Shadow register for compatibility.

The shadowed registers can be locked by writing "XXXXX101" to PR1A(3?5.3D). This lock overrides any other locks. Then setting PR1A Bit 3 to 1 selects the Shadow register for read.

HORIZONTAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.00	7:0	Group 0	Horizontal Total
3?5.02	7:0	Group 0	Start Horizontal Blanking
3?5.03	4:0	Group 0	End Horizontal Blanking
3?5.05	7	Group 0	Bit 6 of EHB
3?5.04	7:0	Group 0	Start Horizontal Retrace
3?5.05	4:0	Group 0	End Horizontal Retrace
3?5.03	6:5	Group 0	Display Enable Skew
3?5.05	6:5	Group 0	Horizontal Retrace Skew
VERTICAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.06	7:0	Group 2	Vertical Total
3?5.07	5,0	Group 2	Bits 9, 8 of VT
3?5.10	7:0	Group 3	Vertical Retrace Start
3?5.07	7,2	Group 2	Bits 9, 8 of VRS
3?5.11	3:0	Group 3	Vertical Retrace Start
3?5.15	7:0	Group 3	Start Vertical Blank
3?5.07	3	Group 2	Bit 8 of SVB
3?5.09	5	Group 2	Bit 9 of SVB
3?5.16	7:0	Group 3	End Vertical Blank

Note:
Group 0: Registers will be locked if PR3(5) = 1 or 3?5.11 bit 7 = 1
Group 2: Registers will be locked if PR3(0) = 1 or 3?5.11 bit 7 = 1
Group 3: Registers will be locked if PR3(0) = 1
Group 0, 2, 3 registers listed above will be locked if PR1A = "xxxxx101", regardless of the contents of PR3.
The Horizontal Display End and the Vertical Display End registers are not shadowed.

TABLE 15-1. SHADOW REGISTER IMPLEMENTATION

16.0 SIGNATURE ANALYZER

A signature analyzer is designed for use in the WD90C31A. The primary purpose of the signature analyzer is to aid in IC test and board level test. The signature analyzer allows the video output path to be included in diagnostics. Signature analysis is a method of compressing large amounts of data to be compared. Each video frame (video data and mode dependent) has a unique signature capable of detecting single bit errors.

16.1 DESCRIPTION

The basis of the signature analyzer is a Linear Feedback Shift Register (LFSR). The inputs to the LFSR tap onto the VID[7:0] output of the IC. The signal path of the video outputs is not modified by adding the signature analyzer. A block diagram is shown below. The primary variables in designing a signature analyzer are length of the shift register and the feedback terms to be used. The length will affect the probability of masking an error. The chance of masking an error is approximately $1/2^n$, where n is the length of the shift register. A 16-bit signature register is used on the WD90C31A. Selection of an optimal feedback polynomial will depend on the type of errors expected. The CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$) has been implemented on the WD90C31A. It was modified for multiple inputs as shown in the block diagram.

16.2 OPERATION

The signature analyzer is designed to collect signature of the VID[7:0] outputs over one vertical frame. The signal path of the VID[7:0] has not been altered. The signature analyzer register (LFSR) is enabled at the falling edge of the internal VSYNC (before polarity selection) if the start bit is high. The following rising edge of the VSYNC signal will disable the LFSR. In the case of interlaced operation, signature is collected from the beginning of the even field to the end of the odd field. The signature analyzer contains a 4-bit control register PR19 (address 3?5.3F). Power-up-reset clears this register to 00H. This register has both read and write locks. The read lock originates from PR10 Bits 7 and 3. The write lock originates from PR10 Bits 2 through 0. PR10 also serves as the lock for other registers.

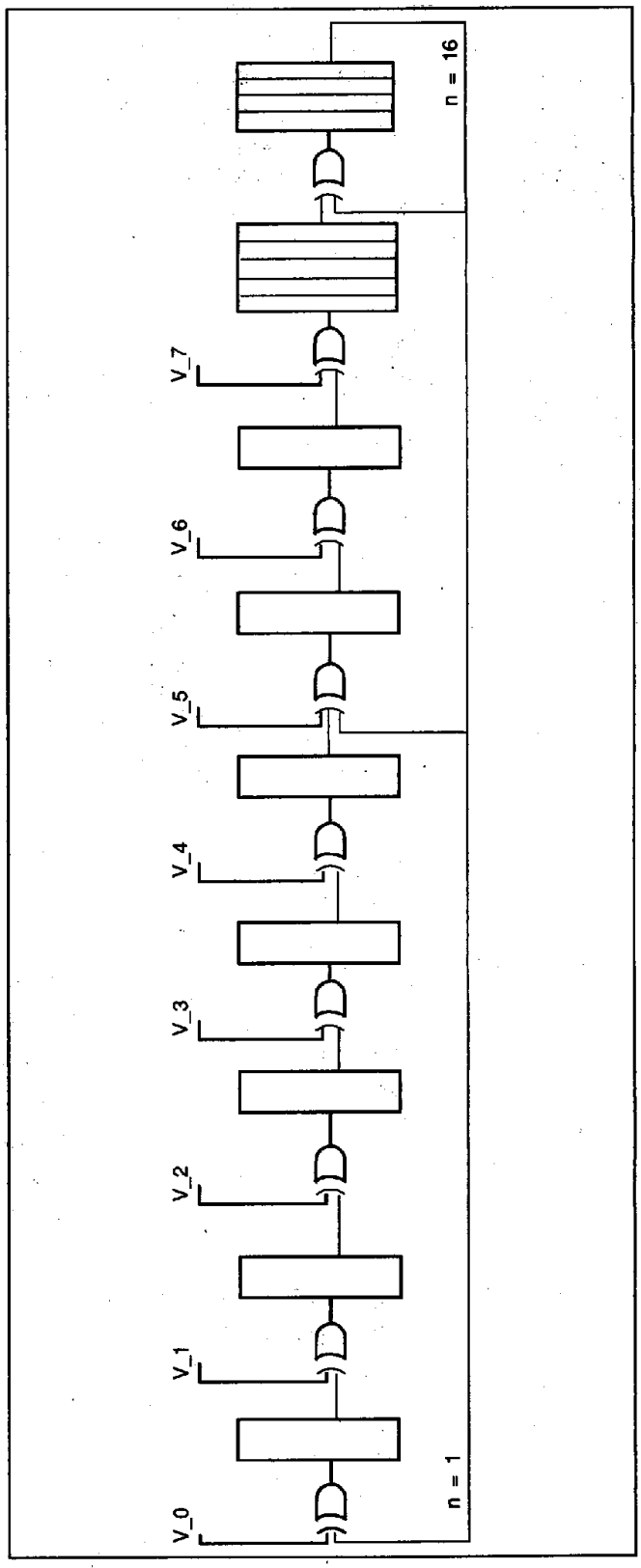

FIGURE 16-1. LINEAR FEEDBACK SHIFT REGISTER

BIT	FUNCTION	READ/WRITE	DESCRIPTION
0	Start/status	R/W	Writing "1" to this bit position enables the signature analyzer to collect a signature at the falling edge of the next vertical sync pulse. This bit may be read to check status if the read lock is disabled. 1: Busy 0: Finished or not enabled
1	Clear	R/W	Writing "0" to this bit position preloads the LFSR with 0001H. This bit must be set to operate the signature analyzer. 1: Normal operation 0: Preload LFSR
2	Disable Video Input	R/W	This bit is used in a self-test mode. A fixed signature will be generated for any given mode (independent of video memory data). 1: Disable video inputs 0: Enable video inputs
3	Lock Read Port	R/W	This bit must be set in order to read the signature and status. 1: Enable read of LFSR (addresses 3?5.20 and 3?5.21). 0: Disable reads of LFSR

TABLE 16-1. CONTROL REGISTER PR19

The following programming steps highlight the sequence that will setup, check, and read the signature.

Step 1) 85H-> 3?5.29; release control register (PR10) read and write lock

Step 2) 00H-> 3?5.3F; clear signature analyzer

Step 3) 03H-> 3?5.3F; enable signature analyzer to collect signature

Step 4) read 3?5.3F; check status for busy
if LSB = 1 repeat step 4
if LSB = 0 signature is collected, proceed to step 5

Step 5) OAH-> 3?5.3F; enable signature analyzer read port

Step 6) read 3?5.20; read low byte of signature

Step 7) read 3?5.21; read high byte of signature

Step 8) 00H-> 3?5.3F; clear signature analyzer and lock read port.

17.0 I/O MAPPING

17.1 INTRODUCTION

The I/O Mapping is designed for use by the WD90C31A to isolate board level solder defects. The I/O Mapping allows the WD90C31A to enter a test mode where all pins in the WD90C31A are divided into various groups as inputs and outputs. The path from PCB trace through input, WD90C31A, output and PCB trace can be treated as a simple path. With test points on the board, a test for opens and shorts can be performed quickly.

17.2 TEST MODE

There are four requirements that must be met for the WD90C31A to enter the I/O mapping test mode:

- $\overline{\text{MWR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CONFIGURATION SWITCH 2 is HIGH (MD2 is pulled high)
- RESET is HIGH

If both $\overline{\text{MWR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in AT machines and a reserved condition in PS/2 machines. Configuration switch 2 high ensures that the WD90C31A is in AT mode. Reset controls a transparent latch as shown in Figure 17-1. Reset can be dropped low to latch the test mode. All the bidirectional pins are forced to input mode when in the test mode.

17.3 PIN GROUPINGS

The following pin groupings are done to minimize routing overhead of I/O pin mapping. Multiple input pins in a row are ORed together to the output shown in the following table. The input column lists the input pin number(s) along with the signal name(s). The output column lists the output pin number along with the pin name that corresponds to the input pin(s).

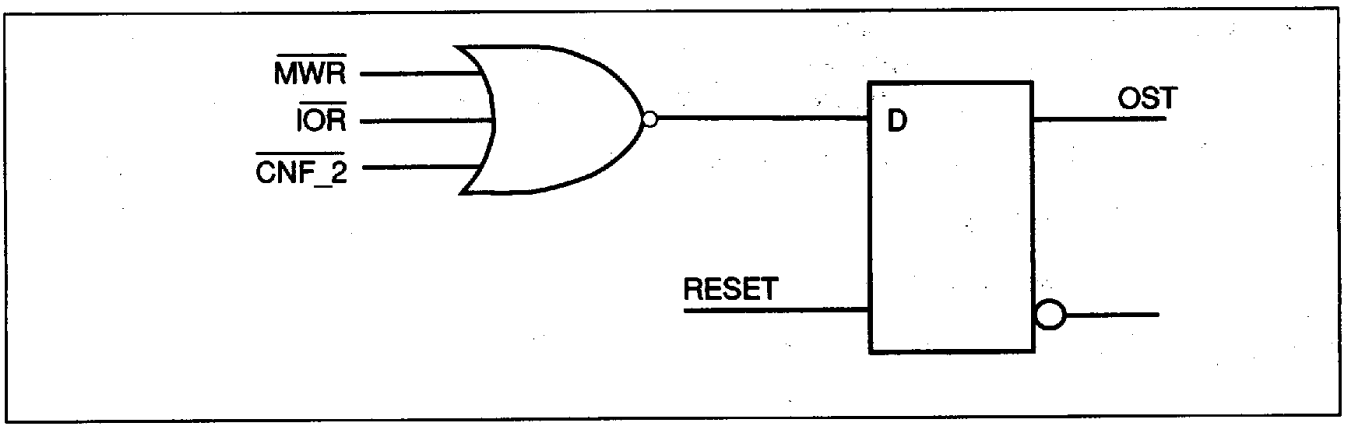

FIGURE 17-1. TEST MODE CIRCUIT

INPUT PINS		OUTPUT PINS	
PIN	NAME	PIN	NAME
P1	MDET	P123	VID4
P4	MCLK	P124	VID5
P8	MD31	P125	VID6
P9	MD30	P126	VID7
P10 + P13	MD29 + MD26	P2	USR1
P11 + P14	MD28 + MD25	P3	USR0
P12	MD27	P7	$\overline{WE3}$
P15	MD24	P6	$\overline{OE}$
P19 + P24 + P31	MD23 + MD18 + MD15	P27	$\overline{RAS4}$
P20	MD22	P16	$\overline{WE2}$
P21 + P25 + P32	MD21 + MD17 + MD14	P28	$\overline{RAS3}$
P22 + P26 + P33	MD20 + MD16 + MD13	P30	$\overline{WE1}$
P23 + P34 + P43	MD19 + MD12 + MD6	P39	$\overline{RAS}$
P35 + P38	MD11 + MD8	P52	$\overline{WE0}$
P36 + P41	MD10 + $\overline{CAS}$	P53	MA0
P37 + P42 +P46	MD9 + MD7 + MD3	P54	MA1
P44 + P47	MD5 + MD2	P55	MA2
P45 + P49	MD4 + MD0	P56	MA3
P48 + P62	MD1 + A17	P57	MA4
P63 + P68	A18 + A22	P59	MA6
P64 + P69 + P72	A19 + A23 + $\overline{BHE}$	P58	MA5
P65	A20	P60	MA7
P66 + P73 + P86	A21 + ALE + $\overline{ROM16}$	P61	MA8
P70 + P77 + P80	$\overline{IOCS16}$ + $\overline{IOW}$ + RESET	P74	IRQ
P90 + P93 + P95 P79 + P89	$\overline{DA15}$ + DA12 + DA10 + $\overline{MWR}$ + A16	P71	$\overline{MEMCS16}$
P75 + P78 + P88	$\overline{EMEM}$ + $\overline{MRD}$ + $\overline{EDBUFH}$	P82	IOCHRDY

TABLE 17-1. WD90C31A PIN SCAN MAP FOR 132-PIN PACKAGE

INPUT PINS		OUTPUT PINS	
PIN	**NAME**	**PIN**	**NAME**
P85 + P92	$\overline{EIO}$ + DA13	P81	$\overline{0WS}$
P91 + P94	DA14 + DA11	P87	$\overline{EBROM}$
P76 + P77	$\overline{IOR}$ + $\overline{IOW}$	P100	DIR**
P96 + P101	DA9 + DA7	P115	$\overline{RPLT}$
P97 + P102	DA8 + DA6	P114	$\overline{WPLT}$
P98 + P103	$\overline{EABUF}$ + DA5	P113	$\overline{HTL}$
P104 + P109	DA4 + $\overline{EDBUFL}$	P112	$\overline{BLANK}$
P105 + P107	DA3 + DA1	P110	VSYNC
P106 + P108	DA2 + DA0	P111	HSYNC
P128	VCLK0	P118	PLCK
P129	VCLK1	P119	VID0
P130	VCLK2	P120	VID1
P131	$\overline{EXPCLK}$	P121	VID2
P132	$\overline{EXVID}$	P122	VID3

Note:
A "+" in the input column indicates an OR function for the test input pins only.
** This mapping for DIR output is valid only during RESET HIGH.

TABLE 17-1. WD90C31A PIN SCAN MAP FOR 132-PIN PACKAGE (Continued)

Refer to Table 4-3 for the comparable pin number for a 144-pin package.

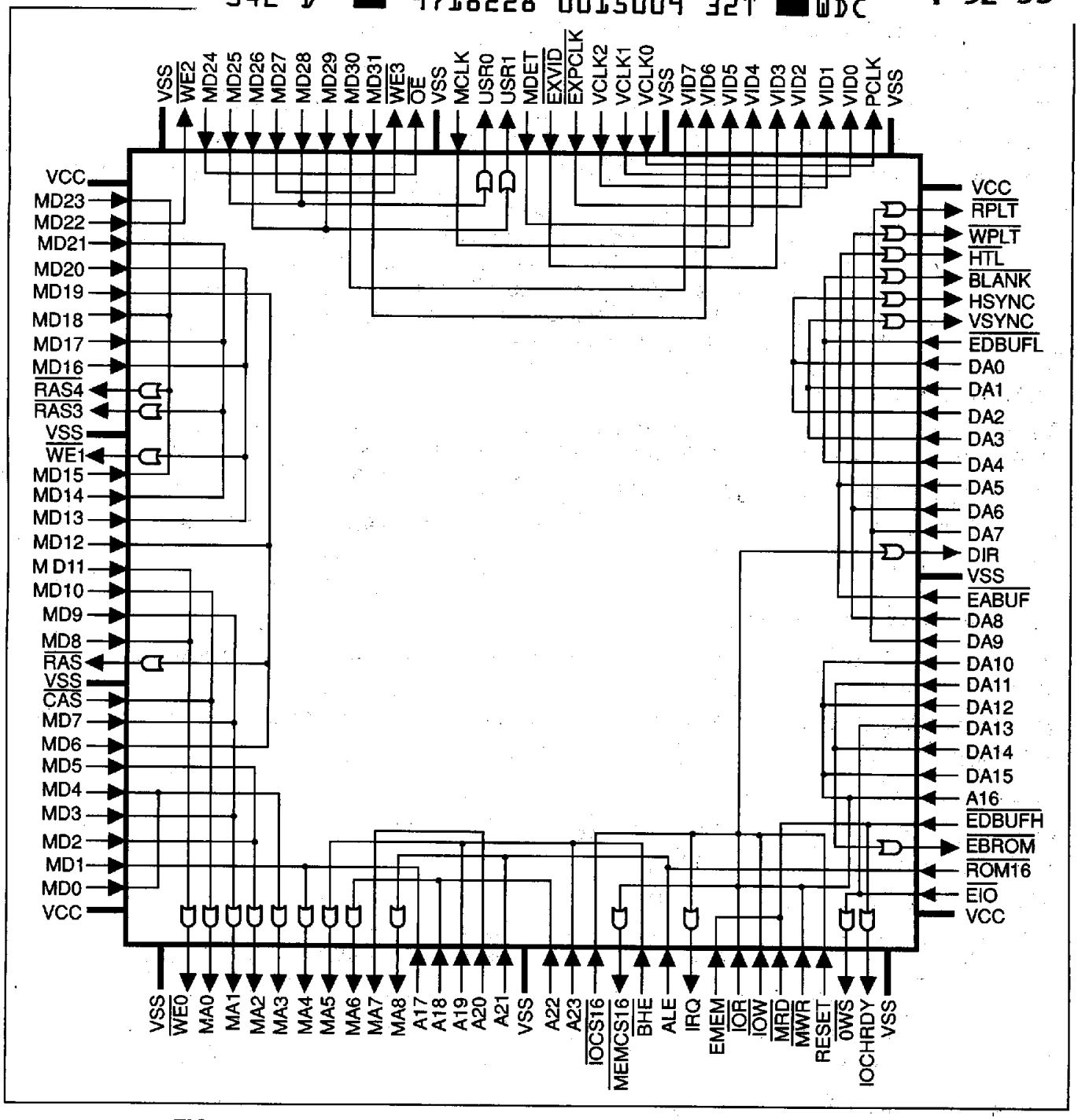

FIGURE 17-2. WD90C31A PIN SCAN MAP FOR A 132-PIN PACKAGE

18.0 DC ELECTRICAL SPECIFICATIONS

T-52-33-45

18.1 MAXIMUM RATINGS

Voltage on any pin with respect to Vss . . . . . -0.3 to 7 Volts

Ambient Temperature Under Bias . . . . . 0°C to 70°C (32°F to 158°F)

Storage Temperature . . . . . -40°C to 125°C (-40°F to 257°F)

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

18.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range . . . . . 0°C to 70°C (32°F to 158°F)

Power Supply Voltage . . . . . 4.75 to 5.25 Volts

Power Dissipation . . . . . 140 mA

18.3 DC CHARACTERISTICS

Pins MDET, $\overline{BHE}$, $\overline{EXVID}$, $\overline{EXPCLK}$, MD31:0, DA15:0 and VCLK2 have internal pullup resistors with a minimum pullup resistance of 50KΩ.

With the following exceptions the WD90C31A outputs have 2.0 mA maximum source and sink capability.

IRQ, IOCHRDY, $\overline{0WS}$, $\overline{MEMCS16}$, $\overline{IOCS16}$ = 24 mA sink.

PCLK, VID7:0, $\overline{BLANK}$ = 8 mA source/sink.

DRAM Interface = 4.0 mA source/sink($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, MA, MD)

HSYNC, VSYNC, DA15:0 = 6 mA sink.

$\overline{ROM16}$ = 16 mA sink.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC = 5V ±5%
V(IH)	Input High Voltage	2.0	VCC +0.3	V	VCC = 5V ±5%
I(IL)	Input Low Current	--	±10	µA	VIN = 0.0V
I(IH)	Input High Current	--	±10	µA	VIN = VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0 mA
V(OH)	Output High Voltage	2.4	--	V	IOH = -2.0 mA
I(OZ)	High Impedance Leakage Current	-10.0	10.0	µA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	F = 1 MHz
C(OUT)	Output Capacitance	--	10	pF	F = 1 MHz
C(I/O)	I/O Pin Capacitance	--	12	pF	F = 1 MHz

TABLE 18-1. DC CHARACTERISTICS

19 .0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

- All units are in nanoseconds.
- CL = 30 pF unless otherwise noted.
- nt implies n X t, (n times the period t). e.g. 1t, 2t etc.
- #n refers to the spec number in column 1 of the same table.

NUMBER	CHARACTERISTIC		MIN	MAX	TEST CONDITION
	RESET TIMING				
1	RESET Pulse Width		10t		t = 1/MCLK (For configuration at power up.)
2	MD Setup to RESET low		50		
3	MD Hold from RESET low		30		
4	RESET low to first $\overline{IOW}$		10t		
	CLOCK TIMING				
1	VCLK period	Note 1	12.5	72.0	
2	VCLK high		5		At 1/2 VDD
3	VCLK low		5		At 1/2 VDD
4	Clock rise time	Note 1		2	1V - (VDD - 1V)
5	Clock fall time	Note 1		2	1V - (VDD - 1V)
6	VCLK to PCLK delay		8	20	45 ns at 120 pF load
7a	VCLK to HSYNC delay		8	25	
7b	VCLK to VSYNC delay		8	25	
7c	VCLK to $\overline{BLANK}$ delay		8	20	
7d	VCLK to VID(7:0) delay		8	20	45 ns at 120 pF load up to 30 MHz
8	MCLK period	Note 2	20	30	Max 50 MHz, Min 33.3 MHz
9	MCLK high		8		At 1/2 VDD
10	MCLK low		8		At 1/2 VDD
11	VID (7:0) setup to PCLK		3		
12	VID (7:0) hold from PCLK		3		

Note 1 - Apply to both VCLK and MCLK.

Note 2 - VCLK0 and MCLK use CMOS level input buffers. $V(IL)_{max}$ = 1.5 V, $V(IH)_{min}$ = VDD - 1.5 V

TABLE 19-1. AC TIMING CHARACTERISTICS

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$, $\overline{MWR}$ high	10		
3a	A(23:17) setup to ALE low	20		
3b	$\overline{BHE}$, DA(15:0) setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	18		
4a	A(23:17) hold from ALE low	10		
4b	DA(15:0) hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	10		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	10		
7a	$\overline{EABUF}$ high from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	9	25	
7b	$\overline{EDBUF}$ low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	13.5	35	
7c	$\overline{HTL}$ low from $\overline{MRD}$ low		25	
8a	$\overline{EABUF}$ low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	14.5	35	
8b	$\overline{EDBUF}$ high from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	8.5	25	
8c	$\overline{HTL}$ high from $\overline{MRD}$ high		25	
9	DIR high from $\overline{IOR}$, $\overline{MRD}$ low		20	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		20	
11	DA(15:0) write data setup to $\overline{IOW}$, $\overline{MWR}$ high	20		
12a	DA(15:0) read data hold from $\overline{IOR}$ high or $\overline{MRD}$ high	10		
12b	DA(15:0) write data hold from $\overline{IOW}$, $\overline{MWR}$ high	10		
13	DA(15:0) read data valid after $\overline{IOR}$ low		70	
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15	Memory read data valid from RDY high		40	Note 3
16a	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	25	C_L = 100 pF
16b	RDY low from $\overline{IOW}$, $\overline{IOR}$ low	10	25	C_L = 100 pF
17a	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
17b	RDY tristate from $\overline{IOW}$, $\overline{IOR}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		37	
20b	RPLT low from $\overline{IOR}$ low		30	

Note 3 Depends on setting of PR31 (3C5H, Index 11H) bits 4, 3. t = ^{1}/MCLK
00 max 40 ns
01 max 40 ns + 1t
10 max 40 ns + 2t
11 max 40 ns - 1t

TABLE 19-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	I/O AND MEMORY READ/WRITE AT MODE TIMING (Continued)			
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high	9	15	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high	9	20	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H port)		1t + 20	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H port)		25	
24	VCLK1 low from $\overline{IOW}$ low (3C2H port)		1t + 24	
25	VCLK1 high from $\overline{IOW}$ high (3C2H port)		15	
26	A(15:0) valid to $\overline{IOCS16}$ low		35	C_L = 100pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		20	C_L = 100pF
28	A(23:17) valid to $\overline{MEMCS16}$ or $\overline{ROM16}$ low		41	C_L = 100pF
29	$\overline{MEMCS16}$ tristate from the next active ALE		39	C_L = 100pF
30a	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ high	2t + 15		t = ^{1}/MCLK Note 4
30b	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ low	2t		t=^{1}/MCLK Note 5
30c	ALE pulse width	30		
31	$\overline{OWS}$, low from $\overline{IOW}$, $\overline{MWR}$ low		15	C_L = 100pF

Note 3 Depends on setting of PR31 (3C5H, Index 11H) bits 4, 3. t = ^{1}/MCLK
00 max 40 ns
01 max 40 ns + 1t
10 max 40 ns + 2t
11 max 40 ns - 1t

Note 4 Minimum of #30a should be the greater of 2t + 15 or (#8a + #3b + delay on the external address buffer)

Note 5 Minimum of #30b should be the greater of 2t or (#7b + #11 + delay on the external data buffer)

TABLE 19-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTICS	MIN	MAX	TEST CONDITION
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	20		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	10		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	15		
5	STATUS setup to $\overline{CMD}$ low	20		
6	STATUS hold from $\overline{CMD}$ low	15		
7a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low	13.5	35	
7b	$\overline{EABUF}$ high from $\overline{CMD}$ low	9	25	
8a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high	8.5	25	
8b	$\overline{EABUF}$ low from $\overline{CMD}$ high	14.5	35	
9	DIR active from $\overline{CMD}$ low		20	
10	DIR inactive from $\overline{CMD}$ high		20	
11	$\overline{CSFB}$ delay from valid address/status		30	C_L = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		30	C_L = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		30	C_L = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	DA(15:0) write data setup to $\overline{CMD}$ high	20		
17	DA(15:0) Write data hold after $\overline{CMD}$ high	10		
18	DA(15:0) I/O Read data valid from $\overline{CMD}$ low		70	
19	RDY high delay from $\overline{CMD}$ low	0	2.45 µs	
20	DA(15:0) Memory Read Data valid from RDY high		40	Note 3
21a	$\overline{CMD}$ high (inactive)	2t + 15		Note 6
21b	$\overline{CMD}$ low	2t		Note 7
22	RDY low delay from valid address/status		30	
23	$\overline{EBROM}$ low from valid address		40	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		30	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low	9	20	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high	9	20	
27	VCLK1 low from $\overline{CMD}$ low (3C2H port)		1t + 30	
28	VCLK1 high from $\overline{CMD}$ high (3C2H port)		25	

Note 3 Depends on setting of PR31 (3C5H, Index 11H) bits 4, 3. t = ^{1}/MCLK
00 max 40 ns
01 max 40 ns + 1t
10 max 40 ns + 2t
11 max 40 ns - 1t

Note 6 Minimum of #21a is the greater of 2t + 5 or (#8b + #1 + delay on external address buffer)

Note 7 Minimum of #21b is the greater of 2t or (#7a + #16 + delay on external data buffer)

TABLE 19-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	DRAM TIMING (256K By 4, 256K By 16)			
1	$\overline{RAS}$ cycle time	6t		Note 8
2	$\overline{RAS}$ pulse width low	3.5t - d		Note 8
3	$\overline{RAS}$ high time (precharge)	2.5t + d		Note 8
4	$\overline{RAS}$ low to $\overline{CAS}$ low	2.5t - 9	2.5t - d	Note 8
5	$\overline{CAS}$ cycle time	2t		
6	$\overline{CAS}$ pulse width low	1t + d		Note 8
7	$\overline{CAS}$ high time (precharge)	1t - d		Note 8
8	Row address setup to $\overline{RAS}$ low	1t - 10		
9	Row address hold time from $\overline{RAS}$ low	1t		
10	Column address setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	3		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	0.5t + 5		Note 9
16	$\overline{WE}$ low setup $\overline{CAS}$ low	1t - 5	1t + 5	
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as CAS low		
18	$\overline{OE}$ high before $\overline{WE}$ low	2t - 10		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	1t - 10		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t + 10		

Note 8
The timing is the result of setting PR33 (3C5, Index = 13) = XXX00000.
Timings are adjustable by PR33.
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 1.
t = ^{1}/MCLK
(MCLK = 37.5 MHz for 80 ns DRAM)
(MCLK = 40 MHz for some faster 80ns DRAM)
(MCLK = 44.4 MHz for 70 ns DRAM)
(MCLK = 49.5 MHz for 60 ns DRAM)
} Maximum MCLK frequency
d = Delay of between 4 and 7 ns.

Note 9
0.5t refers to the high pulse width of the MCLK measured at 2.5V.

TABLE 19-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	DRAM TIMING (64K by 16)			
1	$\overline{RAS}$ cycle time	5t		Note 10
2	$\overline{RAS}$ pulse width low	3t - 7		Note 10
3	$\overline{RAS}$ high time (precharge)	2t		Note 10
4	$\overline{RAS}$ low to $\overline{CAS}$ low	1.5t	1.5t	Note 10
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	1t + 2d		Note 10
7	$\overline{CAS}$ high time (precharge)	1t - 2d		Note 10
8	Row address setup to $\overline{RAS}$ low	1t		
9	Row address hold time from $\overline{RAS}$ low	1/2t		
10	Column adress setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	0.5t + 5		Note 9
16	$\overline{WE}$ low setup before $\overline{CAS}$ low	1t - 10		
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as CAS low		
18	$\overline{OE}$ high before $\overline{WE}$ low	1t + 2		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 16		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	0.5t		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t		

Note 9
0.5t refers to the high pulse width of the MCLK measured at 2.5V.

MCLK edge to $\overline{RAS}$, $\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns.

Note 10
The timing is the result of setting PR33 (3C5H, Index = 13H) = xxx01110.
Timings are adjustable by PR33.
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 0.
t = ^{1}/MCLK (MCLK = 36 MHz for 80 ns, 64K by 16 DRAM).
d = Delay of between 4 and 7 ns.

TABLE 19-1. AC TIMING CHARACTERISTICS (Continued)

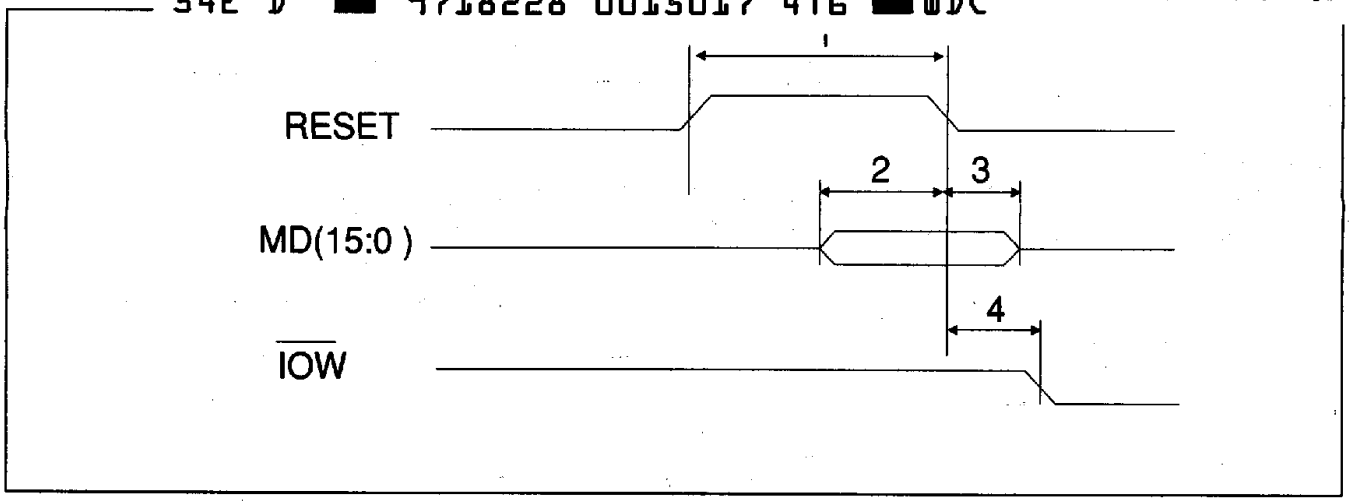

FIGURE 19-1. RESET TIMING

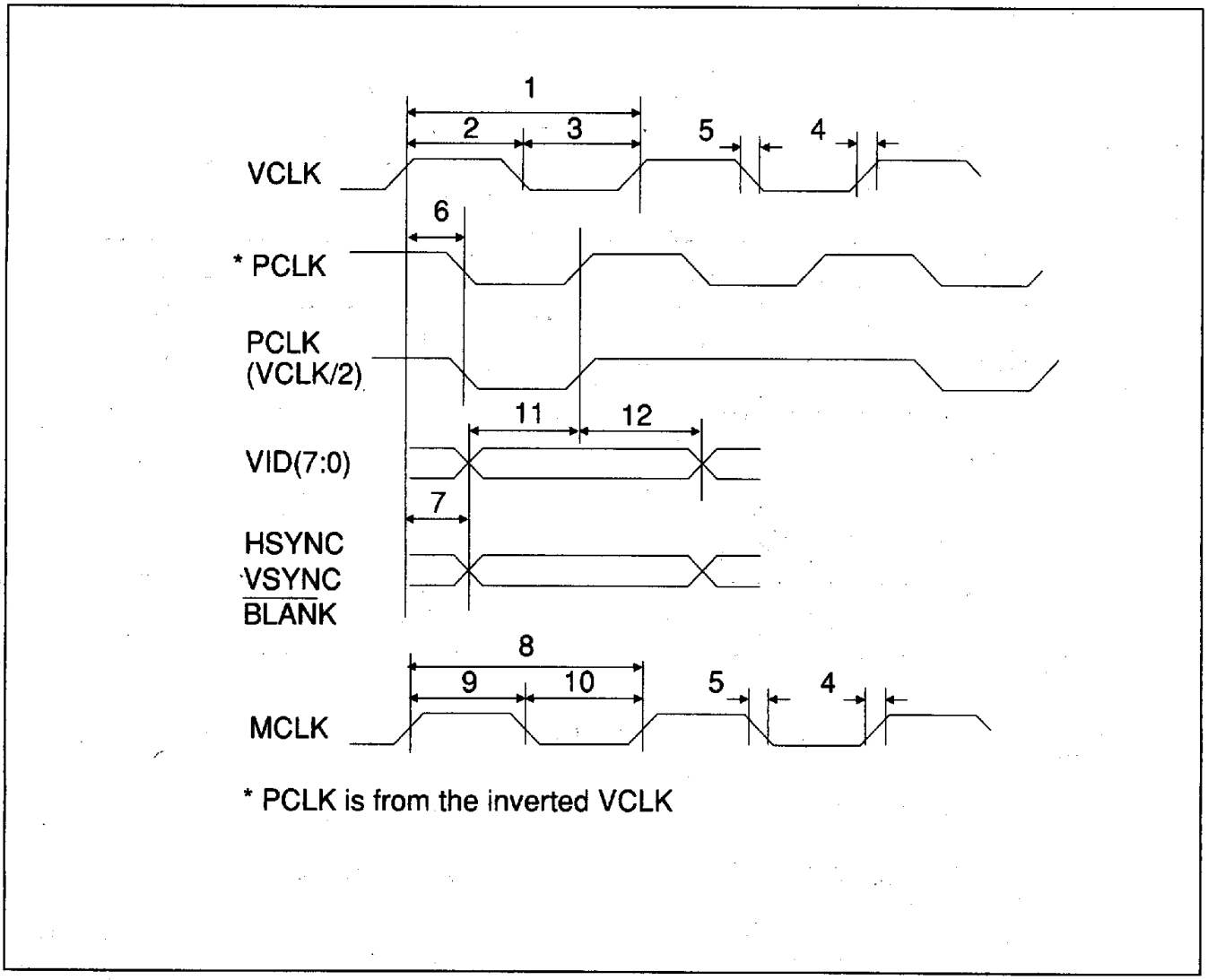

FIGURE 19-2. CLOCK AND VIDEO TIMING

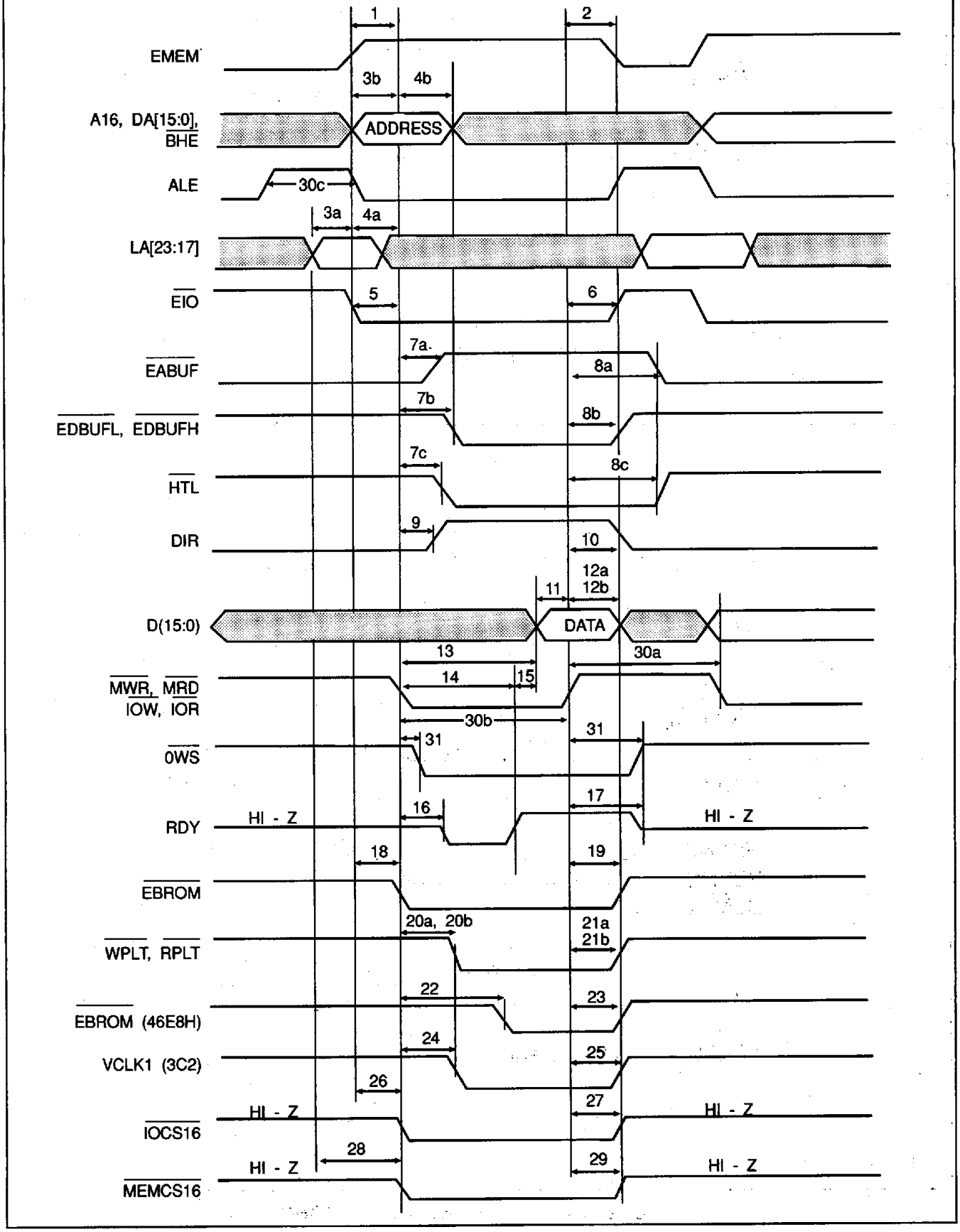

FIGURE 19-3. AT MODE BUS TIMING

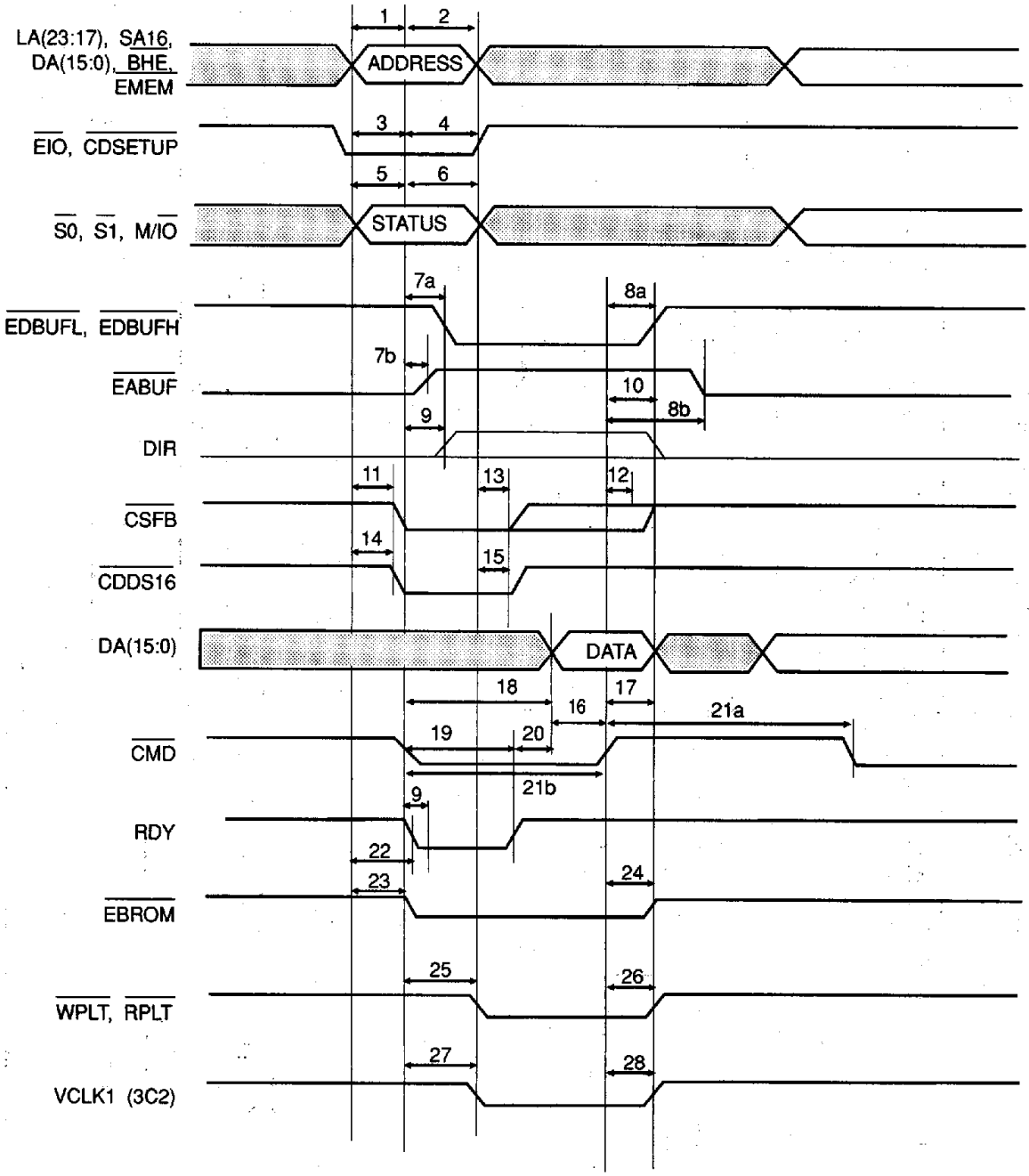

FIGURE 19-4. MICRO CHANNEL MODE BUS TIMING

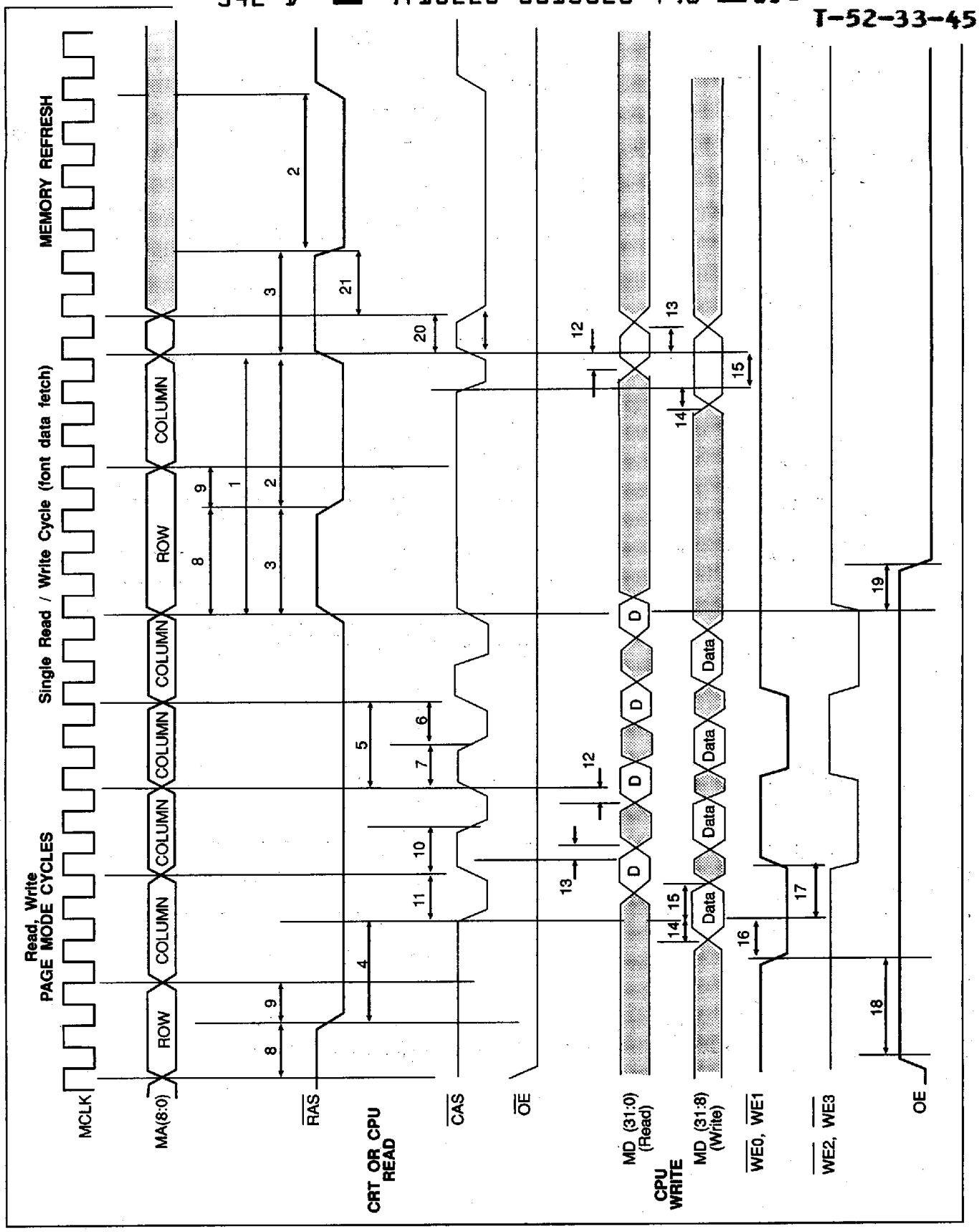

FIGURE 19-5. DRAM TIMING

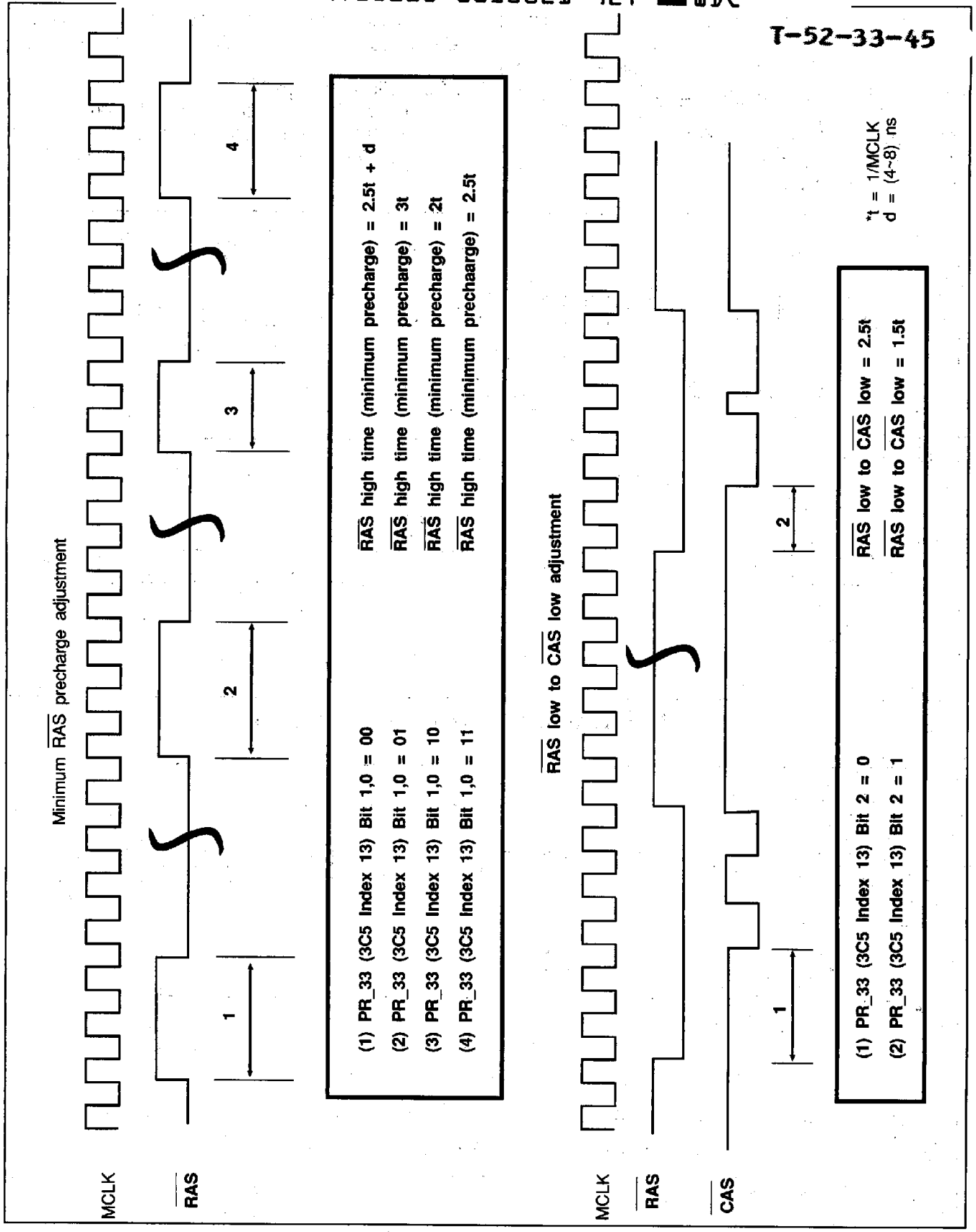

FIGURE 19-6. DRAM TIMING ADJUSTMENT

DRAM Timing Adjustment: The RAS, CAS timing can be adjusted by register PR33 (3C5H, Index 3H) bits 4 through 0. Only the following timing may be affected: (See Figures 19-5 and 19-6).

3 $\overline{RAS}$ high time (precharge)
4 $\overline{RAS}$ low to CAS low
6 $\overline{CAS}$ pulse width

CAS pulse width adjustment: CAS cycle time is always equal to 2t {t = 1/MCLK}, {d = (4~ 8) ns}.

PR33 (Bits 4 through 3) =

00, $\overline{CAS}$ low = 1t + d;	$\overline{CAS}$ high = 1t - d
01, $\overline{CAS}$ low = 1t + 2d;	$\overline{CAS}$ high = 1t - 2d
1X, $\overline{CAS}$ low = 1.5t;	$\overline{CAS}$ high = $^1/2$t

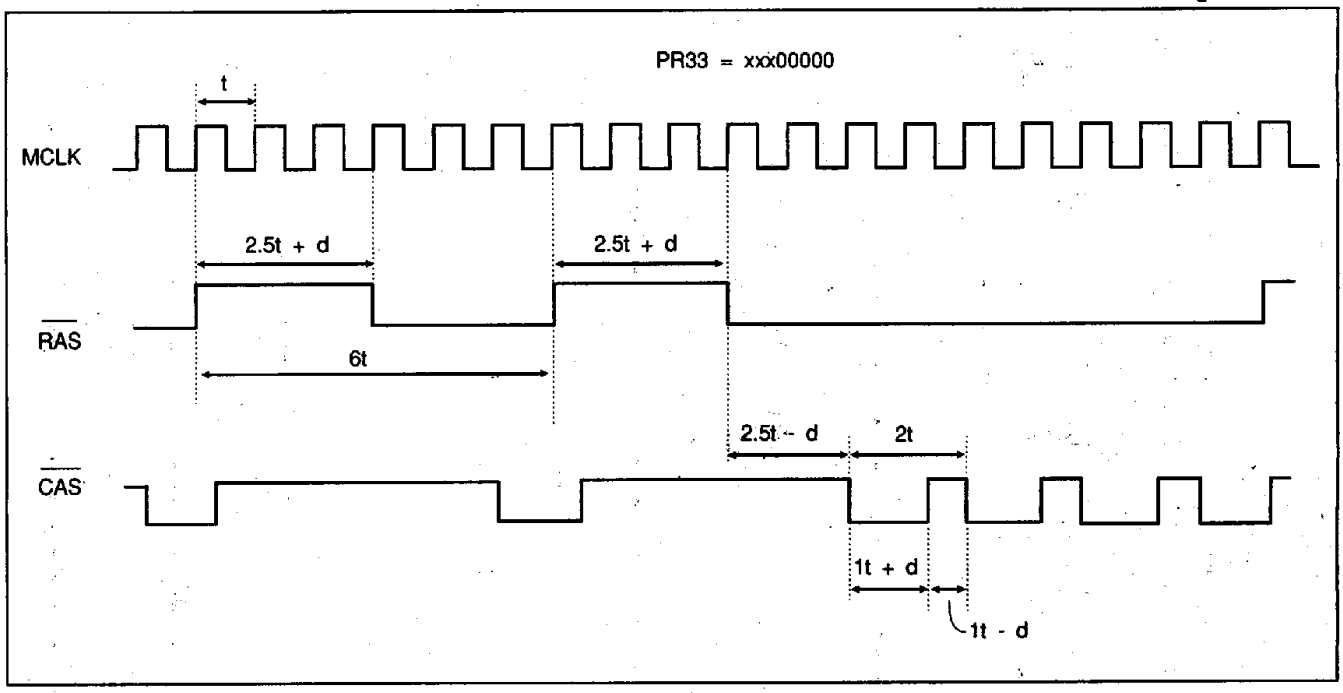

FIGURE 19-7. 256K BY 4 DRAM TIMING

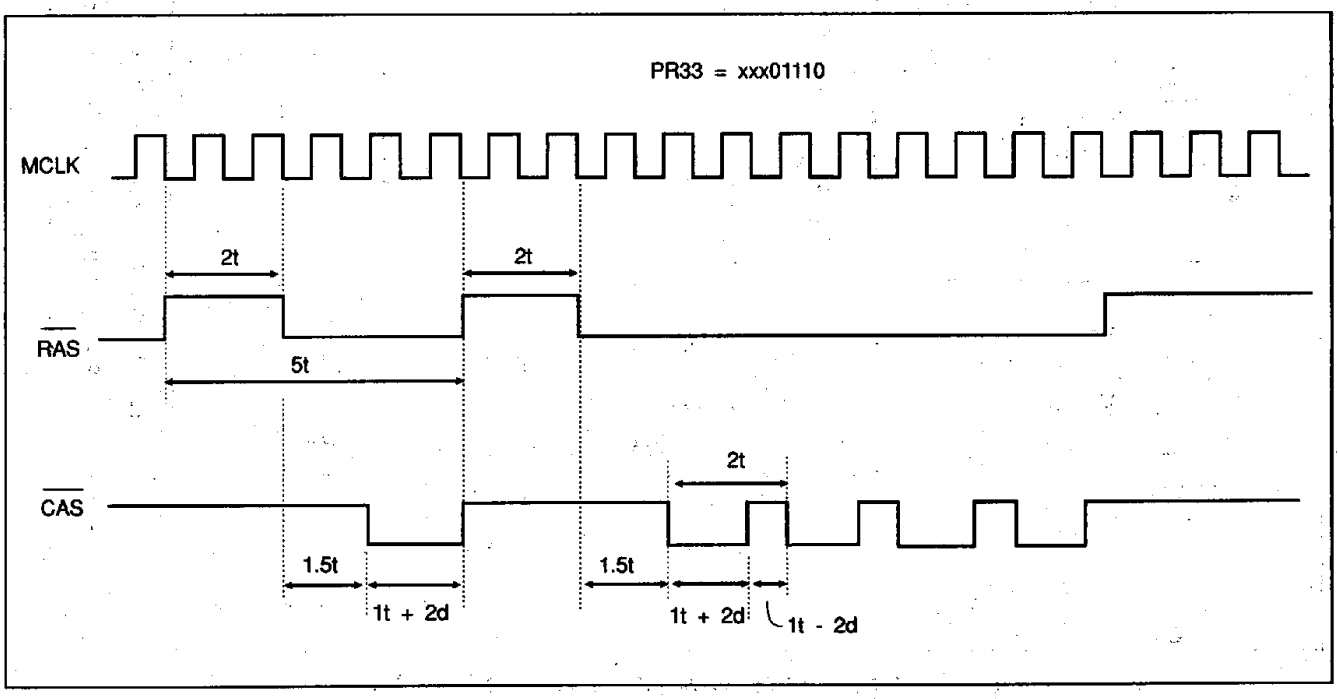

FIGURE 19-8. 64K BY 16 DRAM TIMING

20.0 PACKAGE DIMENSIONS

Figure 20-1 illustrates the 132-pin PQFP package showing the dimensions in inches. Figure 20-2 illustrates the 144-pin MQFP package showing the dimensions in millimeters and inches.

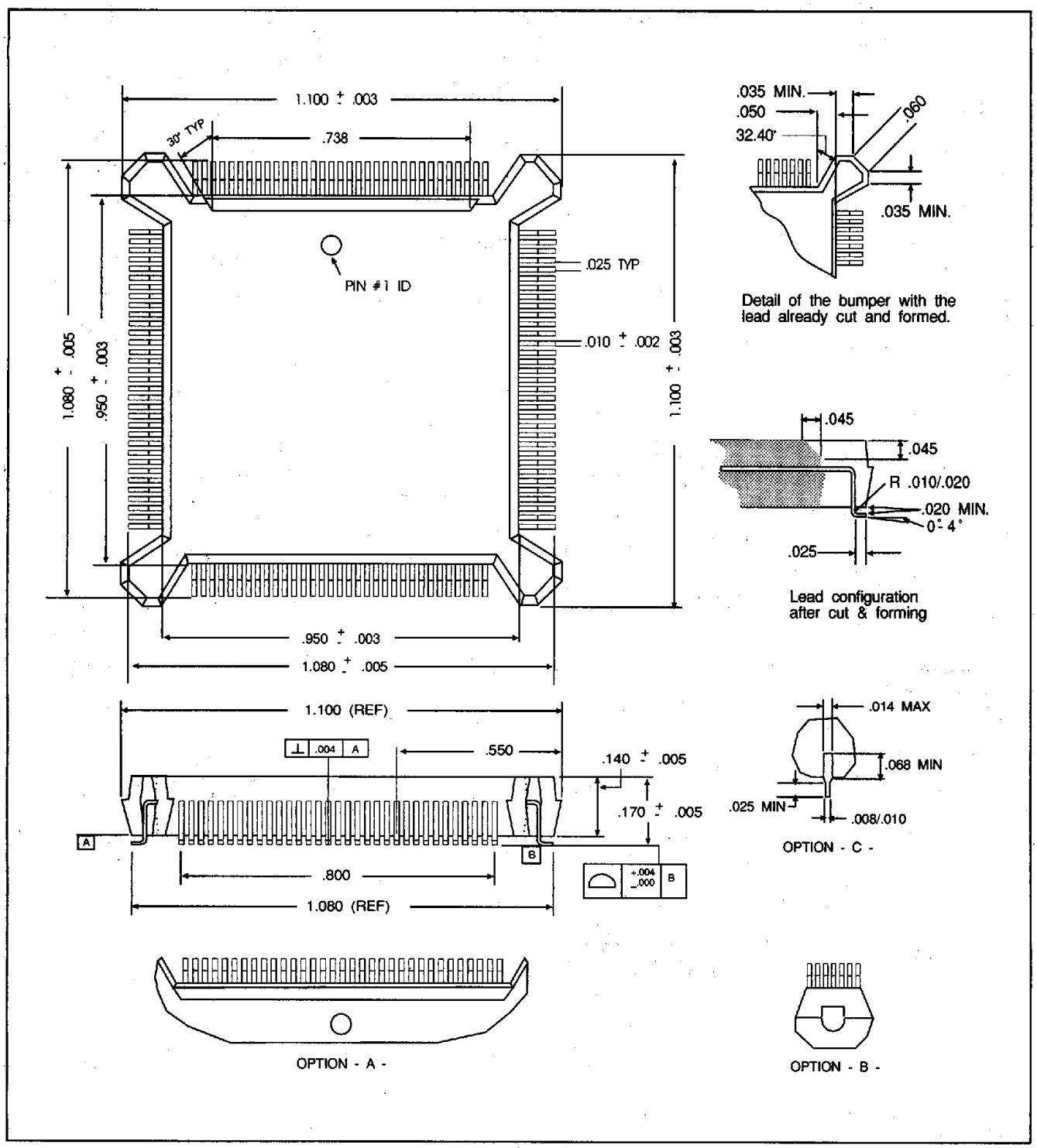

FIGURE 20-1. 132-PIN PQFP PACKAGE

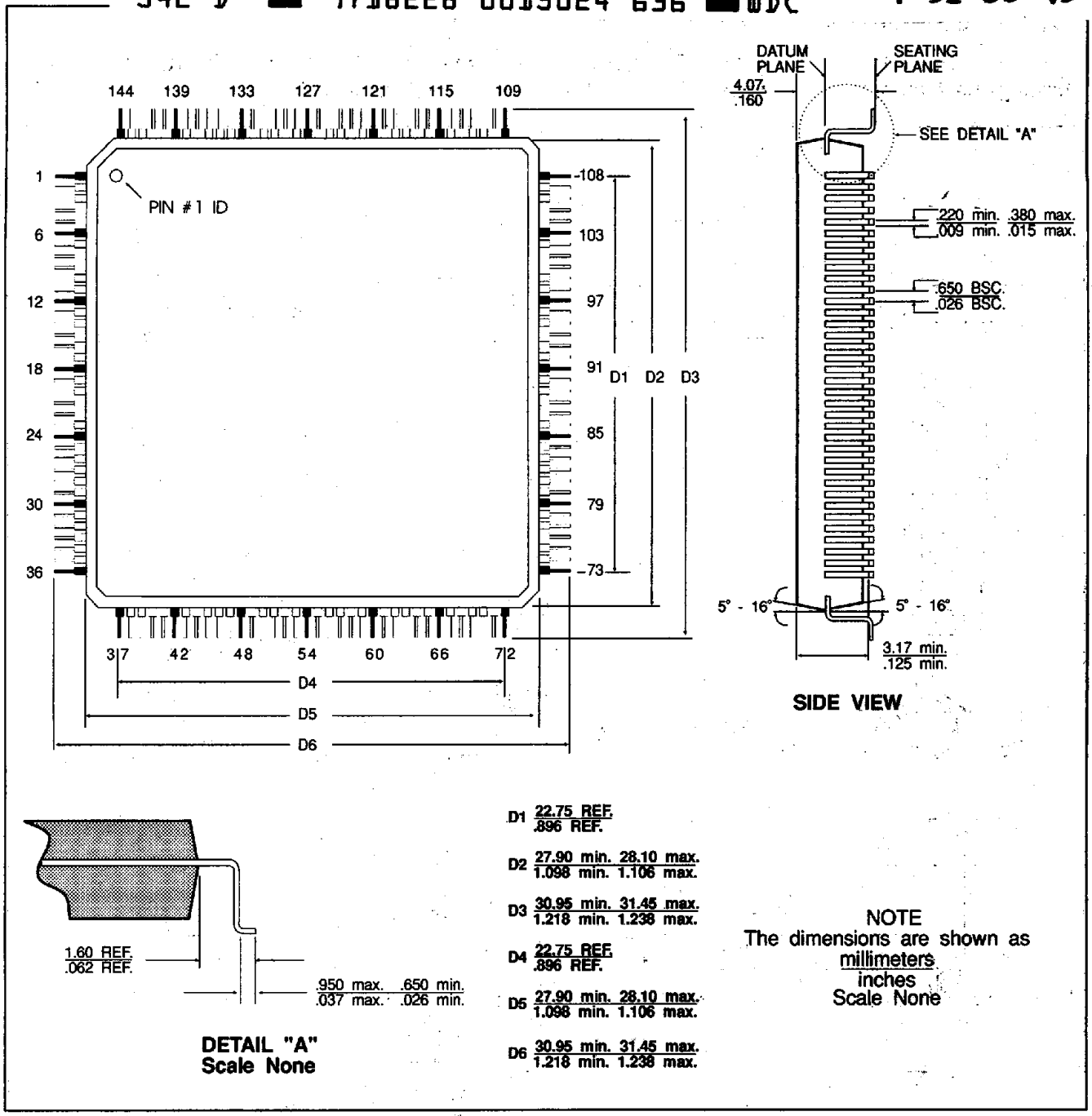

FIGURE 20-2. 144-PIN MQFP PACKAGE