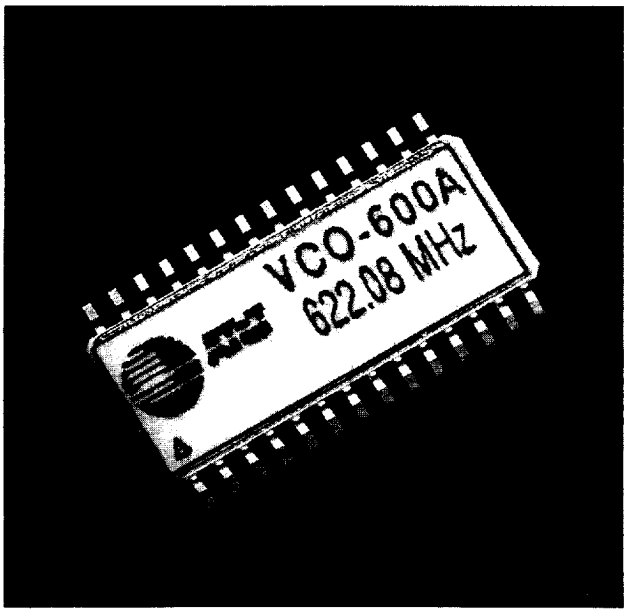
Data Sheet
June 1994

AT&T Microelectronics

VCO-600 Voltage-Controlled SAW Oscillator



The VCO-600 Voltage-Controlled SAW Oscillator.

Features

- Output frequencies between 155 MHz and 1.1 GHz
- Low phase jitter
- Ideal for clock generation and data retiming applications
- 10K ECL logic levels with fast transition times
- Complementary outputs
- Low-profile, surface-mount package
- Output disable feature
- Low-frequency clock through feature
- Miniature hermetically sealed ceramic surface-mount package (S0-28, approx. 0.7 in. x 0.3 in.)

Description

The VCO-600 is a SAW-stabilized, voltage-controlled oscillator that operates at the fundamental frequency of the internal SAW filter. This filter is a high-stability, high-Q quartz device which enables the circuit to achieve low phase noise performance over a wide temperature range.

The oscillator is housed in a hermetically sealed 28-lead ceramic surface-mount package. It has a unique output disable and clock through feature which improves on-board testing.

The VCO-600 is available with center frequencies between 155 MHz and 1.1 GHz, including the SONET/ATM standard frequencies of 155.52 MHz, 311.04 MHz, and 622.08 MHz. Typical applications of the VCO-600 are data retiming and synchronization as part of a phase-locked loop (PLL), as well as frequency synthesis and frequency translation (see Figure 3).

Pin Information

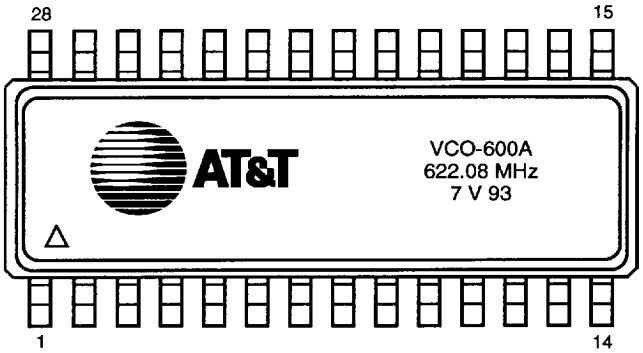


Figure 1. Pin Diagram

Table 1. Pin Descriptions

Pin #	I/O	Symbol	Description
2	I	VCC	Positive supply.
4	I	CLKIN	Test clock input.*
5, 6, 7, 8	—	NC	No connect.
10	I	VEE	Negative supply.
12	I	VCC	Positive supply.
17	I	VBW	Modulation bandwidth control.†
19	I	VC	Voltage control.
21	I	OD	Output disable.‡
23	O	CLKOUT	ECL output.
25	O	CLKOUTB	ECL inverted output.
27	I	VCC	Positive supply.
1, 3, 9, 11, 13, 14, 15, 16, 18, 20, 22, 24, 26, 28	—	Case	Case ground.

* By setting OD to low, a test signal may be applied at CLKIN and fed through the VCO-600 to both CLKOUT and CLKOUTB, for board testing purposes. The test signal input applied at CLKIN may be either an ECL signal or a sinusoidal input (up to 1 V peak to peak, ac coupled to CLKIN). CLKIN is biased internally to VBB (VCC – 1.3 V).

† An optional capacitor to ground can be placed on VBW to reduce the modulation bandwidth for narrow bandwidth phase-locked loop applications. The modulation bandwidth, in Hz, will be 1/(12000C), where the capacitance (C) is in farads. If the optional capacitor is not used, VBW becomes a no connect (NC), and the modulation bandwidth is equal to the center frequency ÷ 1200.

‡ By setting OD low, the outputs of the VCO-600 are disabled with CLKOUT going high and CLKOUTB going low (no signal present at CLKIN). The threshold for OD is 1.4 V above VEE. OD should not be driven above midsupply and, during normal operation, OD should be left floating (use with an open collector or 3-state gate for interfacing with standard logic). If the OD feature is used during normal operation, then CLKIN should be tied 10 kΩ to ground to avoid the possibility of chatter on the CLKOUT and CLKOUTB outputs.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Rating	Unit
Power Supply	V_{EE}	–8 to 0	V
Output Current (avg. each output)*	Io	20	mA
Output Current (avg. each output)†	Io	50	mA
Voltage Control Range Vc*	Vc	V_{EE} to V_{CC}	V
Voltage Control Range Vc†	Vc	V_{CC} + 0.5 to V_{EE} – 0.5	V

* Limits beyond which performance cannot be guaranteed.
† Limits beyond which device life may be impaired.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters:

Model	Minimum	Unit
Human Body	1000	V
Charged Device	1000	V

Electrical Characteristics

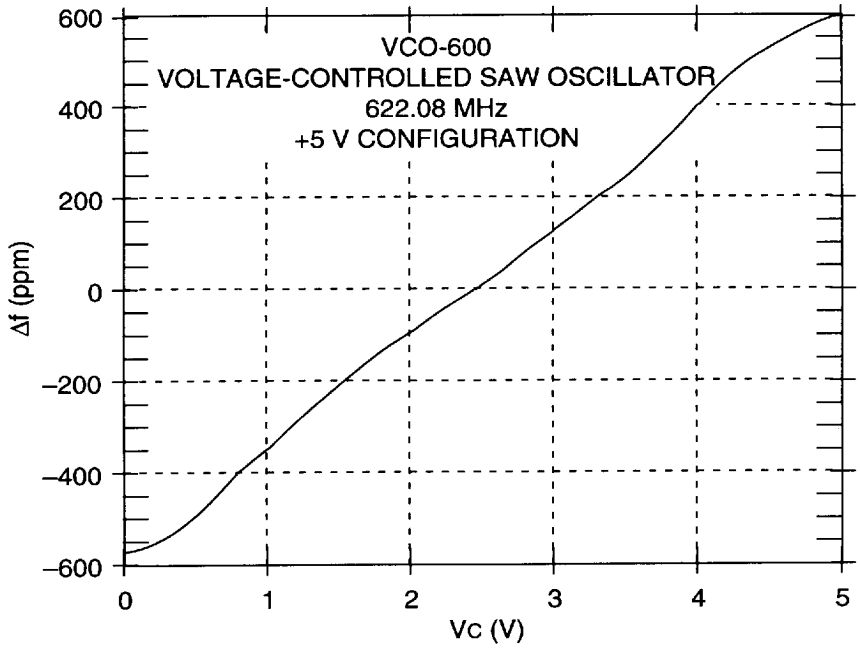
T_A = –40 °C to +85 °C

The absolute pull range (APR) is the range of frequencies to which the VCO-600 can be adjusted over the –0.5 V to –4.5 V control range on the Vc pin. The actual tuning curve, shown in Figure 2, is much wider. APR takes into account all tolerances such as initial setting, temperature, supply, and aging variation. This ensures that the following is true over all operational and lifetime conditions: If the desired clock frequency is within the APR (i.e., ±50 ppm), then the device can be set to that frequency by a control voltage within the –0.5 V to –4.5 V range. For PLL applications, it is important to note that the loop filter input to Vc must be capable of covering this range. This is most easily accomplished with CMOS type op amps with rail-to-rail output swing.

Parameter	Symbol	Min	Typical	Max	Unit
Center Frequency	Fo	155	–	1100	MHz
Operational Temperature Range	T	–40	25	85	°C
Absolute Pull Range					
Vc = 0.5 V	APR	–50	—	—	ppm from Fo
Vc = 4.5 V	APR	50	—	—	ppm from Fo
Total Frequency Deviation (See Figure 2.)					
Vc = 0.5 V	ΔF	—	–400	—	ppm from Fo
Vc = 4.5 V	ΔF	—	400	—	ppm from Fo
Supply Voltage*	V_{EE}	–4.5	–5.0	–5.5	V
Supply Current	I_{EE}	45	55	70	mA
Output Levels†					
Output High	V_{OH}	–0.980	—	–0.750	V
Output Low	V_{OL}	–1.950	—	–1.630	V
Transition Times‡					
Rise Time	t_{RISE}	100	250	400	ps
Fall Time	t_{FALL}	100	250	400	ps
Frequency Stability (Vc = constant)	–	–	±150	–	ppm from Fo
Symmetry or Duty Cycle	SYM	45	49/51	55	%
Control Voltage Range	Vc	V_{EE}	–	V_{CC}	V
Linearity (Vc = V_{EE} to V_{CC})	—	—	±3	—	%
Spurious Output Suppression	–	–50	–60	—	dB
Control Voltage Input Impedance	Zc	8	10	12	kΩ
Control Voltage Modulation Bandwidth§	BW	—	500	—	kHz

* The VCO-600 may also be configured for positive ECL (PECL) operation. All outputs and inputs, including Vc, are referenced to V_{CC}.
† Output levels are standard 10K, fully compatible with 100K.
‡ Transition times are measured at 20% and 80% of full 10K ECL swing.
§ The modulation bandwidth is a function of the center frequency of the VCO-600, or it can be adjusted by using an external capacitor. Please see the description of V_{BW} in the Pin Information section.

Electrical Characteristics (continued)



Notes:
The tuning curve, when expressed in parts per million (ppm), is typical of the VCO-600 at other frequencies.

The center frequency for this curve is normalized at 2.5 V. In practice, the room temperature center voltage (the voltage that tunes the device to the center frequency) is set to account for temperature and aging variations.

Figure 2. Typical VCO-600 Tuning Curve

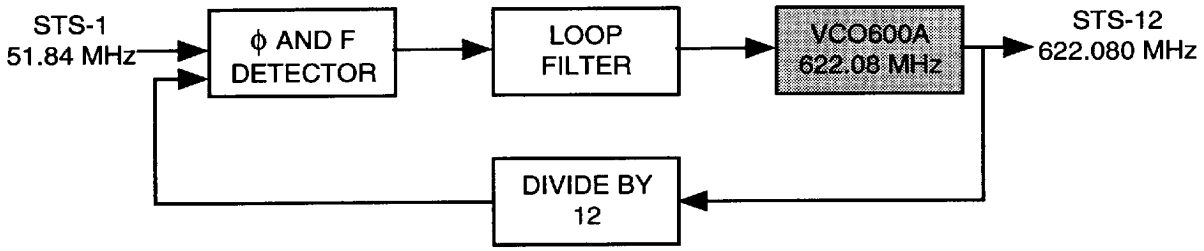


Figure 3. Typical SONET/SDH Frequency Translation Application

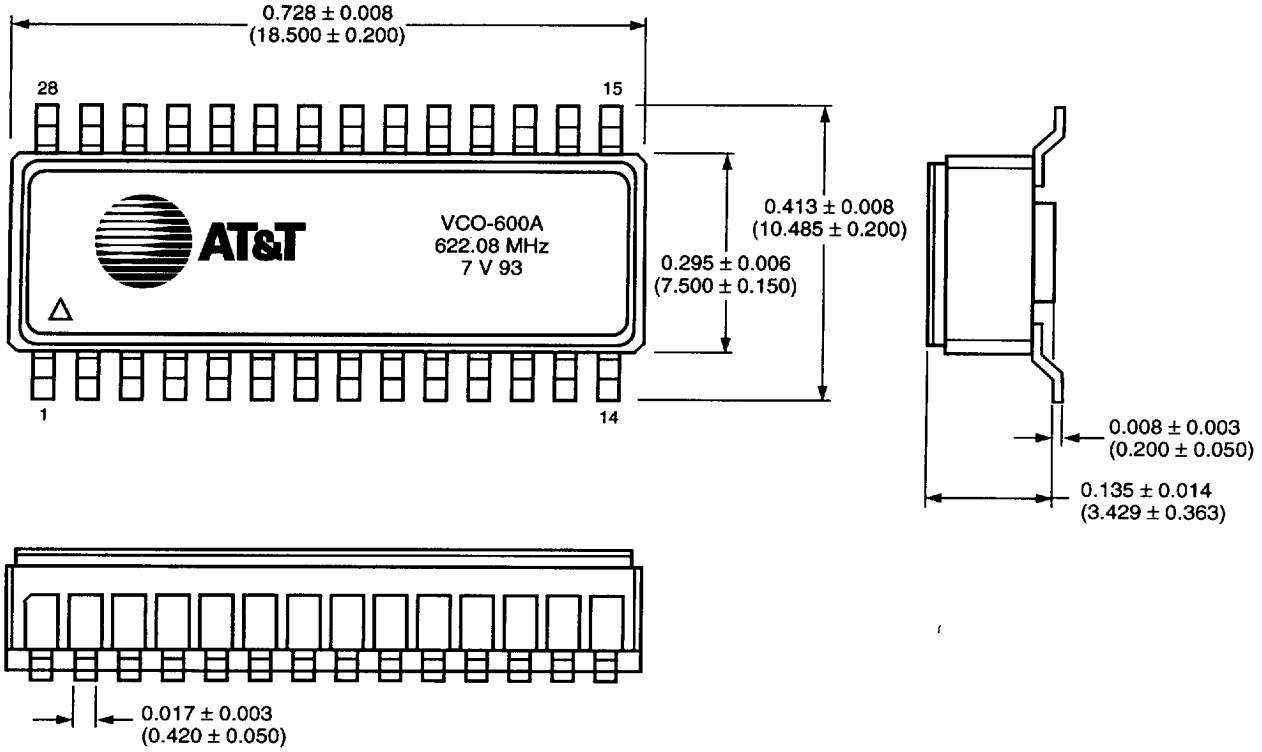
Mechanical Characteristics

Parameter	Value
Mechanical Shock	MIL-STD-883C 2002.3 Test A
Mechanical Vibration	MIL-STD-883C 2007.1 Test A
Solderability	MIL-STD-883C 2003.5
Gross Leak Test	MIL-STD-883C 1014.7
Fine Leak Test	MIL-STD-883C 1014.7 (5 x 10^{-8} atm Helium)
Storage Temperature	–55 °C to +125 °C
Resistance to Solvents	MIL-STD-883C 2016

Outline Diagram

VCO-600 Package

Dimensions are in inches and (millimeters).



For additional information, contact your AT&T Account Manager or the following:

U.S.A.: AT&T Microelectronics, Dept. AL-500404200, 555 Union Boulevard, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)

ASIA PACIFIC: AT&T Microelectronics Asia/Pacific, 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
Tel. (65) 778-8833, FAX (65) 777-7495

JAPAN: AT&T Microelectronics, AT&T Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3-5421-1600, FAX (81) 3-5421-1700

For data requests in Europe:

AT&T DATALINE: **Tel. (44) 732 742 999**, FAX (44) 732 741 221

For technical inquiries in Europe:

CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 344 487 111** (Bracknell UK),
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