

128 macrocell CPLD with enhanced clocking

PZ5128C/PZ5128N

FEATURES

- Industry's first TotalCMOS™ PLD – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- 5 Volt, In-System Programmable (ISP) using a JTAG interface
 - On-chip supervoltage generation
 - ISP commands include: Enable, Erase, Program, Verify
 - Supported by multiple ISP programming platforms
 - 4 pin JTAG interface (TCK, TMS, TDI, TDO)
 - JTAG commands include: Bypass, Idcode
- High speed pin-to-pin delays of 7.5ns
- Ultra-low static power of less than 100µA
- Dynamic power that is 70% lower at 50MHz than competing devices
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- Up to 20 clocks available
- Support for complex asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E²CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Philips CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
 - Programmable 3-State buffer
 - Asynchronous macrocell register preset/reset
 - up to 2 asynchronous clocks
- Programmable global 3-State pin facilitates 'bed of nails' testing without using logic resources
- Available in TQFP and LQFP packages
- Available in both Commercial and Industrial grades

DESCRIPTION

The PZ5128C/PZ5128N CPLD (Complex Programmable Logic Device) is a member of the Fast Zero Power (FZP™) family of CPLDs from Philips Semiconductors. These devices combine high speed and zero power in a 128 macrocell CPLD. With the FZP™ design technique, the PZ5128C/PZ5128N offers true pin-to-pin speeds of 7.5ns, while simultaneously delivering power that is less than 100µA at standby without the need for 'turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD – 70% lower at 50MHz. These devices are the first TotalCMOS™ PLDs, as they use both a CMOS process technology and the patented full CMOS FZP™ design technique.

The Philips FZP™ CPLDs introduce the new patented XPLA™ (eXtended Programmable Logic Array) architecture. The XPLA™ architecture combines the best features of both PLA and PAL™ type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA™ structure in each logic block provides a fast 7.5ns PAL™ path with 5 dedicated product terms per output. This PAL™ path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2ns, regardless of the number of PLA product terms used, which results in worst case t_{PD} 's of only 9.5ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The PZ5128C/PZ5128N CPLDs are supported by industry standard CAE tools (Cadence, Exemplar Logic, Mentor, ORCAD, Synopsys, Synario, Viewlogic, MINC), using text (Abel, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses either MINC or Philips Semiconductors-developed tools.

The PZ5128C/PZ5128N CPLD is electrically reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others. The PZ5128C/PZ5128N also includes an industry-standard, IEEE 1149.1, JTAG interface through which In-System Programming (ISP) and reprogramming of the device are supported.

Table 1. PZ5128C/PZ5128N Features

	PZ5128C/PZ5128N
Usable gates	4000
Maximum inputs	100
Maximum I/Os	96
Number of macrocells	128
Propagation delay (ns)	7.5
Packages	100-pin TQFP 128-pin LQFP

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ORDERING INFORMATION

ORDER CODE	DESCRIPTION	I/O COUNT	DRAWING NUMBER
PZ5128CS7BP	100-pin TQFP, 7.5ns t _{PD} , Commercial temp range, 5 volt power supply, ± 5%	80	SOT386-1
PZ5128CS10BP	100-pin TQFP, 10ns t _{PD} , Commercial temp range, 5 volt power supply, ± 5%	80	SOT386-1
PZ5128CS12BP	100-pin TQFP, 12ns t _{PD} , Commercial temp range, 5 volt power supply, ± 5%	80	SOT386-1
PZ5128NS10BP	100-pin TQFP, 10ns t _{PD} , Industrial temp range, 5 volt power supply, ± 10%	80	SOT386-1
PZ5128NS15BP	100-pin TQFP, 15ns t _{PD} , Industrial temp range, 5 volt power supply, ± 10%	80	SOT386-1
PZ5128CS7BE	128-pin LQFP, 7.5ns t _{PD} , Commercial temp range, 5 volt power supply, ± 5%	96	SOT425-1
PZ5128CS10BE	128-pin LQFP, 10ns t _{PD} , Commercial temp range, 5 volt power supply, ± 5%	96	SOT425-1
PZ5128CS12BE	128-pin LQFP, 12ns t _{PD} , Commercial temp range, 5 volt power supply, ± 5%	96	SOT425-1
PZ5128NS10BE	128-pin LQFP, 10ns t _{PD} , Industrial temp range, 5 volt power supply, ± 10%	96	SOT425-1
PZ5128NS15BE	128-pin LQFP, 15ns t _{PD} , Industrial temp range, 5 volt power supply, ± 10%	96	SOT425-1

XPLA™ ARCHITECTURE

Figure 1 shows a high level diagram of a 128 macrocell device implementing the XPLA™ architecture. The XPLA™ architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner™ family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

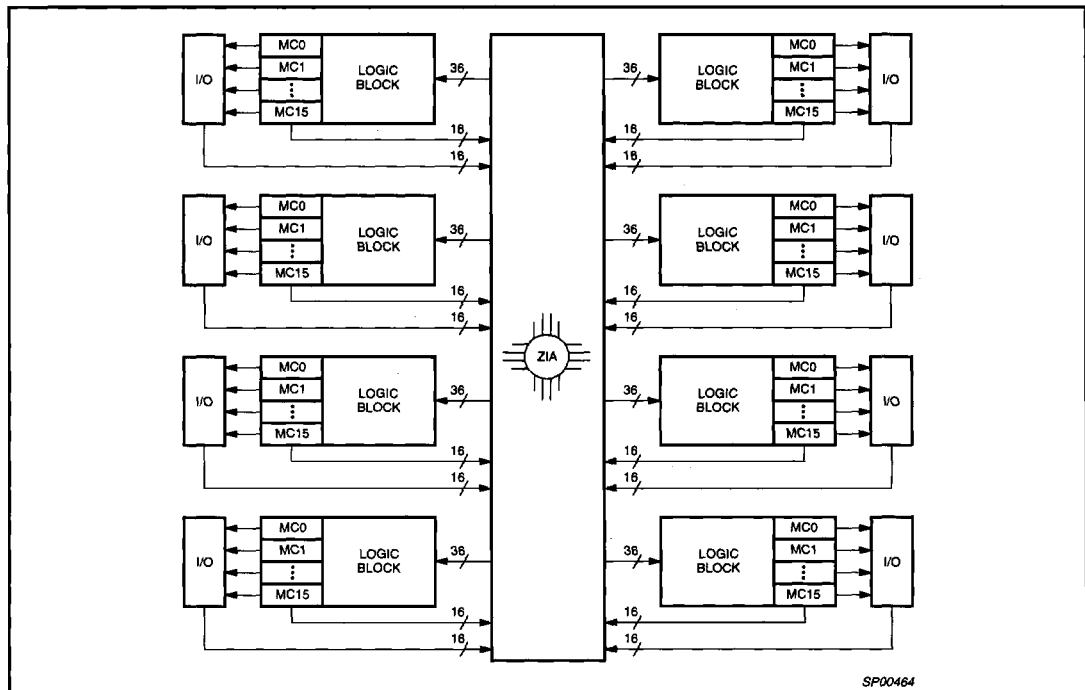


Figure 1. Philips XPLA CPLD Architecture

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Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. The 6 control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. In addition, two of the control terms can be used as clock signals (see Macrocell Architecture section for details). The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has 5 dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the PZ5128C/PZ5128N device through the PAL array is 7.5ns. If a macrocell needs more than 5 product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using 1 or all 32 PLA product terms is just 2ns. So the total pin-to-pin t_{PD} for the PZ5128C/PZ5128N using 6 to 37 product terms is 9.5ns (7.5ns for the PAL + 2ns for the PLA).

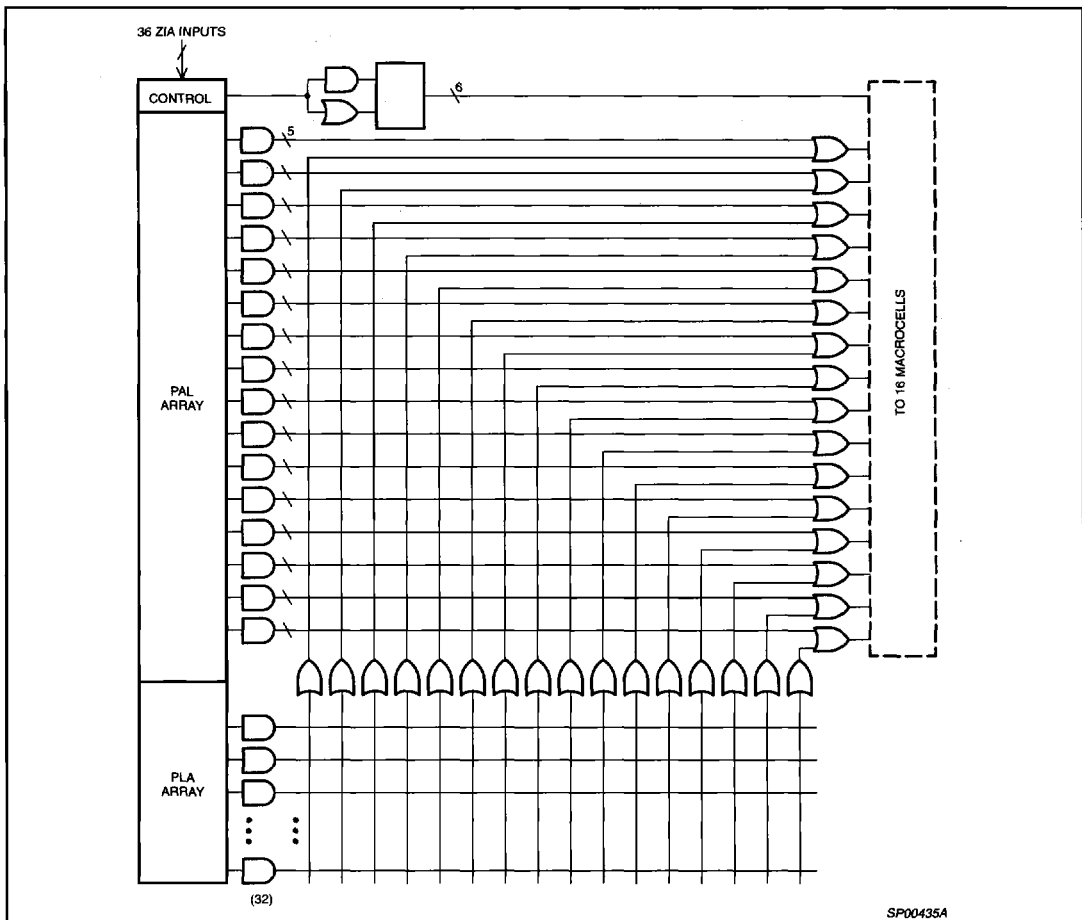


Figure 2. Philips XPLA Logic Block Architecture

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Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner™ PZ5128C/PZ5128N. The macrocell can be configured as either a D or T type flip-flop or a combinatorial logic function. A D-type flip-flop is generally more useful for implementing state machines and data buffering while a T-type flip-flop is generally more useful in implementing counters. Each of these flip-flops can be clocked from any one of six sources. Four of the clock sources (CLK0, CLK1, CLK2, CLK3) are connected to low-skew, device-wide clock networks designed to preserve the integrity of the clock signal by reducing skew between rising and falling edges. Clock 0 (CLK0) is designated as a "synchronous" clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can be used as "synchronous" clocks that are driven by an external source, or as "asynchronous" clocks that are driven by a macrocell equation. CLK0, CLK1, CLK2 and CLK3 can clock the macrocell flip-flops on either the rising edge or the falling edge of the clock signal. The other clock sources are two of the six control terms (CT2 and CT3) provided in each logic block. These clocks can be individually configured as either a PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. The timing for asynchronous and control term clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced. Please see the application note titled "Understanding CoolRunner Clocking Options" for more detail.

The six control terms of each logic block are used to control the asynchronous Preset/Reset of the flip-flops and the enable/disable of the output buffers in each macrocell. Control terms CT0 and CT1

are used to control the asynchronous Preset/Reset of the macrocell's flip-flop. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied, and that the Preset/Reset feature for each macrocell can also be disabled. Control terms CT2 and CT3 can be used as a clock signal to the flip-flops of the macrocells, and as the Output Enable of the macrocell's output buffer. Control terms CT4 and CT5 can be used to control the Output Enable of the macrocell's output buffer. Having four dedicated Output Enable control terms ensures that the CoolRunner™ devices are PCI compliant. The output buffers can also be always enabled or always disabled. All CoolRunner™ devices also provide a Global Tri-State (GTS) pin, which, when enabled and pulled Low, will 3-State all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails Testing".

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin feedback path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-States and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated (see the section on Terminations in this data sheet and the Application Note *Terminating Unused CoolRunner™ I/O Pins*).

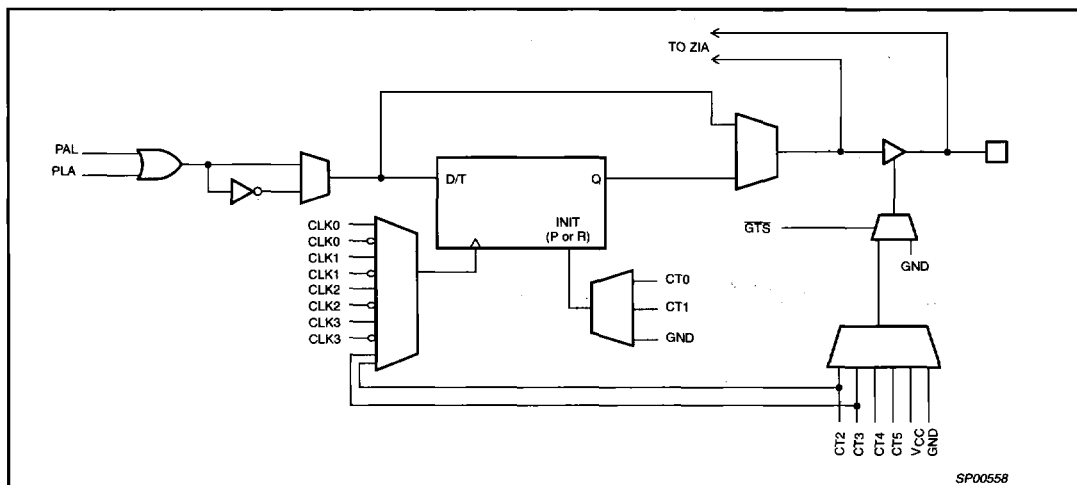


Figure 3. PZ5128C/PZ5128N Macrocell Architecture

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Simple Timing Model

Figure 4 shows the CoolRunner™ Timing Model. The CoolRunner™ timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD} , t_{SU} , and t_{CO} . In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA™ architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ CPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 2 showing the I_{DD} vs. Frequency of our PZ5128C/PZ5128N TotalCMOS™ CPLD (data taken w/eight up/down, loadable 16 bit counters @5V, 25°C).

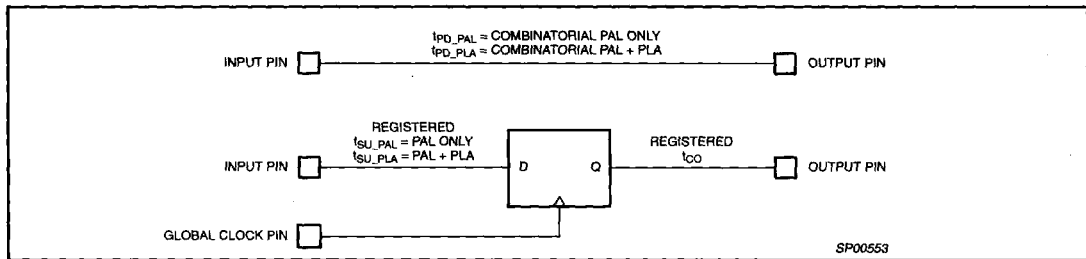


Figure 4. CoolRunner™ Timing Model

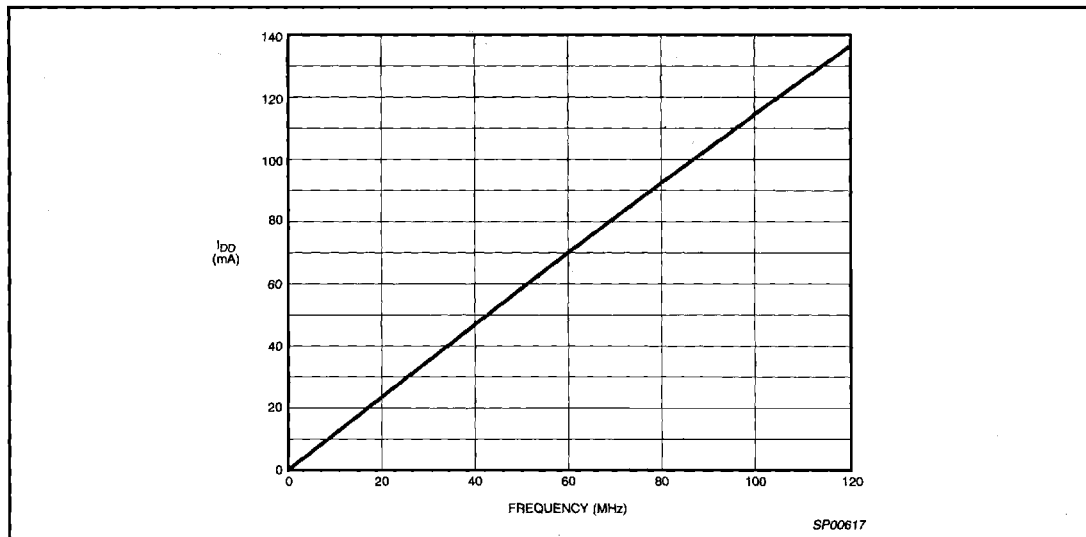


Figure 5. I_{DD} vs. Frequency @ $V_{DD} = 5.0V, 25^{\circ}C$

Table 2. I_{DD} vs. Frequency

$V_{DD} = 5.00V$

FREQUENCY (MHz)	0	1	20	40	60	80	100	120
Typical I_{DD} (mA)	0.048	1.281	23.55	46.93	70.05	92.45	114.4	136.2

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JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. The Philips PZ5128C/PZ5128N devices use the JTAG Interface for In-System Programming/Reprogramming. Although only a subset of the full JTAG command set is implemented (see Table 5), the devices are fully capable of sitting in a JTAG scan chain.

The Philips PZ5128C/PZ5128N's JTAG interface includes a TAP Port defined by the IEEE 1149.1 JTAG Specification. As implemented in the Philips PZ5128C/PZ5128N, the TAP Port includes four of the five pins (refer to Table 3) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST* (Test Reset). TRST* is considered an optional signal, since it is not actually required to perform BST or ISP. The Philips PZ5128C/PZ5128N saves an I/O pin for general purpose use by not implementing the optional TRST* signal in the JTAG interface. Instead, the Philips PZ5128C/PZ5128N supports the test reset functionality through the use of its power up reset circuit, which is included in all Philips CPLDs. The pins associated with the TAP Port should connect to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

In the Philips PZ5128C/PZ5128N, the four mandatory JTAG pins each require a unique, dedicated pin on the device. The devices

come from the factory with these I/O pins set to perform JTAG functions, but through the software, the final function of these pins can be controlled. If the end application will require the device to be reprogrammed at some future time with ISP, then the pins can be left as dedicated JTAG functions, which means they are not available for use as general purpose I/O pins. However, unlike competing CPLDs, the Philips PZ5128C/PZ5128N allow the macrocells associated with these pins to be used as buried logic when the JTAG/ISP function is enabled. This is the default state for the software, and no action is required to leave these pins enabled for the JTAG/ISP functions. If, however, JTAG/ISP is not required in the end application, the software can specify that this function be turned off and that these pins be used as general purpose I/O. Because the devices initially have the JTAG/ISP functions enabled, the JEDEC file can be downloaded into the device once, after which the JTAG/ISP pins will become general purpose I/O. This feature is good for manufacturing because the devices can be programmed during test and assembly of the end product and yet still use all of the I/O pins after the programming is done. It eliminates the need for a costly, separate programming step in the manufacturing process. Of course, if the JTAG/ISP function is never required, this feature can be turned off in the software and the device can be programmed with an industry-standard programmer, leaving the pins available for I/O functions. Table 4 defines the dedicated pins used by the four mandatory JTAG signals for each of the PZ5128C/PZ5128N package types.

Table 3. JTAG Pin Description

PIN	NAME	DESCRIPTION
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

Table 4. PZ5128C/PZ5128N JTAG Pinout by Package Type

DEVICE	(PIN NUMBER / MACROCELL #)			
	TCK	TMS	TDI	TDO
PZ5128C/PZ5128N				
100-pin TQFP	62/F15	15/C15	4/B15	73/G15
128-pin LQFP	82/F15	21/C15	8/B15	95/G15

Table 5. PZ5128C/PZ5128N Low-Level JTAG Boundary-Scan Commands

INSTRUCTION (Instruction Code) Register Used	DESCRIPTION
Bypass (1111) Bypass Register	Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.
Idcode (0001) Boundary-Scan Register	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.

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5-Volt, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
 - Faster time-to-market
 - Debug partitioning and simplified prototyping
 - Printed circuit board reconfiguration during debug
 - Better device and board level testing
- Manufacturing
 - Multi-Functional hardware
 - Reconfigurability for Test
 - Eliminates handling of “fine lead-pitch” components for programming
 - Reduced Inventory and manufacturing costs
 - Improved quality and reliability
- Field Support
 - Easy remote upgrades and repair
 - Support for field configuration, re-configuration, and customization

The Philips PZ5128C/PZ5128N allows for 5-Volt, in-system programming/reprogramming of its EEPROM cells via its JTAG interface. An on-chip charge pump eliminates the need for externally-provided superelevations, so that the PZ5128C/PZ5128N may be easily programmed on the circuit board using only the 5-volt supply required by the device for normal operation. A set of low-level ISP basic commands implemented in the PZ5128C/PZ5128N enable this feature. The ISP commands implemented in the Philips PZ5128C/PZ5128N are specified in Table 6. Please note that an ENABLE command must precede all ISP commands **unless** an ENABLE command has already been given for a preceding ISP command.

Terminations

The CoolRunner™ PZ5128C/PZ5128N CPLDs are TotalCMOS™ devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. The PZ5128C/PZ5128N CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-downs are automatically activated by the fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. We recommend that any unused I/O pins on the PZ5128C/PZ5128N device be left unconnected.

There are no on-chip pull-down structures associated with the dedicated input pins. Philips recommends that any unused dedicated inputs be terminated with external 10kΩ pull-up resistors. These pins can be directly connected to V_{CC} or GND, but using the external pull-up resistors maintains maximum design flexibility should one of the unused dedicated inputs be needed due to future design changes.

When using the JTAG/ISP functions, it is also recommended that 10kΩ pull-up resistors be used on each of the pins associated with the four mandatory JTAG signals. Letting these signals float can cause the voltage on TMS to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times. See the application notes *JTAG and ISP in Philips Devices and Terminating CoolRunner™ I/O Pins* for more information.

Table 6. Low Level ISP Commands

INSTRUCTION (Register Used)	INSTRUCTION CODE	DESCRIPTION
Enable (ISP Shift Register)	1001	Enables the Erase, Program, and Verify commands. Using the ENABLE instruction before the Erase, Program, and Verify instructions allows the user to specify the outputs the device using the JTAG Boundary-Scan SAMPLE/PRELOAD command.
Erase (ISP Shift Register)	1010	Erases the entire EEPROM array. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Program (ISP Shift Register)	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Verify (ISP Shift Register)	1100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The outputs during this operation can be defined by the user.

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JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLD's and other integrated circuits. The Philips PZ5128C/PZ5128N supports the following methods:

- PC Parallel Port
- Workstation or PC Serial Port
- Embedded Processor

- Automated Test Equipment
- Third party Programmers
- High-End ISP Tools

For more details on JTAG and ISP for the PZ5128C/PZ5128N, refer to the related application note: *JTAG and ISP in Philips CPLDs*.

Table 7. Programming Specifications

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Parameters				
V _{CCP}	V _{CC} supply program/verify	4.5	5.5	V
I _{CCP}	I _{CC} limit program/verify		200	mA
V _{IH}	Input voltage (High)	2.0		V
V _{IL}	Input voltage (Low)		0.8	V
V _{SOL}	Output voltage (Low)		0.5	V
V _{SOH}	Output voltage (High)	2.4		V
TDO_I _{OL}	Output current (Low)	12		mA
TDO_I _{OH}	Output current (High)	-12		mA
AC Parameters				
f _{MAX}	TCK maximum frequency	10		MHz
PWE	Pulse width erase	100		ms
PWP	Pulse width program	10		ms
PWV	Pulse width verify	10		μs
INIT	Initialization time	100		μs
TMS_SU	TMS setup time before TCK ↑	10		ns
TDI_SU	TDI setup time before TCK ↑	10		ns
TMS_H	TMS hold time after TCK ↑	20		ns
TDI_H	TDI hold time after TCK ↑	20		ns
TDO_CO	TDO valid after TCK ↓		30	ns

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DD}	Supply voltage ²	-0.5	7.0	V
V _I	Input voltage	-1.2	V _{DD} +0.5	V
V _{OUT}	Output voltage	-0.5	V _{DD} +0.5	V
I _{IN}	Input current	-30	30	mA
I _{OUT}	Output current	-100	100	mA
T _J	Maximum junction temperature	-40	150	°C
T _{str}	Storage temperature	-65	150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

OPERATING RANGE

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to +70°C	5.0 ±5% V
Industrial	-40 to +85°C	5.0 ±10% V

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DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICESCommercial: $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +70^{\circ}\text{C}$; $4.75\text{V} \leq V_{\text{DD}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	$V_{\text{DD}} = 4.75\text{V}$		0.8	V
V_{IH}	Input voltage high	$V_{\text{DD}} = 5.25\text{V}$	2.0		V
V_{I}	Input clamp voltage	$V_{\text{DD}} = 4.75\text{V}$, $I_{\text{IN}} = -18\text{mA}$		-1.2	V
V_{OL}	Output voltage low	$V_{\text{DD}} = 4.75\text{V}$, $I_{\text{OL}} = 12\text{mA}$		0.5	V
V_{OH}	Output voltage high	$V_{\text{DD}} = 4.75\text{V}$, $I_{\text{OH}} = -12\text{mA}$	2.4		V
I_{I}	Input leakage current	$V_{\text{IN}} = 0$ to V_{DD}	-10	10	μA
I_{OZ}	3-Stated output leakage current	$V_{\text{IN}} = 0$ to V_{DD}	-10	10	μA
I_{DDO}^1	Standby current	$V_{\text{DD}} = 5.25\text{V}$, $T_{\text{amb}} = 0^{\circ}\text{C}$		100	μA
$I_{\text{DDO}}^{1,2}$	Dynamic current	$V_{\text{DD}} = 5.25\text{V}$, $T_{\text{amb}} = 0^{\circ}\text{C}$ @ 1MHz		3	mA
		$V_{\text{DD}} = 5.25\text{V}$, $T_{\text{amb}} = 0^{\circ}\text{C}$ @ 50MHz		75	mA
I_{OS}	Short circuit output current ³	1 pin at a time for no longer than 1 second	-50	-200	mA
C_{IN}	Input pin capacitance ³	$T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$		8	pF
C_{CLK}	Clock input capacitance ³	$T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$	5	12	pF
$C_{\text{I/O}}$	I/O pin capacitance ³	$T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$		10	pF

NOTES:

- See Table 2 on page 168 for typical values.
- This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
- Typical values, not tested.

AC ELECTRICAL CHARACTERISTICS¹ FOR COMMERCIAL GRADE DEVICESCommercial: $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +70^{\circ}\text{C}$; $4.75\text{V} \leq V_{\text{DD}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	7		10		12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{\text{PD_PAL}}$	Propagation delay time, input (or feedback node) to output through PAL	2	7.5	2	10	2	12	ns
$t_{\text{PD_PLA}}$	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	9.5	3	12	3	14.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	5.5	2	7	2	8	ns
$t_{\text{SU_PAL}}$	Setup time (from input or feedback node) through PAL	4.5		7		8		ns
$t_{\text{SU_PLA}}$	Setup time (from input or feedback node) through PAL + PLA	6.5		9		10.5		ns
t_{H}	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		4		ns
t_{CL}	Clock Low time	3		4		4		ns
t_{R}	Input Rise time		20		20		20	ns
t_{F}	Input Fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate ² $1/(t_{\text{CH}} + t_{\text{CL}})$	167		125		125		MHz
f_{MAX2}	Maximum internal frequency ² $1/(t_{\text{SUPAL}} + t_{\text{CF}})$	111		80		69		MHz
f_{MAX3}	Maximum external frequency ² $1/(t_{\text{SUPAL}} + t_{\text{CO}})$	95		71		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
$t_{\text{PDF_PAL}}$	Input (or feedback node) to internal feedback node delay time through PAL	2	6	2	8.5	2	10.5	ns
$t_{\text{PDF_PLA}}$	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	8	3	10.5	3	13	ns
t_{CF}	Clock to internal feedback node delay time		4		5.5		6.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50		50	μs
t_{ER}	Input to output disable ^{2,3}		9		12		15	ns
t_{EA}	Input to output valid ²		9		12		15	ns
t_{RP}	Input to register preset ²		11		12.5		15	ns
t_{RR}	Input to register reset ²		11		12.5		15	ns

NOTES:

- Specifications measured with one output switching. See Figure 6 and Table 8 for derating.
- This parameter guaranteed by design and characterization, not by test.
- Output $C_{\text{L}} = 5\text{pF}$.

128 macrocell CPLD with enhanced clocking

PZ5128C/PZ5128N

DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICESIndustrial: $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq +85^{\circ}\text{C}$; $4.5\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	$V_{\text{DD}} = 4.5\text{V}$		0.8	V
V_{IH}	Input voltage high	$V_{\text{DD}} = 5.5\text{V}$	2.0		V
V_{I}	Input clamp voltage	$V_{\text{DD}} = 4.5\text{V}$, $I_{\text{IN}} = -18\text{mA}$		-1.2	V
V_{OL}	Output voltage low	$V_{\text{DD}} = 4.5\text{V}$, $I_{\text{OL}} = 12\text{mA}$		0.5	V
V_{OH}	Output voltage high	$V_{\text{DD}} = 4.5\text{V}$, $I_{\text{OH}} = -12\text{mA}$	2.4		V
I_{I}	Input leakage current	$V_{\text{IN}} = 0$ to V_{DD}	-10	10	μA
I_{OZ}	3-States output leakage current	$V_{\text{IN}} = 0$ to V_{DD}	-10	10	μA
I_{DDO}^1	Standby current	$V_{\text{DD}} = 5.5\text{V}$, $T_{\text{amb}} = -40^{\circ}\text{C}$		125	μA
$I_{\text{DDD}}^{1,2}$	Dynamic current	$V_{\text{DD}} = 5.5\text{V}$, $T_{\text{amb}} = -40^{\circ}\text{C}$ @ 1MHz		4	mA
		$V_{\text{DD}} = 5.5\text{V}$, $T_{\text{amb}} = -40^{\circ}\text{C}$ @ 50MHz		80	mA
I_{OS}	Short circuit output current ³	1 pin at a time for no longer than 1 second	-50	-230	mA
C_{IN}	Input pin capacitance ³	$T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$		8	pF
C_{CLK}	Clock input capacitance ³	$T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$	5	12	pF
$C_{\text{I/O}}$	I/O pin capacitance ³	$T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$		10	pF

NOTES:

- See Table 2 on page 168 for typical values.
- This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
- Typical values, not tested.

AC ELECTRICAL CHARACTERISTICS¹ FOR INDUSTRIAL GRADE DEVICESIndustrial: $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq +85^{\circ}\text{C}$; $4.5\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$

SYMBOL	PARAMETER	10		15		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{\text{PD_PAL}}$	Propagation delay time, input (or feedback node) to output through PAL	2	10	2	15	ns
$t_{\text{PD_PLA}}$	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	12	3	17.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7	2	8	ns
$t_{\text{SU_PAL}}$	Setup time (from input or feedback node) through PAL	6		8		ns
$t_{\text{SU_PLA}}$	Setup time (from input or feedback node) through PAL + PLA	10		10.5		ns
t_{H}	Hold time		0		0	ns
t_{CH}	Clock High time	5		5		ns
t_{CL}	Clock Low time	5		5		ns
t_{R}	Input Rise time		20		20	ns
t_{F}	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate ² $1/(t_{\text{CH}} + t_{\text{CL}})$	100		100		MHz
f_{MAX2}	Maximum internal frequency ² $1/(t_{\text{SUPAL}} + t_{\text{CF}})$	71		69		MHz
f_{MAX3}	Maximum external frequency ² $1/(t_{\text{SUPAL}} + t_{\text{CO}})$	66		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
$t_{\text{PDF_PAL}}$	Input (or feedback node) to internal feedback node delay time through PAL	2	8.5	2	13.5	ns
$t_{\text{PDF_PLA}}$	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	10.5	3	16	ns
t_{CF}	Clock to internal feedback node delay time		6		6.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50	μs
t_{ER}	Input to output disable ^{2,3}		15		15	ns
t_{EA}	Input to output valid ²		15		15	ns
t_{RP}	Input to register preset ²		15		17	ns
t_{RR}	Input to register reset ²		15		17	ns

NOTES:

- Specifications measured with one output switching. See Figure 6 and Table 8 for derating.
- This parameter guaranteed by design and characterization, not by test.
- Output $C_{\text{L}} = 5\text{pF}$.

128 macrocell CPLD with enhanced clocking

PZ5128C/PZ5128N

SWITCHING CHARACTERISTICS

COMPONENT	VALUES
R1	390Ω
R2	390Ω
C1	35pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Closed
t_p	Closed	Closed

NOTE: For t_{PZH} and t_{PZL} C = 5pF, and 3-State levels are measured 0.5V from steady state active level.

SP00618

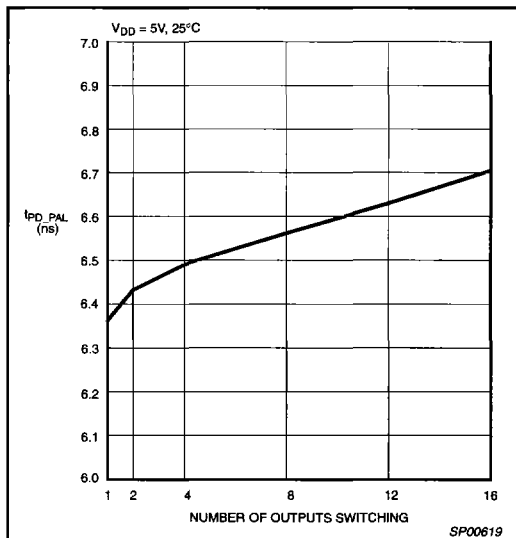


Figure 6. t_{PD_PAL} vs. Outputs Switching

VOLTAGE WAVEFORM

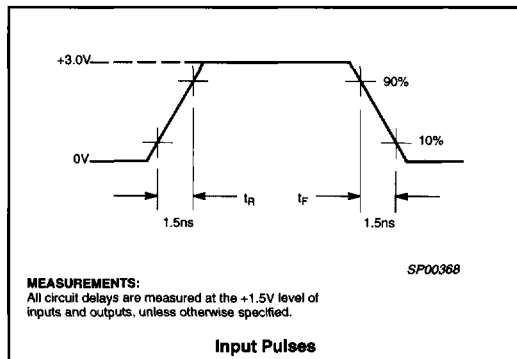


Table 8. t_{PD_PAL} vs. Number of Outputs Switching

V_{DD} = 5.00V, 25°C

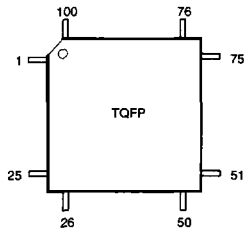
NUMBER OF OUTPUTS	1	2	4	8	12	16
Typical (ns)	6.362	6.432	6.49	6.562	6.63	6.705

128 macrocell CPLD with enhanced clocking

PZ5128C/PZ5128N

PIN DESCRIPTIONS

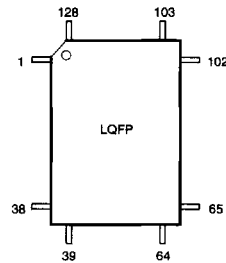
100-Pin Thin Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O-A2	35	I/O-D4	69	I/O-G8
2	I/O-A0	36	I/O-D2	70	I/O-G10
3	V _{DD}	37	I/O-D0/CLK2	71	I/O-G12
4	I/O-B15 (TDI)	38	GND	72	I/O-G13
5	I/O-B13	39	V _{DD}	73	I/O-G15 (TDO)
6	I/O-B12	40	I/O-E0/CLK1	74	GND
7	I/O-B10	41	I/O-E2	75	I/O-H0
8	I/O-B8	42	I/O-E4	76	I/O-H2
9	I/O-B7	43	GND	77	I/O-H4
10	I/O-B5	44	I/O-E5	78	I/O-H5
11	GND	45	I/O-E7	79	I/O-H7
12	I/O-B4	46	I/O-E8	80	I/O-H8
13	I/O-B2	47	I/O-E10	81	I/O-H10
14	I/O-B0	48	I/O-E12	82	V _{DD}
15	I/O-C15 (TMS)	49	I/O-E13	83	I/O-H12
16	I/O-C13	50	I/O-E15	84	I/O-H13
17	I/O-C12	51	V _{DD}	85	I/O-H15
18	V _{DD}	52	I/O-F0	86	GND
19	I/O-C10	53	I/O-F2	87	IN0/CLK0
20	I/O-C8	54	I/O-F4	88	IN2-gtsn
21	I/O-C7	55	I/O-F5	89	IN1
22	I/O-C5	56	I/O-F7	90	IN3
23	I/O-C4	57	I/O-F8	91	V _{DD}
24	I/O-C2	58	I/O-F10	92	I/O-A15/CLK3
25	I/O-C0	59	GND	93	I/O-A13
26	GND	60	I/O-F12	94	I/O-A12
27	I/O-D15	61	I/O-F13	95	GND
28	I/O-D13	62	I/O-F15 (TCK)	96	I/O-A10
29	I/O-D12	63	I/O-G0	97	I/O-A8
30	I/O-D10	64	I/O-G2	98	I/O-A7
31	I/O-D8	65	I/O-G4	99	I/O-A5
32	I/O-D7	66	V _{DD}	100	I/O-A4
33	I/O-D5	67	I/O-G5		
34	V _{DD}	68	I/O-G7		

SP00485

128-Pin Low Profile Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O-A3	44	I/O-D7	87	V _{DD}
2	I/O-A2	45	I/O-D5	88	I/O-G5
3	I/O-A0	46	V _{DD}	89	I/O-G7
4	NC	47	I/O-D4	90	I/O-G8
5	NC	48	I/O-D3	91	I/O-G10
6	NC	49	I/O-D2	92	I/O-G11
7	V _{DD}	50	I/O-D0/CLK2	93	I/O-G12
8	I/O-B15 (TDI)	51	GND	94	I/O-G13
9	I/O-B13	52	V _{DD}	95	I/O-G15 (TDO)
10	I/O-B12	53	I/O-E0/CLK1	96	GND
11	I/O-B11	54	I/O-E2	97	NC
12	I/O-B10	55	I/O-E3	98	NC
13	I/O-B8	56	I/O-E4	99	NC
14	I/O-B7	57	GND	100	I/O-H0
15	I/O-B5	58	I/O-E5	101	I/O-H2
16	GND	59	I/O-E7	102	I/O-H3
17	I/O-B4	60	I/O-E8	103	I/O-H4
18	I/O-B3	61	I/O-E10	104	I/O-H5
19	I/O-B2	62	I/O-E11	105	I/O-H7
20	I/O-B0	63	I/O-E12	106	I/O-H8
21	I/O-C15 (TMS)	64	I/O-E13	107	I/O-H10
22	I/O-C13	65	I/O-E15	108	V _{DD}
23	I/O-C12	66	V _{DD}	109	I/O-H11
24	I/O-C11	67	I/O-F0	110	I/O-H12
25	V _{DD}	68	NC	111	I/O-H13
26	I/O-C10	69	NC	112	I/O-H15
27	I/O-C8	70	NC	113	GND
28	I/O-C7	71	I/O-F2	114	IN0/CLK0
29	I/O-C5	72	I/O-F3	115	IN2-gtsn
30	I/O-C4	73	I/O-F4	116	IN1
31	I/O-C3	74	I/O-F5	117	IN3
32	I/O-C2	75	I/O-F7	118	V _{DD}
33	NC	76	I/O-F8	119	I/O-A15/CLK3
34	NC	77	I/O-F10	120	I/O-A13
35	NC	78	GND	121	I/O-A12
36	I/O-C0	79	I/O-F11	122	I/O-A11
37	GND	80	I/O-F12	123	GND
38	I/O-D15	81	I/O-F13	124	I/O-A10
39	I/O-D13	82	I/O-F15 (TCK)	125	I/O-A8
40	I/O-D12	83	I/O-G0	126	I/O-A7
41	I/O-D11	84	I/O-G2	127	I/O-A5
42	I/O-D10	85	I/O-G3	128	I/O-A4
43	I/O-D8	86	I/O-G4		

SP00469A

128 macrocell CPLD with enhanced clocking

PZ5128C/PZ5128N

Package Thermal Characteristics

Philips Semiconductors uses the Temperature Sensitive Parameter (TSP) method to test thermal resistance. This method meets Mil-Std-883C Method 1012.1 and is described in Philips 1995 IC Package Databook. Thermal resistance varies slightly as a function of input power. As input power increases, thermal resistance changes approximately 5% for a 100% change in power.

Figure 7 is a derating curve for the change in Θ_{JA} with airflow based on wind tunnel measurements. It should be noted that the wind flow dynamics are more complex and turbulent in actual applications than in a wind tunnel. Also, the test boards used in the wind tunnel contribute significantly to forced convection heat transfer, and may not be similar to the actual circuit board, especially in size.

Package	Θ_{JA}
100-pin TQFP	47.4 °C/W
128-pin LQFP	45.0 °C/W

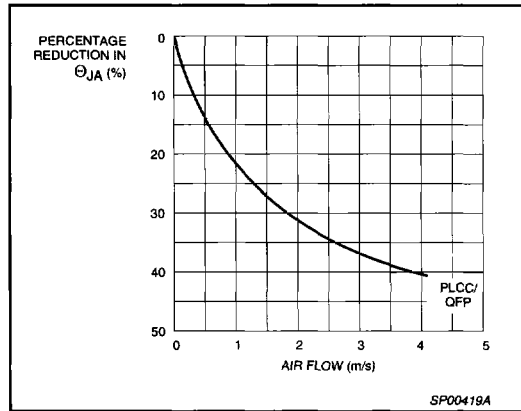


Figure 7. Average Effect of Airflow on Θ_{JA}