MCM36M32
MCM36M64

Product Preview

32K x 36 and 64K x 36 Bit BurstRAM™ Synchronous Static RAM Module for the MC68040

With Burst Counter and Self-Timed Write

The MCM36M32/64 are 1M/2M Static RAM Modules organized 32,768/65,536 words of 36 bits designed to provide a burstable, high performance, secondary cache for the MC68040. The module is a 80-lead single-in-line memory module (SIMM) consisting of four/eight MCM62940A packaged in 44-lead PLCC and mounted on a printed circuit board along with four/eight decoupling capacitors.

The MCM62940A is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the MC68040 microprocessor. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ8), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive-edge-triggered non-inverting registers.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM62940A (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 12/14/19/24 ns Max and Cycle Times: 20/20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- Fully TTL-Compatible

PIN NAMES			
A0 – A14	Address Inputs	$\overline{BAA}$	Burst Address Advance
K	Clock	$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{W}$1 – $\overline{W}$4	Write Enables	DQ0 – DQ35	Data Input/Output
$\overline{G}$1, $\overline{G}$2	Output Enables	V_{CC}	+ 5 V Power Supply
S0, S1	Chip Selects	V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device

PIN ASSIGNMENT
80 PIN SIMM
64K x 36 / 32K x 36

PD0	2	1	V_{SS}
PD2	4	3	PD1
DQ0	6	5	DQ1
DQ2	8	7	DQ3
DQ4	10	9	DQ5
V_{CC}	12	11	DQ7
DQ6	14	13	A0
DQ8	16	15	A1
A3	18	17	A2
A5	20	19	A4
A6	22	21	V_{SS}
A7	24	23	DQ9
DQ10	26	25	DQ11
DQ12	28	27	DQ13
DQ14	30	29	DQ15
DQ16	32	31	DQ17
V_{CC}	34	33	$\overline{BAA}$
$\overline{W}$1	36	35	$\overline{W}$2
$\overline{G}$1	38	37	NC / $\overline{G}$2*
*$\overline{S}$1 / $\overline{S}$	40	39	NC / S0*
K	42	41	V_{CC}
NC	44	43	NC
NC	46	45	NC
$\overline{W}$3	48	47	$\overline{W}$4
$\overline{TSP}$	50	49	$\overline{TSC}$
DQ18	52	51	V_{CC}
DQ20	54	53	DQ19
DQ22	56	55	DQ21
DQ24	58	57	DQ23
DQ26	60	59	DQ25
V_{SS}	62	61	A8
A10	64	63	A9
A12	66	65	A11
A14	68	67	A13
NC	70	69	DQ27
DQ28	72	71	DQ29
DQ30	74	73	V_{CC}
DQ32	76	75	DQ31
DQ34	78	77	DQ33
V_{SS}	80	79	DQ35

*64Kx36 pin designation.

BurstRAM is a trademark of Motorola, Inc.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice

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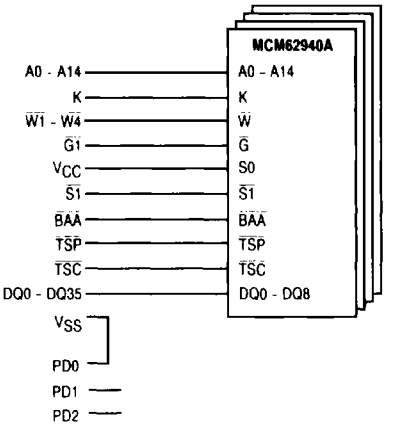
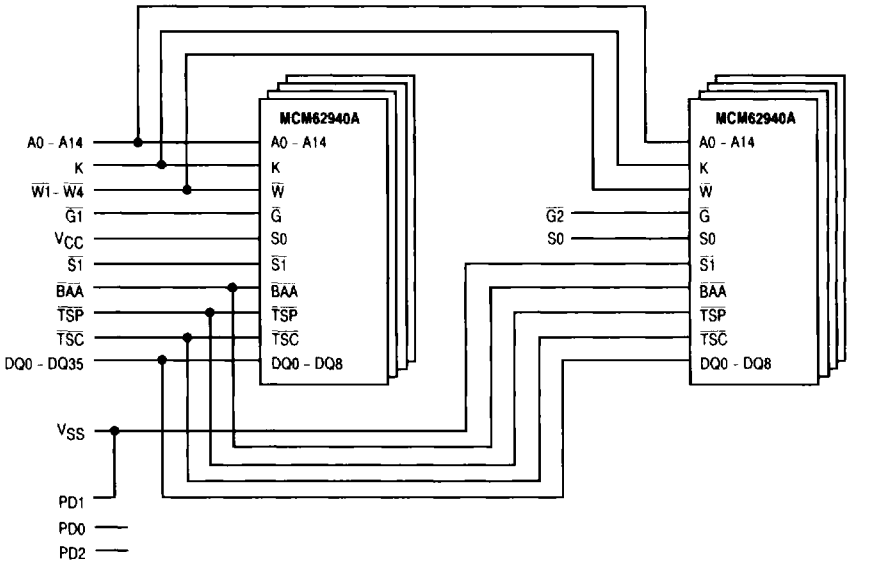
FUNCTIONAL BLOCK DIAGRAM

MCM36M32
32K x 36 VERSION



MCM36M64
64K x 36 VERSION



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