IS61NSCS25672
IS61NSCS51236

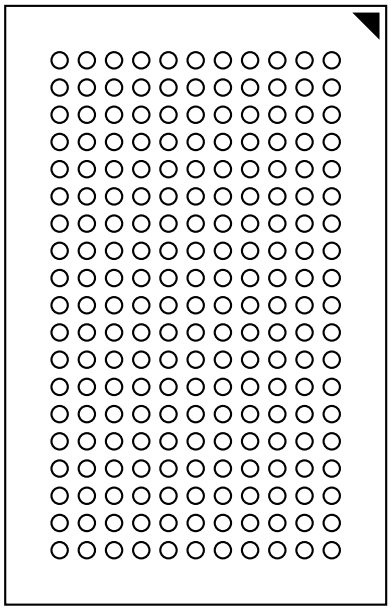
ISSI®

ADVANCE INFORMATION
JUNE 2002

ΣRAM 256K X 72, 512K X 36
18MB SYNCHRONOUS SRAM

FEATURES

- JEDEC SigmaRam pinout and package standard
- Single 1.8V power supply (V_{CC}): 1.7V (min) to 1.9V (max)
- Dedicated output supply voltage (V_{CCQ}): 1.8V or 1.5V typical
- LVCMOS-compatible I/O interface
- Common data I/O pins (DQs)
- Single Data Rate (SDR) data transfers
- Pipelined (PL) read operations
- Double Late Write (DLW) write operations
- Burst and non-burst read and write operations, selectable via dedicated control pin (ADV)
- Internally controlled Linear Burst address sequencing during burst operations
- Full read/write coherency
- Byte write capability
- Two cycle deselect
- Single-ended input clock (CLK)
- Data-referenced output clocks (CQ/$\overline{CQ}$)
- Selectable output driver impedance via dedicated control pin (ZQ)
- Echo clock outputs track data output drivers
- Depth expansion capability (2 or 4 banks) via programmable chip enables (E2, E3, EP2, EP3)
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 209 Ball (11x19), 1mm pitch, 14mm x 22mm Ball Grid Array (BGA) package



Bottom View
209-Ball, 14 mm x 22 mm BGA
1 mm Ball Pitch, 11 x 19 Ball Array

SIGMARAM FAMILY OVERVIEW

The IS61NSCS series ΣRAMs are built in compliance with the SigmaRAM pinout standard for synchronous SRAMs. The implementations are 18,874,368-bit (18Mb) SRAMs. These are the first in a family of wide, very low voltage CMOS I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

ISSI's ΣRAMs are offered in a number of configurations that emulate other synchronous SRAMs, such as Burst RAMs, NBT RAMs, Late Write, or Double Data Rate (DDR) SRAMs. The logical differences between the protocols employed by these RAMs hinge mainly on various combinations of address bursting, output data registering and write cueing. ΣRAMs allow a user to implement the interface protocol best suited to the task at hand.

This specific product is Common I/O, SDR, Double Late Write & Pipelined Read (same as Pipelined NBT) and in the family is identified as 1x1Dp.

FUNCTIONAL DESCRIPTION

Because SigmaRAM is a synchronous device, address, data Inputs, and read/write control inputs are captured on the rising edge of the input clock. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

Single data rate ΣRAMs incorporate a rising-edge-triggered output register. For read cycles, ΣRAM's output data is temporarily stored by the edge-triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

IS61NSCS series ΣRAMs are implemented with ISSI's high performance CMOS technology and are packaged in a 209-Ball BGA.

IS61NSCS25672 PINOUT

256K x 72 COMMON I/O—TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A (16M)	ADV	A (8M)	E3	A	DQb	DQb
B	DQg	DQg	$\overline{Bc}$	$\overline{Bg}$	NC	$\overline{W}$	A	$\overline{Bb}$	$\overline{Bf}$	DQb	DQb
C	DQg	DQg	$\overline{Bh}$	$\overline{Bd}$	NC (128M)	$\overline{E1}$	NC	$\overline{Be}$	$\overline{Ba}$	DQb	DQb
D	DQg	DQg	GND	NC	NC	MCL	NC	NC	GND	DQb	DQb
E	DQPg	DQPc	V_{CCQ}	V_{CCQ}	V_{CC}	V_{CC}	V_{CC}	V_{CCQ}	V_{CCQ}	DQPf	DQPb
F	DQc	DQc	GND	GND	GND	ZQ	GND	GND	GND	DQf	DQf
G	DQc	DQc	V_{CCQ}	V_{CCQ}	V_{CC}	EP2	V_{CC}	V_{CCQ}	V_{CCQ}	DQf	DQf
H	DQc	DQc	GND	GND	GND	EP3	GND	GND	GND	DQf	DQf
J	DQc	DQc	V_{CCQ}	V_{CCQ}	V_{CC}	M4	V_{CC}	V_{CCQ}	V_{CCQ}	DQf	DQf
K	CQ2	$\overline{CQ2}$	CLK	NC	GND	MCL	GND	NC	NC	$\overline{CQ1}$	CQ1
L	DQh	DQh	V_{CCQ}	V_{CCQ}	VCC	M2	V_{CC}	V_{CCQ}	V_{CCQ}	DQa	DQa
M	DQh	DQh	GND	GND	GND	M3	GND	GND	GND	DQa	DQa
N	DQh	DQh	V_{CCQ}	V_{CCQ}	VCC	MCH	V_{CC}	V_{CCQ}	V_{CCQ}	DQa	DQa
P	DQh	DQh	GND	GND	GND	MCL	GND	GND	GND	DQa	DQa
R	DQPd	DQPh	V_{CCQ}	V_{CCQ}	V_{CC}	V_{CC}	V_{CC}	V_{CCQ}	V_{CCQ}	DQPa	DQPe
T	DQd	DQd	GND	NC	NC	MCL	NC	NC	GND	DQe	DQe
U	DQd	DQd	NC	A	NC (64M)	A	NC (32M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

11 x 19 Ball BGA—14 x 22 mm^2 Body—1 mm Ball Pitch

IS61NSCS51236 PINOUT

512K x 36 COMMON I/O—TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A (16M)	ADV	A	E3	A	DQb	DQb
B	NC	NC	$\overline{Bc}$	NC	A (x36)	$\overline{W}$	A	$\overline{Bb}$	NC	DQb	DQb
C	NC	NC	NC	$\overline{Bd}$	NC (128M)	$\overline{E1}$	NC	NC	$\overline{Ba}$	DQb	DQb
D	NC	NC	GND	NC	NC	MCL	NC	NC	GND	DQb	DQb
E	NC	DQPc	V_{CCQ}	V_{CCQ}	V_{CC}	V_{CC}	V_{CC}	V_{CCQ}	V_{CCQ}	NC	DQPb
F	DQc	DQc	GND	GND	GND	ZQ	GND	GND	GND	NC	NC
G	DQc	DQc	V_{CCQ}	V_{CCQ}	V_{CC}	EP2	V_{CC}	V_{CCQ}	V_{CCQ}	NC	NC
H	DQc	DQc	GND	GND	GND	EP3	GND	GND	GND	NC	NC
J	DQc	DQc	V_{CCQ}	V_{CCQ}	V_{CC}	M4	V_{CC}	V_{CCQ}	V_{CCQ}	NC	NC
K	CQ2	$\overline{CQ2}$	CLK	NC	GND	MCL	GND	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	V_{CCQ}	V_{CCQ}	V_{CC}	M2	V_{CC}	V_{CCQ}	V_{CCQ}	DQa	DQa
M	NC	NC	GND	GND	GND	M3	GND	GND	GND	DQa	DQa
N	NC	NC	V_{CCQ}	V_{CCQ}	V_{CC}	MCH	V_{CC}	V_{CCQ}	V_{CCQ}	DQa	DQa
P	NC	NC	GND	GND	GND	MCL	GND	GND	GND	DQa	DQa
R	DQPd	NC	V_{CCQ}	V_{CCQ}	V_{CC}	V_{CC}	V_{CC}	V_{CCQ}	V_{CCQ}	DQPa	NC
T	DQd	DQd	GND	NC	NC	MCL	NC	NC	GND	NC	NC
U	DQd	DQd	NC	A	NC (64M)	A	NC (32M)	A	NC	NC	NC
V	DQd	DQd	A	A	A	A1	A	A	A	NC	NC
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

11 x 19 Ball BGA—14 x 22 mm^2 Body—1 mm Ball Pitch

PIN DESCRIPTION TABLE

Symbol	Pin Location	Description	Type	Comments
A	A3, A5, A7, A9, B7, U4, U6, U8, V3, V4, V5, V6, V7, V8, V9, W5, W6, W7	Address	Input	—
A	B5	Address	Input	x36 version
ADV	A6	Advance	Input	Active High
$\overline{Bx}$	B3, C9	Byte Write Enable	Input	Active Low (all versions)
$\overline{Bx}$	B8, C4	Byte Write Enable	Input	Active Low (x36 and x72 versions)
$\overline{Bx}$	B4, B9, C3, C8	Byte Write Enable	Input	Active Low (x72 version only)
CK	K3	Clock	Input	Active High
CQ	K1, K11	Echo Clock	Output	Active High
$\overline{CQ}$	K2, K10	Echo Clock	Output	Active Low
DQ	E2, F1, F2, G1, G2, H1, H2, J1, J2, L10, L11, M10, M11, N10, N11, P10, P11, R10 A10, A11, B10, B11, C10, C11, D10, D11, E11, R1, T1, T2, U1, U2, V1, V2, W1, W2	Data I/O Data I/O	Input/Output Input/Output	x36, and x72 versions
DQ	A1, A2, B1, B2, C1, C2, D1, D2, E1, E10, F10, F11, G10, G11, H10, H11, J10, J11, L1, L2, M1, M2, N1, N2, P1, P2, R2, R11, T10, T11, U10, U11, V10, V11, W10, W11	Data I/O	Input/Output	x72 version only
$\overline{E1}$	C6	Chip Enable	Input	Active Low
E2 & E3	A4, A8	Chip Enable	Input	Programmable Active High or Low
EP2 & EP3	G6, H6	Chip Enable Program Pin	Input	—
TCK	W9	Test Clock	Input	Active High
TDI	W4	Test Data In	Input	—
TDO	W8	Test Data Out	Output	—
TMS	W3	Test Mode Select	Input	—
M2, M3 & M4	L6, M6, J6	Mode Control Pins	Input	Must tie to High, Low, High
MCH	N6	Must Connect High	Input	—
MCL	D6, K6, P6,T6	Must Connect Low	Input	—

PIN DESCRIPTION TABLE

Symbol	Pin Location	Description	Type	Comments
NC	C5, D4, D5, D7, D8, K4, K8, K9, T4, T5, T7, T8, U3, U5, U7, U9	No Connect	—	Not connected to die (all versions)
NC	B5	No Connect	—	Not connected to die (x72 version)
NC	C7	No Connect	—	Not connected to die (x72/x36 versions)
NC	A1, A2, B1, B2, B4, B9, C1, C2, C3, C8, D1, D2, E1, E10, F10, F11, G10, G11, H10, H11, J10, J11, L1, L2, M1, M2, N1, N2, P1, P2, R2, R11, T10, T11, U10, U11, V10, V11, W10, W11	No Connect	—	Not connected to die (x36 version)
$\overline{W}$	B6	Write	Input	Active Low
V_{CC}	E5, E6, E7, G5, G7, J5, J7, L5, L7, N5, N7, R5, R6, R7	Core Power Supply	Input	1.8 V Nominal
V_{CCQ}	E3, E4, E8, E9, G3, G4, G8, G9, J3, J4, J8, J9 L3, L4, L8, L9, N3, N4 N8, N9, R3, R4, R8, R9	Output Driver Power Supply	Input	1.8 V or 1.5 V Nominal
GND	D3, D9, F3, F4, F5, F7, F8, F9, H3, H4, H5, H7, H8, H9, K5, K7, M3, M4, M5, M7, M8, M9, P3, P4, P5, P7, P8, P9, T3, T9	Ground	Input	—
ZQ	F6	Output Impedance Control	Input	Low = Low Impedance [High Drive] High = High Impedance [Low Drive] Default = High

BACKGROUND

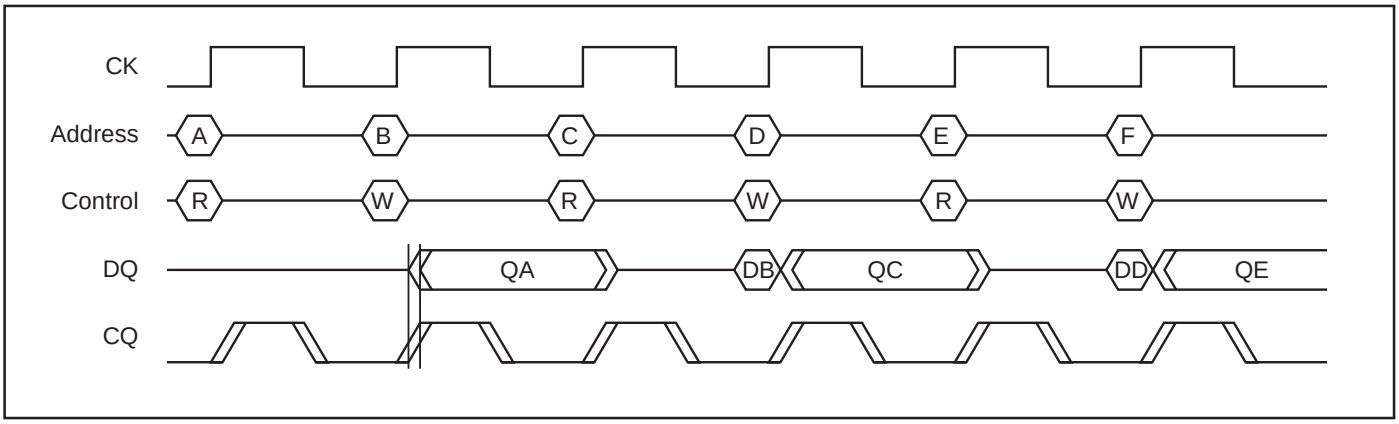
The central characteristics of the ISSI ΣRAMs are that they are extremely fast and consume very little power. Because both operating and interface power is low, ΣRAMs can be implemented in a wide (x72) configuration, providing very high single package bandwidth (in excess of 20 Gb/s in ordinary pipelined configuration) and very low random access time (~3 ns). The use of very low voltage circuits in the core and 1.8V or 1.5V interface voltages allow the speed, power and density performance of ΣRAMs.

Although the SigmaRAM family pinouts have been designed to support a number of different common read and write protocol options, not all SigmaRAM implementations will support all possible protocols. The following timing diagrams provide a quick comparison between read and write protocols options available in the context of the SigmaRAM standard. This data sheet covers the single data rate (non-DDR), Double Late Write, Pipelined Read SigmaRAM.

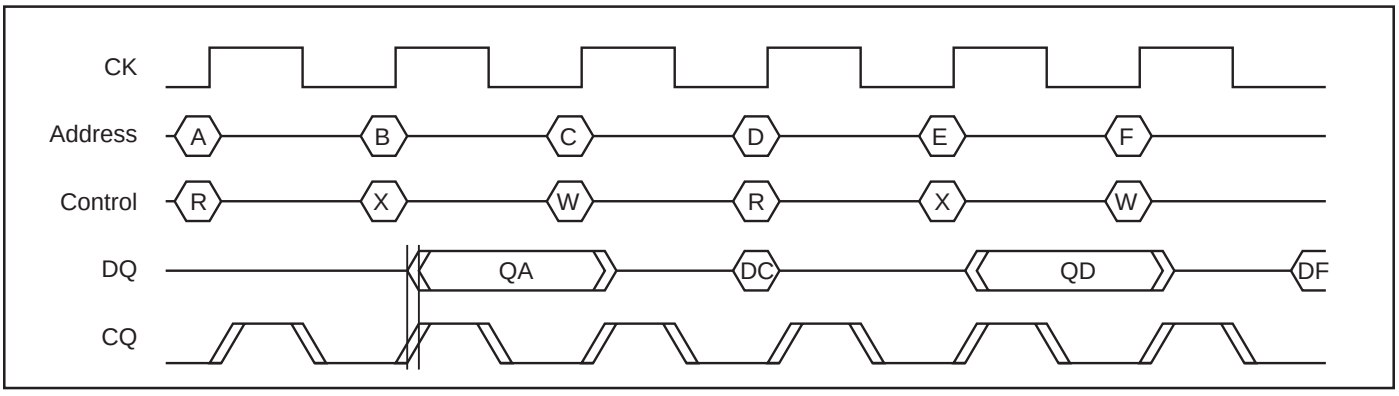
The character of the applications for fast synchronous SRAMs in networking systems are extremely diverse. ΣRAMs have been developed to address the diverse needs of the networking market in a manner that can be supported with a unified development and manufacturing infrastructure. ΣRAMs address each of the bus protocol options commonly found in networking systems. This allows the ΣRAM to find application in radical shrinks and speed-ups of existing networking chip sets that were designed for use with older SRAMs, like the NBT and Late Write, or Double Data Rate SRAMs, as well as with new chip sets and ASIC's that employ the Echo Clocks and realize the full potential of the ΣRAMs.

COMMON I/O SIGMARAM FAMILY MODE COMPARISON—LATE WRITE VS. DOUBLE LATE WRITE

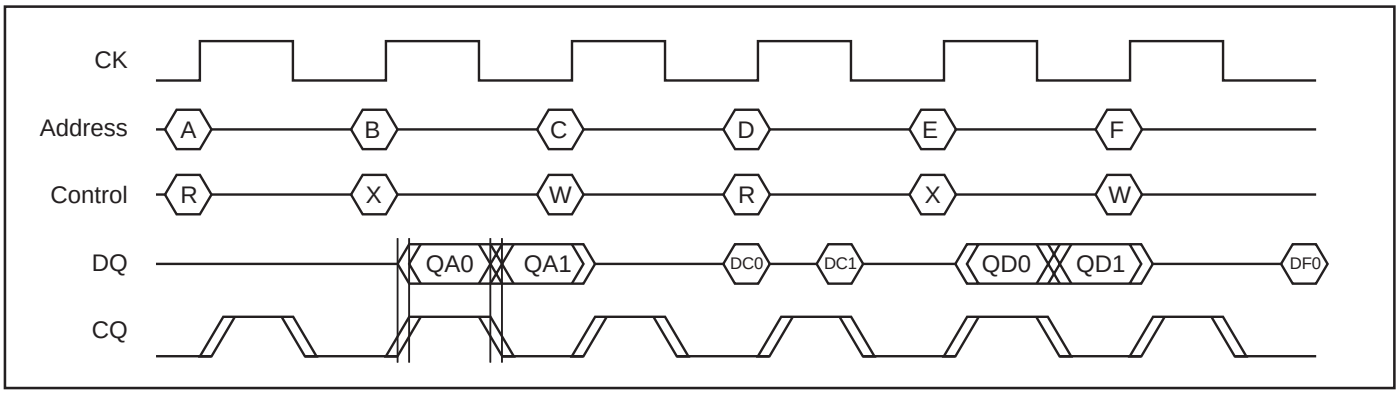
DOUBLE LATE WRITE—PIPELINED READ (Σ1x1Dp). For reference only.



LATE WRITE—PIPELINED READ (Σ1x1Lp). For reference only.



DOUBLE DATA RATE WRITE—DOUBLE DATA RATE READ (Σ1x2Lp). For reference only.



READ OPERATIONS

Pipelined Read

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: All three chip enables ($\overline{E1}$, E2, and E3) are active, the write enable input signal ($\overline{W}$) is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

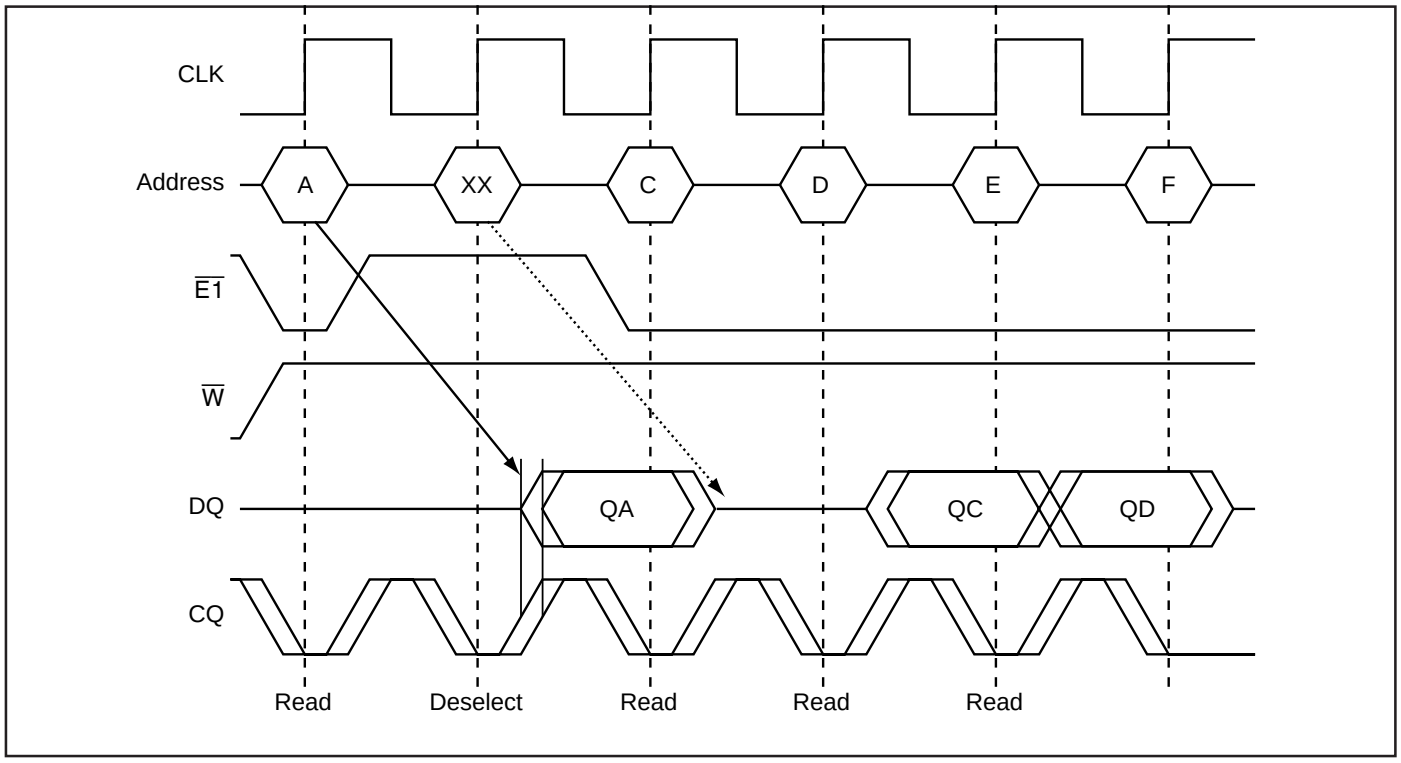
WRITE OPERATIONS

Write operation occurs when the following conditions are satisfied at the rising edge of clock: All three chip enables ($\overline{E1}$, E2, and E3) are active and the write enable input signal ($\overline{W}$) is asserted low.

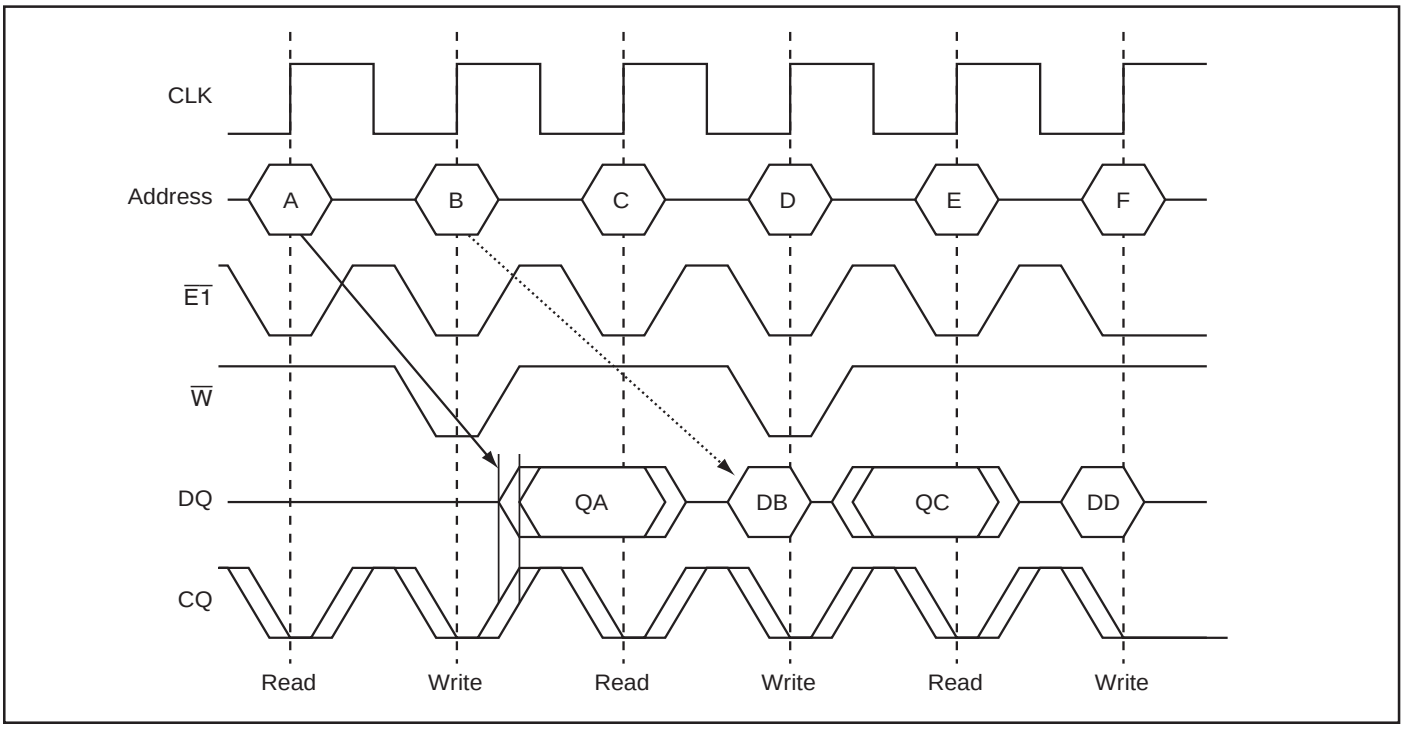
Double Late Write

Double Late Write means that Data In is required on the third rising edge of clock. Double Late Write is used to implement Pipeline mode NBT SRAMs.

SINGLE DATA RATE PIPELINED READ



DOUBLE LATE WRITE WITH PIPELINED READ



SPECIAL FUNCTIONS

Burst Cycles

ΣRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the ΣRAM to advance the internal address counter and use the counter generated address to read or write the ΣRAM. The starting address for the first cycle in a burst cycle series is loaded into the ΣRAM by driving the ADV pin low, into Load mode.

Burst Order

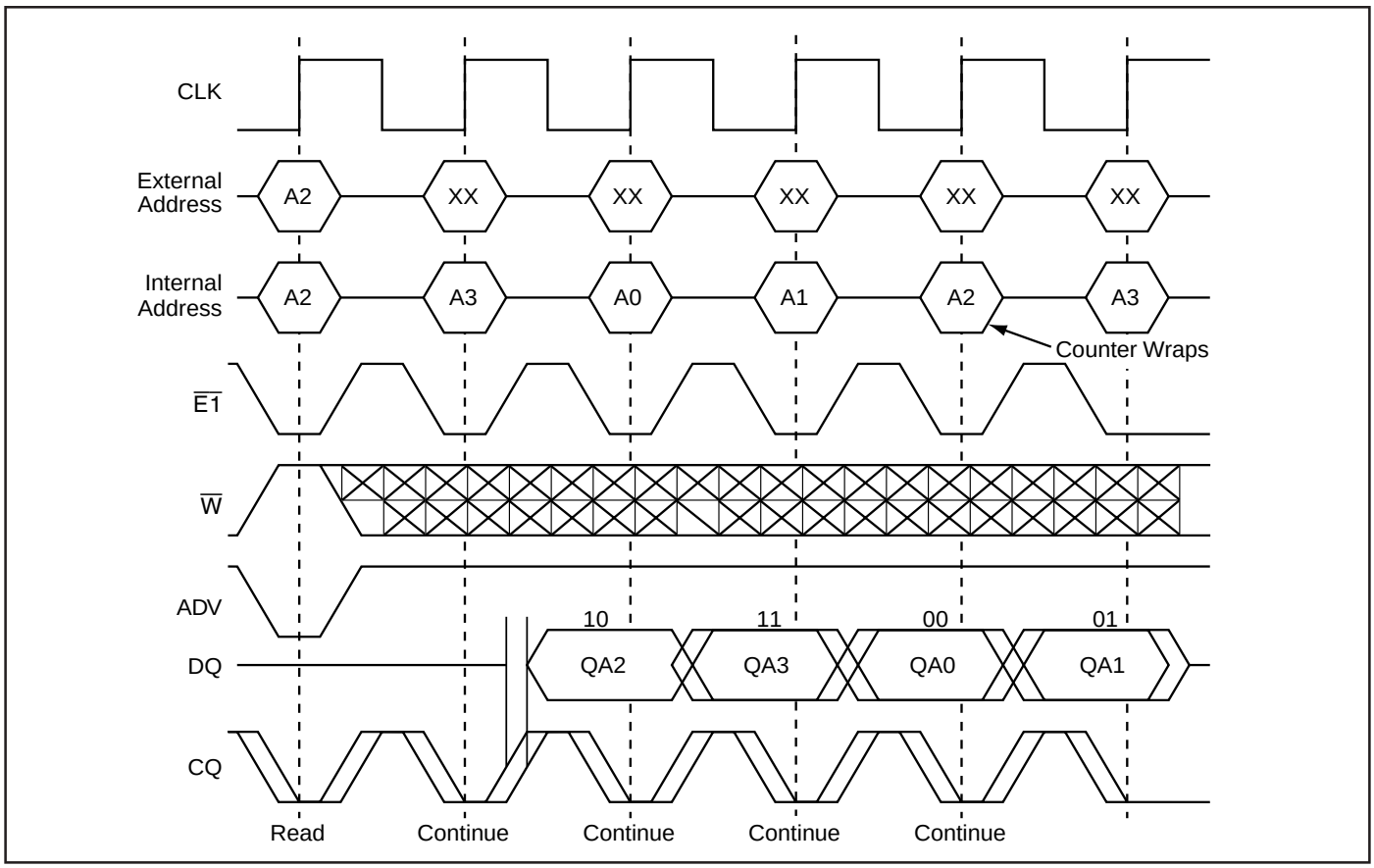
The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. SigmaRAMs always count in linear burst order.

Linear Burst Order

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
1. The burst counter wraps to initial state on the 5th rising edge of clock.

SIGMA PIPELINED BURST READS WITH COUNTER WRAP-AROUND



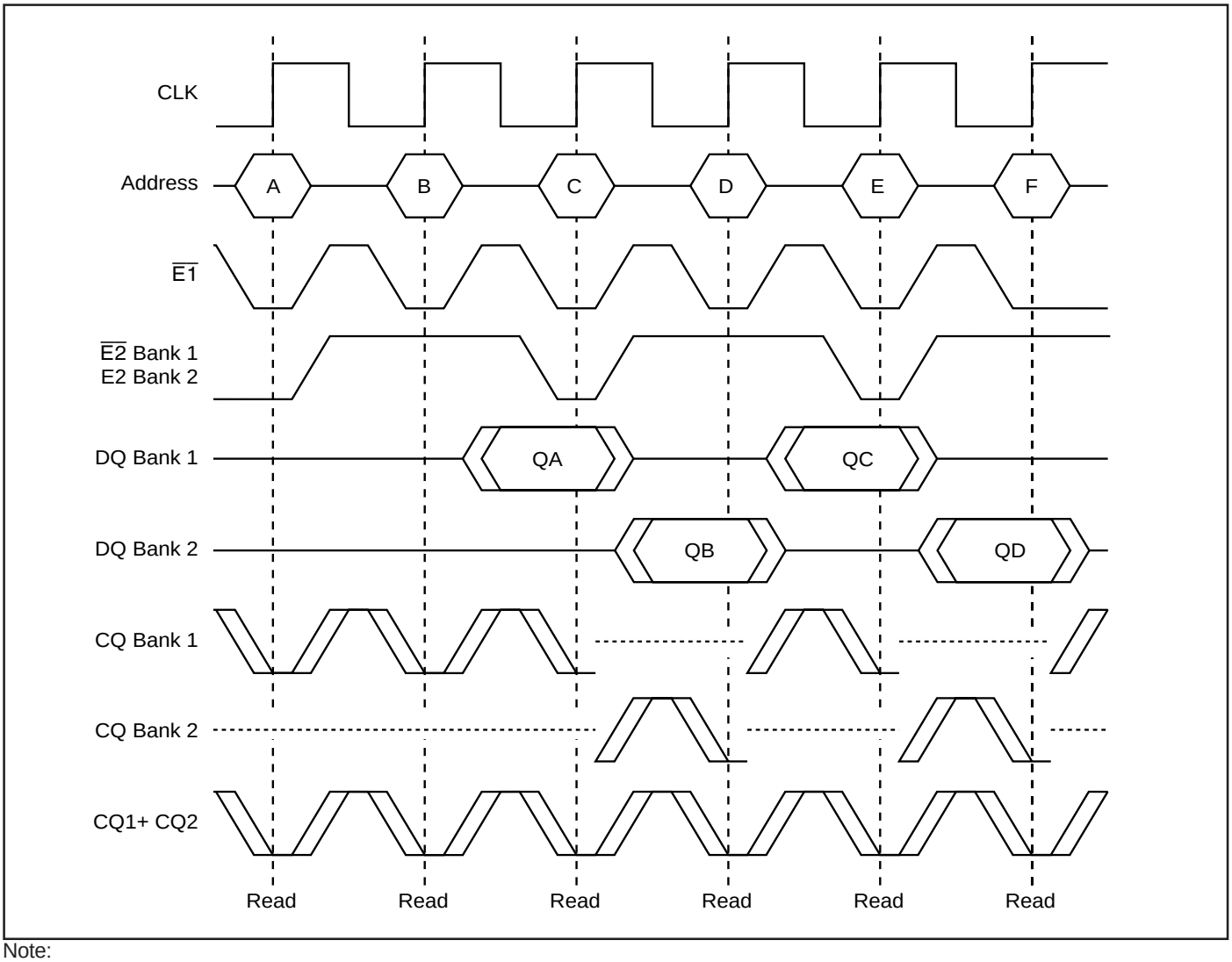
ECHO CLOCK

ΣRAMs feature Echo Clocks, CQ1,CQ2, $\overline{CQ1}$, and $\overline{CQ2}$ that track the performance of the output drivers. The Echo Clocks are delayed copies of the main RAM clock, CLK. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The Echo Clocks are designed to fire with the rest of the data output drivers. Sigma RAMs provide both in-phase, or true, Echo Clock outputs (CQ1 and CQ2) and inverted Echo Clock outputs ($\overline{CQ1}$ and $\overline{CQ2}$).

It should be noted that deselection of the RAM via E2 and E3 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. Deselection of the RAM via $\overline{E1}$ does not deactivate the Echo Clocks.

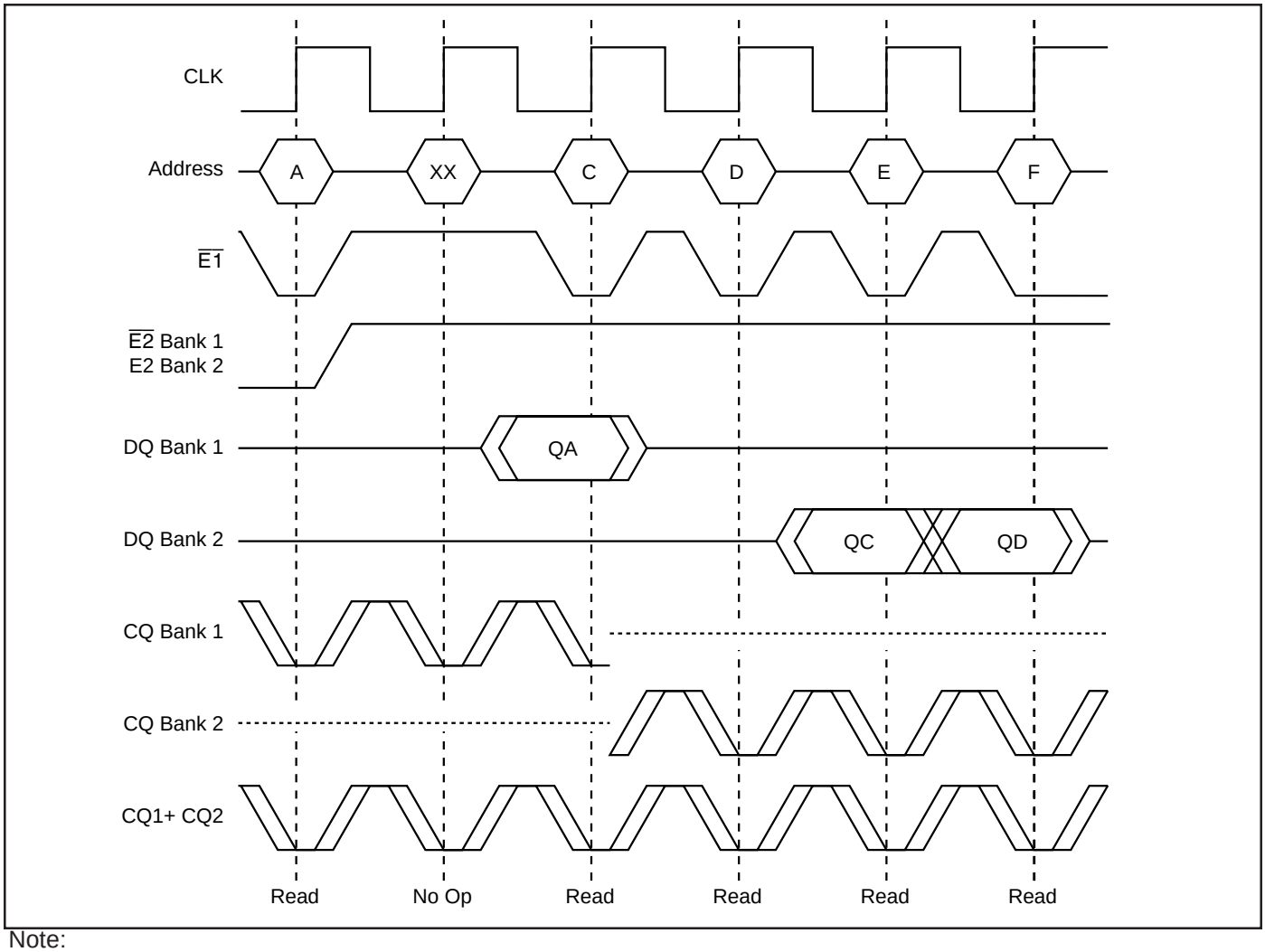
In some applications it may be appropriate to pause between banks; to deselect both RAMs with E1 before resuming read operations. An E1 deselect at a bank switch will allow at least one clock to be issued from the new bank before the first read cycle in the bank. Although the following drawing illustrates a E1 read pause upon switching from Bank 1 to Bank 2, a write to Bank 2 would have the same effect, causing the RAM in Bank 2 to issue at least one clock before it is needed.

ECHO CLOCK CONTROL IN TWO BANKS OF SIGMA PIPELINED SRAMS



Note:
E1 does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.

PIPELINED READ BANK SWITCH WITH E1 DESELECT



Note:
$\overline{E1}$ does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.

OUTPUT DRIVER IMPEDANCE CONTROL

SigmaRAMs may be supplied with either selectable (high) impedance output drivers. The ZQ pin of SigmaRAMs supplied with selectable impedance drivers, allows selection between ΣRAM nominal drive strength (ZQ low) for multi-drop bus applications and low drive strength (ZQ floating or high) point-to-point applications. The impedance of the data and clock output drivers in these devices can be controlled via the static input ZQ. When ZQ is tied "low", output driver impedance is set to ~25 Ω. When ZQ is tied "high" or left unconnected, output driver impedeance is set to ~50Ω. See the DC Electrical Characteristics section for further information. The SRAM requires 32K cycles of power-up time after V_{CC} reaches its operating range.

OUTPUT DRIVER CHARACTERISTICS - TBD

PROGRAMMABLE ENABLES

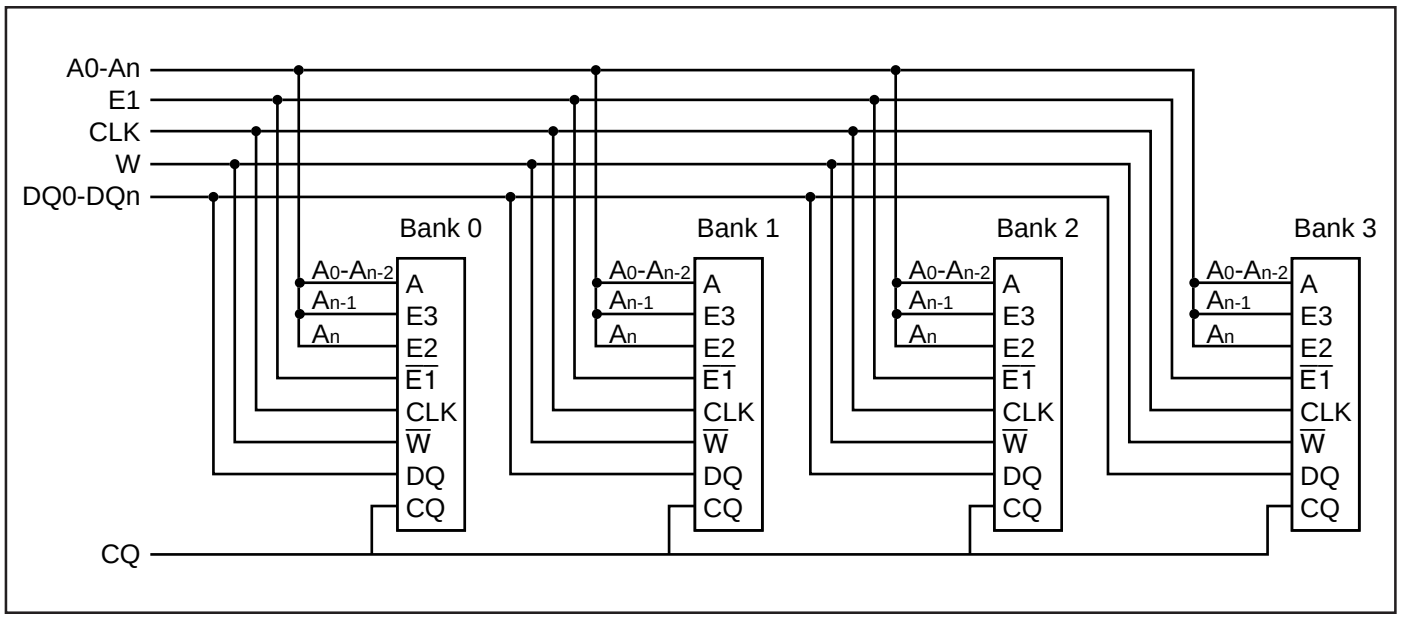
SRAMs feature two user-programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and EP3. For example, if EP2 is held at Vcc , E2 functions as an active high enable. If EP2 is held to GND , E2 functions as an active low chip enable input.

Programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four SRAMs in binary sequence (00, 01, 10, 11) and driving the enable inputs with two address inputs, four SRAMs can be made to look like one larger RAM to the system.

BANK ENABLE TRUTH TABLE

	EP2	EP3	E2	E3
Bank 0	GND	GND	Active Low	Active Low
Bank 1	GND	Vcc	Active Low	Active High
Bank 2	Vcc	GND	Active High	Active Low
Bank 3	Vcc	Vcc	Active High	Active High

EXAMPLE FOUR BANK DEPTH EXPANSION SCHEMATIC

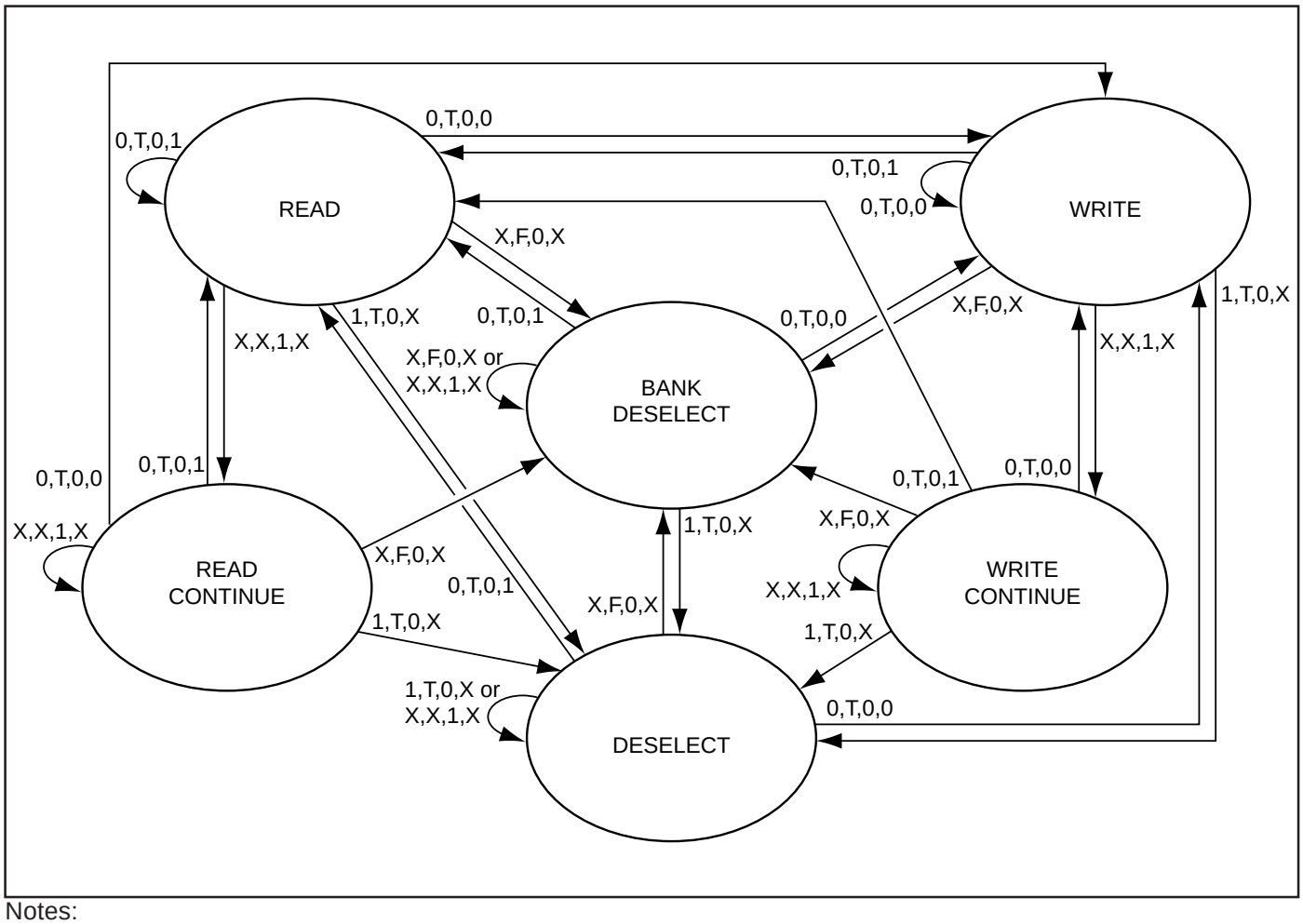


SYNCHRONOUS TRUTH TABLE

CLK	$\overline{E1}$ (tn)	E (tn)	ADV (tn)	$\overline{W}$ (tn)	$\overline{BW}$ (tn)	Previous Operation	Current Operation	DQ/CQ (tn)	DQ/CQ (tn+1)
0→1	X	F	0	X	X	X	Bank Deselect	***	Hi-Z
0→1	X	X	1	X	X	Bank Deselect	Bank Deselect (Continue)	Hi-Z	Hi-Z
0→1	1	T	0	X	X	X	Deselect	***	Hi-Z/CQ
0→1	X	X	1	X	X	Deselect	Deselect (Continue)	Hi-Z/CQ	Hi-Z/CQ
0→1	0	T	0	0	T	X	Write Loads new address Stores DQx if $\overline{BWx}$ = 0	***	Dn/CQ (tn)
0→1	0	T	0	0	F	X	Write (Abort) Loads new address No data stored	***	Hi-Z/CQ
0→1	X	X	1	X	T	Write	Write Continue Increments address by 1 Stores DQx if $\overline{BWx}$ = 0	Dn-1/CQ (tn-1)	Dn/CQ (tn)
0→1	X	X	1	X	F	Write	Write Continue (Abort) Increments address by 1 No data stored	Dn-1/CQ (tn-1)	Hi-Z/CQ
0→1	0	T	0	1	X	X	Read Loads new address	***	Qn/CQ (tn)
0→1	X	X	1	X	X	Read	Read Continue Increments address by 1	Qn-1/CQ (tn-1)	Qn/CQ (tn)

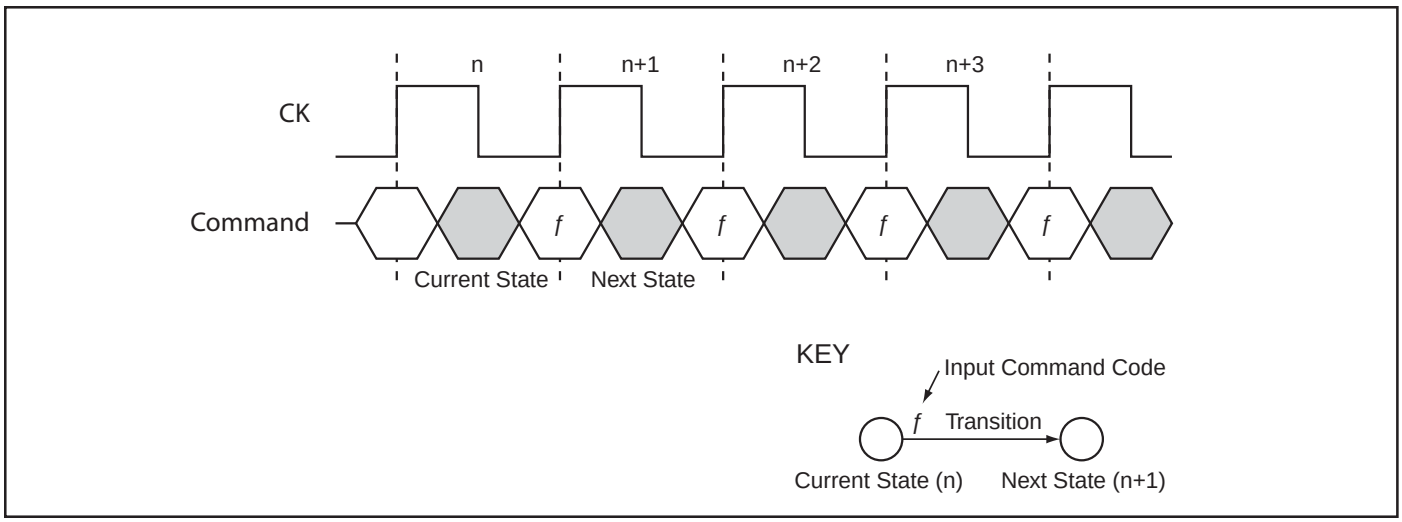
Notes:
1. If E2 = EP2 and $\overline{E3}$ = EP3 then E = "T" else E = "F".
2. If one or more $\overline{BWx}$ = 0 then BW = "T" else BW = "F".
3. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
4. "***" indicates that the DQ input requirement/output state and CQ output state are determined by the previous operation.
5. DQs are tri-stated in response to Bank Deselect, Deselect, and Write commands, one full cycle after the command is sampled.
6. CQs are tri-stated in response to Bank Deselect commands only, one full cycle after the command is sampled.
7. Up to 3 Continue operations may be initiated after iniating a Read or Write operation to burst transfer up to 4 distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

READ/WRITE CONTROL STATE DIAGRAM



Notes:
1. The notation “X,X,X,X” controlling the state transitions above indicate the states of inputs $\overline{E1}$, E, ADV, and $\overline{W}$ respectively.
2. If (E2 = EP2 and E3 = EP3) then E = “T” else E = “F”.
3. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.

CURRENT STATE & NEXT STATE DEFINITION FOR READ/WRITE CONTROL STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(All voltages reference to GND)

Symbol	Description	Value	Unit
V_{CC}	Voltage on V_{CC} Pins	–0.5 to 2.5	V
V_{CCQ}	Voltage in V_{CCQ} Pins	–0.5 to 2.3V	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{CCQ} +0.5 (≤ 2.3 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{CCQ} +0.5 (≤ 2.3 V max.)	V
I_{IN}	Input Current on Any Pin	±100	mA dc
I_{OUT}	Output Current on Any Pin	±100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	-55 to 125	°C

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Operation should be limited to Recommended Operating Conditions. Exposure to conditions exceeding Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

POWER SUPPLY CHARACTERISTICS (T_A = 0 min., 25 typ, 70 max °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	1.7	1.8	1.9	V
V_{CCQ}[1]	1.8 V I/O Supply Voltage	1.7	1.8	V_{CC}	V
	1.5 V I/O Supply Voltage	1.4	1.5	1.6 V	V

Note:

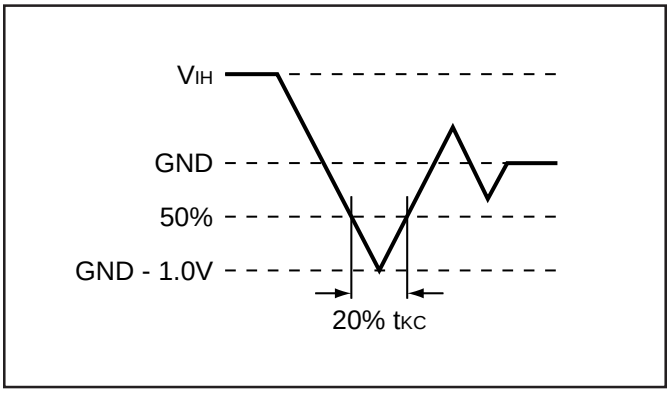
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 1.4 V ≤ V_{CCQ} ≤ 1.6V (i.e., 1.5 V I/O) and 1.7 V ≤ V_{CCQ} ≤ 1.9 V (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.

CMOS I/O DC INPUT CHARACTERISTICS

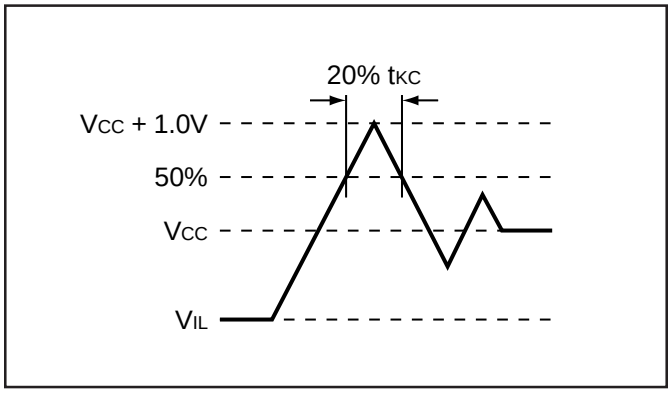
Symbol	Parameter	V_{CCQ}	Min.	Typ.	Max.	Unit
V_{IH}	CMOS Input High Voltage	1.8	1.2	—	V_{CCQ} + 0.3	V
		1.5	1.0	—	V_{CCQ} + 0.3	
V_{IL}	CMOS Input Low Voltage	1.8	–0.3	—	0.6	V
		1.5	–0.3	—	0.5	

Note:
For devices supplied with CMOS input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



I/O CAPACITANCE (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter		Test conditions	Min.	Max.	Unit
C_A	Address	Input Capacitance	V_{IN} = 0 V	—	3.5	pF
C_B	Control	Input Capacitance	V_{IN} = 0 V	—	3.5	pF
C_{CK}	Clock	Input Capacitance	V_{IN} = 0 V	—	3.5	pF
C_{DQ}	Data	Output Capacitance	V_{OUT} = 0 V	—	4.5	pF
C_{CQ}	CQ Clock	Output Capacitance	V_{OUT} = 0 V	—	4.5	pF

Note: These parameters are sampled and not 100% tested.

AC TEST CONDITIONS

(V_{CC} = 1.8V ± 0.1V, T_A = 0 to 85°C)

Parameter	Symbol	Conditions		Units
V_{CCQ}		1.5V±0.1	1.8 ±0.1	V
Input High Level	V_{IH}	1.25	1.4	V
Input Low Level	V_{IL}	0.25	0.4	V
Input Rise & Fall Time		2.0	2.0	V/ns
Input Reference Level		0.75	0.9	V
Clock Input High Voltage	V_{KIH}	1.25	1.4	V
Clock Input Low Voltage	V_{KIL}	0.25	0.4	V
Clock Input Rise & Fall Time		2.0	2.0	V/ns
Clock Input Reference Level		0.75	0.9	V
Output Reference Level		0.75	0.9	V
Output Load Conditions ZQ = V_{IH}		see below	see below	

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown unless otherwise noted.

AC TEST LOADS

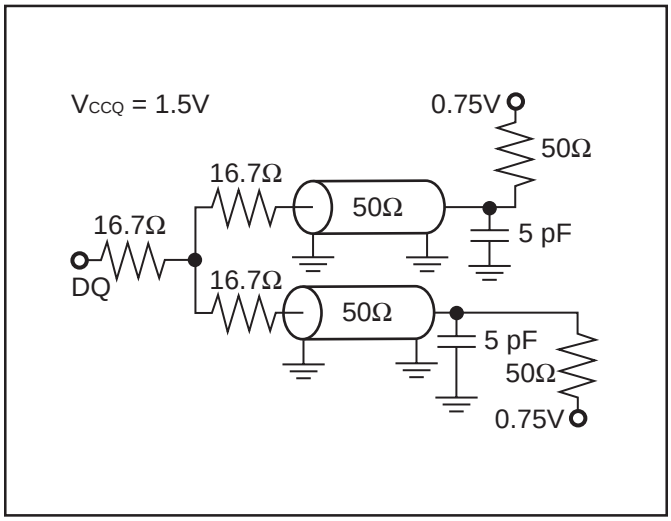


Figure 1 (V_{CCQ} = 1.5V)

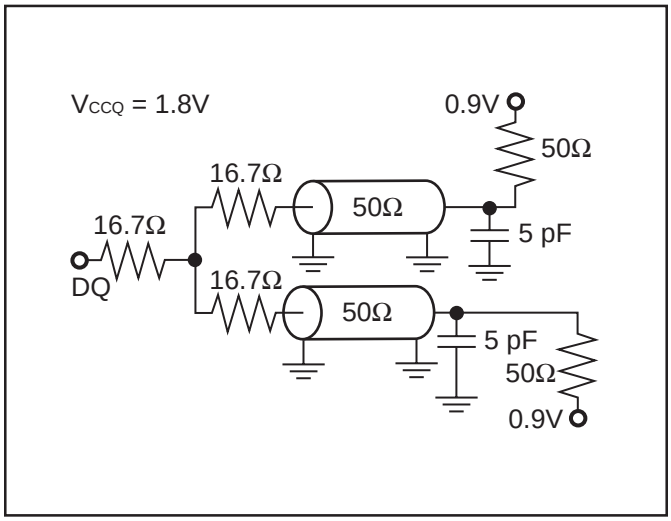


Figure 2 (V_{CCQ} = 1.8V)

SELECTABLE IMPEDANCE OUTPUT DRIVER DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OHL}(1)	Low Drive Output High Voltage	I_{OHL} = –4 mA	V_{CCQ} – 0.4	—	V
V_{OLL}(1)	Low Drive Output Low Voltage	I_{OLL} = 4 mA	—	0.4	V
V_{OHH}(2)	High Drive Output High Voltage	I_{OHH} = –8 mA	V_{CCQ} – 0.4	—	V
V_{OLH}(2)	High Drive Output Low Voltage	I_{OLH} = 8 mA	—	0.4	V

Notes:
1. ZQ = 1; High Impedance output driver setting
2. ZQ = 0; Low Impedance output driver setting

OUTPUT RESISTANCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R_{OUT}	Output Resistance	$V_{OH}, V_{OL} = V_{CCQ}/2$ ZQ = V_{IL}	17	25	33	Ω
		$V_{OH}, V_{OL} = V_{CCQ}/2$ ZQ = V_{IH}	35	50	65	Ω

OPERATING CURRENTS

Symbol	Parameter	Test Conditions		-333 Com.	-333 Ind.	-300 Com.	-300 Ind.	Units
I_{CC}	Operating Current	E1 ≤ V_{IL} Max. $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IL} \geq V_{IN} \geq V_{IH}$	Pipeline x72 x36	800 700		800 700		mA
I_{SB1} & I_{SB2}	Bank Deselect Current & Chip Disable Current	E1 ≤ V_{IH} Min. or E2 or E3 False $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IL} \geq V_{IN} \geq V_{IH}$	Pipeline x72 x36	250 225		250 225		mA
I_{SB3}	CMOS Deselect Current All inputs	Device Deselected x36 GND+0.10V ≥ V_{IN} ≥ V_{CC}–0.10V	Pipeline x72	150 150		150 150		mA

Note: Com. = 0°C to 70°C
Ind. = –40°C to +85°C

OPERATING CURRENTS (continued)

Symbol	Parameter	Test Conditions		-250 Com.	-250 Ind.	-225 Com.	-225 Ind.	-200 Com.	-200 Ind.	Units
I_{CC}	Operating Current	E1 ≤ V_{IL} Max. $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IL} \geq V_{IN} \geq V_{IH}$	Pipeline x72 x36	650 550		650 550		650 550		mA
I_{SB1} & I_{SB2}	Bank Deselect Current & Chip Disable Current	E1 ≤ V_{IH} Min. or E2 or E3 False $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IL} \geq V_{IN} \geq V_{IH}$	Pipeline x72 x36	250 225		250 225		250 225		mA
I_{SB3}	CMOS Deselect Current	Device Deselected All inputs GND+0.10V ≥ $V_{IN} \geq V_{CC}$–0.10V	Pipeline x72 x36	150 150		150 150		150 150		mA

Note: Com. = 0°C to 70°C
Ind. = –40°C to +85°C

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V ±0.1V, GND = 0V, T_A = 0° to 85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current (Address, Control, Clock)	V_{IN} = GND to V_{CCQ}	-5	—	5	uA
I_{MLI}	Input Leakage Current (EP2, EP3, M2, M3, M4, ZQ)	V_{MIN} = GND to V_{CC}	-10	—	10	uA
I_{DLI}	Input Leakage Current (Data)	V_{DIN} = GND to V_{CCQ}	-10	—	10	uA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	-333 Min	-333 Max	-300 Min	-300 Max	-250 Min	-250 Max	Unit
t_{KHKH}	Clock Cycle Time	3.0	—	3.3	—	4.0	—	ns
t_{KHKL}	Clock HIGH Time	1.2	—	1.3	—	1.5	—	ns
t_{KLKH}	Clock LOW Time	1.2	—	1.3	—	1.5	—	ns
t_{KHCQX1}(2)	Clock High to Echo Clock Low-Z	0.5	—	0.5	—	0.5	—	ns
t_{KHCQH}	Clock High to Echo Clock High	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{CQHCQL}(2)	Echo Clock High Time	t_{KHKL} ±200 ps		t_{KHKL} ±200 ps		t_{KHKL} ±250 ps		ns
t_{KLCQL}	Clock Low to Echo Clock Low	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{CQLCQH}(2)	Echo Clock Low Time	t_{KLKH} ±200 ps		t_{KLKH} ±200 ps		t_{KLKH} ±250 ps		ns
t_{KHCQZ}(1, 2)	Clock High to Echo Clock High-Z	—	1.5	—	1.7	—	2.0	ns
t_{KHQX1}(1)	Clock High to Output in Low-Z	0.5	—	0.5	—	0.5	—	ns
t_{KHQV}	Clock High to Output Valid	—	1.6	—	1.8	—	2.1	ns
t_{KHQX}	Clock High to Output Invalid	0.5	—	0.5	—	0.5	—	ns
t_{KHQZ}(1)	Clock High to Output in High-Z	0.5	1.6	0.5	1.8	0.5	2.1	ns
t_{CQHQV}(2)	Echo Clock High to Output Valid	—	0.4	—	0.4	—	0.5	ns
t_{CQHQX}(2)	Output Invalid to Echo Clock High	—	–0.4	—	–0.4	—	–0.5	ns
t_{AVKH}	Address Valid to Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHAX}	Clock High to Address Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{EVKH}	Enable Valid to Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHEX}	Clock High to Enable Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{WVKH}	Write Valid to Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHWX}	Clock High to Write Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{BVKH}	Byte Write Valid to Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHBX}	Clock High to Byte Write Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{DVKH}	Data In Valid to Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHDX}	Clock High to Data In Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{advVKH}	ADV Valid to Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHadvX}	Clock High to ADV Don't Care	0.4	—	0.4	—	0.5	—	ns

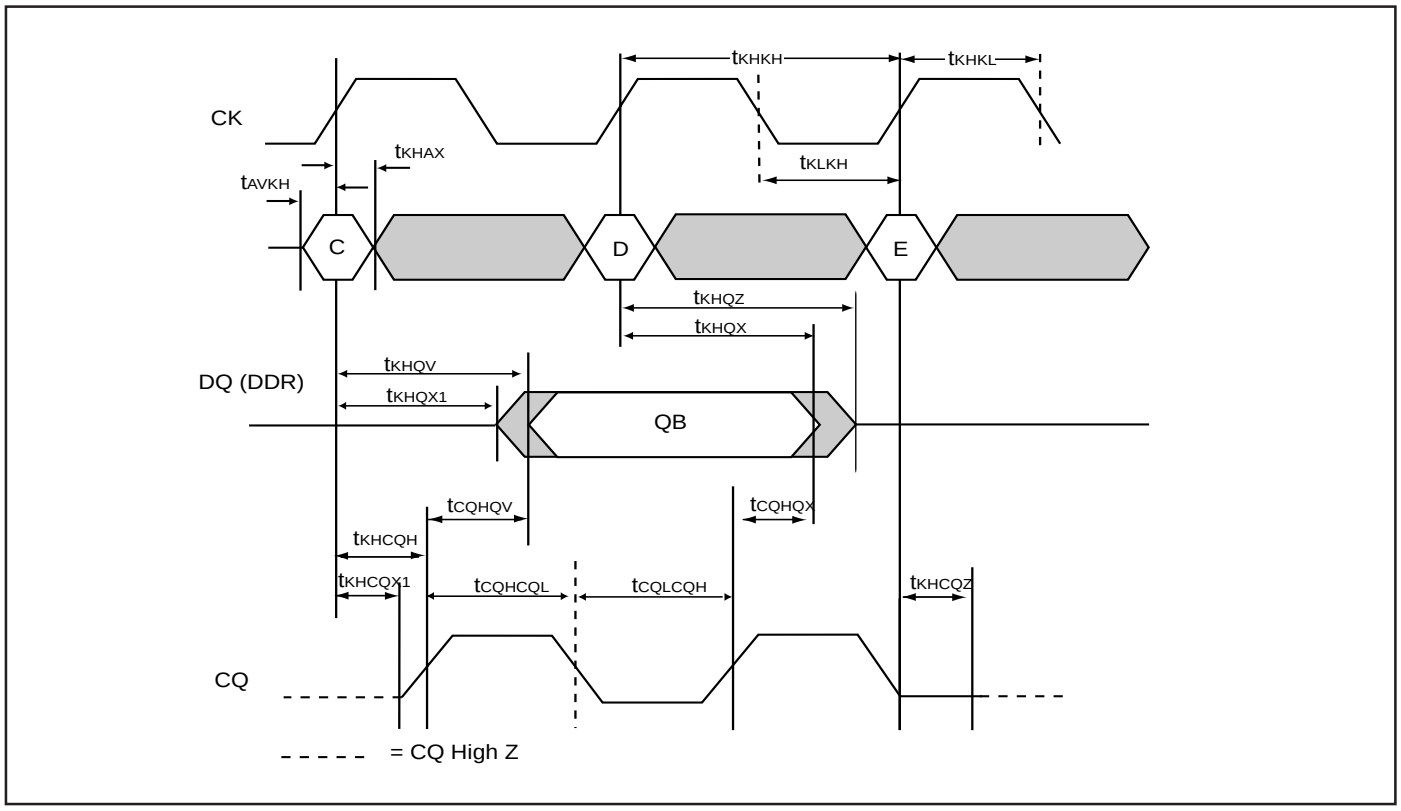
Notes:
1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.
3. For any specific temperature and voltage $t_{KHCZ} < t_{KHCX}1$.

AC ELECTRICAL CHARACTERISTICS

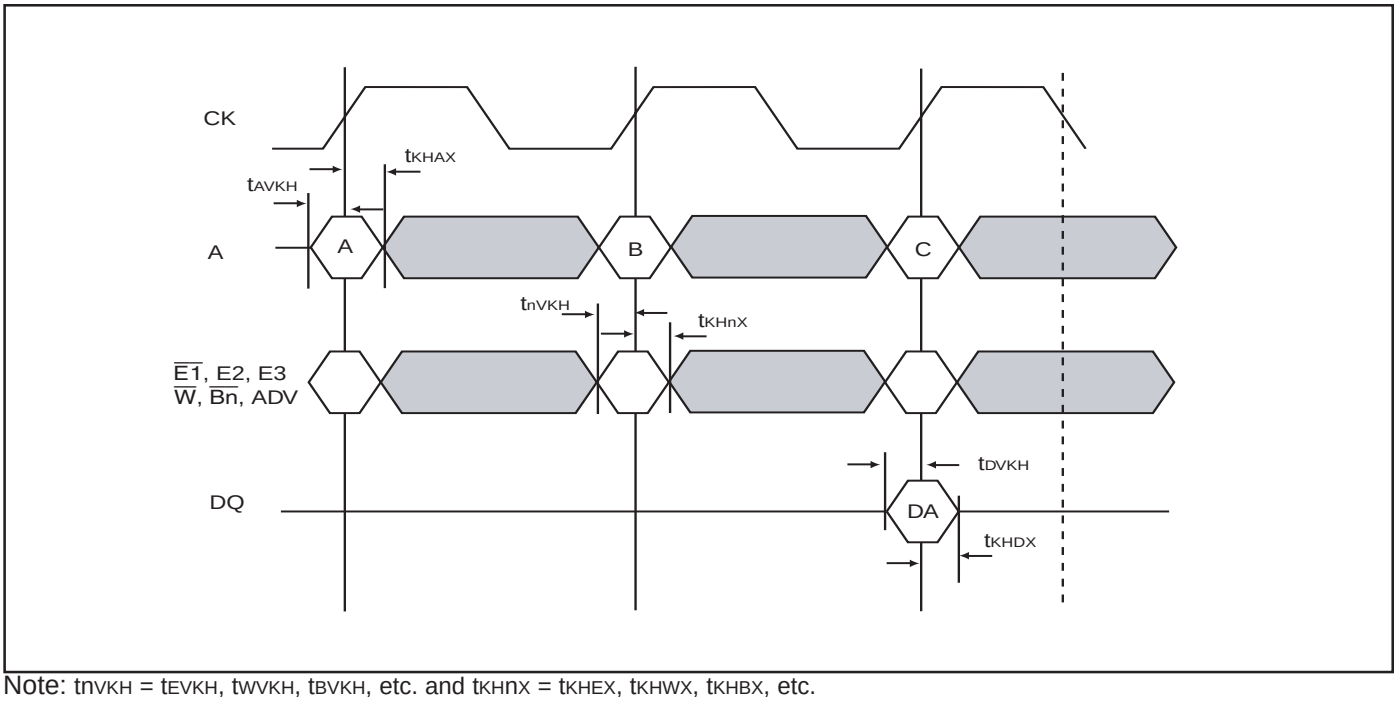
Symbol	Parameter	-225 Min	-225 Max	-200 Min	-200 Max	Unit
t_{KHKH}	Clock Cycle Time	4.5	—	5.0	—	ns
t_{KHKL}	Clock HIGH Time	1.8	—	2.0	—	ns
t_{KLKH}	Clock LOW Time	1.8	—	2.0	—	ns
t_{KHCX1}(2)	Clock High to Echo Clock Low-Z	0.5	—	0.5	—	ns
t_{KHCH}	Clock High to Echo Clock High	0.5	2.5	0.5	3.0	ns
t_{CHCL}(2)	Echo Clock High Time	t_{KHKL} ±250 ps		t_{KHKL} ±250 ps		ns
t_{KLCL}	Clock Low to Echo Clock Low	0.5	2.5	0.5	3.0	ns
t_{CLCH}(2)	Echo Clock Low Time	t_{KLKH} ±200 ps		t_{KLKH} ±200 ps		ns
t_{KHCZ}(1, 2)	Clock High to Echo Clock High-Z	—	2.5	—	3.0	ns
t_{KHQX1}(1)	Clock High to Output in Low-Z	0.5	—	0.5	—	ns
t_{KHQV}	Clock High to Output Valid	—	2.6	—	3.1	ns
t_{KHQX}	Clock High to Output Invalid	0.5	—	0.5	—	ns
t_{KHQZ}(1)	Clock High to Output in High-Z	0.5	2.6	0.5	3.1	ns
t_{CHQV}(2)	Echo Clock High to Output Valid	—	0.5	—	0.5	ns
t_{CHQX}(2)	Output Invalid to Echo Clock High	—	–0.5	—	–0.5	ns
t_{AVKH}	Address Valid to Clock High	1.1	—	1.5	—	ns
t_{KHAX}	Clock High to Address Don't Care	0.5	—	0.5	—	ns
t_{EVKH}	Enable Valid to Clock High	1.1	—	1.5	—	ns
t_{KHEX}	Clock High to Enable Don't Care	0.5	—	0.5	—	ns
t_{WVKH}	Write Valid to Clock High	1.1	—	1.5	—	ns
t_{KHWX}	Clock High to Write Don't Care	0.5	—	0.5	—	ns
t_{BVKH}	Byte Write Valid to Clock High	1.1	—	1.5	—	ns
t_{KHBX}	Clock High to Byte Write Don't Care	0.5	—	0.5	—	ns
t_{DVKH}	Data In Valid to Clock High	1.1	—	1.5	—	ns
t_{KHDX}	Clock High to Data In Don't Care	0.5	—	0.5	—	ns
t_{advVKH}	ADV Valid to Clock High	1.1	—	1.5	—	ns
t_{KHadvX}	Clock High to ADV Don't Care	0.5	—	0.5	—	ns

Notes:
1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.
3. For any specific temperature and voltage $t_{KHCZ} < t_{KHCX}1$.

TIMING PARAMETER KEY—PIPELINED READ CYCLE TIMING



TIMING PARAMETER KEY—DOUBLE LATE WRITE MODE CONTROL AND DATA IN TIMING



Note: tnVKH = tEVKH, tWVKH, tBVKH, etc. and tKHnX = tKHEX, tKHWX, tKHBX, etc.

JTAG PORT OPERATION

Overview

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and four TAP Registers. The TAP Registers consist of one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the RAM with the JTAG Port unused, TCK should be tied Low, TDI and TMS may be left floating or tied to V_{CC} . TDO should be left unconnected.

JTAG PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP Controller. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG PORT REGISTERS

Overview

The JTAG registers, refered to as Test Access Port (TAP) registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

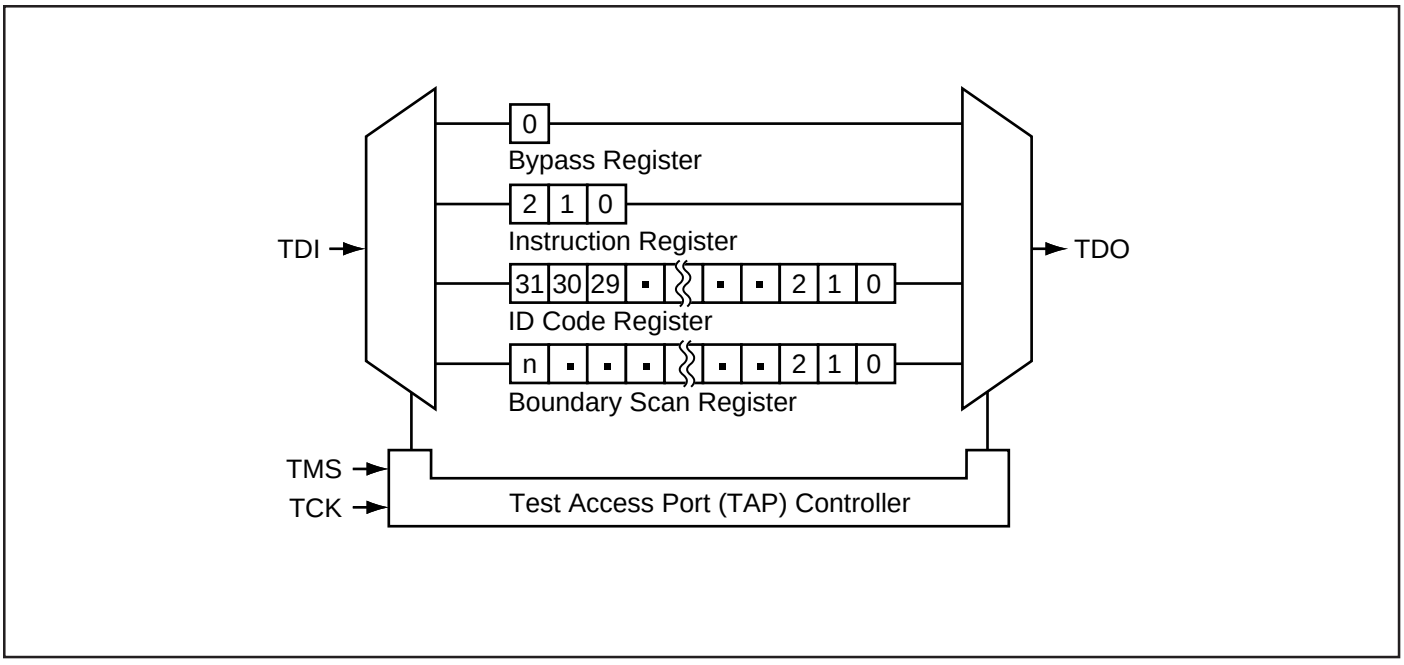
Bypass Register

The Bypass Register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the following Scan Order Table. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP BLOCK DIAGRAM



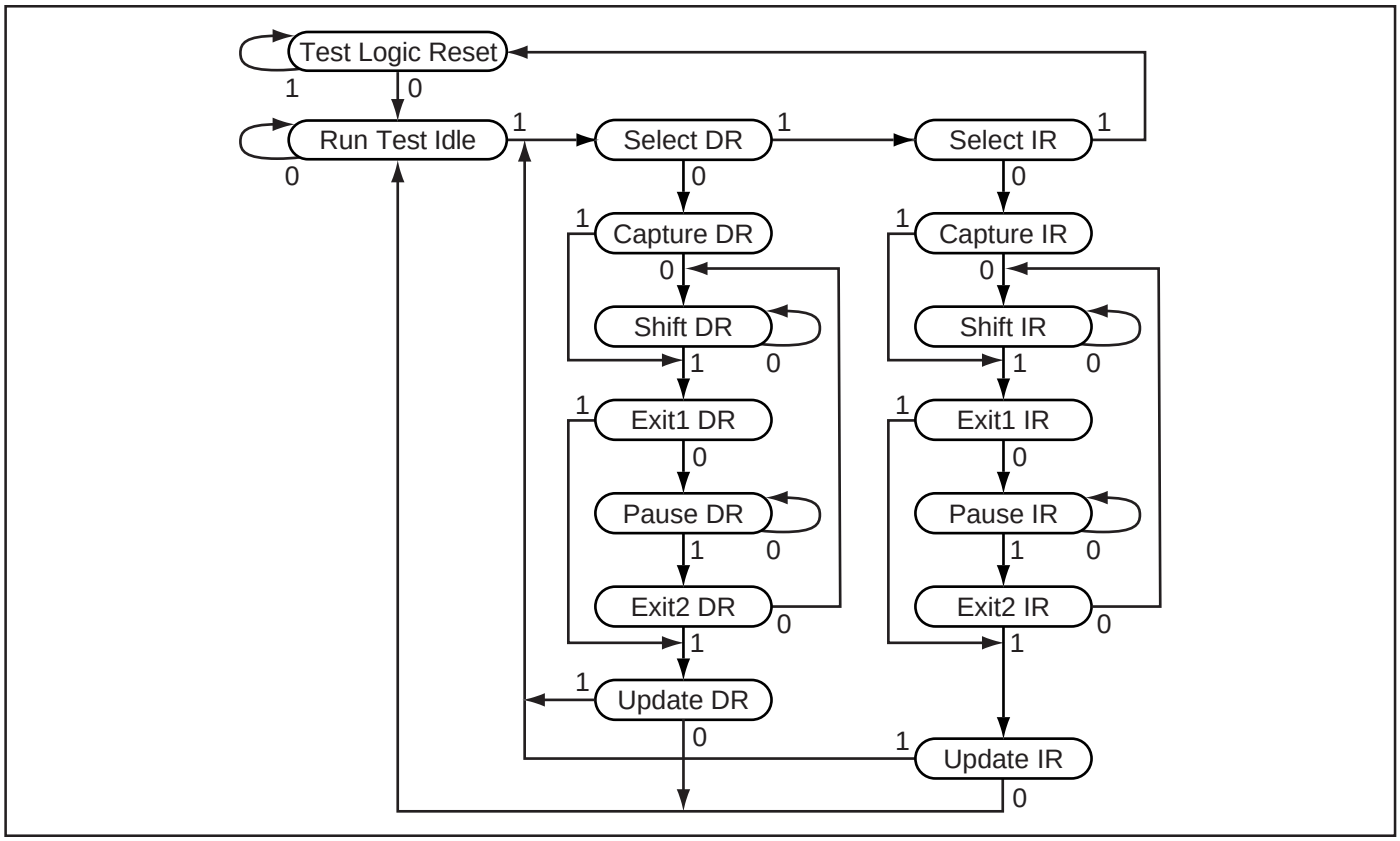
IDENTIFICATION (ID) REGISTER

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID REGISTER CONTENTS

	Die Revision Code				Not Used												I/O Configuration				ISSI Technology JEDEC Vendor ID Code										Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x72	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1	0	1	0	1	1
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1

JTAG TAP CONTROLLER STATE DIAGRAM



TAP CONTROLLER INSTRUCTION SET

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; standard (public) instructions, and device specific (private) instructions. Some public instructions are mandatory for 1149.1 compliance. Optional public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads. This device will not perform INTEST but can preform the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 001. When the controller is moved to the Shift-IR state, the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the JTAG TAP Instruction Set Summary.

JTAG TAP INSTRUCTION SET SUMMARY

Instruction	Code	Description
EXTEST(1)	000	Places the Boundary Scan Register between TDI and TDO. When EXTEST is selected, data will be driven out of the DQ pad.
IDCODE(1,2)	001	Preloads ID Register and places it between TDI and TDO.
SAMPLE-Z(1)	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z.
RFU(1)	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.
SAMPLE/PRELOAD(1)	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.
Private(1)	101	Private instruction.
RFU(1)	110	Do not use this instruction; Reserved for Future Use.
BYPASS(1)	111	Places Bypass Register between TDI and TDO.

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in Test-Logic-Reset state.

JTAG DC RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 85°C)

Symbol	Parameter		Test Conditions	Min.	Max.	Unit
V_{TIH}	JTAG Input High Voltage			1.2	V_{CC} +0.3	V
V_{TIL}	JTAG Input Low Voltage			-0.3	0.6	V
V_{TOH}	JTAG Output High Voltage	CMOS	I_{TOH} = -100µA	V_{CC}-0.1	—	V
		TTL	I_{TOH} = -8mA	V_{CC}-0.4	—	
V_{TOL}	JTAG Output Low Voltage	CMOS	I_{TOL} = 100µA	—	0.1	V
		TTL	I_{TOL} = 8mA	—	0.4	
I_{TLI}	JTAG Input Leakage Current		V_{TIN}=GND to V_{CC}	-10	10	µA

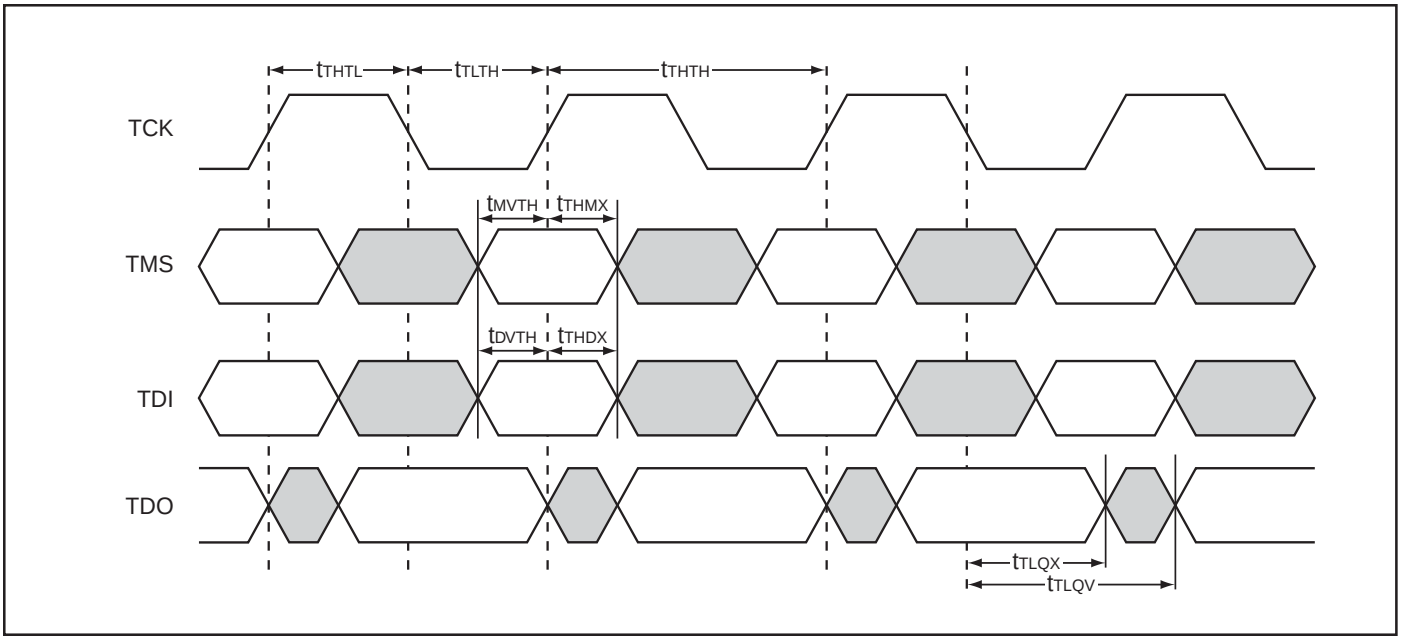
JTAG AC TEST CONDITIONS (V_{CC} = 1.8V ±0.1V, T_A = 0 to 85°C)

Symbol	Parameter	Test Conditions	Unit
V_{TIH}	JTAG Input High Voltage	1.6	V
V_{TIL}	JTAG Input Low Voltage	0.2	V
	JTAG Input Rise & Fall Time	1.0	V/ns
	JTAG Input Reference Level	0.9	V
	JTAG Output Reference Level	0.9	V
	JTAG Output Load Condition	see AC TEST LOADS	

JTAG PORT AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
t_{THTH}	TCK Cycle Time	20	—	ns
t_{THTL}	TCK High Pulse Width	8	—	ns
t_{TLTH}	TCK Low Pulse Width	8	—	ns
t_{MVTH}	TMS Setup Time	5	—	ns
t_{THMX}	TMS Hold Time	5	—	ns
t_{DVTH}	TDI Set Up Time	5	—	ns
t_{THDX}	TDI Hold Time	5	—	ns
t_{TLQV}	TCK Low to TDO Valid	—	10	ns
t_{TLQX}	TCK Low to TDO Hold	0	—	ns

JTAG PORT TIMING DIAGRAM



INSTRUCTION DESCRIPTIONS

BYPASS

When the BYPASS instruction is loaded to the Instruction Register, the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Some Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the BSDL file. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (t_{TS} plus t_{TH}). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the Boundary Scan Register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin (pin marked NC), are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state. Boundary Scan Register contents may then be shifted serially through the register using the Shift-DR command or the controller can be skipped to the Update-DR command. When the controller is placed in the Update-DR state, a RAM that has fully compliant EXTEST function drives out the value of the Boundary Scan Register location associated with each output pin.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded to the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded to the instruction register, all RAM outputs are forced to inactive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are reserved for future use. In this device they replicate the BYPASS instruction.

BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) PH =Place Holder

X72		Ball Loc.	X36	
Sequence	Pkg. Ball		Sequence	Pkg. Ball
1	A0	W6	1	A0
2	A	V7	2	A
3	A	V8	3	A
4	A	U8	4	A
5	A	V9	5	A
6	A	U6	6	A
7	PH(1)	U5	7	PH(1)
8	A	W7	8	A
9	PH(1)	U7	9	PH(1)
10	MCL	T6	10	MCL
11	M3	M6	11	M3
12	M4	J6	12	M4
13	MCL	K6	13	MCL
14	MCL	D6	14	MCL
15	PH(1)	C7	15	PH(1)
16	$\overline{Be}$	C8		
17	$\overline{Ba}$	C9	16	$\overline{Ba}$
18	$\overline{Bb}$	B8	17	$\overline{Bb}$
19	$\overline{Bf}$	B9		
20	$\overline{W}$	B6	18	$\overline{W}$
21	ADV	A6	19	ADV
22	A	B7	20	A
23	E3	A8	21	E3
24	A	A9	22	A
25	ZQ	F6	23	ZQ
26	A	A3	24	A
27	E2	A4	25	E2
28	A	A5	26	A
29	A	A7	27	A
		B5	28	AO36
30	$\overline{Bc}$	B3	29	$\overline{Bc}$
31	$\overline{Bg}$	B4		
32	$\overline{Bh}$	C3		
33	$\overline{Bd}$	C4	30	$\overline{Bd}$
34	PH(1)	C5	31	PH(1)
35	$\overline{CE}1$	C6	32	$\overline{CE}1$
36	CP2	G6	33	CP2
37	CP3	H6	34	CP3
38	CK	K3	35	CK
39	M2	L6	36	M2

Note:
1. Input of PH register connected to Vss.

BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) Continued:

X72		Ball Loc.	X36	
Sequence	Pkg. Ball		Sequence	Pkg. Ball
40	$\overline{SD}$	N6	37	$\overline{SD}$
41	MCL	P6	38	MCL
42	A	V3	39	A
43	A	U4	40	A
44	A	V4	41	A
45	A	V5	42	A
46	A	W5	43	A
47	A	V6	44	A
48	DQd	W2	45	DQd
49	DQd	W1	46	DQd
50	DQd	V2	47	DQd
51	DQd	V1	48	DQd
52	DQd	U2	49	DQd
53	DQd	U1	50	DQd
54	DQd	T2	51	DQd
55	DQd	T1	52	DQd
56	DQPd	R1	53	DQPd
57	DQPh	R2		
58	DQh	P2		
59	DQh	P1		
60	DQh	N2		
61	DQh	N1		
62	DQh	M2		
63	DQh	M1		
64	DQh	L2		
65	DQh	L1		
66	$\overline{CQ2}$	K2	54	$\overline{CQ2}$
67	CQ2	K1	55	CQ2
68	DQc	J2	56	DQc
69	DQc	J1	57	DQc
70	DQc	H2	58	DQc
71	DQc	H1	59	DQc
72	DQc	G2	60	DQc
73	DQc	G1	61	DQc
74	DQc	F2	62	DQc
75	DQc	F1	63	DQc
76	DQPc	E2	64	DQPc
77	DQPg	E1		
78	DQg	D2		
79	DQg	D1		
80	DQg	C2		
81	DQg	C1		

BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) Continued:

X72		Ball Loc.	X36	
Sequence	Pkg. Ball		Sequence	Pkg. Ball
82	DQg	B2		
83	DQg	B1		
84	DQg	A2		
85	DQg	A1		
86	DQb	A10	65	DQb
87	DQb	A11	66	DQb
88	DQb	B10	67	DQb
89	DQb	B11	68	DQb
90	DQb	C10	69	DQb
91	DQb	C11	70	DQb
92	DQb	D10	71	DQb
93	DQb	D11	72	DQb
94	DQPb	E11	73	DQPb
95	DQPf	E10		
96	DQf	F10		
97	DQf	F11		
98	DQf	G10		
99	DQf	G11		
100	DQf	H10		
101	DQf	H11		
102	DQf	J10		
103	DQf	J11		
104	CQ1	K11	74	CQ1
105	$\overline{CQ1}$	K10	75	$\overline{CQ1}$
106	DQa	L10	76	DQa
107	DQa	L11	77	DQa
108	DQa	M10	78	DQa
109	DQa	M11	79	DQa
110	DQa	N10	80	DQa
111	DQa	N11	81	DQa
112	DQa	P10	82	DQa
113	DQa8	P11	83	DQa8
114	DQPa9	R10	84	DQPa9
115	DQPe1	R11		
116	DQe2	T10		
117	DQe3	T11		
118	DQe4	U10		
119	DQe5	U11		
120	DQe6	V10		
121	DQe7	V11		
122	DQe8	W10		
123	DQe9	W11		

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

	Frequency	Order Part No.	Package
256K x 72	200	IS61NSCS25672-200B	209-Ball BGA
	225	IS61NSCS25672-225B	209-Ball BGA
	250	IS61NSCS25672-250B	209-Ball BGA
	300	IS61NSCS25672-300B	209-Ball BGA
	333	IS61NSCS25672-333B	209-Ball BGA
512K x 36	200	IS61NSCS51236-200B	209-Ball BGA
	225	IS61NSCS51236-225B	209-Ball BGA
	250	IS61NSCS51236-250B	209-Ball BGA
	300	IS61NSCS51236-300B	209-Ball BGA
	333	IS61NSCS51236-333B	209-Ball BGA

Industrial Range: -40°C to 85°C

	FrequencySpeed (ns)	Order Part No.	Package
		TBD	