Honeywell

HXNV0100
64K x 16 Non-Volatile Magnetic RAM

Advanced Information

The 64K x 16 radiation hardened low power nonvolatile Magnetic RAM (MRAM) is a high performance 65,536 word x 16-bit magnetic random access memory with industry-standard functionality.

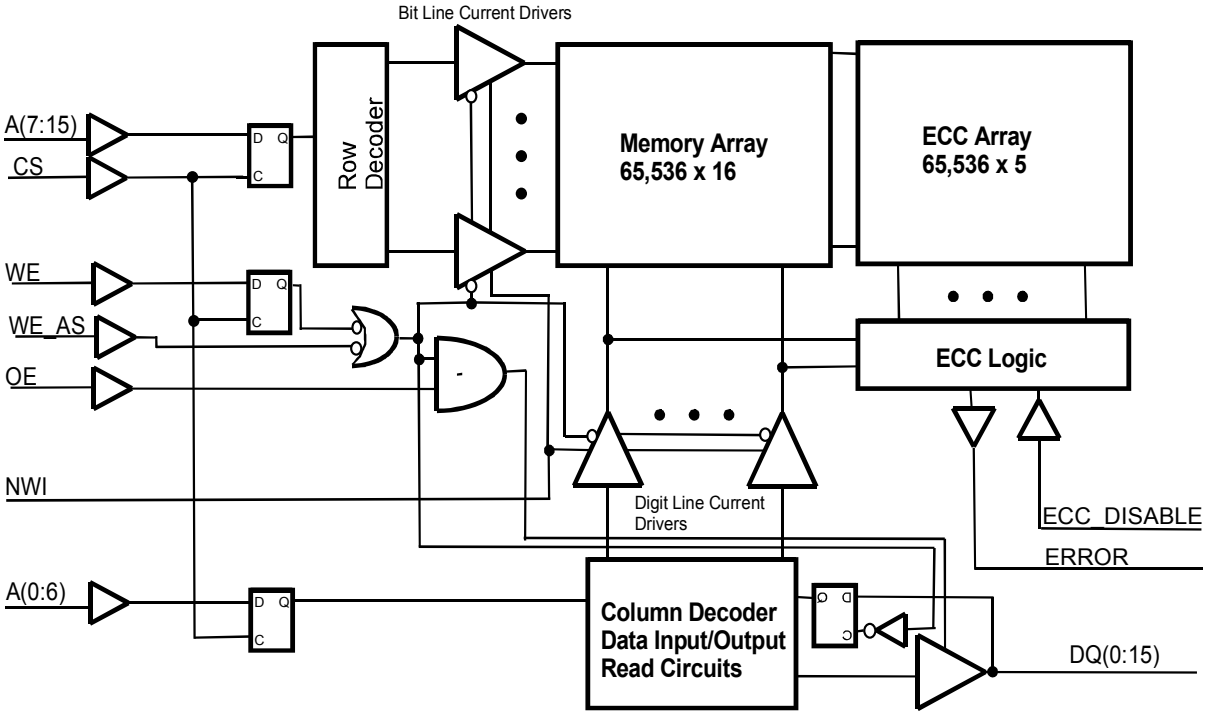
The MRAM is designed for very high reliability. Redundant write control lines, error correction coding and low-voltage write protection ensure the correct operation of the memory and that it is protected from inadvertent writes.

Integrated Power Up and Power Down circuitry controls the condition of the device during power transitions. It is fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology, and is designed for use in low-voltage systems operating in radiation environments. The MRAM operates over the full military temperature range and is operated with 3.3 ± 0.3V and 1.8 ± 0.15 V power supplies.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS Underlayer Technology
- 150 nm Process (Leff = 130 nm)
- Total Dose Hardness ≥ $3x10^5$ rad (SiO_2)
- Dose Rate Upset Hardness ≥ $1x10^{10}$ rad(Si)/s
- Dose Rate Survivability ≥$1x10^{12}$ rad(Si)/s
- Soft Error Rate ≤$1x10^{-10}$ upsets/bit-day
- Neutron Hardness ≥$1x10^{13}$ cm^{-2}
- No Latchup
- Read Cycle Time ≤60 ns
- Write Cycle Time ≤100ns
- Typical Operating Power ≤500 mW
- Unlimited Read/Write (>1E15 Cycles)
- >10 years Power-Off Data Retention
- Synchronous Operation
- Single-Bit Error Detection & Correction (ECC)
- Dual Power Supplies
  - 1.8 V ± 0.15V, 3.3 V ±0.3V
  - 3.3V CMOS Compatible I/O
- Operating Range is -55°C to +125°C
- Package: 64 Lead Shielded ceramic Quad Flat Pack

FUNCTIONAL BLOCK DIAGRAM



SIGNAL DESCRIPTION

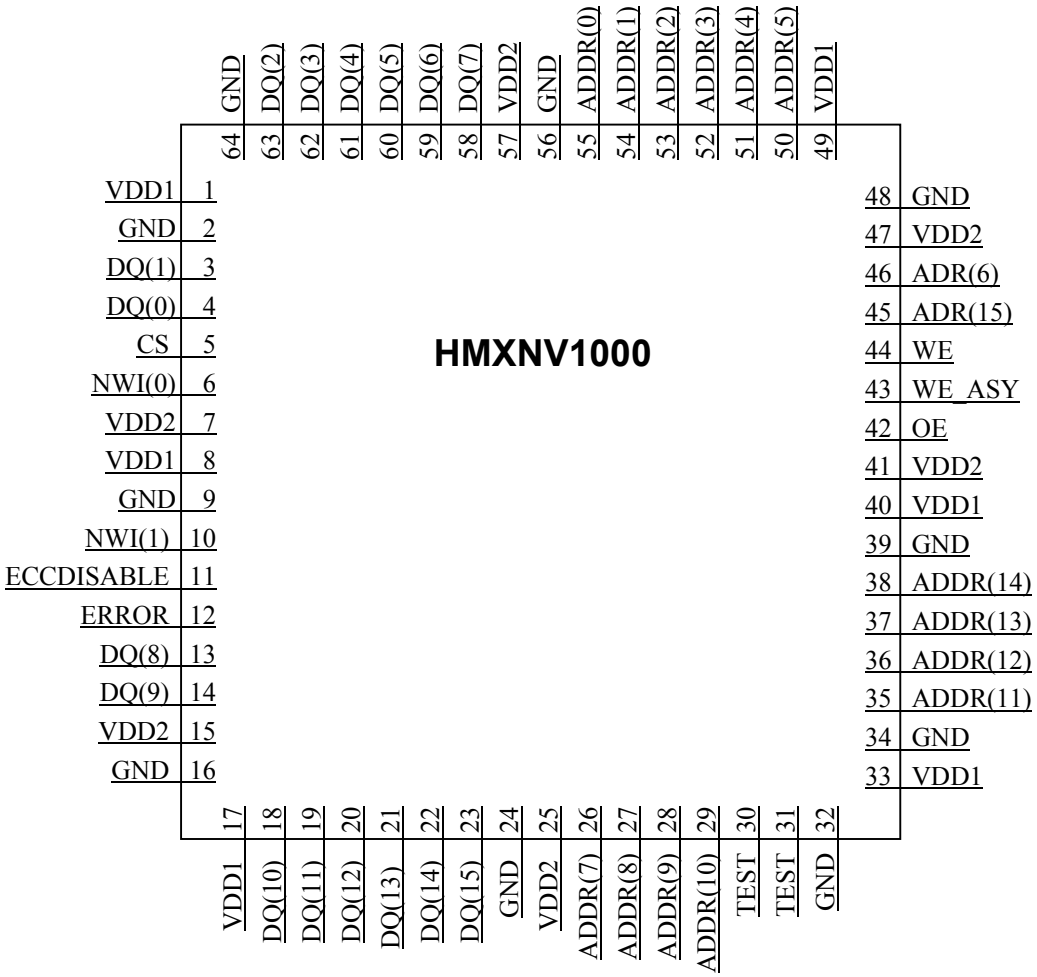
Signal	Definition
A(0:6)	Column Select Address Input. Signals which select a column within the memory array.
A–(7:15)	Row Select Address Input. Signals which select a row within the memory array.
DQ(0:15)	Data Input/Output Signals. Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation.
CS	Chip select. The rising edge of CS will clock in the address and WE signals
WE	Write Enable. This signal is latched to enable a write.
WE_AS	Write Enable Asynchronous – This signal can be used to delay the beginning of the write cycle
OE	Output Enable.
NWI_0 NWI_1	Not Write Inhibit – When set low, these signals inhibit writes to the memory. A high level allows the memory to be written. NWI(0) controls address locations A(15:0) = 0x0000 to 0x7FFF. NWI(1) controls address locations A(15:0) = 0x1000 to 0xFFFF.
ECC_Disable	Error Correction Disable – Disables the error correction function.
ERROR	ECC Error flag
Test_1 Test_2	These signals are for Honeywell test purposes only. These should be grounded in normal operation.
VDD1	DC Power Source Input: 1.8V
VDD2	DC Power Source Input: 3.3V

TRUTH TABLE

NWI	WE & WE_ASY	OE	MODE	DQ
L	X	L	Deselected	High Z
H	L	L	Disabled	High Z
H	L	H	Read	Data Out
H	H	X	Write	Data In

X: $V_I = V_{IH}$ or V_{IL}

PACKAGE PINOUT



RAM and ROM Functional Capability

This MRAM incorporates two write control signals allowing the two sections of the memory to be controlled independently. The two NOT WRITE INHIBIT signals, NWI(0) and NWI(1), allow one section of the devices to operate as a RAM and the other to operate as a ROM at the full control of the user.

SOI AND MAGNETIC MEMORY TECHNOLOGY

Honeywell's S150 Silicon On Insulator (SOI) is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. The 150 nm process is a technology with a 32Å gate oxide for 1.8 V transistors and 70Å gate oxide for 3.3 V transistors. The memory element is a magnetic tunnel junction (MTJ) that is composed of a magnetic storage layer structure and a magnetic pinned layer structure separated by an insulating tunnel barrier interlayer. During a write cycle, the storage layer is written by the application of two orthogonal currents of the desired polarity using row-and-column addressing. The resistance of the MTJ depends on the magnetic state of the storage layer, which uses the pinned layer structure as a reference, and which enables sensing, signal amplification, and readback. The resistance change is a consequence of the change in tunneling magnetoresistance (TMR) between the storage and pinned layers that depends on the magnetic state of the storage layer. With read and write cycles in excess of 10^{15}, there is no wear-out.

ERROR CORRECTION CODE (ECC)

Hamming 5-Bit ECC

A 5-bit Hamming ECC is generated for all data written into memory. This code allows for the correction of all single-bit errors per address. On a read cycle, the data is read from memory and corrected, if necessary, before being placed on the output data bus. There is no change made to the actual data in the memory cells based on the ECC results. Actual data in memory is changed only upon writing new values.

RADIATION CHARACTERISTIC

Total Ionizing Radiation Dose

The MRAM will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at typical VDD and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 KeV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 KeV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The MRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset specification, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ±10%), it is suggested that stiffening capacitance be placed near the package VDD_2 and ground (GND).

It is recommended that the inductance between the MRAM package leads and the stiffening capacitance be less that 1.0 nH. If there are no operate through or valid stored-data requirements, typical circuit board mounted de-coupling capacitors are recommended. The MRAM will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under

recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The MRAM will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes equivalent neutron energy of 1 MeV.

Soft Error Rate

The MRAM is capable of meeting the specified Soft Error Rate (SER) under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits.

Latchup

The MRAM will not latch up under any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR-type latchup structures. Sufficient transistor body tie connections to the p-channel and n-channel substrates are made to ensure no source/drain snapback occurs.

Radiation-Hardness Ratings

Parameter	Limits	Units	Test Conditions
Total Dose: R-Level F-Level H-Level	 $\geq 1 \times 10^5$ $\geq 3 \times 10^5$ $\geq 1 \times 10^6$	Rads(SiO_2)	VDD1= 1.95 Volts, VDD2= 3.6 Volts T_A = 25C, X-Ray or Co^{60}
Soft Error Rate:	$\leq 1 \times 10^{-10}$	Upsets/bit-day	VDD1= 1.8 Volts, VDD2= 3.3 Volts T_C = -55 to 125°C
Transient Dose Rate Upset	$\geq 1 \times 10^{10}$	Rads(Si)/s	VDD1= 1.65 Volts, VDD2= 3.0 Volts T_C = 125°C Pulse Width = 1µsec, X-Ray
Transient Dose Rate Survivability	$\geq 1 \times 10^{12}$	Rads(Si)/s	VDD1= 1.95 Volts, VDD2= 3.6 Volts T_A = 25°C Pulse Width = 50 nsec, X-Ray
Neutron Fluence	$1x10^{13}$	N/cm^{-2}	1MeV equivalent energy

MAGNETIC FIELD CHARACTERISTICS

The MRAM will meet all stated functional and electrical specifications over the entire operating temperature range when exposed to the specified magnetic fields. The magnetic field hardening is achieved through a combination of SOI technology characteristics, circuit design and specialized packaging.

MAGNETIC FIELD RATING

Parameter	Limits	Units	Test Conditions
Magnetic Field	50	Oe	VDD1= 1.8 Volts, VDD2= 3.3 Volts T_C = -55 to 125°C

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Ratings		Units
		Min	Max	
V_{DD_1}	Positive Supply Voltage (2)	-0.5	2.5	Volts
V_{DD_2}	Positive Supply Voltage (2)	-0.5	4.5	Volts
V_{PIN}	Voltage on Any Pin (2)	-0.5	V_{DD_2} + 0.5	Volts
T_{STORE}	Storage Temperature	-65	150	°C
T_{SOLDER}	Soldering Temperature		225°C	°C*sec (5)
P_D	Package Power Dissipation (3)		2.5	W
P_{JC}	Package Thermal Resistance (Junction to Case)		2.0	°C/W
V_{PROT}	Electrostatic Discharge Protection Voltage (4)	2000		V
T_J	Junction Temperature		175	°C

1. Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
2. Voltage referenced to GND
3. RAM power dissipation due to I_{DDS}, I_{DDOP}, and I_{DDSEI}, plus RAM output driver power dissipation due to external loading must not exceed this specification
4. Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015
5. Maximum soldering temp of 225°C can be maintained for no more than 5 seconds.

RECOMMENDED OPERATING CONDITIONS (1)

		Limits			
Symbol	Parameter	Min	Typical	Max	Units
V_{DD_1}	Positive Supply Voltage	1.65	1.8	1.95	Volts
V_{DD_2}	Positive Supply Voltage	3.0	3.3	3.6	Volts
T_C	External Package Temperature	-55	25	125	°C
V_{PIN}	Voltage On Any Pin	-0.3		V_{DD_2}+0.3	Volts

(1) Voltages referenced to GND

DC ELECTRICAL CHARACTERISTICS

			Limits			
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**	**Test Conditions**
VIL	Low Level Input Voltage			0.3VDD	V	
VIH	High-level Input Voltage	0.7VDD			V	
VOL	Low-level Output Voltage		0.35	0.5	V	VDD = 3.0 volts
VOH	High-level Output Voltage	VDD-0.5	2.66 (2.95)		V	VDD = 3.0 volts (VDD = 3.3 volts)
IOZ	Output Leakage Current		TBD		μA	
IL	Input Leakage Current		TBD		μA	
IO	Output Drive Current		6		mA	
IDDSB	Standby Current VDD1 (1.8V) VDD2 (3.3V)		 3 3		mA	

AC ELECTRICAL CHARACTERISTICS

			Limits			
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**	**Test Conditions**
IDDWR	Average Write Current VDD1 (1.8V) VDD2 (3.3V)		 15 260		mA	Continuous write cycle at 10 MHz (1)
IDDRD	Average Read Current VDD1 (1.8V) VDD2 (3.3V)		 15 3		mA	Continuous read cycle at 10 MHz (1)

1. Current consumption is reduced with lower duty cycle. The scale is linear with respect to duty cycle with 3 mA minimum values of on each VDD signal.

CAPACITANCE (1)

		Limits			Test Conditions
Symbol	**Parameter**	**Min**	**Max**	**Units**	
C_a and C_C	Address and Control line Capacitance		6	pF	TBD
C_D	Data Line Capacitance		9	pF	Value is I/O buffer only.
C_{NWI}	Not Write Inhibit Capacitance		100	pF	

Note: 1. These values are tested at characterization only.

RISE/FALL TIMES

Symbol	Parameter	Value		Units	Test Conditions
		Min	Max		
R_t	Rise Time		1.4	ns	Cload = 5 pF
R_t	Rise Time		2.9	ns	Cload = 25 pF
F_t	Fall Time		1.4	ns	Cload = 5 pF
F_t	Fall Time		2.9	ns	Cload = 25 pF

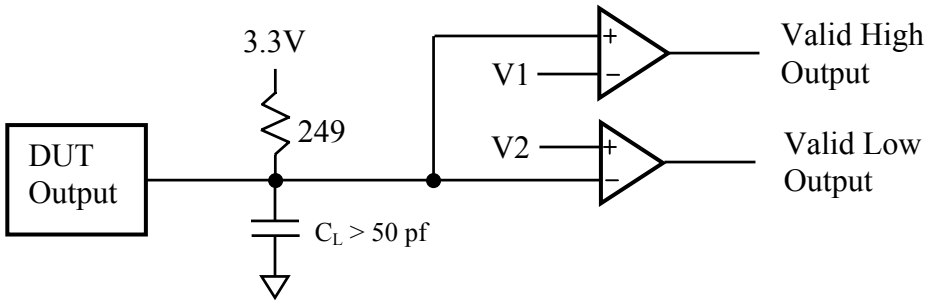
DATA ENDURANCE

Parameter	Ratings		Units	Test Conditions
	Min	Max		
Data Endurance	$1x10^{15}$		Cycles	

DATA RETENTION

Parameter	Ratings		Units	Test Conditions
	Min	Max		
Data Retention	>10		years	

Tester Equivalent Load Circuit

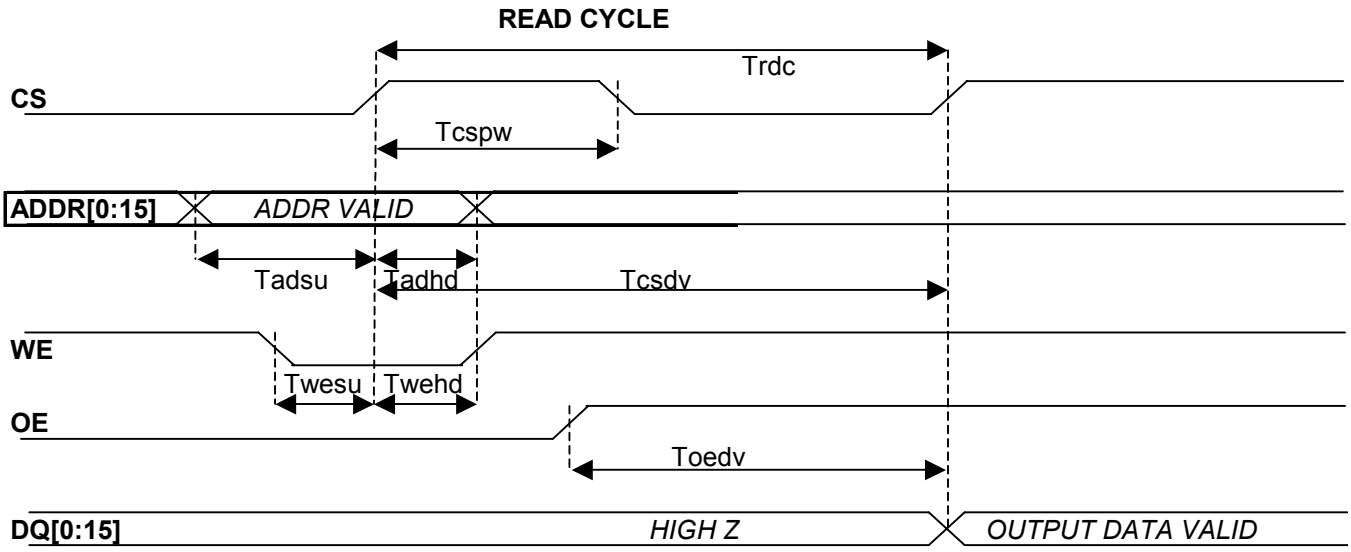


READ CYCLE

The RAM is synchronous in operation relative to the rising edge of the Chip Select (CS) signal. With the initiation of a CS signal, the address and the Write Enable (WE) signal are latched into the device and the read operation begins. The memory locations are read and compared with the ECC values. Any single bit errors are detected and corrected.

If WE was low when latched in, the data is sent to the output drivers. In addition to WE low being latched, Output Enable (OE) must be set to a high value to enable the DQ output buffers. OE is not latched, and may be set high before or after the rising edge of CS.

READ CYCLE AC TIMING CHARACTERISTICS



		Min	Typ	Max
Tcspw	CS pulse width (for valid read)	10ns	------	------
Tcspi	CS ignored pulse width (glitch tolerance)	------	------	1ns
Twesu	WE setup time with respect to rising edge of CS	3ns	------	------
Twehd	WE hold time with respect to rising edge of CS	2ns	------	------
Tadsu	Address setup time with respect to rising edge of CS	8ns	------	------
Tadhd	Address hold time with respect to rising edge of CS	2ns	------	------
Tcsdv	Output data valid with respect to rising edge of CS	------	------	60ns
Toedv	Output data valid with respect to rising edge of OE	------	------	10ns
Trdc	CS rising edge to next CS rising edge (read cycle time)	60ns	------	------

WRITE CYCLE

The RAM is synchronous in operation relative to the rising edge of the Chip Select (CS) signal. With the initiation of a CS signal, the address and the Write Enable (WE) signal are latched into the device.

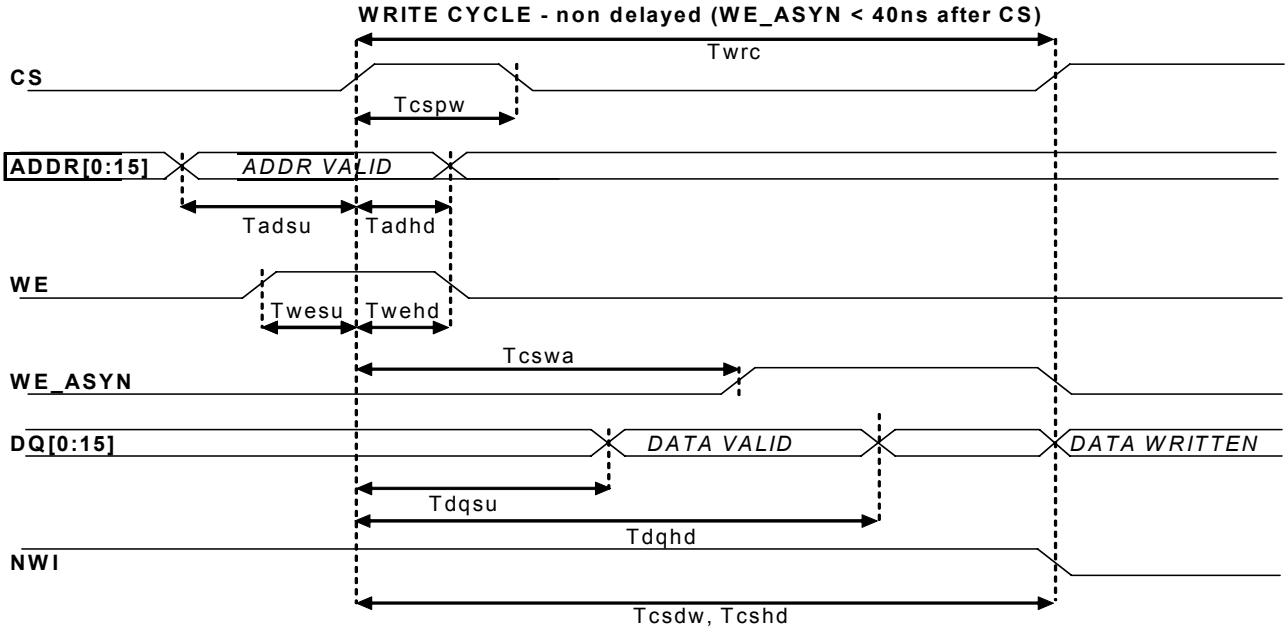
If WE was high when latched in, the Write Asynchronous (WE_AS) signal is checked. If WE_AS is high, the WRITE CYCLE will begin. If WE_AS is low, the WRITE CYCLE will be delayed until WE_AS is set high. This allows control by the host processor of the actual time the data is written to memory.

The WRITE CYCLE begins by reading the current value in memory. The current memory data is compared to the data to be written. If the location needs to change value, the data is then written.

The bit cell construction of this device does not provide a method of simply writing a “1” or a “0” to match the data. The “write” to a bit can only change its state, thus the need to read the bit locations first. Only the bits which need to “change state” are actually written.

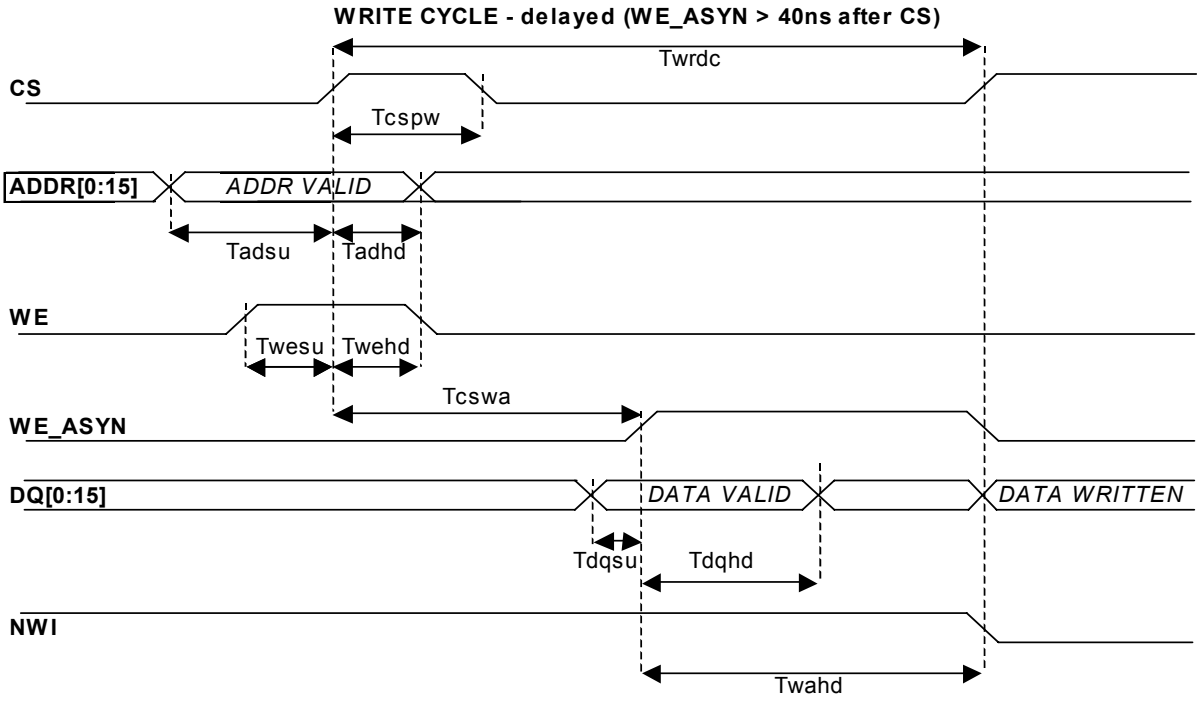
WRITE CYCLE AC TIMING CHARACTERISTICS

NON-DELAYED



		Min	Typ	Max
Tcspw	CS pulse width (for valid write)	10ns	------	------
Tcspi	CS ignored pulse width (glitch tolerance)	------	------	1ns
Twesu	WE setup time with respect to rising edge of CS	3ns	------	------
Twehd	WE hold time with respect to rising edge of CS	2ns	------	------
Tadsu	Address setup time with respect to rising edge of CS	8ns	------	------
Tadhd	Address hold time with respect to rising edge of CS	2ns	------	------
Tcswa	WE_ASYN delay from rising edge of CS			40ns
Tdqsu	DQ setup time after rising edge of CS	------	------	20ns
Tdqhd	DQ hold time with respect to rising edge of CS	60ns	------	------
Tcsdw	Valid data write time *WRT* rising edge of CS	------	------	100ns
Tcshd	NWI,WE_ASYNC hold time *WRT* rising edge of CS	100ns	------	------
Twrc	CS rising edge to next CS rising edge (write cycle time)	100ns	------	------

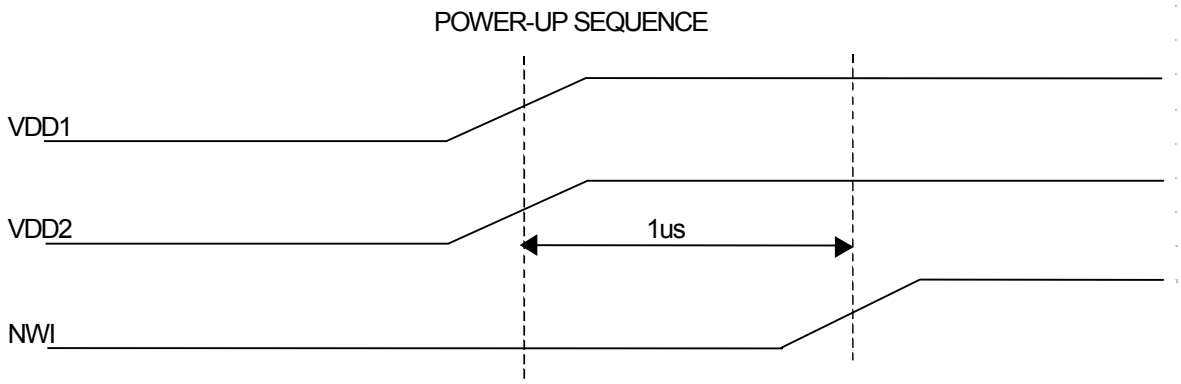
DELAYED



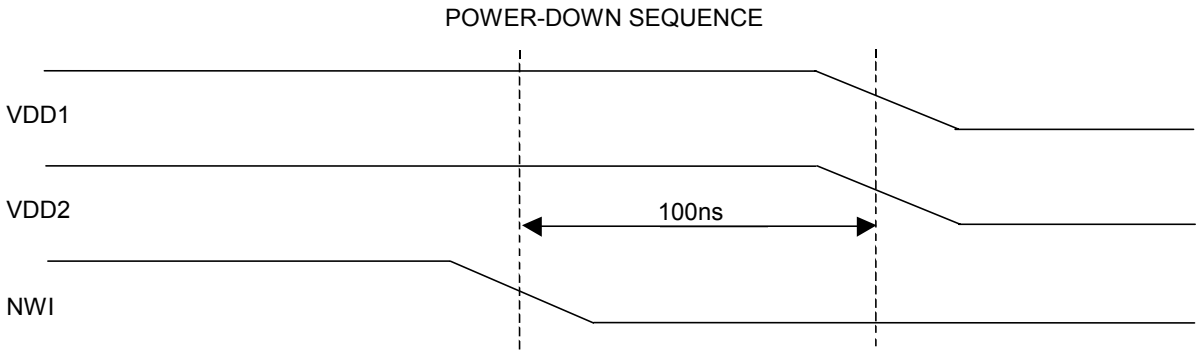
		Min	Typ	Max
Tcspw	CS pulse width (for valid write)	10ns	------	------
Tcspi	CS ignored pulse width (glitch tolerance)	------	------	1ns
Twesu	WE setup time with respect to rising edge of CS	3ns	------	------
Twehd	WE hold time with respect to rising edge of CS	2ns	------	------
Tadsu	Address setup time with respect to rising edge of CS	8ns	------	------
Tadhd	Address hold time with respect to rising edge of CS	2ns	------	------
Tcswa	WE_ASYN delay from rising edge of CS	40ns	------	------
Tdqsu	DQ setup time to rising edge of WE_ASYN	4ns	------	------
Tdqhd	DQ hold time *WRT* rising edge of WE_ASYN	20ns	------	------
Twadw	Valid data write time *WRT* rising edge of WE_ASYNC	------	------	60ns
Twahd	NWI,WE_ASYN, hold time *WRT* rising edge of WE_ASYN	60ns	------	------
Twrdc	CS rising edge to next CS rising edge (write cycle time)	Tcswa + 60ns	------	------

POWER UP TIMING

During power-up there are no restrictions on which supply comes up first provided NWI is asserted (low). NWI is de-asserted within 1us of both supplies reaching their 90% values.



POWER DOWN TIMING



QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process and six sigma controls. It is part of a “Total Quality Assurance Program”, the computer-based process performance tracking system and a radiation hardness assurance stategy.

SCREENING LEVELS

Honeywell offers several levels of device screeing to meet your needs. “Engineering Devices” are available with limited perfomrance and screening for prototype development and evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883.

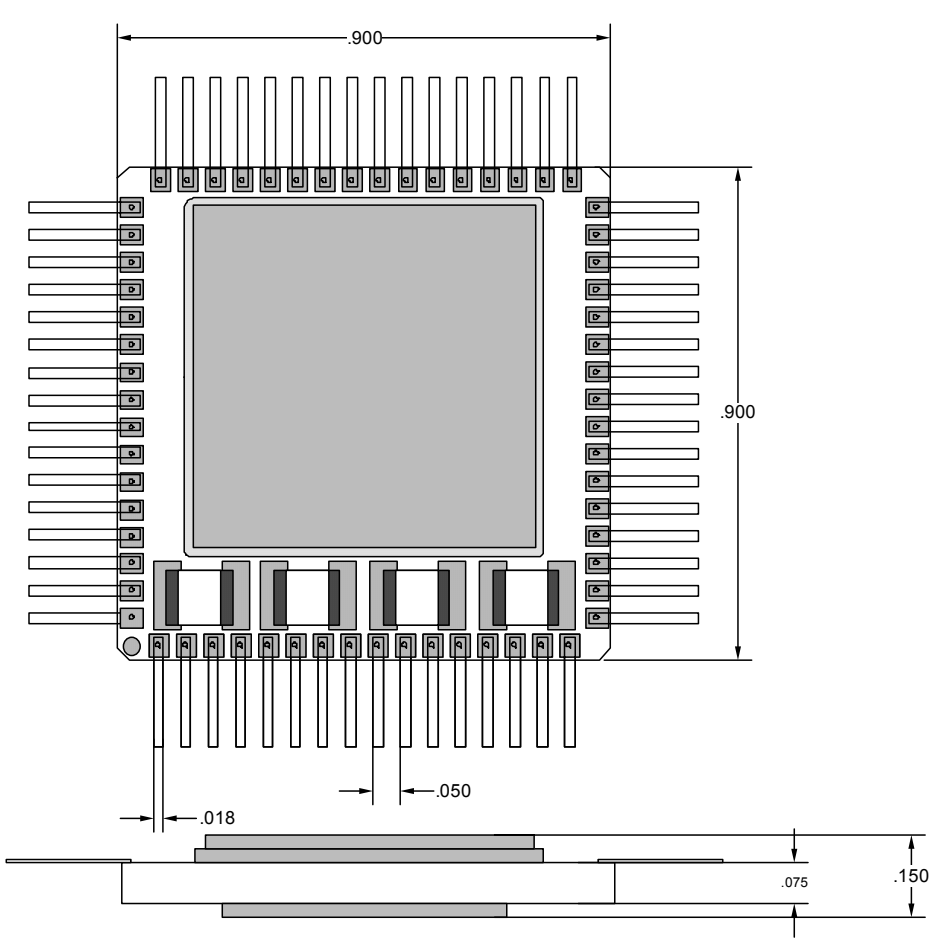
RELIABILITY

Honeywell understands the stringent reliability requirements that space and defense systems require. Honeywell has extensive experience in reliability testing on programs of this nature. Reliability attributes of the SOI process were characterized by testing specially designed structures to evaluate failure mechanisms including hot carriers, electro migration, and time-dependent dielectric breakdown. The results are feedback to improve the process to ensure the highest reliability products.

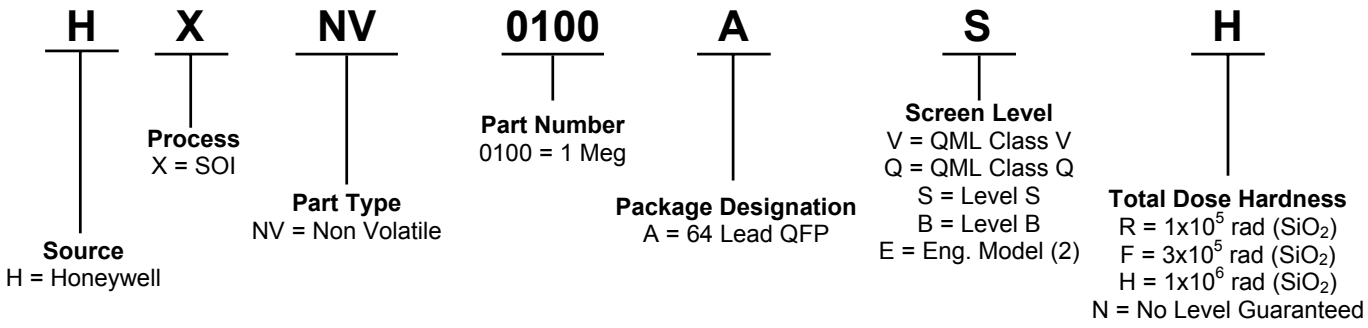
In addition, our products are subjected to dynamic, accelerated life tests. The packages used are qualified through MIL-STD-883, TM 5005 Class S. The product screening flow can be modified to meet the specific requirements. Quality conformance testing is performed as an option on all production lots to ensure on-going reliability.

PACKAGE OUTLINE

The 64 Lead Shielded Ceramic QFP Package shown is preliminary and is subject to change, including external capacitors. The outline is for reference only.



ORDERING INFORMATION (1)



(1) To order parts or obtain technical assistance, call 1-800-323-8295
(2) Engineering Model Description: Parameters are tested from-55 to 1250C, 24-hour burn-in, no radiation guarantee.

For more information about Honeywell's MRAM product and our family of memory and ASIC products and services, visit www.myspaceparts.com.

Honeywell

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