

ADVANCED INFORMATION

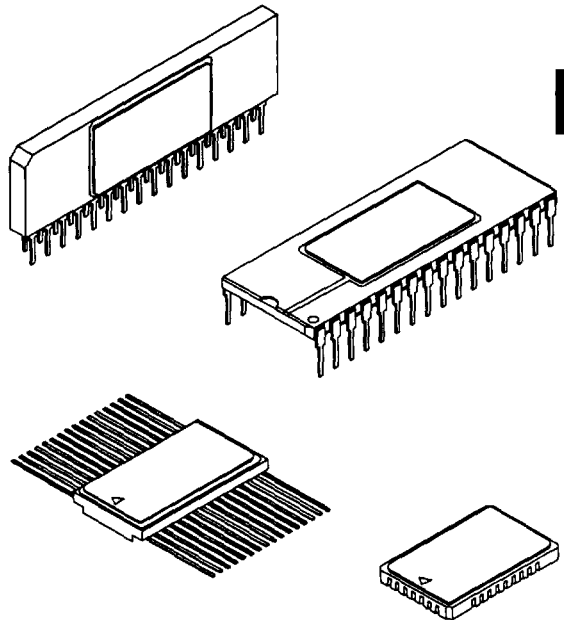
DESCRIPTION:

The DPS128M8A is a high speed monolithic 128K X 8 Static Random Access Memory (SRAM) fabricated using CMOS technology. It is designed for use in high density, high speed, low power applications. All pins are TTL compatible and a single +5 Volt power supply is required.

The DPS128M8A has extremely low standby power dissipation making it suitable for battery backup.

The 600-mil wide, 32-pin ceramic, Dual-In-Line Package (DIP), conforms to the JEDEC standard. Dense-Pac also offers a 32-pin ceramic FLATPACK, a 32-Pad Leadless Chip Carrier (LCC), and a space saving 32-pin Zig-Zag-In-Line Package (ZIP).

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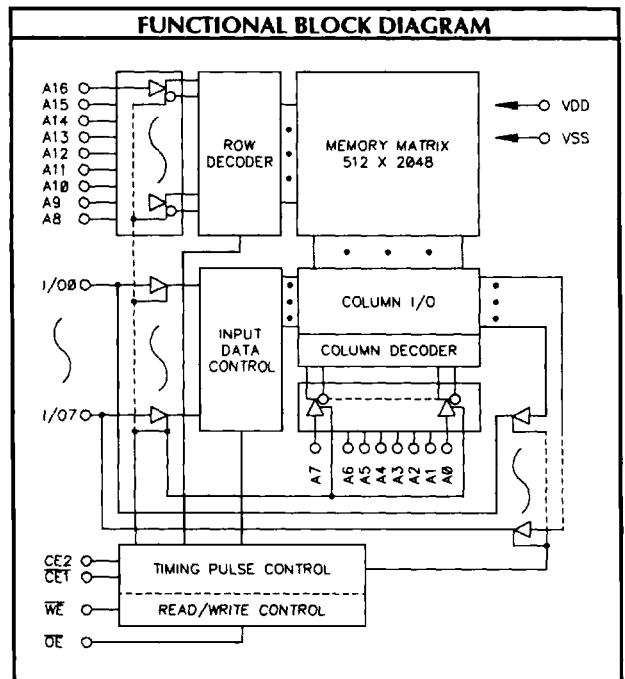


FEATURES:

- 131,072 by 8-Bits Organization
- Access Times: 35*, 45, 55, 70ns (max.)
- Low Power: 50 μ W (typ.) Standby
300mW (typ.) Operating
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, \pm 10% Tolerance
- Two Chip Enables
- Output Enable Functions
- Faster Access Speeds Available Upon Request
- Package Types:
 - 32-Pin Ceramic Side Brazed DIP
 - 32-Pin Ceramic FLATPACK
 - 32-Pin Ceramic ZIP
 - 32-Pad Ceramic LCC

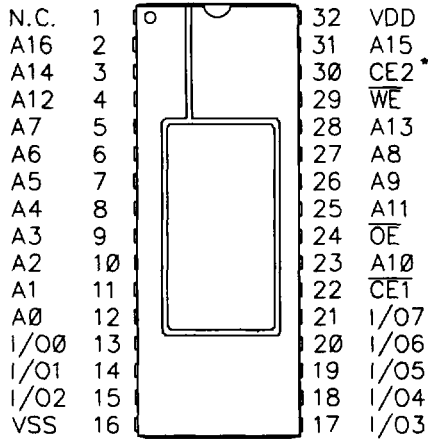
* Commercial Only

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE1}$, CE2	Chip Enables
\overline{WE}	Write Enable
\overline{OE}	Output Enable
VDD	Power (+5V)
VSS	Ground
N.C.	No Connect

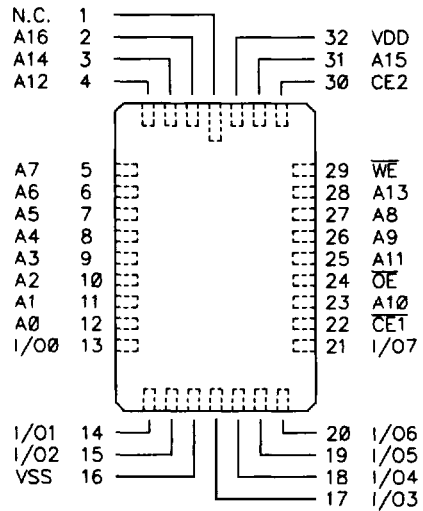


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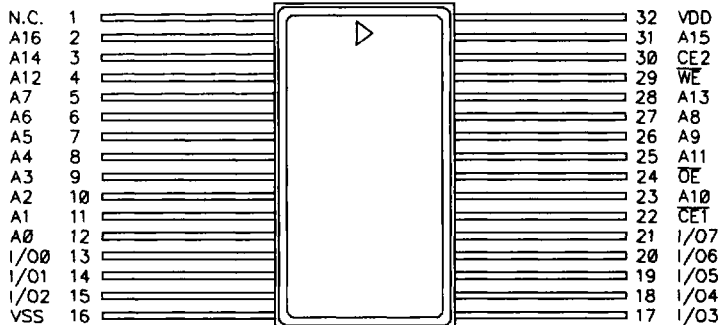
PIN-OUT DIAGRAMS (TOP VIEW)



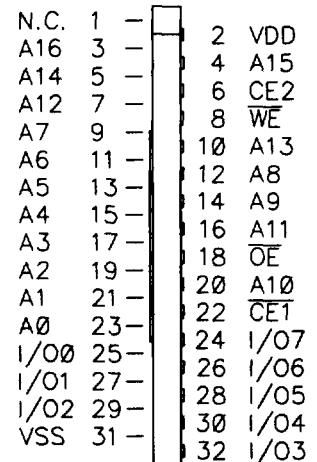
CERDIP



CERAMIC LCC



CERAMIC FLATPACK



CERAMIC ZIP

* Cerdip also available with one Chip Enable (DPS128M8ANS). Pin 30 on this version is a no connect (N.C.) consult factory.

ADVANCED INFORMATION

RECOMMENDED OPERATING RANGE¹

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V

ABSOLUTE MAXIMUM RATINGS³

Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V

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TRUTH TABLE

Mode	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	I/O Pin	Supply Current
Not Selected	H	X	X	X	HIGH-Z	Standby
Not Selected	X	L	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	H	HIGH-Z	Active
Read	L	H	L	H	DOUT	Active
Write	L	H	X	L	D _{IN}	Active

L = LOW

H = HIGH

X = Don't Care

CAPACITANCE⁴: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	8	pF	V _{IN} = 0V
C _{ADR}	Address Input	8		
C _{WE}	Write Enable	8		
C _{OE}	Output Enable	8		
C _{I/O}	Data Input/Output	10		

DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	TYP. (°)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-	-2	2	-2	2	-2	2	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-	-2	2	-2	2	-2	2	μA
I _{CC1}	Active Supply Current	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	40		70		80		80	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA	70		110		120		120	mA
I _{SB1}	Full Standby Supply Current (CMOS)	$\overline{CE} \geq V_{DD} - 0.2V$	0.01		1		2		3	mA
I _{SB2}	Standby Supply (TTL)	$\overline{CE} = V_{IH}$	6		10		15		15	mA
I _{DR3}	Data Retention Supply Current (3V)	V _{DR} = 3V, $\overline{CE1} \geq V_{DR} - 0.2V$, CE2 $\geq V_{DR} - 0.2V$ or CE2 $\leq 0.2V$	10		120		200		700	μA
I _{DR2}	Data Retention Supply Current (2V)	V _{DR} = 2V, $\overline{CE1} \geq V_{DR} - 0.2V$, CE2 $\geq V_{DR} - 0.2V$ or CE2 $\leq 0.2V$	5		100		170		500	μA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA	-		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	-		2.4		2.4		2.4	V

* Typical Values at +25°C and +5V.

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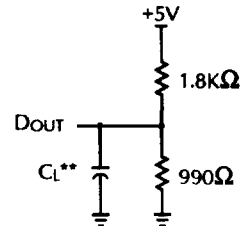
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	C _L	Parameters Measured
1	100 pF	except t _{CLZ} , t _{CHZ} , t _{OHZ} , t _{OLZ} , t _{WLZ} and t _{WHZ}
2	5 pF	t _{CLZ} , t _{CHZ} , t _{OHZ} , t _{OLZ} , t _{WLZ} and t _{WHZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-35†		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	35		45		55		70		ns
2	t _{AA}	Address Access Time		35		45		55		70	ns
3	t _{CO1}	Chip Enable (CE1) to Output Valid		35		45		55		70	ns
4	t _{CO2}	Chip Enable (CE2) to Output Valid		35		45		55		70	ns
5	t _{OE}	Output Enable to Output Valid		20		25		30		40	ns
6	t _{LZ1}	Chip Enable (CE1) to Output in LOW-Z ^{4, 5}	5		5		5		5		ns
7	t _{LZ2}	Chip Enable (CE2) to Output in LOW-Z ^{4, 5}	5		5		5		5		ns
8	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 5}	0		0		0		0		ns
9	t _{HZ1}	Chip Enable (CE1) to Output in HIGH-Z ^{4, 5}		15		20		25		30	ns
10	t _{HZ2}	Chip Enable (CE2) to Output in HIGH-Z ^{4, 5}		15		20		25		30	ns
11	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 5}		15		20		25		30	ns
12	t _{OH}	Output Hold from Address Change	5		5		5		10		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6,7} : Over operating ranges											
No.	Symbol	Parameter	-35†		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t _{WC}	Write Cycle Time	35		45		55		70		ns
14	t _{AW}	Address Valid to End of Write	30		40		45		65		ns
15	t _{CW}	Chip Enable to End of Write	30		40		45		65		ns
16	t _{AS}	Address Setup Time***	0		0		0		0		ns
17	t _{WP}	Write Pulse Width	30		35		40		55		ns
18	t _{WR}	Write Recovery Time	5		5		5		5		ns
19	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 5}		15		20		25		30	ns
20	t _{DW}	Data to Write Time Overlap	18		20		25		35		ns
21	t _{DH}	Data Hold from Write Time	0		0		0		0		ns
22	t _{OW}	Output Active from End of Write	5		5		5		5		ns

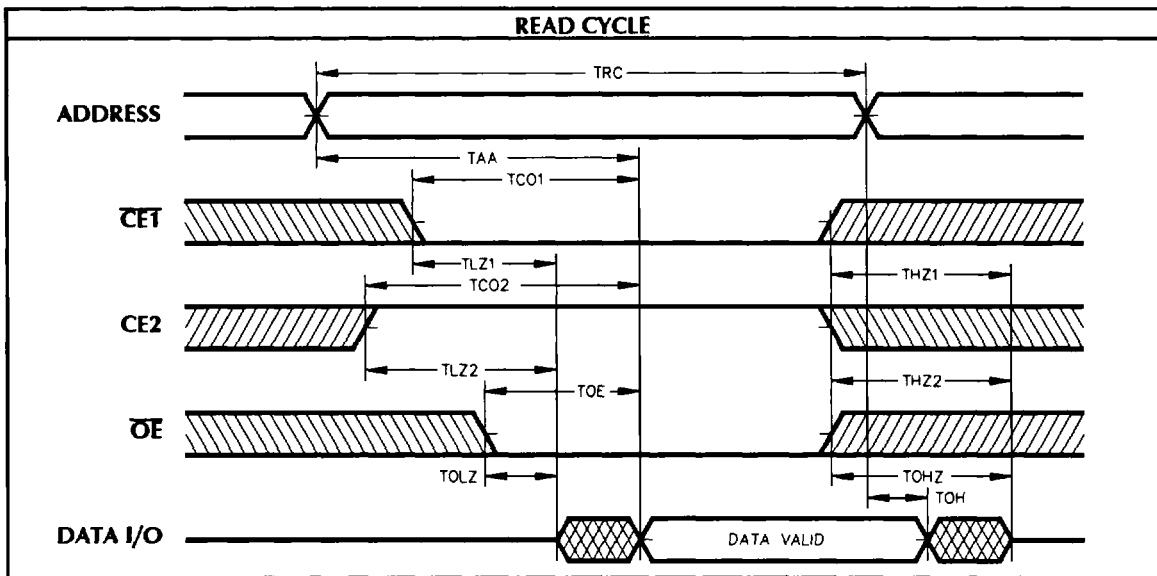
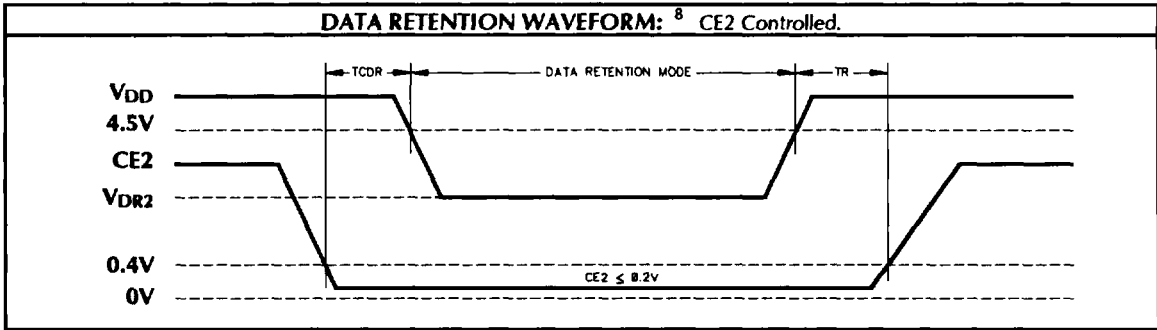
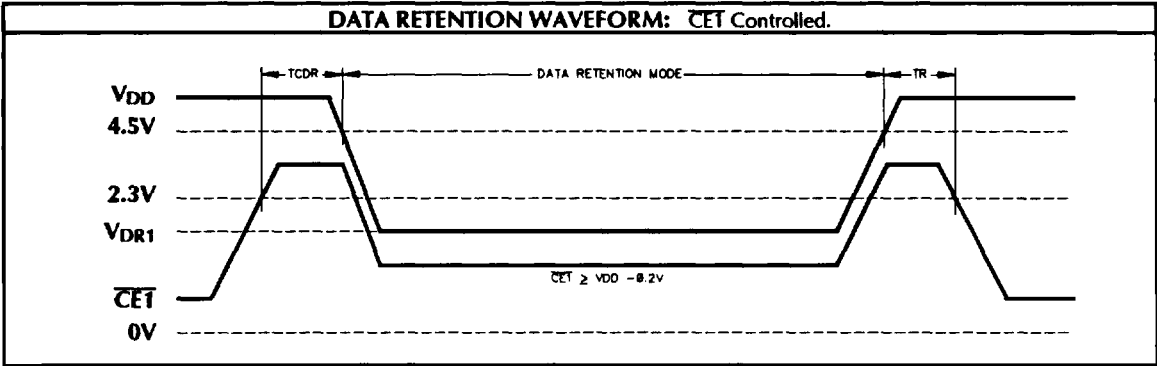
*** Valid for both Read and Write Cycles.

† Commercial only.

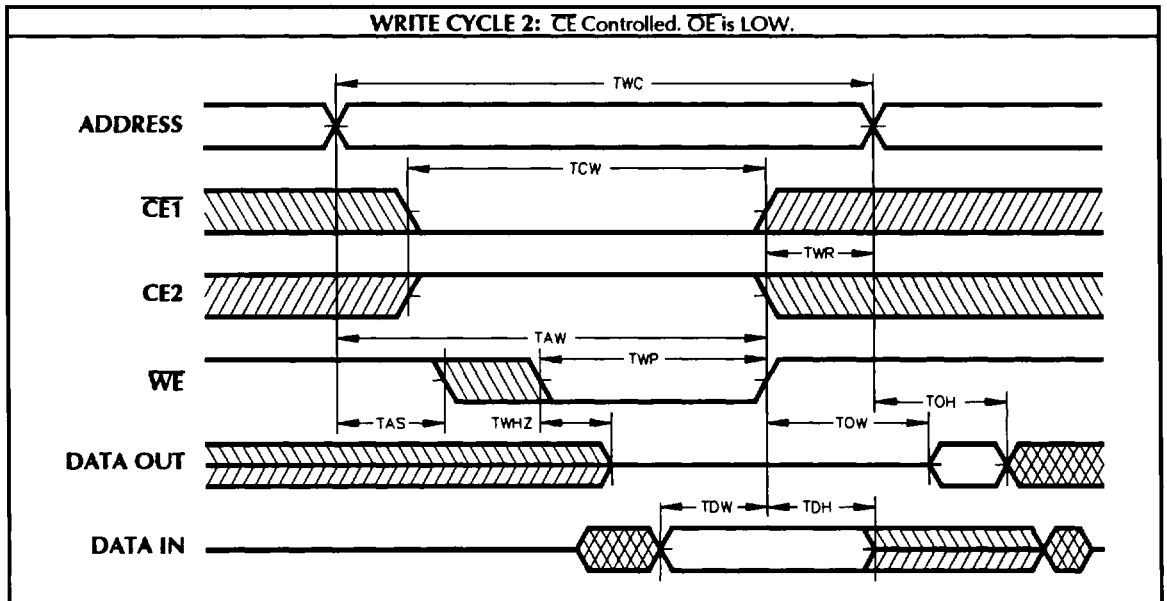
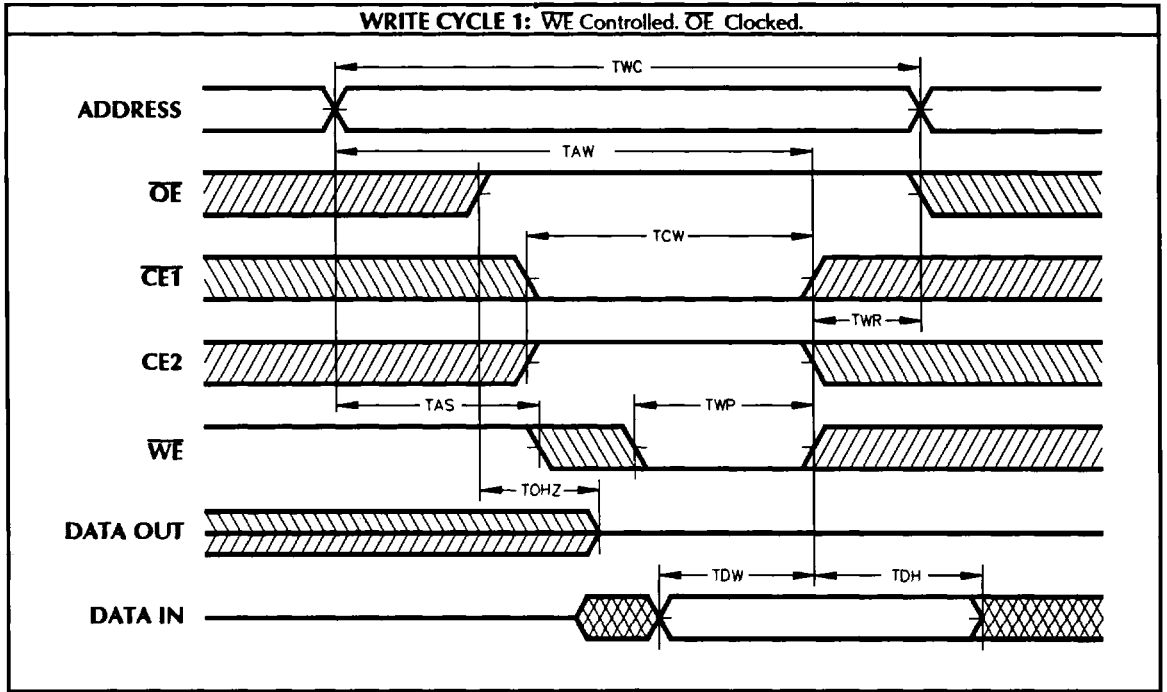
Data Retention AC Characteristics						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	CET ≥ V _{DD} - 0.2V, CE2 ≥ V _{DD} - 0.2V or CE2 ≤ V _{DD} + 0.2V	2.0	-	-	V
t _{CDR}	Chip Disable to Data Retention Time	See Retention Waveform	0	-	-	ns
t _R	Operation Recovery Time	See Retention Waveform	5	-	-	ms

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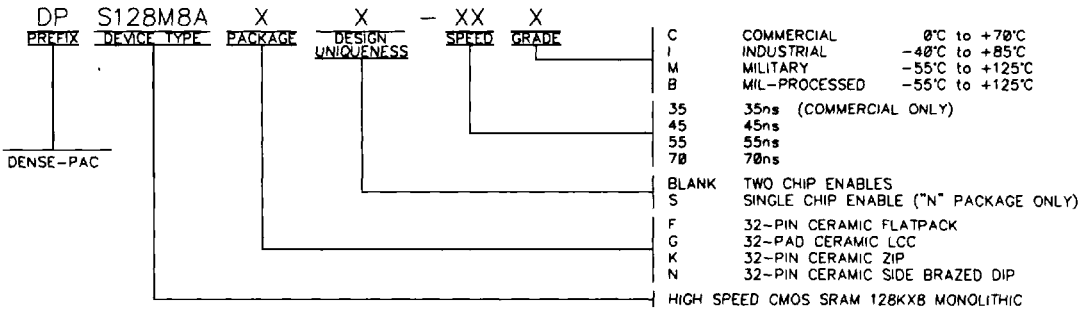


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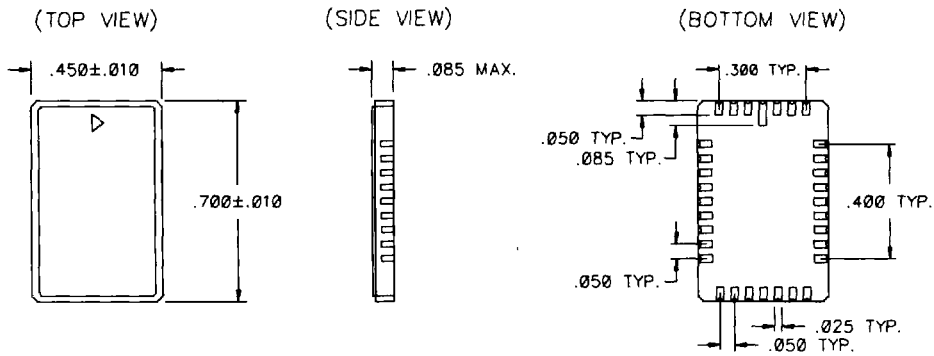


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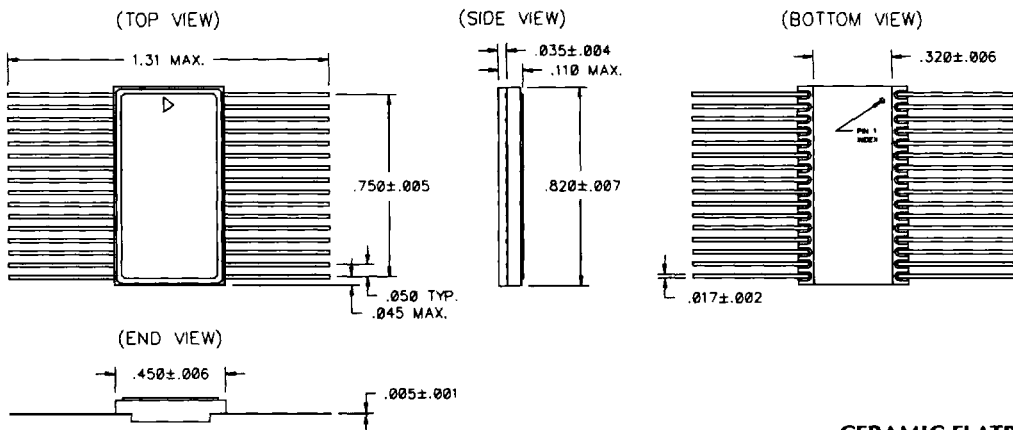
ORDERING INFORMATION



MECHANICAL DIAGRAMS

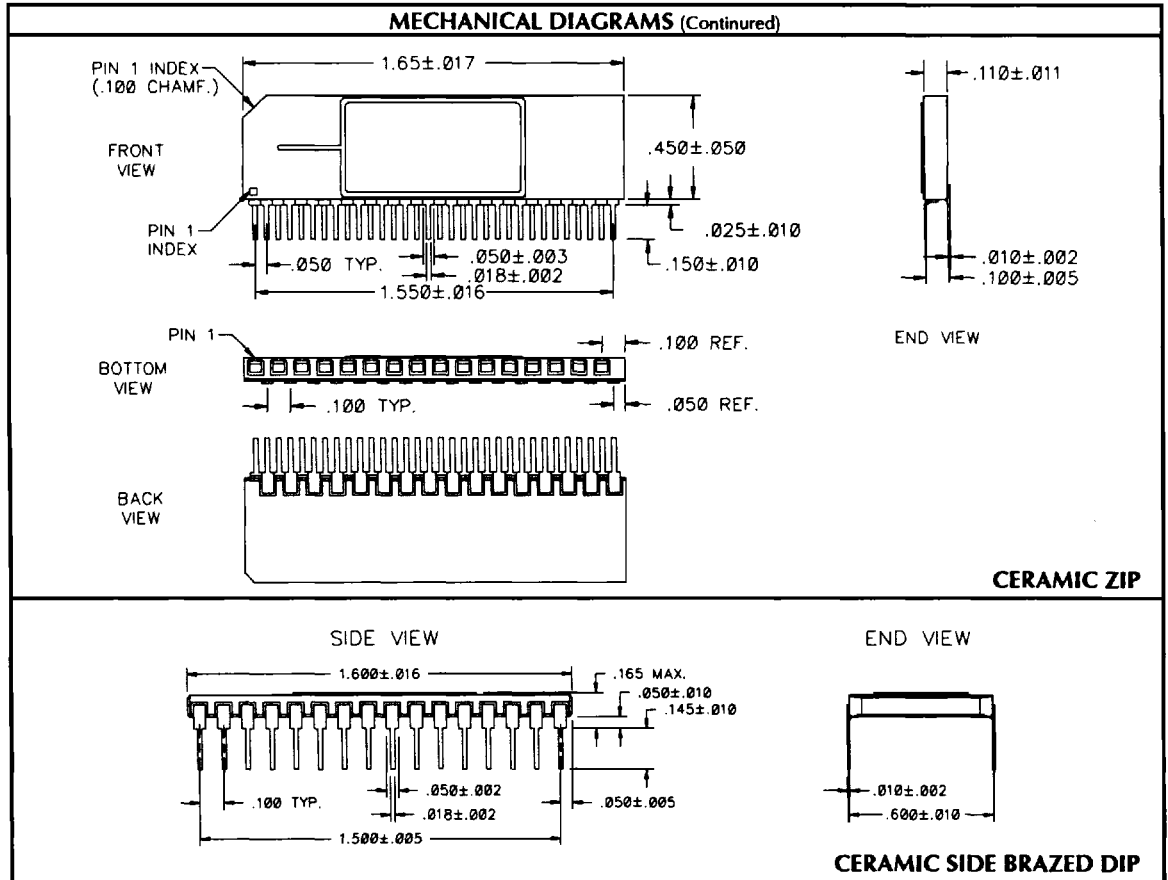


CERAMIC LCC



CERAMIC FLATPACK

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NOTES:

1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500 mV from steady state voltage.
6. When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.
8. CE2 controls address buffer, \overline{WE} buffer, \overline{CET} buffer and \overline{OE} buffer and D_{IN} buffer. If CE2 controls Data Retention Mode, V_{IN} levels (Address, \overline{WE} , \overline{OE} , $\overline{CS1}$, I/O) can be in the high impedance state. If \overline{CET} controls Data Retention Mode, CE2 must be $CE2 \geq V_{DD} - 0.2V$ or $0V \leq CE2 \leq 0.2V$. The other input levels (Address, \overline{WE} , \overline{OE} , I/O) can be in the High Impedance State.

Dense-Pac Microsystems, Inc.

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