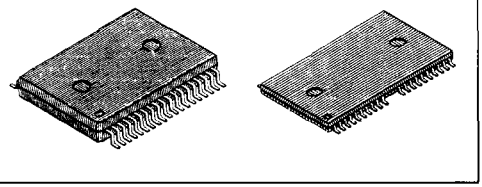
SONY

CXK1206AM/ATM

Video Signal Field Memory

CXK1206AM 38 pin SOP (Plastic)

CXK1206ATM 44 pin TSOP (II) (Plastic)



Description

The CXK1206AM/ATM is a 3-port VRAM capable of coping with both NTSC and PAL and of storing pictures for one 8-bit field with two chips, and is suitable as a memory for improving the picture quality including NR + TBC, and NR + double speed.

Features

- Asynchronous 3-ports, one for Write and two for Read.
- 960 column × 306 row × 4 bit structure (suitable for video signal processing).
- NTSC and PAL are respectively compatible with 4 fsc.
- Applicable to various uses in recursive mode/non-recursive mode.
- Random access : column → by block (Write only)
  row → by line.
- Transmission between I/O ports and the internal memory can be automatically controlled from the inside.
- Transfer synchronizing function.
- Power consumption: 100 mW (Typ.)
- Power supply: +5V ±10%.
- I/O level: TTL Low input capacitance.
- Substrate bias generator built in.

Structure

Silicon gate three-layered polysilicon, CMOS

Applications

Video signal processing field memory

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

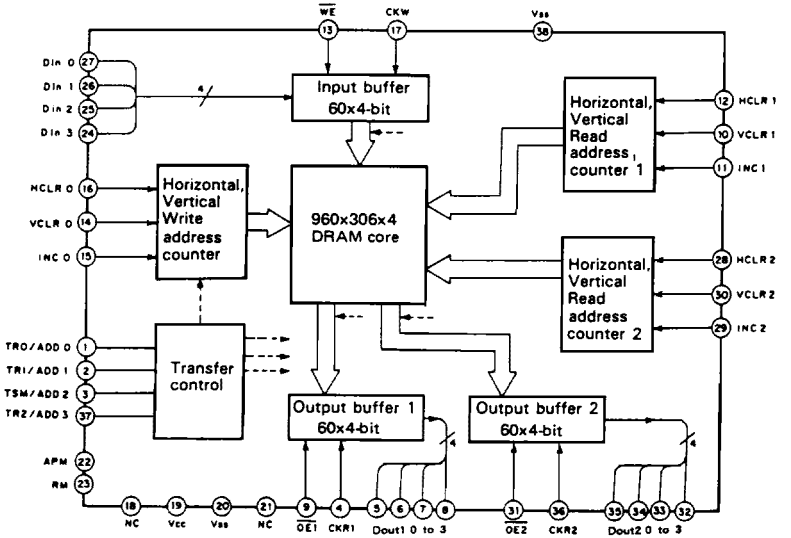
• Supply voltage	V_{CC}	−1.0 to +7.0	V
• Operating temperature	T_{opr}	0 to +70	°C
• Storage temperature	T_{stg}	−55 to +125	°C
• Allowable power dissipation	P_D	1.0	W

Recommended Operating Conditions (Ta = 0 to 70°C, Vss = 0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Supply voltage	V_{SS}	0	V
• Input voltage "H level"	V_{IH}	2.4 to 6.5	V
• Input voltage "L level"	V_{IL}	−2.0 to +0.8	V

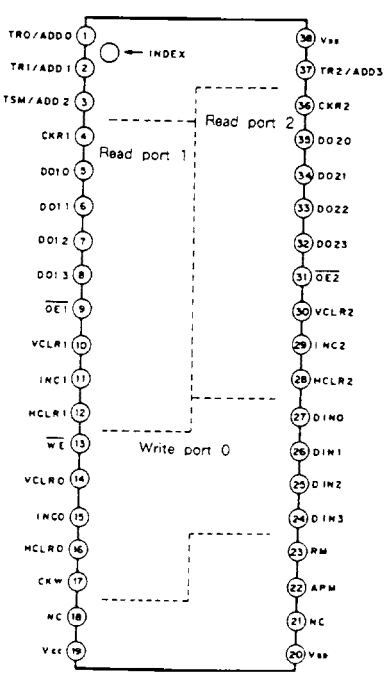
E91938A2Z - ST

Block Diagram (SOP)

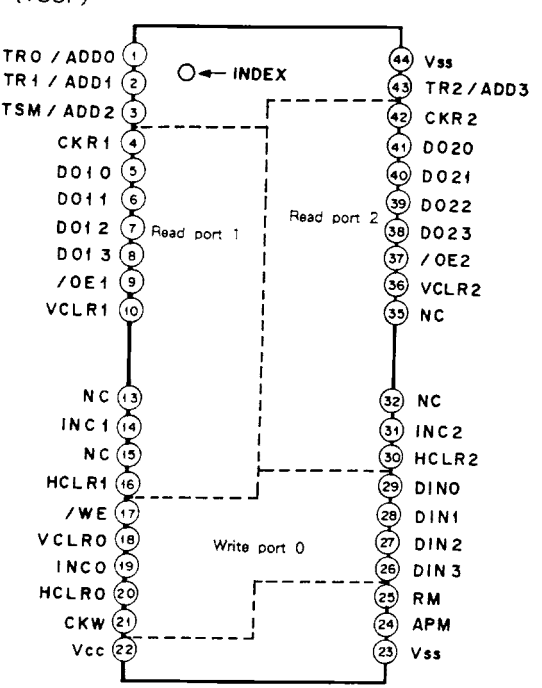


Pin Configuration (Top View)

(SOP)



(TSOP)



Pin Description

Pin No. SOP	Pin No. TSOP	Symbol	I/O	Description
1	1	TR0/ADD0	I/O	Write port 0 transfer synchronous Signal/Address 0 input
2	2	TR1/ADD1	I/O	Read port 1 transfer synchronous Signal/Address 1 input
3	3	TSM/ADD2	I	Transfer synchronous Mode/Address 2 input
4	4	CKR1	I	Port 1 shift signal
5	5	DO10	O	Port 1 data output
6	6	DO11	O	Port 1 data output
7	7	DO12	O	Port 1 data output
8	8	DO13	O	Port 1 data output
9	9	$\overline{OE1}$	I	Port 1 output enable
10	10	VCLR1	I	Port 1 vertical clear
11	14	INC1	I	Port 1 line increment
12	16	HCLR1	I	Port 1 horizontal clear
13	17	$\overline{WE}$	I	Port 0 write enable
14	18	VCLR0	I	Port 0 vertical clear
15	19	INC0	I	Port 0 line increment
16	20	HCLR0	I	Port 0 horizontal clear
17	21	CKW	I	Port 0 shift signal
19	22	Vcc	—	Power supply (+5V)
20	23	Vss	—	Ground
22	24	APM	I	Address preset mode enable
23	25	RM	I	Recursive mode enable
24	26	DIN3	I	Port 0 data input
25	27	DIN2	I	Port 0 data input
26	28	DIN1	I	Port 0 data input
27	29	DIN0	I	Port 0 data input
28	30	HCLR2	I	Port 2 horizontal clear
29	31	INC2	I	Port 2 line increment
30	36	VCLR2	I	Port 2 vertical clear
31	37	$\overline{OE2}$	I	Port 2 output enable
32	38	DO23	O	Port 2 data output
33	39	DO22	O	Port 2 data output
34	40	DO21	O	Port 2 data output
35	41	DO20	O	Port 2 data output
36	42	CKR2	I	Port 2 shift signal
37	43	TR2/ADD3	I/O	Read port 2 transfer synchronous Signal/Address 3 input
38	44	Vss	—	Ground
—	—	NC	—	No connection

RM

According to the status of this pin, the CXK1206AM/ATM operates in any of the two modes: one is the recursive mode with this pin set at high level, and the other is the non-recursive mode with this pin set at low level.

- Recursive mode : This mode permits sequential access to 960 × 306 memory cells up to 0 to 293759. Initialization is conducted by VCLR0, 1 and 2 pin input. In the case of Write, the serial data input when VCLR0 high level is latched by CKW is treated as the data input of Line 0 /Block 0. In the case of Read, the serial data output is given as the data for Line 0/Block 0 with a lag of 64 clocks from the moment when VCLR1 and 2 high level is latched by CKR1 and 2, respectively.
- Non-recursive mode : The mode treats 960 × 306 memory cells with a unit of 1 line/16 blocks (60 bits per block) and controls lines with VCLR0, 1 and 2 and INC0, 1 and 2 and blocks with HCLR0, 1 and 2. It is different from the recursive mode in that, in the case of Write, the serial data input when HCLR0 is latched by CKW is handled as the data input for Line 0 /Block 0, and in the case of Read, the serial data output is output from Read ports 1 and 2 as the data for line 0/Block 0 with a lag of 64 clocks from the moment when HCLR1 and 2 are latched by CKR1 and 2.

APM

This pin is necessary for the mode for presetting the block address in one line of the Write port, and the address preset mode is valid only when RM is set to low level (non-recursive mode). If this pin is at high level when HCLR0 is latched by CKW, one of 16 blocks is selected by four bits ADD0 to 3. When the address preset mode is not in use, do not fail to select low level, in which case, TSM, TR0, TR1 and TR2 become available from among the multi-functional pins (TR0/ADD0, TR1/ADD1, TSM/ADD2 and TR2/ADD3).

TR0/ADD0, TR1/ADD1, TSM/ADD2, TR2/ADD3

These pins serve as block address presetting pins when APM is at high level (address preset mode), (non-recursive mode) and as pins for transfer synchronization mode when APM is at low level.

- In the address preset mode, one of 16 line blocks of the Write port with the use of ADD0 to 3 four-bit binary data can be selected, and the data input is accepted as in the non-recursive mode.
- When TSM is at low level (master), signals for synchronizing other CXK1206s with master CXK1206AM/ATM are output from TR0, TR1 and TR2, and when it is at high level (slave), in contrast, synchronizing signals are received. Also, use TSM pin with a fixed DC and does not change it during device operation.
- TR0 is the I/O pin for Write transfer synchronization of the Write port.
- TR1 is the I/O pin for Read transfer synchronization of the Read port 1.
- TR2 is the I/O pin for Read transfer synchronization of the Read port 2.
- When using in Transfer Synchronize mode, be sure to connect between master and slave for all of TR0, TR1 and TR2.

CKW

The rising edge of this pin issues a signal for latching data from input pins DIN0 to 3 into the shift register and input of internal address pointer control pins (VCLR0, HCLR0 and INC0). Since this signal serves also as the basic signal for start control of the internal clock synchronizing logical circuit and the dynamic RAM, it is necessary to cause clock operation irrespective of the presence of Write operation.

VCLR0

The pin plays different roles between high level (recursive mode) and low level (non-recursive mode) of pin RM.

The number of counts of VCLR0 is counted only for latch of high level after recognition of low level of the latched state by CKW. Continuation of high level is counted as one.

- In recursive mode : When CKW latches VCLR0's high level, the then Serial write data input is taken in as the data of * (0, 0). From among the data entered so far data of less than a block as partitioned by block (60 bits) are rejected.
  * (0, 0) means Line 0/Block 0 ; (v, h) means the number of lines and that of blocks upon input of control signal.
- In non-recursive mode : When CKW latches high level of VCLR0, shift advances until the block (60 bits) during Serial write is filled up, and the line is cleared. More specifically, if VCLR0 is entered during Serial write, it is transferred to the (v, h) memory cell after the completion of input of 60 bits, and the data to be serially written are transferred to (0, h + 1) memory cell.

HCLR0

When high level of this pin is latched by CKW, the then input data is first taken in as (v, 0) data. Input data already entered and not sufficient to fill up a block (60 bits) are rejected. When pin RM is at high level (recursive mode), a signal to this pin has no meaning.

The number of counts of HCLR0 is counted only for the latch of high level after recognition of low level of the latched state by CKW for each time. Continuation of high level is counted as one.

INC0

When this pin is latched by CKW, the lines in the corresponding number are incremented. The incremented lines become valid in two cases : when HCLR0's high level is latched, or when VCLR0's high level is latched, and the shift register then advances to the end of that block. When pin RM is at high level (recursive mode), a signal to this pin has no meaning.

The number of counts of INC0 is counted only for the latch of high level after recognition of low level of the state latched by CKW. Continuation of high level is counted as one.

- When combining with VCLR0, the number of counts n of INC0 during the time from the state of VCLR0 latched by CKW until the shift register is filled up with 60 bits during Write causes Write of data input for the next 60 bits to be written into (n, h + 1) memory cell.
  INC0 is invalid, however, when INC0 is used simultaneously with VCLR0.
- When combining with HCLR0, the number of counts n of INC0 during the period from HCLR0's state latched by CKW last time up to the current latch causes 60 bits of data input to be entered next to be written into (v + n, 0) memory.
  INC0 is valid when INC0 is used simultaneously with HCLR0.

CKR1 and 2

The rising edge of these pins moves the shift register of the Read port and issues a signal for output of data to output pins DO10 to 13 and DO20 to 23 and a signal for latching the input of each internal address pointer control pin (VCLR1 and 2, HCLR1 and 2, and INC1 and 2).

VCLR1 and 2

The role of these pins is different between high level (recursive mode) and low level (non-recursive mode) of pin RM.

The number of counts of VCLR1 and 2 is counted only for latch of high level after recognition of low level of the state latched by CKR1 and 2, respectively. Continuation of high level is counted as one.

- In recursive mode : When CKR1 or 2 latches high level of VCLR1 or 2, (0, 0) data is output with a lag of 64 clocks from that moment. In the meantime, the shift register (60 bits) in shift is output to the full to retain the last output.
- In non-recursive mode : When CKR1 or 2 latches high level of VCLR1 or 2, it outputs the block currently in Serial read and 60 bits of the next block, and then output of consecutive blocks of the cleared line is started. More particularly, when VCLR1 or 2 is latched and the line of the internal address counter is hence cleared, the data (v, h + 1) for the next serial output have already been transferred from the memory cell to the data register, and while outputting the data, it transfers (0, h + 2) data and then outputs (0, h + 2) data.

HCLR1 and 2

When high level of this pin is latched by CKR1 or 2, (v, 0) data are output with a lag of 64 clocks from that moment. In the meantime, it outputs the shift register data in shift to the full to retain the final output. When pin RM is at high level (recursive mode), a signal to any of these pins has no meaning.

The number of counts of HCLR1 and 2 is counted only for high level latch after recognition of the state latched by CKR1 or 2. Continuation of high level is counted as one.

INC1 and 2

When high level of these pins is latched by CKR1 or 2, lines corresponding to the number of times of latching are incremented. The incremented lines become valid in two cases : when HCLR1 or 2 high level is latched, or when high level of VCLR1 or 2 is latched, and then the line address is latched at clock 57 of that block. When pin RM is at high level (recursive mode), a signal to any of these pins has no meaning.

The number of counts n of INC1 and 2 is counted only for the latch of high level after recognition of low level of the state latched by CKR1 or 2. Continuation of high level is counted as one.

- When combining with VCLR1 or 2, the number of counts n of INC1 and 2 prior to clock 56 of the block of VCLR1 or 2 latched by CKR1 or 2 causes (n, h + 2) memory cell data to become data to be output from the shift register for the 2'nd next time.

  When INC1 and 2 are used simultaneously with VCLR1 and 2, respectively, however, INC1 and 2 are invalid.
- When combining with HCLR1 and 2, the number of counts n of INC1 and 2 during the time from the last latching of HCLR1 and 2 by CKR1 and 2, respectively, up to the current latching causes (v + n, 0) memory cell data to become shift data to be output with a lag of 64 clocks from HCLR1 and 2.

  When INC1 and 2 are used simultaneously with HCLR1 and 2, respectively, INC1 and 2 are valid.

Data Input (DIN0 to 3)

Information to a data input pin is accepted at rising edge of CKW in the state of "L" of $\overline{WE}$, and entered into the shift register. When $\overline{WE}$ is at "H", input data are not accepted, without operation of the Write shift register (Write clock gate function).

Input into the shift register is accomplished immediately, whereas the information is loaded to the data register after completion of input of one block (60 bits) and transferred to the memory cell before the shift register is filled up with new data. Therefore, Serial write data input in the case of Serial write is transferred to the memory cell with a lag of one block.

Input control ($\overline{WE}$)

Input control to DIN0 to 3 is conducted with $\overline{WE}$. When $\overline{WE}$ is at "L", synchronization with CKW enables input, and when $\overline{WE}$ is at "H", input is not accepted and shift operation of the Write shift register is discontinued. This is used, for example, when thinning out data input (gate function of Write-side input clock (CKW) by $\overline{WE}$).

Data output (DO10 to 13, DO20 to 23)

The three-state TTL level is adopted for the output buffer. When $\overline{OE1}$ and $\overline{2}$ are at "L", output is immediately enabled and data in synchronization with CKR1 and 2 are output. When $\overline{OE1}$ and $\overline{2}$ are at "H", output is in high impedance state, but the shift register operates in synchronization with CKR1 and 2 and conducts transfer between memory cell and data register and load between data register and shift register.

Output from the shift register is made from time to time. Data in output are those transferred from the memory cell to the shift register by one block prior to the block in current output.

Output control ($\overline{OE1}$ and $\overline{2}$)

$\overline{OE1}$ conducts output control of only output pins DO10 to 13, and $\overline{OE2}$ conducts output control of only output pins DO20 to 23, without arresting shift operation of the shift register of Read port. Output control of DO10 to 13 and DO20 to 23 brings about output enable without being synchronized with CKR1 and 2 when $\overline{OE1}$ and $\overline{OE2}$ are at "L", and brings the output to high impedance state without being synchronized with CKR1 and 2 at "H".

Electrical Characteristics

DC characteristics

(Vcc = 5V ± 10%, Vss = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current*1	I_{CC1}	tscw0 = 70ns tscr1, 2 = 70ns	—	—	45	mA
(Normal operation)	I_{CC2}	tscw0 = 70ns tscr1, 2 = 35ns	—	—	60	mA
(Normal operation)	I_{CC3}	tscw0 = 50ns tscr1, 2 = 50ns	—	—	60	mA
(Normal operation)	I_{CC4}	tscw0 = 50ns tscr1, 2 = 30ns	—	—	75	mA
Supply current (upon refreshing) *1, 2	I_{CC5}	tscw0 = 420ns tscr = 70ns	—	—	20	mA

Item	Symbol	Min.	Max.	Unit
Input leak current (total input) (0V ≦ Vin ≦ 5.5V; 0V, Vcc = 5.5V except for testing pins)	I_I (L)	−10	10	μA
Output leak current (output high impedance state; 0V ≦ Vout ≦ 5.5V)	Io (L)	−10	10	μA
Output voltage "H" level (I_{OH} = −2 mA)	V_{OH}	2.4	—	V
Output voltage "L" level (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V

Note) *1. Output pin is open.
Supply current is dependent upon cycle time and output load.
*2. WE = "H", only one Read port operates.

AC characteristics

(Vcc = 5V ± 10%, Vss = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Refreshing interval	t_{REF}		—	—	21	ms
CKR cycle time	t_{SCR}		30	—	70	ns
CKR, CKW pulse duration	t_{CK}		8	—	—	ns
CKR, CKW precharge time	t_{SP}		8	—	—	ns
Access time from CKR	t_{SAC}		—	—	25	ns
Data output hold time from CKR	t_{SOH}		5	—	—	ns
Access time from $\overline{OE}$	t_{OEA}		—	—	20	ns
Data output hold time from $\overline{OE}$	t_{OEH}		5	—	—	ns

Note) Input dummy cycle after a pause of over 200 μs from the time power supply is turned on. Input dummy cycle to each port at least one. In recursive mode, input VCLR, and in non recursive mode, input VCLR and HCLR.

Item	Symbol	Min.	Typ.	Max.	Unit
Data output turnoff delay time from $\overline{OE}$	t_{OEZ}	—	—	20	ns
VCLR HCLR — CKR active setup time INC CKW	t_{CKS}	5	—	—	ns
VCLR HCLR — CKR active hold time INC CKW	t_{CKH}	7	—	—	ns
VCLR HCLR — CKR inactive setup time INC CKW	t_{CK1}	5	—	—	ns
VCLR HCLR — CKR inactive hold time INC	t_{CK2}	7	—	—	ns
CKW cycle time	t_{SCW}	50	—	2tscr	ns
DIN, CKW setup time	t_{DS}	5	—	—	ns
DIN, CKW hold time	t_{DH}	7	—	—	ns
$\overline{WE}$, CKW active setup time	t_{WES}	5	—	—	ns
$\overline{WE}$, CKW active hold time	t_{WEH}	7	—	—	ns
$\overline{WE}$, CKW inactive setup time	t_{WE1}	5	—	—	ns
$\overline{WE}$, CKW inactive hold time	t_{WE2}	7	—	—	ns
ADD, CKW setup time	t_{AS}	10	—	—	ns
ADD, CKW hold time	t_{AH}	8	—	—	ns
Input pulse rising and falling period	t_T	3	—	40	ns

Clock correlation

CXK1206AM/ATM uses a DRAM in the memory block. Accordingly and in order to hold data, either of the following clock relations has to be satisfied. In NRM (Non Recursive Mode) and using HCLR with INC, keep access time to all memory zones utilized, within 21msec.

T_{SCW}	T_{SCR1}	T_{SCR2}	
50 to 2 × T_{SCR1}	30 to T_{MAX}	T_{SCR1} to stop	ns
50 to 2 × T_{SCR2}	T_{SCR2} to stop	30 to T_{MAX}	ns

To access 1 picture (960 dots × 306 lines) in less than 21msec, maximum cycle time, TMAX when CKR1 (or CKR2) is applied continuously is obtained as follows.

$$T_{MAX} = \frac{21\text{msec}}{960 \text{ dots} \times 306 \text{ lines}} \fallingdotseq 70\text{nsec}$$

Standby mode to hold image data

To reduce power consumption while image data is held, keep WE = H fixed and use only 1 port of the read side. In this case write in is not performed. Clock correlation turns out as either of the following cases. In NRM (Non Recursive Mode) and using HCLR with INC, keep access time to all memory zones utilized, within 21msec.

T_{SCW}	T_{SCR1}	T_{SCR2}	
50 to 6 × T_{SCR1}	30 to T_{MAX}	Stop	ns
50 to 6 × T_{SCR2}	Stop	30 to T_{MAX}	ns

To access 1 picture (960 dots × 306 lines) in less than 21msec, maximum cycle time, TMAX when CKR1 (or CKR2) is applied continuously is obtained as follows.

$$T_{MAX} = \frac{21\text{msec}}{960 \text{ dots} \times 306 \text{ lines}} \fallingdotseq 70\text{nsec}$$

I/O capacity

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input	C_{IN}	TA = 0°C to +70°C	—	—	7	pF
Data output capacity (DO10 to DO23)	C_D	V_{CC} = +5V ± 10%	—	—	7	pF
I/O capacity (ADD0 to ADD3)	C_T		—	—	10	pF

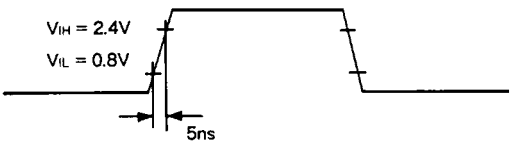
Transfer Synchronize AC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Transfer access time from CKW	*1	t_{TAC}	—	—	25	ns
Number of transfer output pulse						
TR0	*1	t_{TWOP}	5	5		*2
TR1, TR2	*1	t_{TROP}	4	4		
Transfer output • Turn off delay time from CKW	*1	t_{TZ}	—	—	25	ns
Transfer output interval • Number of pulse		t_{TOI}	1			*2
TR0 TR1—CKW active set up time TR2		t_{TS}	15	—	—	ns
TR0 TR1—CKW active hold time TR2		t_{TH}	7	—	—	ns
TR0 TR1—CKW inactive set up time TR2		t_{TSS1}	7	—	—	ns
TR0 TR1—CKW inactive hold time TR2		t_{TSS2}	7	—	—	ns
Number of transfer input pulse						
TR0		t_{TWIP}	5	5		*2
TR1, TR2		t_{TRIP}	4	4		
Transfer input interval • Number of pulse		t_{TII}	1			*2

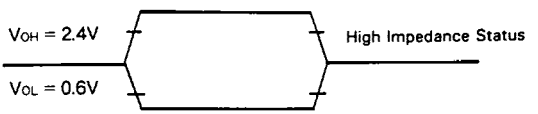
Note) *1. 40pF load
*2. Number of tscw.

AC Characteristic Test Condition

1) Input

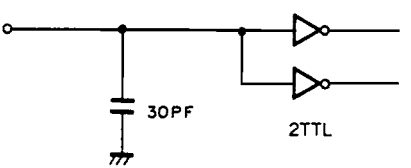


2) Output



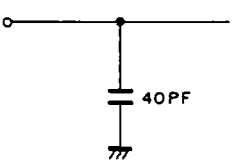
3) Data Output Load

DO10 to 13, 20 to 23



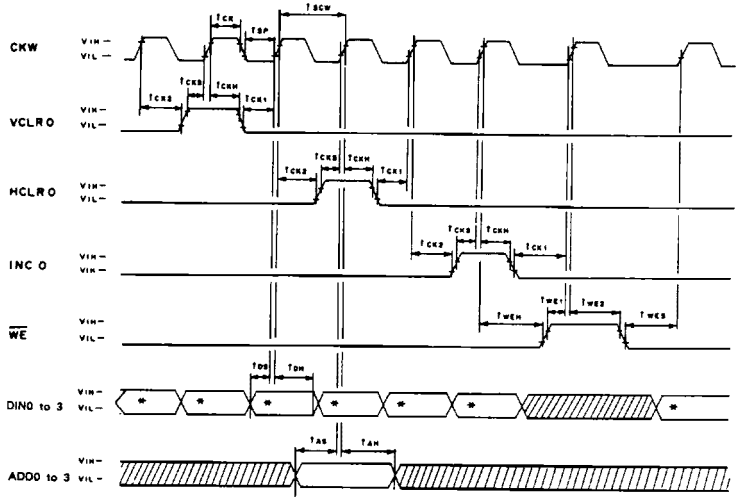
4) Transfer Output Load

TR0, 1, 2



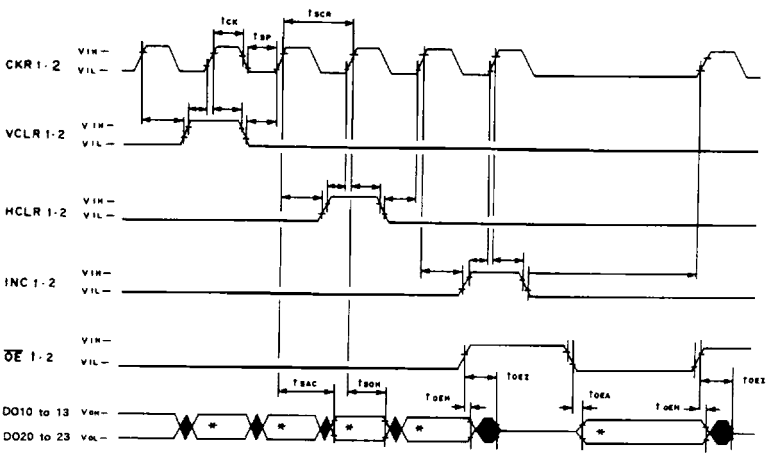
Timing Chart

Write port



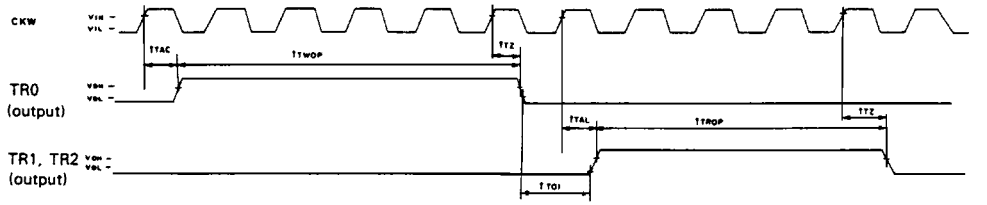
*: Input determination period; irrespective of "H" or "L" by certain control of VCLR0, etc.

Read port

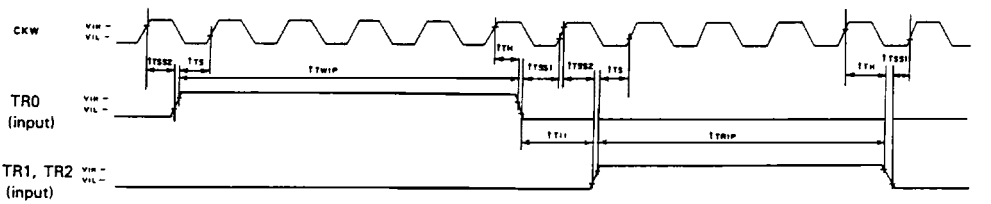


*: Output determination period ■: Invalid data

Transfer synchronizing master chip



Transfer synchronizing slave chip



Description of Operation

CXK1206AM/ATM has the following five operating modes. As to the details of timing, etc., refer to the separate description :

1. Recursive mode, transfer synchronous mode output:
   These modes handle the memory as a simple delay line. Control is accomplished via VCLR0, 1 and 2, $\overline{WE}$, $\overline{OE1}$ and $\overline{OE2}$. The synchronizing signal for use of multiple chips is output (forming master chips).

2. Recursive mode, transfer synchronous mode input:
   A synchronizing signal is entered in the mode as described in 1 above (becoming slave chip).

3. Non-recursive mode, transfer synchronous mode output:
   This is the mode for controlling the memory by block or line. Control is accomplished via VCLR0, 1 and 2, INC0, 1 and 2, HCLR0, 1 and 2, $\overline{WE}$, $\overline{OE1}$ and $\overline{OE2}$. The synchronizing signal for use of multiple chips is output (forming master chips).

4. Non-recursive mode, transfer synchronous mode input:
   A synchronizing signal is entered in the three modes as described above (becoming slave chips).

5. Non-recursive mode, address preset mode:
   This is the mode for controlling the memory by block or line, and permits setting any address by block when writing in the memory. Control is accomplished via VCLR0, 1 and 2, INC0, 1 and 2, HCLR0, 1 and 2, $\overline{WE}$, $\overline{OE1}$, $\overline{OE2}$, and ADD0, 1, 2 and 3. A synchronizing signal cannot be entered or output when using multiple chips in this mode.

Function Table

Function table 1 [List of Operating modes]

Operating mode	Control input			Address input	TS input/output
	RM	TSM	APM	ADD0 to 3	TR0 to 2
Recursive mode, Transfer synchronous mode output	H	L	L	—	Output determination
Recursive mode, Transfer synchronous mode input	H	H	L	—	Input determination
Non-recursive mode, Transfer synchronous mode output	L	L	L	—	Output determination
Non-recursive mode, Transfer synchronous mode input	L	H	L	—	Input determination
Non-recursive mode, Address preset mode	L	—	H	Input determination	—

—: This pin name is non-existent in this mode.

Address-block division correspondence table

Block No.	ADD3	ADD2	ADD1	ADD0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Note) The block number indicates the increasing direction in the order of Write or Read in a line.

Function table 2 [Write]

Mode		Operating cycle	RM	VRO	HRO	ICO	APM	A0 to 3	Internal address pointer
Recursive mode	1	Initial cycle	H	H	—	—	L	—	Goes back to 0.
	2	Normal cycle		L	—	—	L	—	After advancing in order from 0 to 293759, goes back to 0 to repeat the cycle to 293759.
Non-recursive mode	1	Initial cycle	L	H*1	H*1	L	L*5	—	v and h are both cleared. (v, h) → (0, 0)
	2	Normal cycle		L	L	L	L*5	—	Advances up to the end of v line. After that write operation is not performed.
	3	First block cycle		L	H	L	L*5	—	Only h is cleared. (v, h) → (v, 0)
	4	Line address cycle		L	H	nH*2	L*5	—	v advances to n line and h is cleared. (v, h) → (v + n, 0)
	5	VCLR0 special cycle No. 1		H	L	L	L*5	—	After advancing to the end of h block, v is cleared. (v, h) → (0, h + 1)
	5	VCLR0 special cycle No. 2		H	L	nH*3	L*5	—	After advancing to the end of h block, v is set to n line. (v, h) → (n, h + 1)
	5	VCLR0 special cycle No. 3		H*4	H*4	nH*4	L*5	—	v is set to n line and h is cleared. (v, h) → (n, 0)

VR0: VCLR0
HR0: HCLR0
IC0: INC0
A0 to 3: ADD0 to 3
(v, h), v: Number of the line for Write port upon input of control signal
h: Number of the block for Write port upon input of control signal
H: High level latched by CKW
nH: Number of times of high level latched by CKW is n.

Note) • This device is arranged in 306 lines, 16 blocks and 60 bits.
• For Write address counter reset, it is necessary to make at least one input of VCLR0 in recursive mode, or VCLR0 and HCLR0 in non-recursive mode.
• It is necessary to set low or high in DC manner for pins RM and APM input.

*1. It is necessary to enter VCLR0 and HCLR0 at the same time, or to enter HCLR0 prior to the first clock of the block next to the block containing VCLR0.
*2. nH: Number of times of "H" of INC0 prior to HCLR0 after the current HCLR0.
*3. nH: Number of times of "H" of INC0 prior to the first clock of the block next to the h block containing VCLR0.
*4. It is necessary to enter INC0 and HCLR0 prior to the first clock of the block next to that containing VCLR0.
*5. When pin APM is at low level, pin TSM becomes valid, and the Read ports and the Write port are in transfer synchronous mode. When pin TSM is at low level, transfer output is provided (master), and when it is at high level, transfer input is accepted (slave).

Function table 3 [Write]

Mode		Operating cycle	RM	VRO	HRO	ICO	APM	A0 to 3	Internal address pointer
Non-recursive, address preset mode	1	Initial cycle	L	H*1	H*1	L	H*5	Input determination	v is cleared and preset address ADD is set to h. (v, h) → (0, ADD)
	2	Normal cycle		L	L	L	H*5	——	Advances up to the end of v line. After that write operation is not performed.
	3	Address preset cycle		L	H	L	H*5	Input determination	Preset address ADD is set to h. (v, h) → (v, ADD)
	4	Line address, block address preset cycle		L	H	nH*2	H*5	Input determination	v advances to n line, and preset address ADD is set to h. (v, h) → (v + n, ADD)
	5	VCLR0 special cycle No. 1		H	L	L	H*5	——	After advancing to the end of h block, v is cleared. (v, h) → (0, h + 1)
	5	VCLR0 special cycle No. 2		H	L	nH*3	H*5	——	After advancing to the end of h block, v is set to n line. (v, h) → (n, h + 1)
	5	VCLR0 special cycle No. 3		H*4	H*4	nH*4	H*5	Input determination	n line is set to v and preset address ADD is set to h. (v, h) → (n, ADD)

VR0: VCLR0
HR0: HCLR0
IC0: INC0
A0 to 3: ADD0 to 3
(v, h), v: Number of the line for Write port upon input of control signal
h: Number of the block for Write port upon input of control signal
H: High level latched by CKW
nH: Number of times of high level latched by CKW is n.

Note) • This device is arranged in 306 lines, 16 blocks and 60 bits.
• For Write address counter reset, it is necessary to make at least one input of VCLR0 in recursive mode, VCLR0 and HCLR0 in non-recursive mode.
• It is necessary to set low or high in DC manner for pins RM and APM input.

*1. It is necessary to enter VCLR0 and HCLR0 at the same time, or to enter HCLR0 prior to the first clock of the block next to the block containing VCLR0.
*2. nH: Number of times of "H" of INC0 prior to HCLR0 after the current HCLR0.
*3. nH: Number of times of "H" of INC0 prior to the first clock of the block next to the h block containing VCLR0.
*4. It is necessary to enter INC0 and HCLR0 prior to the first clock of the block next to that containing VCLR0.
*5. In the Function table for address preset mode, the block address is latched with high level of HCLR0 latched by CKW.

Function table 4 [Read]

Mode		Operating cycle	RM	VR1	HR1	IC1	Internal address pointer
Recursive mode	1	Initial cycle	H	H	–	–	Advancing to end of (v, h) to (0, 0) with lag of 64 clocks from VCLR1
	2	Normal cycle		L	–	–	Circulating between 0 and 293759
Non-recursive mode	1	Initial cycle	L	H*1	H*1	L	Advancing to end of (v, h), clearing both v and h with lag of 64 clocks from HCLR1, to (0, 0)
	2	Normal cycle		L	L	L	To end of (v, h)
	3	First block cycle		L	H	L	Advancing to end of (v, h) to (v, 0) with lag of 64 clocks from HCLR1
	4	Line address cycle		L	H	nH*2	Advancing to end of (v, h) to (v+n, 0) with lag of 64 clocks from HCLR1
	5	VCLR1 special cycle No. 1		H	L	L	Advancing to end of (v, h+1), clearing v, to (0, h+2)
	5	VCLR1 special cycle No. 2		H	L	nH*3	Advancing to end of (v, h+1), setting v, to (n, h+2)
	5	VCLR1 special cycle No. 3		H*4	H*4	nH*4	Advancing to end of (v, h), setting v and clearing h with lag of 64 clocks from HCLR1, to (n, 0)

VR1: VCLR1
HR1: HCLR1
IC1: INC1
(v, h) v: Number of the line for Read port upon input of control signal
h: Number of the block for Read port upon input of control signal
H: High level latched by CKR1
nH: Number of times of high level latched by CKR1 is n.

Note)
- This device is configured with 306 lines, 16 blocks and 60 bits.
- In Read, address preset cannot be done irrespective of pin APM control, but when pin APM is at low level, the mode becomes transfer synchronous mode.
- For Read address counter reset, it is necessary to make at least one input of VCLR1 and HCLR1 in non-recursive mode.
- It is necessary to set low or high in DC manner for pins RM and APM input.

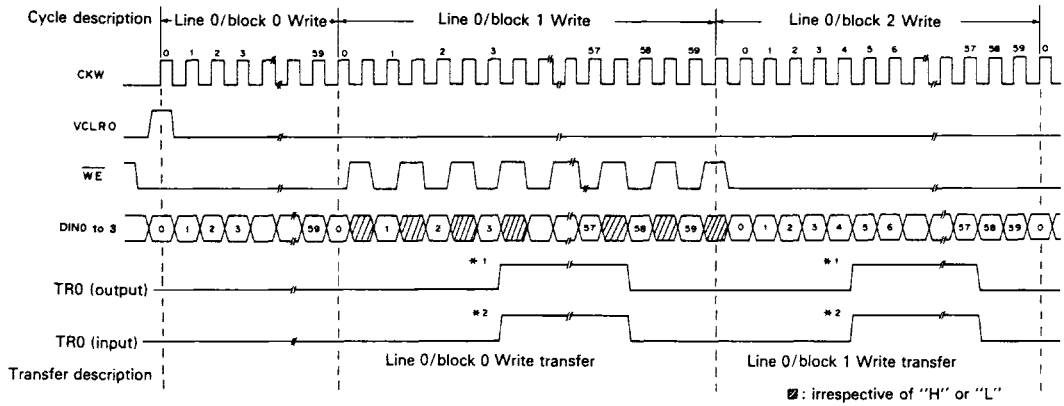
*1. It is necessary to enter VCLR1 and HCLR1 simultaneously, or to enter HCLR1 prior to clock 55 of the block containing VCLR1. To enter VCLR1 before the lapse of 64 clocks from HCLR1 is unabled.
*2. nH: Number of times of "H" of INC1 prior to HCLR1 after the current HCLR1.
*3. nH: Number of times of "H" of INC1 prior to the clock 55 of the h block after the current VCLR 1.
*4. It is necessary to enter INC1 and HCLR1 prior to the clock 55 of the h block containing HCLR1.

Function table 5 [Read 2]

The same particulars as those in Function table 4 apply also for VCLR2, HCLR2 and INC2.

Recursive mode, Write

1. Initial cycle 2. Normal cycle



Note) • After Write of up to Line 0/block 15, the next 60 bits are automatically written in block 0 of the next line.

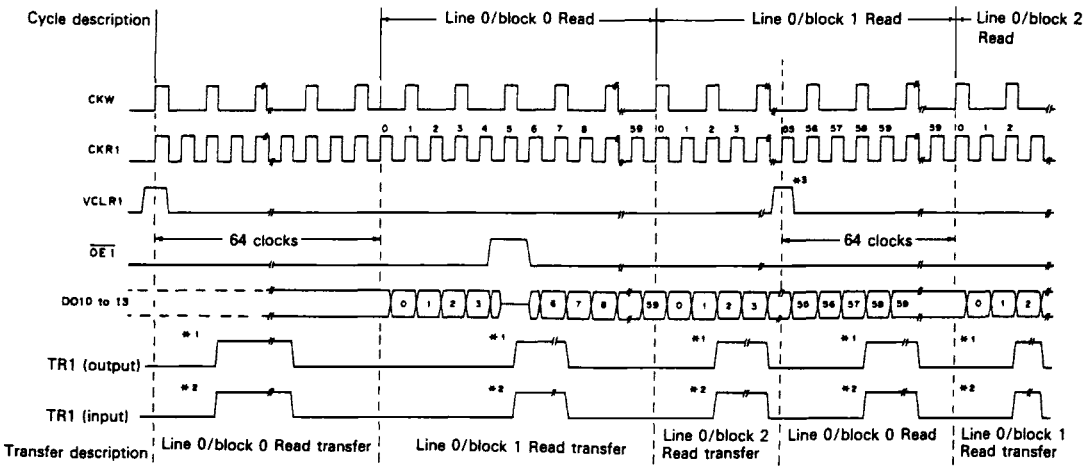
• After Write of up to Line 305/block 15, the next 60 bits are automatically written in line 0/block 0.

*1. When pin TSM = "L", output is made through automatic synchronization with CKW from the interior of device.

*2. Transfer input should be completed within a block Write. In the case of synchronous transfer between two chips, processing is made automatically between devices.

Recursive mode, Read

1. Initial cycle 2. Normal cycle



Note)

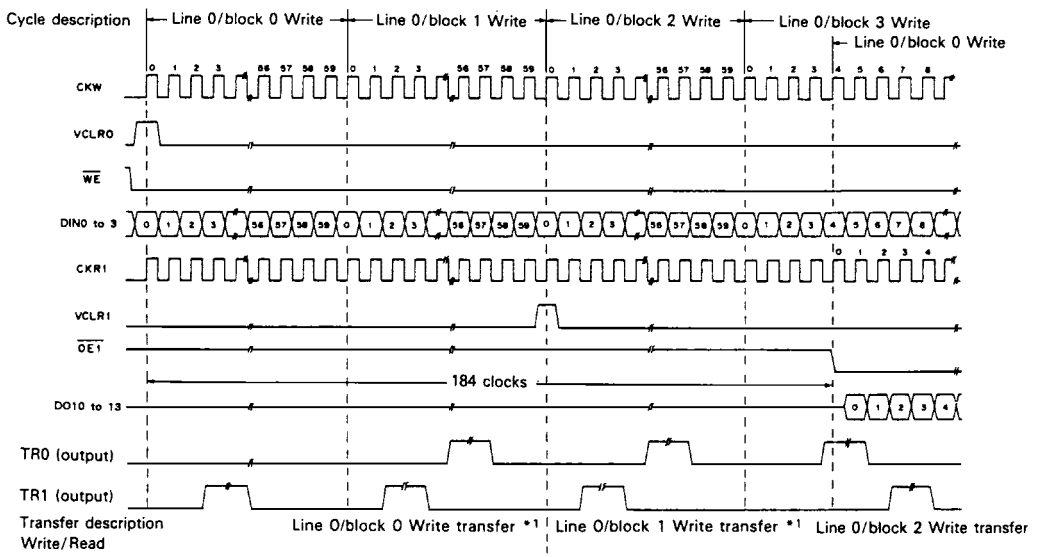
- After Read of up to Line 0/block 15, the next 60 bits are automatically read from block 0 of the next line.
- After Read of up to Line 305/block 15, the next 60 bits are automatically read from line 0/block 0.

*1. When pin TSM = "L", output is made through automatic synchronization with CKW from the interior of device.

*2. Transfer input should be completed within a block Read. In the case of synchronous transfer between two chips, processing is made automatically between devices.

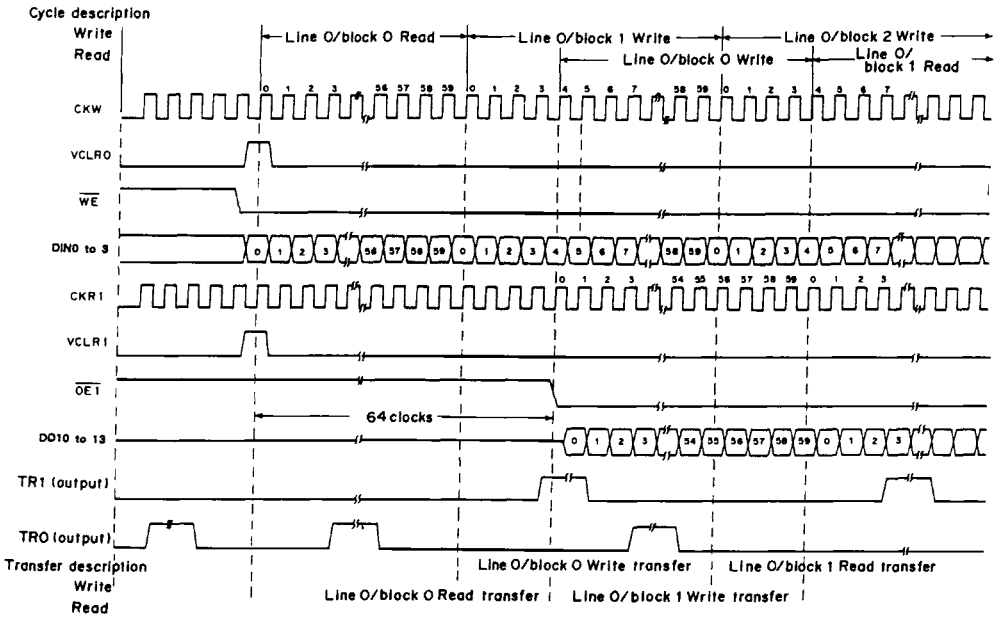
*3. If VCLR comes before 55th clock of the block currently Read, the final data of the block is retained. If VCLR comes after 56th clock of the block currently Read, data of the next block are read, following the current block. and the data of block 0 are output with a lag of 64 clocks from VCLR.

Recursive mode (in non-recursive mode, VCLR in the figure below corresponds to HCLR)
New data access mode



Note) *1. In order to access new data, block Write transfer is conducted after Write of 60 bits, and readout is made after Read transfer of that block. A lag of more than 184 clocks is necessary for Read clock from Write clock.

Recursive mode (in non-recursive mode, VCLR in the figure below corresponds to HCLR)
Old data access mode

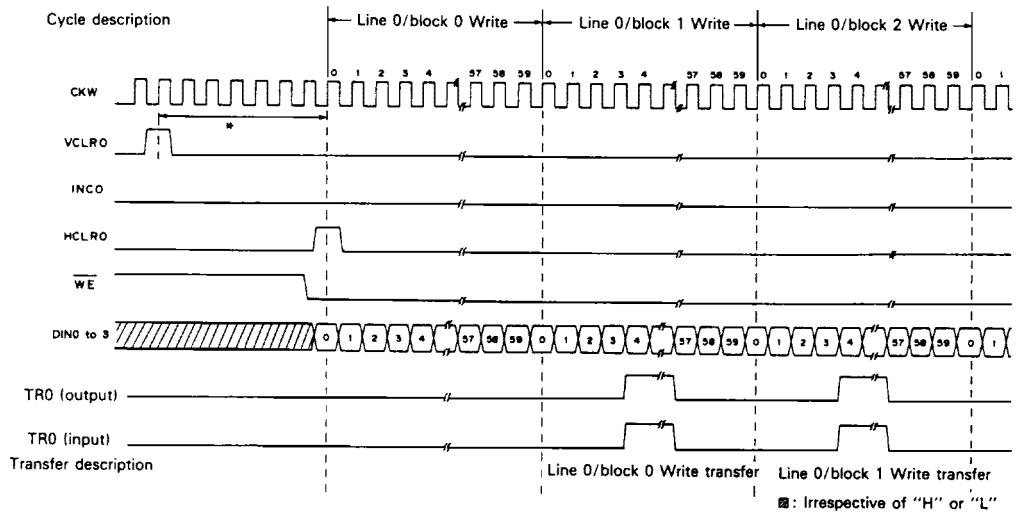


Note) • When the lag of Read clock from Write clock is more than 65 clocks and less than 183 clocks, Write of new data is guaranteed, although it is uncertain whether new data access or old data access.

* In order to access old data, Read transfer of that block should be accomplished before Write transfer of new data. A lag of less than 64 clocks is necessary for Read clock from Write clock.

Non-recursive mode, Write

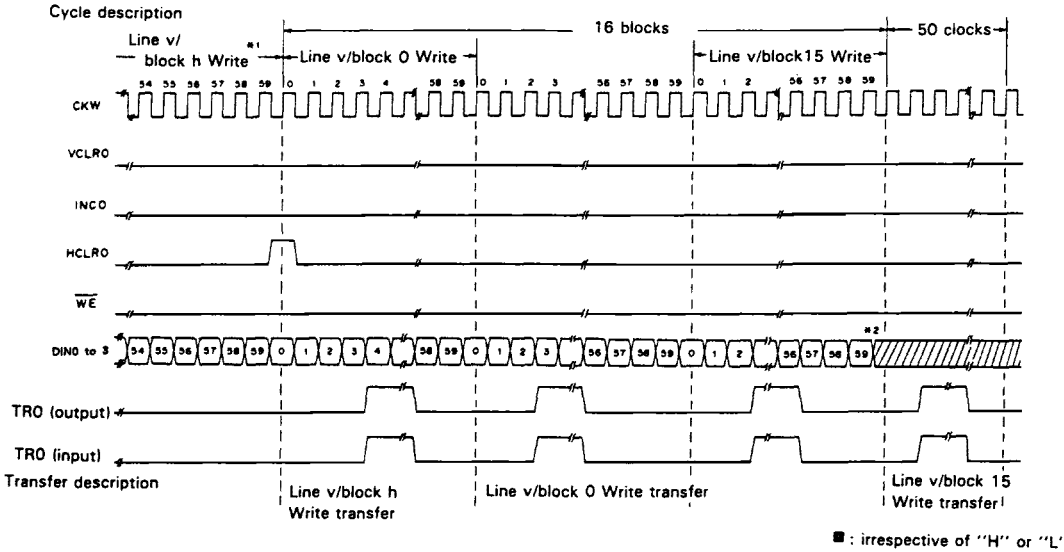
1. Initial cycle (the cycle for Writing from line 0/block 0)
2. Normal cycle



***Note)** In the case of initial cycle, it is necessary to enter VCLR0 and HCLR0 simultaneously, or to enter HCLR0 before the first clock of the block next to that containing VCLR0.

Non-recursive mode, Write

3. First block cycle (the cycle for Writing data from the start of block)

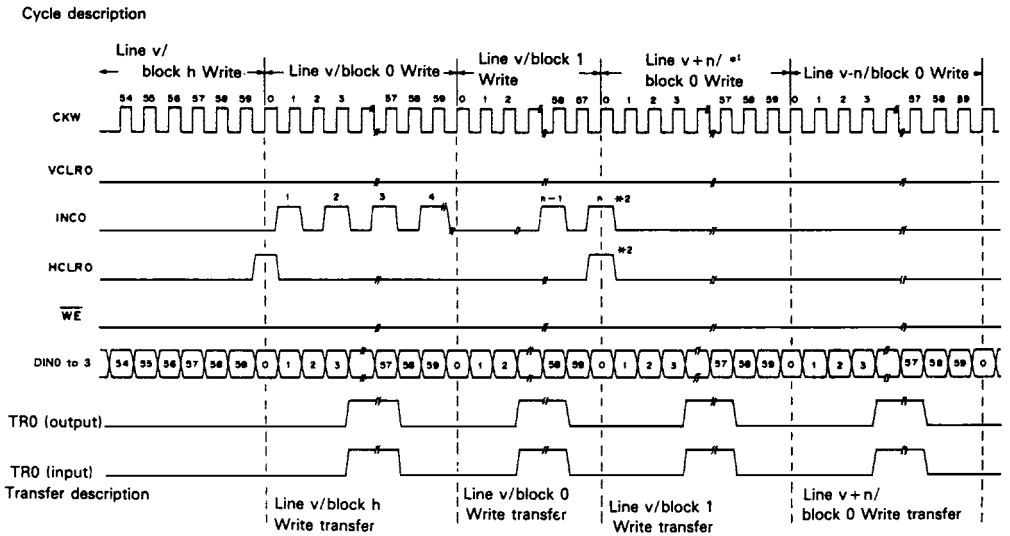


Note) *1. After Write of one block (60 bits), Write transfer is conducted in the next block.

*2. In non-recursive mode, after Write up to the final block of a line, no further Write is performed. Write transfer of the final block is accomplished during 60 clocks after the completion of final block Write.

Non-recursive mode, Write

4. Line address cycle (for address control in line direction)

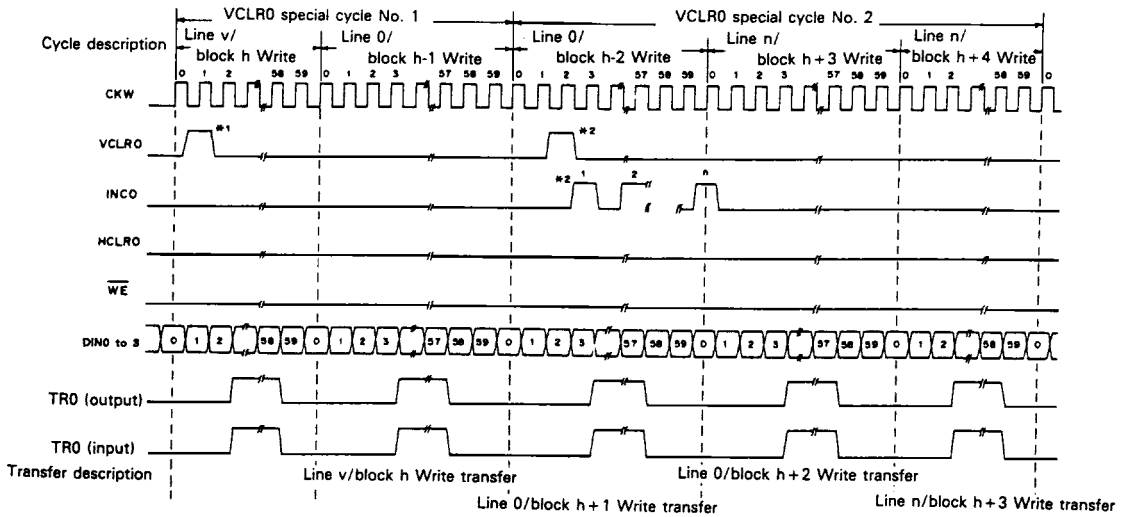


Note) *1. n is the number of times of INC0.

*2. Latch of this HCLR0 covers the range from the last HCLR0 up to INC0 entered at the same time as this HCLR0. Line address recursively circulates from the current address, depending upon the number of times of INC0.

Non-recursive mode, Write

5. VCLR0 special cycle No. 1 and No. 2



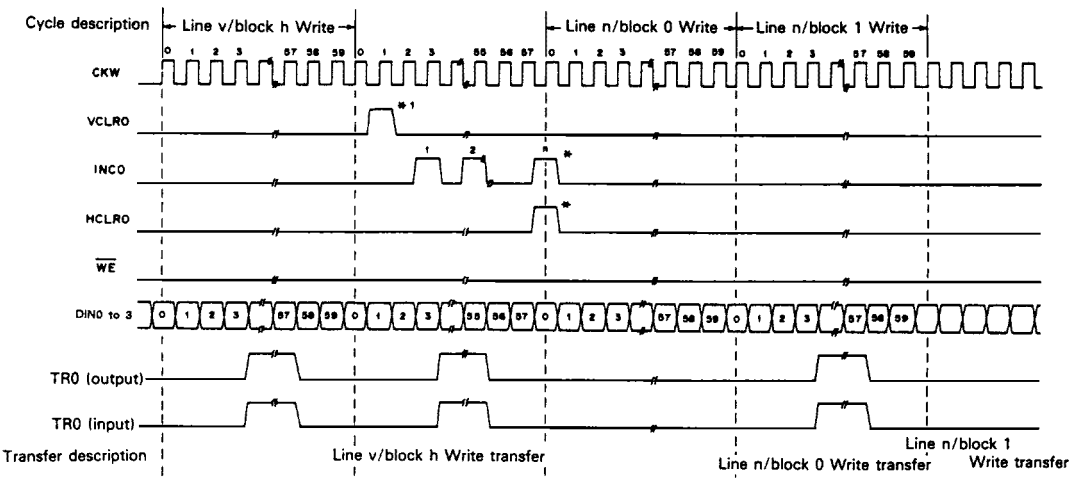
Note) *1. VCLR0 having entered after the 1st clock in the written block resets the line address, and is latched at the end of the block.

*2. When VCLR0 enters after the 1st clock in the written block, followed by INC0, the line address is reset, and line address in the number equal to the number of times of INC0 having entered block 1 Write are incremented, latching the line address at the beginning of the next block.

When VCLR0 and INC0 are simultaneously entered, only address reset becomes valid.

Non-recursive mode, Write

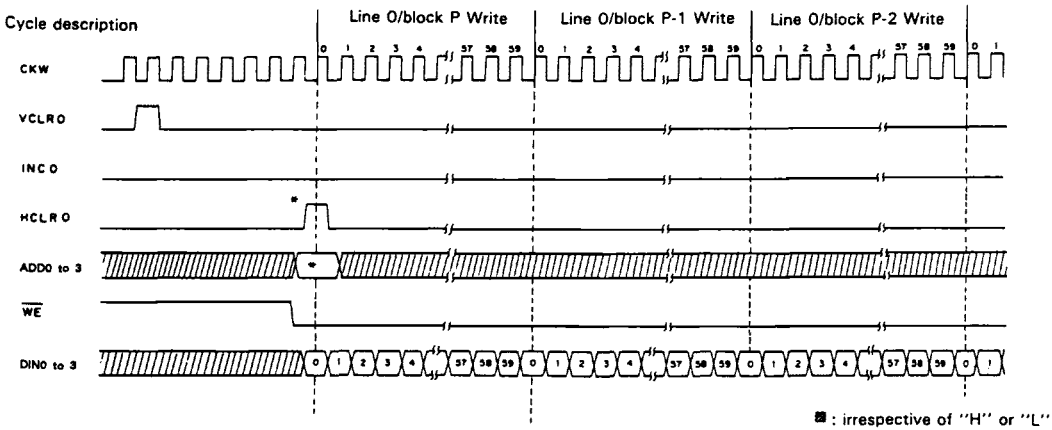
6. VCLR0 special cycle No. 3



***Note)** When VCLR0 enters after the 1st clock in the written block, followed by INC0 n times, and then by HCLR0, the line address is reset, and incremented in the number equal to the number of times of INC0. Latch of the line address and reset of the block address are carried out.

Non-recursive address preset mode, Write

1. Initial cycle 2. Normal cycle



***Note)** The block address is latched by HCLR0 in the case of address preset mode.

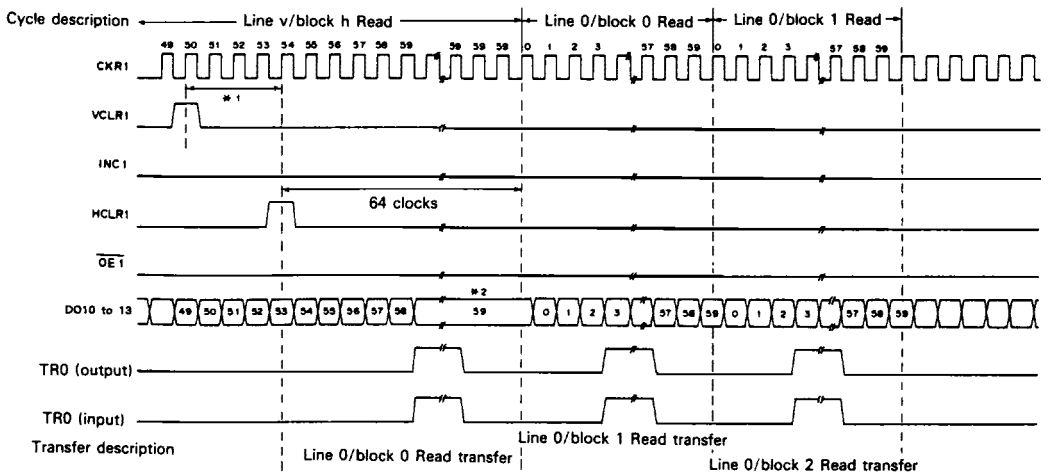
Non-recursive address preset mode, Write

3. Address preset cycle
4. Line address and block address preset cycle
5. VCLR0 special cycles Nos. 1, 2 and 3

For these cycles, refer to non-recursive mode considering the difference from non-recursive mode lying in that the block address is latched by HCLR0.

Non-recursive mode, Read

1. Initial cycle (the cycle Reading data from line 0/block 0)
2. Normal cycle

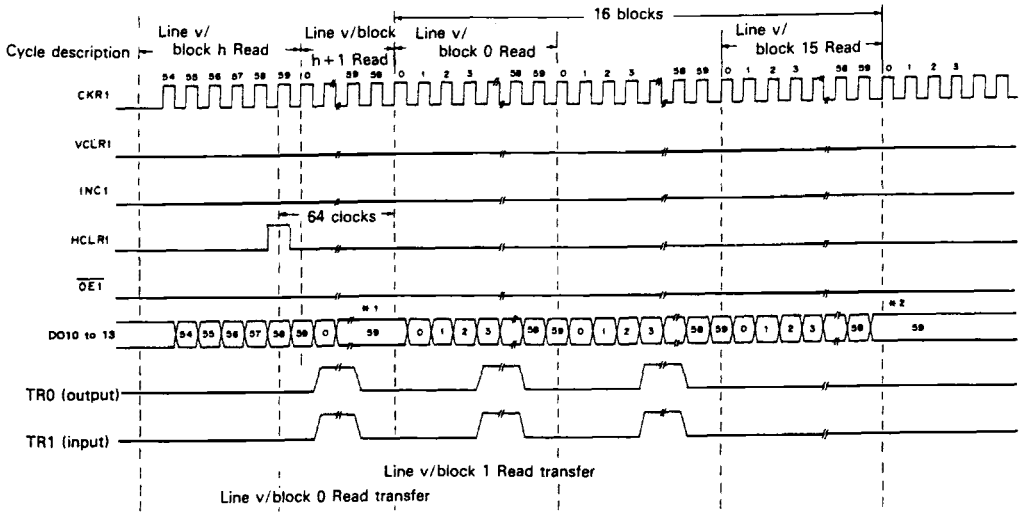


Note) *1. When VCLR1 and HCLR1 are simultaneously entered, or HCLR1 is entered before clock 55 of the block containing VCLR1, the data of line 0/block 0 are output with a lag of 64 clocks from HCLR1.

*2. If HCLR enters before clock 55 of the block currently Read, the final data of the block is retained. If HCLR enters after clock 56 of the block currently Read, the next block data are read, following the current block, and the data of block 0 are output with a lag of 64 clocks from HCLR.

Non-recursive mode, Read

3. First block cycle

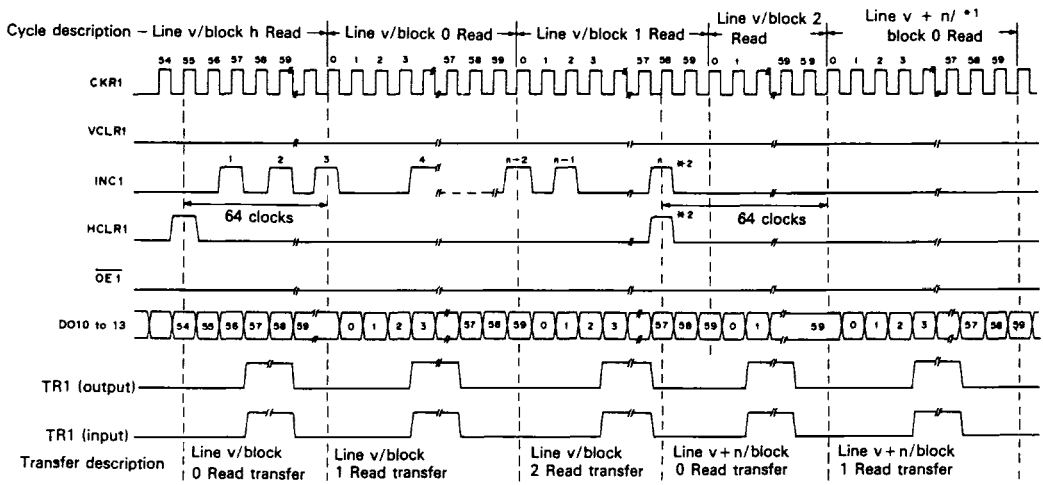


Note) *1. If HCLR enters before clock 55 of the block currently Read, the final data of the block is retained. If HCLR enters after clock 56 of the block currently Read, the next block data are read, following the current block, and the data of block 0 are output with a lag of 64 clocks from HCLR.

*2. In non-recursive mode, after Reading up to the final block of the line, the final data output is retained.

Non-recursive mode, Read

4. Line address cycle

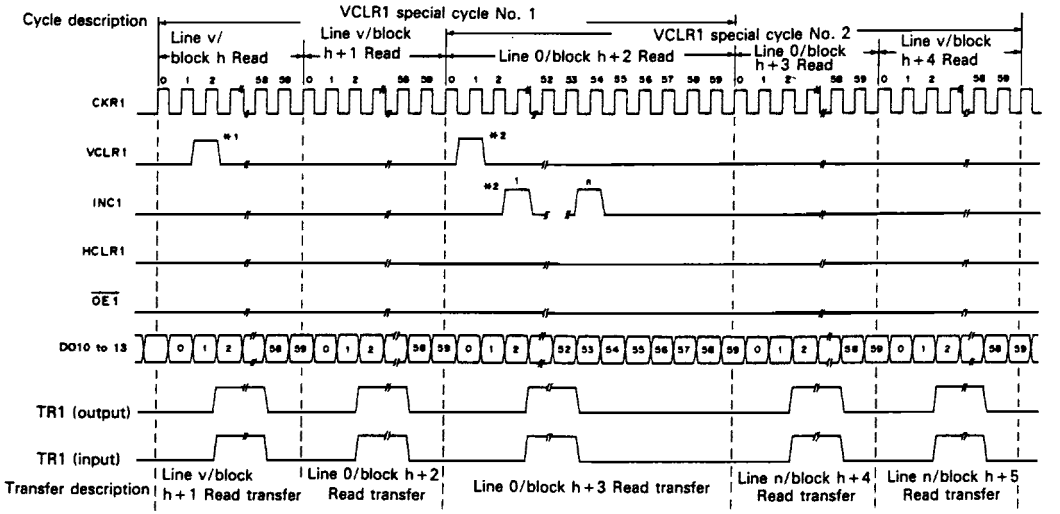


Note) *1. n is the number of times of INC1.

*2. Latch by this HCLR1 covers the range from the clock next to the last HCLR1 up to INC1 having entered simultaneously with this HCLR1. The line address recursively circulates from the current address, depending upon the number of times of INC1.

Non-recursive mode, Read

5. VCLR1 special cycle Nos. 1 and 2

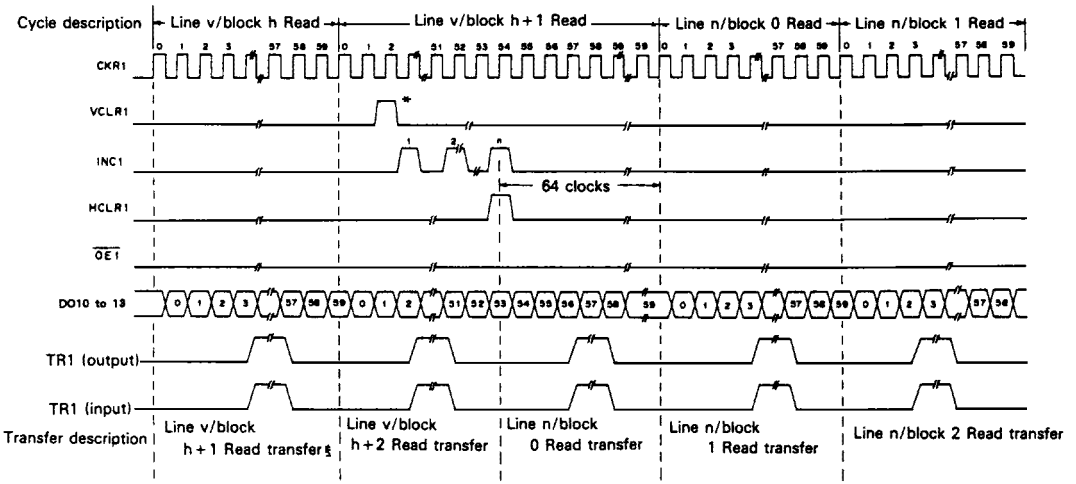


Note) *1. VCLR1 having entered before clock 56 in one block which has been read resets the line address and is latched at clock 57 of the block. In the next block, Read transfer of line 0/block h + 2 is carried out.

*2 When VCLR1 enters before clock 56 in one block which has been read, followed by INC1, the line address is reset, and the line address is incremented in the number equal to the number of times of INC1 having entered before clock 56 in the block which has been read. The line address is latched at clock 57 of the block. When VCLR1 and INC1 enter simultaneously, the address reset becomes valid.

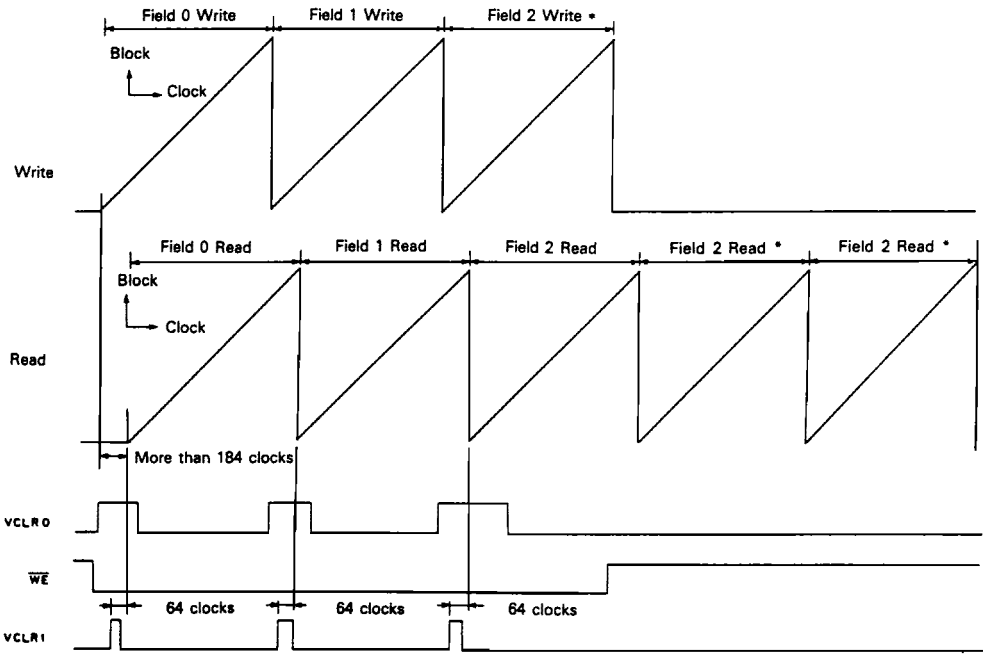
Non-recursive mode, Read

6. VCLR1 special cycle No. 3



***Note)** When VCLR1 enters in one block, followed by INC1 n times, and then followed by HCLR1 before clock 56 of the block, the line address is incremented in the number equal to the number of times of INC1 after reset, and line address latch and block address reset are carried out at the next clock.

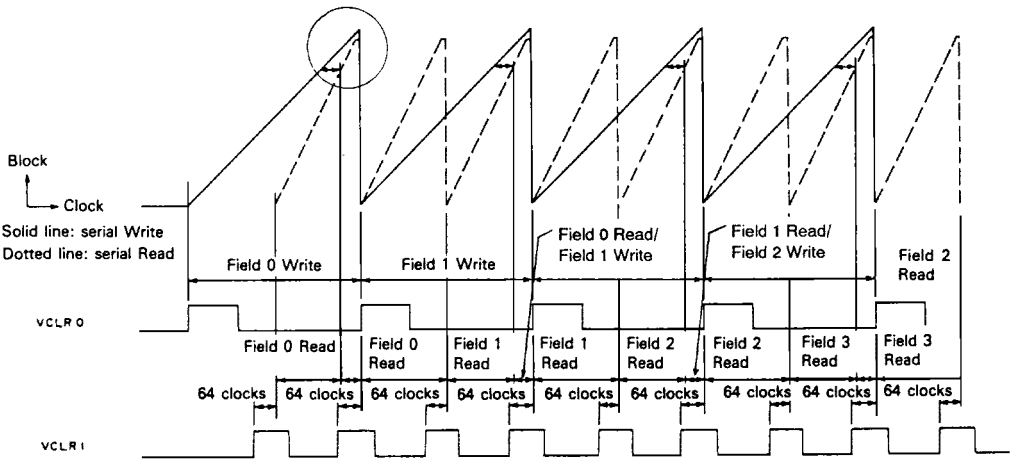
Example of Application 1 Delay line, field memory in case of recursive mode



Continuous input of CKW0, CKR1, $\overline{OE1}$ = "L"

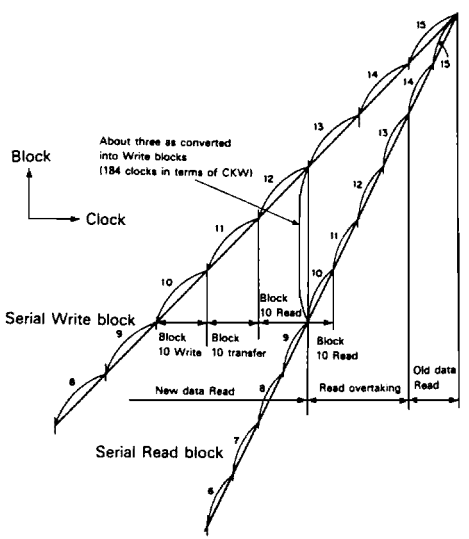
Note) • If the cycle time is equal between CKW and CKR1, this is possible also in the case of asynchronization.
• If the cycle time differs between CKW and CKR1, Read overtaking may occur. Refer to Example of Application 2.
• In non-recursive mode, it is necessary to advance the line for each line through combination of INC and HCLR input.
* When using 306 lines/16 blocks/60 bits, continuous Read is possible by only entering CKR1 and CKW without entering VCLR1.

Example of Application 2 Field double scan conversion in case of recursive mode



Note) Connectinuous input of CKW and CKR1. $\overline{WE}$ = "L", $\overline{OE1}$ = "L".

Description of circled drawing



- Read overtaking
  In order to Read data of written block in the case of field double scan conversion, the phase lag of Read as compared with write must be about three as converted into Write blocks (184 clocks in terms of CKW).
- When using two chips in 8-bit digitalized signal configuration, independent operation of the two chips may cause Read overtaking between the two chips. In order to synchronize Read overtaking between the two chips, use the transfer synchronous mode using one as the master chip, and the other as the slave chip.

Example of Application 3

Write of 1/2-compressed data in memory, non-recursive mode, address preset mode:

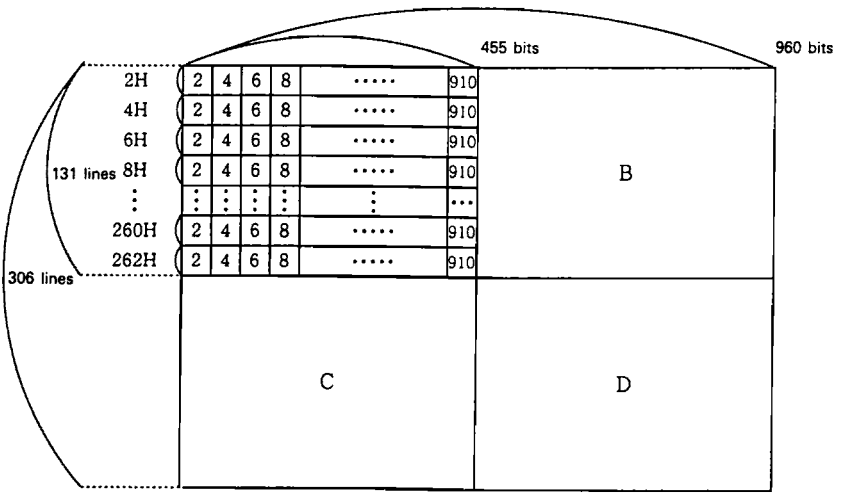
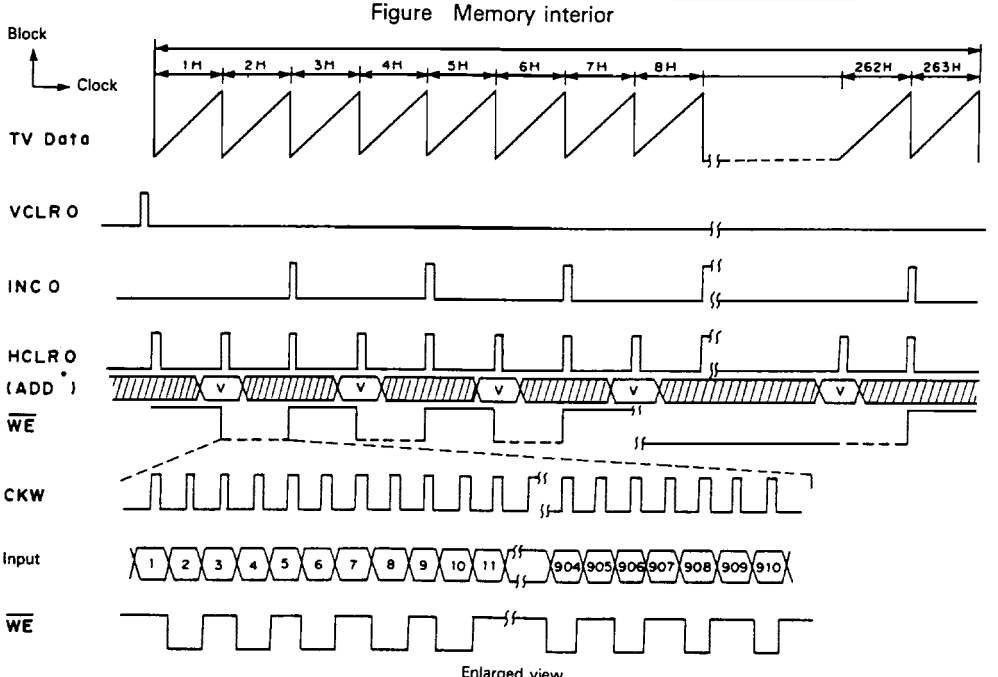


Figure Memory interior



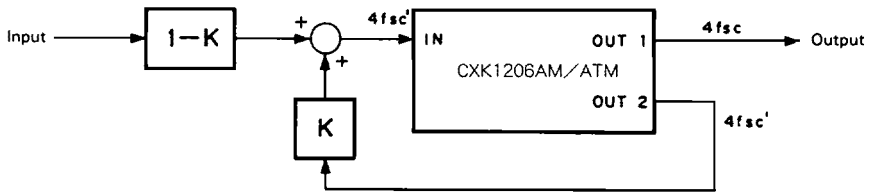
V: Valid address

▨: Irrespective of "H" or "L"

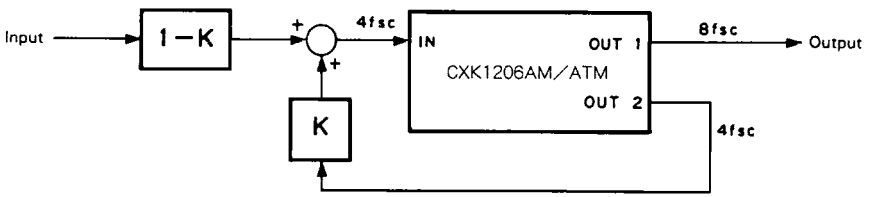
*Note) Use of the address preset mode permits Write to B, C and D areas. Write to area C is also possible by operating INC0 in non-recursive mode.

3-port VRAM Application Example

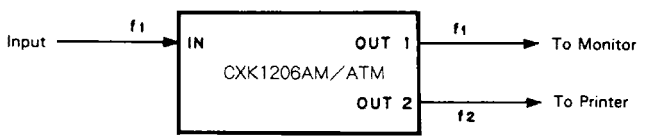
1. NR + TBC



2. NR + double-speed



3. Monitor and Printer Concurrent Drive

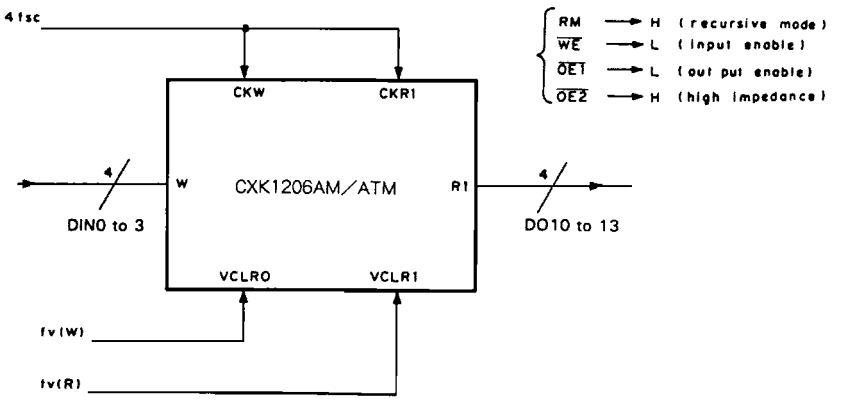


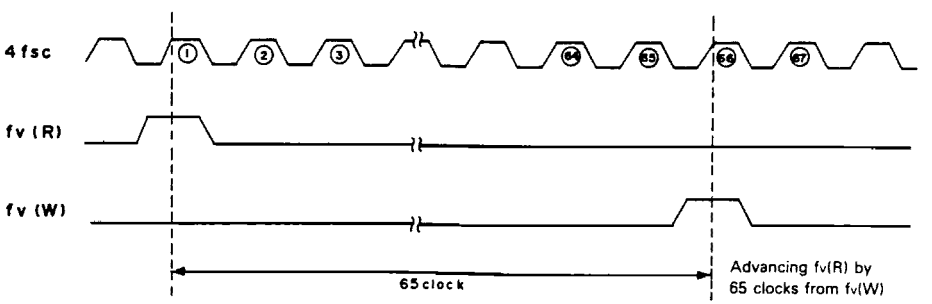
Application Circuit (1)

Using recursive mode: The following diagram shows a circuit with:

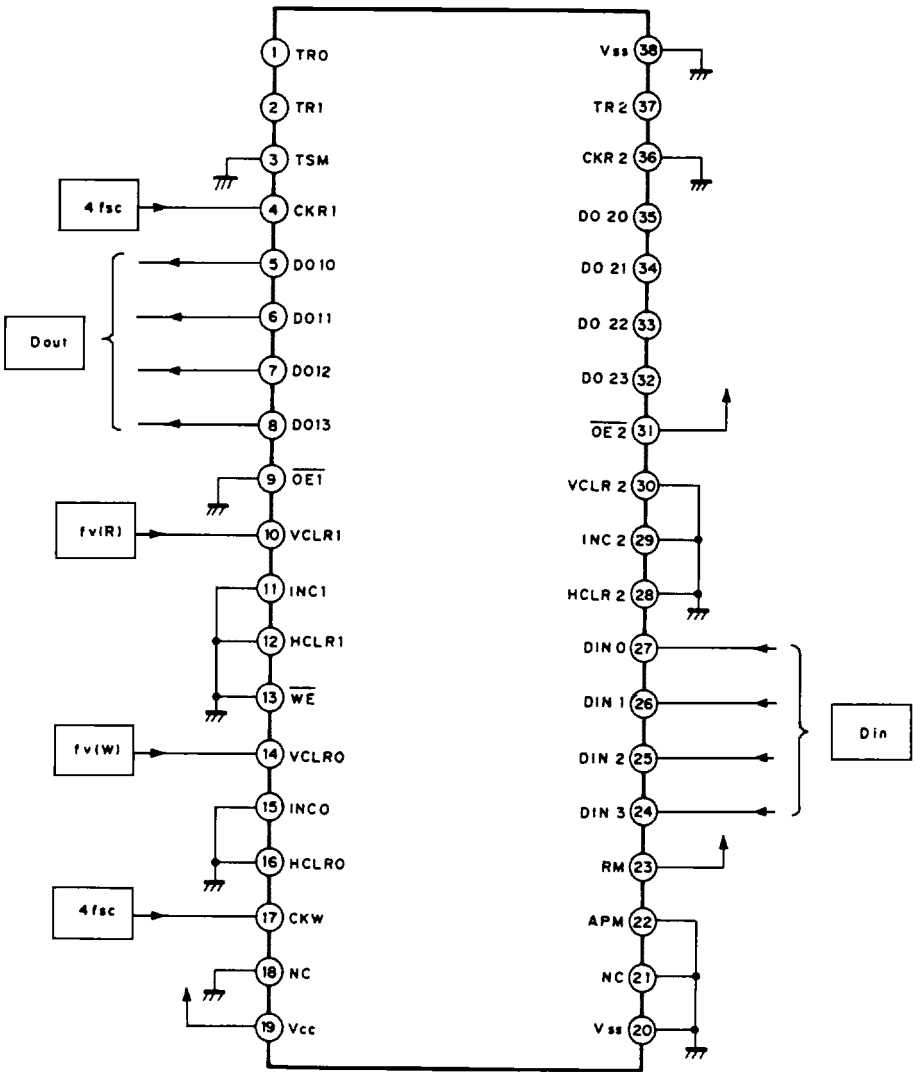
1) 1 field delay
2) 1 frame delay

(1) 1 field delay:

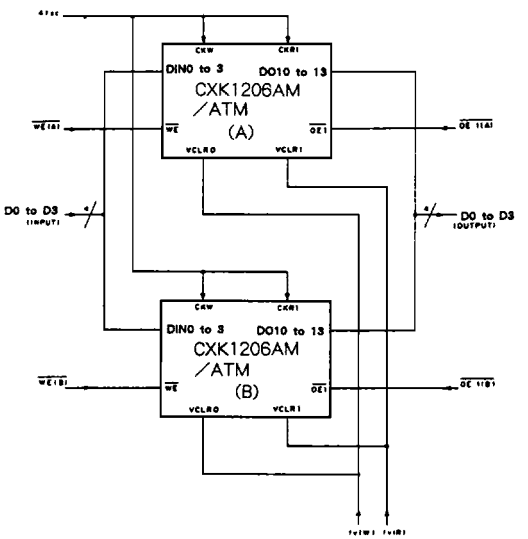


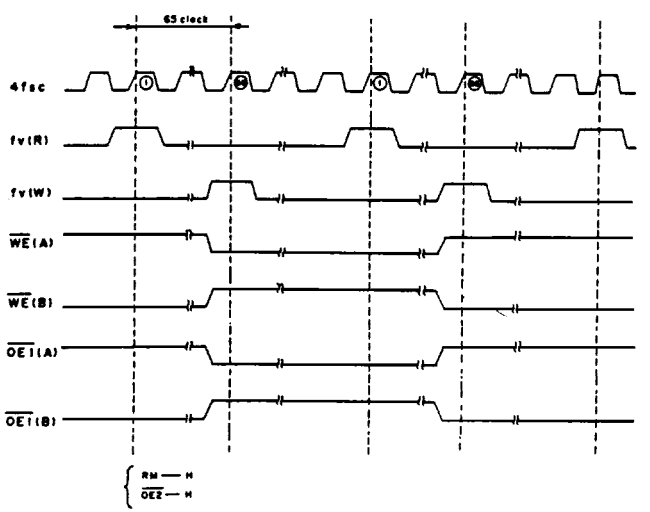


VRAM peripheral connection with 1 field delay (SOP)



Application Circuit (2) 1 frame delay

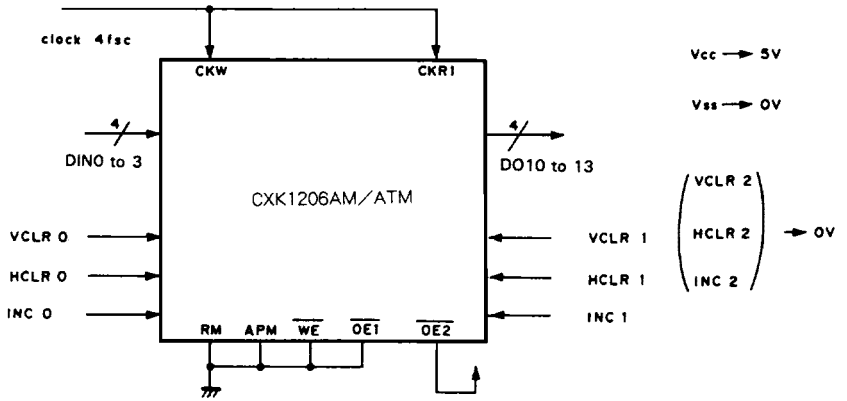


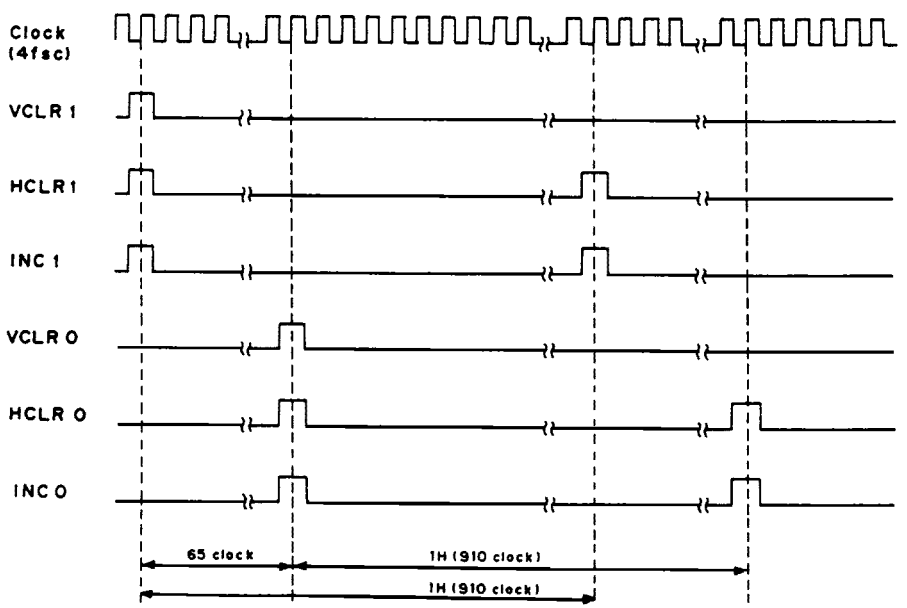


Note) 1. Do not turn off CKW for transfer control between DRAM and I/O port.
2. Do not turn off CKR1 for refreshing.
3. Switchover A chip and B chip with $\overline{WE}$ and $\overline{OE1}$.

Application Circuit (3)

The following is a circuit achieving "1 field delay" using non-recursive mode.

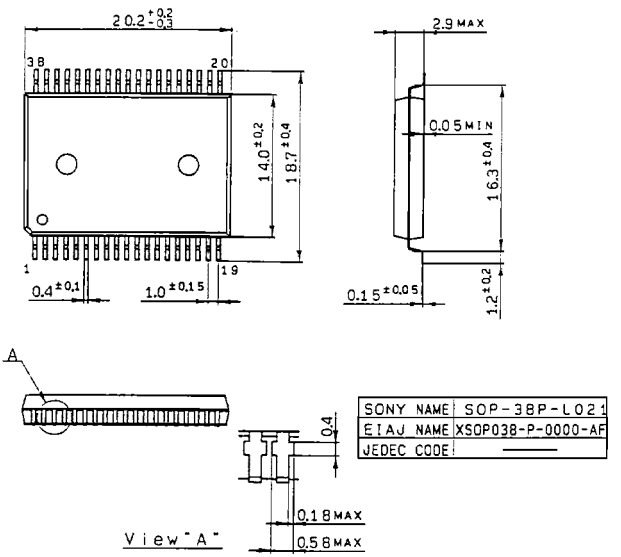




Package Outline Unit : mm

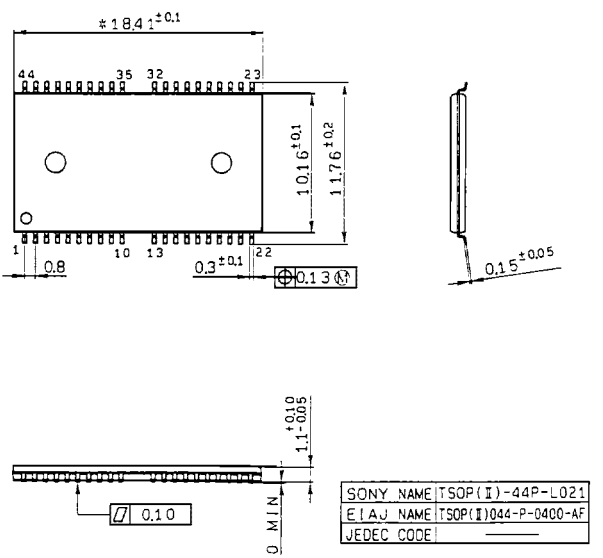
CXK1206AM

38pin SOP (Plastic)



CXK1206ATM

44pin TSOP(II) (Plastic) 400mil



The measurements marked * includes the maximum of 0.15 of residual resin at each end.