# 9. ELECTRICAL DATA

## 9.1 INTRODUCTION

The following sections describe recommended electrical connections for the Intel386 DX, and its electrical specifications.

## 9.2 POWER AND GROUNDING

### 9.2.1 Power Connections

The Intel386 DX is implemented in CHMOS III and CHMOS IV technology and has modest power requirements. However, its high clock frequency and 72 output buffers (address, data, control, and HLDA) can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, 20 $V_{CC}$ and 21 $V_{SS}$ pins separately feed functional units of the Intel386 DX.

Power and ground connections must be made to all external $V_{CC}$ and GND pins of the Intel386 DX. On the circuit board, all $V_{CC}$ pins must be connected on a $V_{CC}$ plane. All $V_{SS}$ pins must be likewise connected on a GND plane.

### 9.2.2 Power Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Intel386 DX. The Intel386 DX driving its 32-bit parallel address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Intel386 DX and decoupling capacitors as much as possible. Capacitors specifically for PGA packages are also commercially available, for the lowest possible inductance.

### 9.2.3 Resistor Recommendations

The ERROR# and BUSY# inputs have resistor pullups of approximately 20 KΩ built-in to the Intel386 DX to keep these signals negated when no Intel387 DX coprocessor is present in the system (or temporarily removed from its socket). The BS16# input also has an internal pullup resistor of approximately 20 KΩ, and the PEREQ input has an internal pulldown resistor of approximately 20 KΩ.

In typical designs, the external pullup resistors shown in Table 9-1 are recommended. However, a particular design may have reason to adjust the resistor values recommended here, or alter the use of pullup resistors in other ways.

### 9.2.4 Other Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. N.C. pins should always remain unconnected.

Particularly when not using interrupts or bus hold, (as when first prototyping, perhaps) prevent any chance of spurious activity by connecting these associated inputs to GND:

| Pin | Signal |
|---|---|
| B7 | INTR |
| B8 | NMI |
| D14 | HOLD |

If not using address pipelining, pullup D13 NA# to $V_{CC}$.

If not using 16-bit bus size, pullup C14 BS16# to $V_{CC}$.

Pullups in the range of 20 KΩ are recommended.

**Table 9-1. Recommended Resistor Pullups to $V_{CC}$**

| Pin and Signal | Pullup Value | Purpose |
|---|---|---|
| E14 ADS# | 20 KΩ ±10% | Lightly Pull ADS# Negated During Intel386 DX Hold Acknowledge States |
| C10 LOCK# | 20 KΩ ±10% | Lightly Pull LOCK# Negated During Intel386 DX Hold Acknowledge States |

## 9.3 MAXIMUM RATINGS

**Table 9-2. Maximum Ratings**

| Parameter | Intel386™ DX 20, 25, 33 MHz Maximum Rating |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Case Temperature Under Bias | −65°C to +110°C |
| Supply Voltage with Respect to $V_{SS}$ | −0.5V to +6.5V |
| Voltage on Other Pins | −0.5V to $V_{CC}$ + 0.5V |

Table 9-2 is a stress rating only, and functional operation at the maximums is not guaranteed. Functional operating conditions are given in **9.4 D.C. Specifications** and **9.5 A.C. Specifications**.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the Intel386 DX contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

## 9.4 D.C. SPECIFICATIONS

Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to 85°C

**Table 9-3. Intel386™ DX D.C. Characteristics**

| Symbol | Parameter | Intel386™ DX 20 MHz, 25 MHz, 33 MHz | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IL}$ | Input Low Voltage | −0.3 | 0.8 | V | (Note 1) |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ + 0.3 | V | |
| $V_{ILC}$ | CLK2 Input Low Voltage | −0.3 | 0.8 | V | (Note 1) |
| $V_{IHC}$ | CLK2 Input High Voltage<br>20 MHz<br>25 MHz and 33 MHz | <br>$V_{CC}$ − 0.8<br>3.7 | <br>$V_{CC}$ + 0.3<br>$V_{CC}$ + 0.3 | <br>V<br>V | |
| $V_{OL}$ | Output Low Voltage<br>$I_{OL}$ = 4 mA: A2–A31, D0–D31<br>$I_{OL}$ = 5 mA: BE0#–BE3#, W/R#, D/C#, M/IO#, LOCK#, ADS#, HLDA | <br><br> | <br>0.45<br>0.45 | <br>V<br>V | |
| $V_{OH}$ | Output High Voltage<br>$I_{OH}$ = 1 mA: A2–A31, D0–D31<br>$I_{OH}$ = 0.9 mA: BE0#–BE3#, W/R#, D/C#, M/IO#, LOCK#, ADS#, HLDA | <br>2.4<br>2.4 | <br><br> | <br>V<br>V | |
| $I_{LI}$ | Input Leakage Current (For All Pins except BS16#, PEREQ, BUSY#, and ERROR#) | | ±15 | µA | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{IH}$ | Input Leakage Current (PEREQ Pin) | | 200 | µA | $V_{IH}$ = 2.4V (Note 2) |
| $I_{IL}$ | Input Leakage Current (BS16#, BUSY#, and ERROR# Pins) | | −400 | µA | $V_{IL}$ = 0.45 (Note 3) |
| $I_{LO}$ | Output Leakage Current | | ±15 | µA | 0.45V ≤ $V_{OUT}$ ≤ $V_{CC}$ |
| $I_{CC}$ | Supply Current<br>CLK2 = 40 MHz: with 20 MHz Intel386™ DX<br>CLK2 = 50 MHz: with 25 MHz Intel386™ DX<br>CLK2 = 66 MHz: with 33 MHz Intel386™ DX | | <br>260<br>320<br>390 | <br>mA<br>mA<br>mA | (Note 4)<br>$I_{CC}$ Typ. = 200 mA<br>$I_{CC}$ Typ. = 240 mA<br>$I_{CC}$ Typ. = 300 mA |
| $C_{IN}$ | Input or I/O Capacitance | | 10 | pF | $F_C$ = 1 MHz |
| $C_{OUT}$ | Output Capacitance | | 12 | pF | $F_C$ = 1 MHz |
| $C_{CLK}$ | CLK2 Capacitance | | 20 | pF | $F_C$ = 1 MHz |

**NOTES:**
1. The min value, −0.3, is not 100% tested.
2. PEREQ input has an internal pulldown resistor.
3. BS16#, BUSY# and ERROR# inputs each have an internal pullup resistor.
4. CHMOS IV Technology (CHMOS III Max $I_{CC}$ at 20 MHz, 25 MHz = 500 mA, 550 mA).

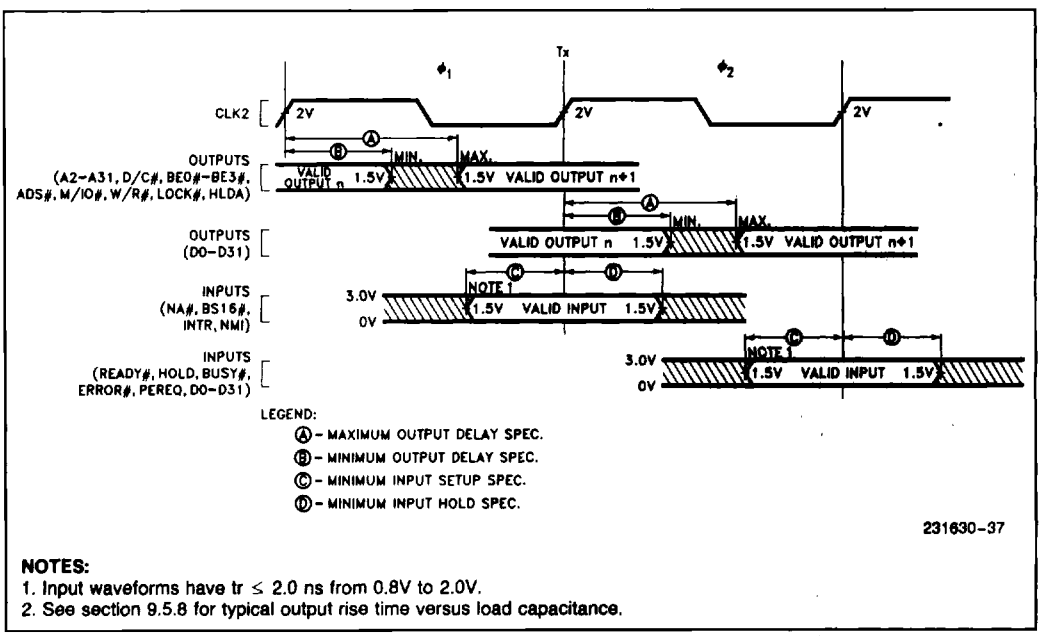
## 9.5 A.C. SPECIFICATIONS

### 9.5.1 A.C. Spec Definitions

The A.C. specifications, given in Tables 9-4, 9-5, and 9-6, consist of output delays, input setup requirements and input hold requirements. All A.C. specifications are relative to the CLK2 rising edge crossing the 2.0V level.

A.C. spec measurement is defined by Figure 9-1. Inputs must be driven to the voltage levels indicated by Figure 9-1 when A.C. specifications are measured. Intel386 DX output delays are specified with minimum and maximum limits, measured as shown. The minimum Intel386 DX delay times are hold times provided to external circuitry, Intel386 DX input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Intel386 DX operation.

Outputs NA#, W/R#, D/C#, M/IO#, LOCK#, BE0#-BE3#, A2-A31 and HLDA only change at the beginning of phase one. D0-D31 (write cycles) only change at the beginning of phase two. The READY#, HOLD, BUSY#, ERROR#, PEREQ and D0-D31 (read cycles) inputs are sampled at the beginning of phase one. The NA#, BS16#, INTR and NMI inputs are sampled at the beginning of phase two.




**NOTES:**
1. Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.
2. See section 9.5.8 for typical output rise time versus load capacitance.

**Figure 9-1. Drive Levels and Measurement Points for A.C. Specifications**

### 9.5.2 A.C. Specification Tables

Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to +85°C

**Table 9-4. 33 MHz Intel386™ DX A.C. Characteristics**

| Symbol | Parameter | 33 MHz Intel386™ DX | | Unit | Ref. Fig. | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| | Operating Frequency | 8 | 33.3 | MHz | | Half of CLK2 Frequency |
| t1 | CLK2 Period | 15.0 | 62.5 | ns | 9-3 | |
| t2a | CLK2 High Time | 6.25 | | ns | 9-3 | at 2V |
| t2b | CLK2 High Time | 4.5 | | ns | 9-3 | at 3.7V |
| t3a | CLK2 Low Time | 6.25 | | ns | 9-3 | at 2V |
| t3b | CLK2 Low Time | 4.5 | | ns | 9-3 | at 0.8V |
| t4 | CLK2 Fall Time | | 4 | ns | 9-3 | 3.7V to 0.8V (Note 3) |
| t5 | CLK2 Rise Time | | 4 | ns | 9-3 | 0.8V to 3.7V (Note 3) |
| t6 | A2–A31 Valid Delay | 4 | 15 | ns | 9-5 | $C_L$ = 50 pF |
| t7 | A2–A31 Float Delay | 4 | 20 | ns | 9-6 | (Note 1) |
| t8 | BE0#–BE3#, LOCK# Valid Delay | 4 | 15 | ns | 9-5 | $C_L$ = 50 pF |
| t9 | BE0#–BE3#, LOCK# Float Delay | 4 | 20 | ns | 9-6 | (Note 1) |
| t10 | W/R#, M/IO#, D/C#, Valid Delay | 4 | 15 | ns | 9-5 | $C_L$ = 50 pF |
| t10a | ADS# Valid Delay | 4 | 14.5 | ns | 9-5 | $C_L$ = 50 pF |
| t11 | W/R#, M/IO#, D/C#, ADS# Float Delay | 4 | 20 | ns | 9-6 | (Note 1) |
| t12 | D0–D31 Write Data Valid Delay | 7 | 24 | ns | 9-5a | $C_L$ = 50 pF, (Note 4) |
| t12a | D0–D31 Write Data Hold Time | 2 | | | 9-5b | $C_L$ = 50 pF |
| t13 | D0–D31 Float Delay | 4 | 17 | ns | 9-6 | (Note 1) |
| t14 | HLDA Valid Delay | 4 | 20 | ns | 9-6 | $C_L$ = 50 pF |
| t15 | NA# Setup Time | 5 | | ns | 9-4 | |
| t16 | NA# Hold Time | 2 | | ns | 9-4 | |
| t17 | BS16# Setup Time | 5 | | ns | 9-4 | |
| t18 | BS16# Hold Time | 2 | | ns | 9-4 | |
| t19 | READY# Setup Time | 7 | | ns | 9-4 | |
| t20 | READY# Hold Time | 4 | | ns | 9-4 | |

## 9.5.2 A.C. Specification Tables (Continued)

Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to +85°C

**Table 9-4. 33 MHz Intel386™ DX A.C. Characteristics (Continued)**

| Symbol | Parameter | 33 MHz Intel386™ DX | | Unit | Ref. Fig. | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| t21 | D0–D31 Read Setup Time | 5 | | ns | 9-4 | |
| t22 | D0–D31 Read Hold Time | 3 | | ns | 9-4 | |
| t23 | HOLD Setup Time | 11 | | ns | 9-4 | |
| t24 | HOLD Hold Time | 2 | | ns | 9-4 | |
| t25 | RESET Setup Time | 5 | | ns | 9-7 | |
| t26 | RESET Hold Time | 2 | | ns | 9-7 | |
| t27 | NMI, INTR Setup Time | 5 | | ns | 9-4 | (Note 2) |
| t28 | NMI, INTR Hold Time | 5 | | ns | 9-4 | (Note 2) |
| t29 | PEREQ, ERROR#, BUSY# Setup Time | 5 | | ns | 9-4 | (Note 2) |
| t30 | PEREQ, ERROR#, BUSY# Hold Time | 4 | | ns | 9-4 | (Note 2) |

**NOTES:**

1. Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.
4. Min. time not 100% tested.

## 9.5.2 A.C. Specification Tables (Continued)

Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to +85°C

**Table 9-5. 25 MHz Intel386™ DX A.C. Characteristics**

| Symbol | Parameter | 25 MHz Intel386™ DX | | Unit | Ref. Fig. | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| | Operating Frequency | 4 | 25 | MHz | | Half of CLK2 Frequency |
| t1 | CLK2 Period | 20 | 125 | ns | 9-3 | |
| t2a | CLK2 High Time | 7 | | ns | 9-3 | at 2V |
| t2b | CLK2 High Time | 4 | | ns | 9-3 | at 3.7V |
| t3a | CLK2 Low Time | 7 | | ns | 9-3 | at 2V |
| t3b | CLK2 Low Time | 5 | | ns | 9-3 | at 0.8V |
| t4 | CLK2 Fall Time | | 7 | ns | 9-3 | 3.7V to 0.8V |
| t5 | CLK2 Rise Time | | 7 | ns | 9-3 | 0.8V to 3.7V |
| t6 | A2–A31 Valid Delay | 4 | 21 | ns | 9-5 | $C_L$ = 50 pF |
| t7 | A2–A31 Float Delay | 4 | 30 | ns | 9-6 | (Note 1) |
| t8 | BE0#–BE3# Valid Delay | 4 | 24 | ns | 9-5 | $C_L$ = 50 pF |
| t8a | LOCK# Valid Delay | 4 | 21 | ns | 9-5 | $C_L$ = 50 pF |
| t9 | BE0#–BE3#, LOCK# Float Delay | 4 | 30 | ns | 9-6 | (Note 1) |
| t10 | W/R#, M/IO#, D/C#, ADS# Valid Delay | 4 | 21 | ns | 9-5 | $C_L$ = 50 pF |
| t11 | W/R#, M/IO#, D/C#, ADS# Float Delay | 4 | 30 | ns | 9-6 | (Note 1) |
| t12 | D0–D31 Write Data Valid Delay | 7 | 27 | ns | 9-5a | $C_L$ = 50 pF |
| t12a | D0–D31 Write Data Hold Time | 2 | | | 9-5b | $C_L$ = 50 pF |
| t13 | D0–D31 Float Delay | 4 | 22 | ns | 9-6 | (Note 1) |
| t14 | HLDA Valid Delay | 4 | 22 | ns | 9-6 | $C_L$ = 50 pF |
| t15 | NA# Setup Time | 7 | | ns | 9-4 | |
| t16 | NA# Hold Time | 3 | | ns | 9-4 | |
| t17 | BS16# Setup Time | 7 | | ns | 9-4 | |
| t18 | BS16# Hold Time | 3 | | ns | 9-4 | |
| t19 | READY# Setup Time | 9 | | ns | 9-4 | |
| t20 | READY# Hold Time | 4 | | ns | 9-4 | |

## 9.5.2 A.C. Specification Tables (Continued)

Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to +85°C

**Table 9-5. 25 MHz Intel386™ DX A.C. Characteristics (Continued)**

| Symbol | Parameter | 25 MHz Intel386™ DX | | Unit | Ref. Fig. | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| t21 | D0–D31 Read Setup Time | 7 | | ns | 9-4 | |
| t22 | D0–D31 Read Hold Time | 5 | | ns | 9-4 | |
| t23 | HOLD Setup Time | 15 | | ns | 9-4 | |
| t24 | HOLD Hold Time | 3 | | ns | 9-4 | |
| t25 | RESET Setup Time | 10 | | ns | 9-7 | |
| t26 | RESET Hold Time | 3 | | ns | 9-7 | |
| t27 | NMI, INTR Setup Time | 6 | | ns | 9-4 | (Note 2) |
| t28 | NMI, INTR Hold Time | 6 | | ns | 9-4 | (Note 2) |
| t29 | PEREQ, ERROR#, BUSY# Setup Time | 6 | | ns | 9-4 | (Note 2) |
| t30 | PEREQ, ERROR#, BUSY# Hold Time | 5 | | ns | 9-4 | (Notes 2, 3) |

**NOTES:**

1. Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3.

| | Symbol | Parameter | Min |
|---|---|---|---|
| $T_C$ = 0°C | t30 | PEREQ, ERROR#, BUSY# Hold Time | 4 |
| $T_C$ = +85°C | t30 | PEREQ, ERROR#, BUSY# Hold Time | 5 |

## 9.5.2 A.C. Specification Tables (Continued)

Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to +85°C

**Table 9.6. 20 MHz Intel386™ DX A.C. Characteristics**

| Symbol | Parameter | 20 MHz Intel386™ DX | | Unit | Ref. Fig. | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| | Operating Frequency | 4 | 20 | MHz | | Half of CLK2 Frequency |
| $t_1$ | CLK2 Period | 25 | 125 | ns | 9-3 | |
| $t_{2a}$ | CLK2 High Time | 8 | | ns | 9-3 | at 2V |
| $t_{2b}$ | CLK2 High Time | 5 | | ns | 9-3 | at ($V_{CC}$ − 0.8V) |
| $t_{3a}$ | CLK2 Low Time | 8 | | ns | 9-3 | at 2V |
| $t_{3b}$ | CLK2 Low Time | 6 | | ns | 9-3 | at 0.8V |
| $t_4$ | CLK2 Fall Time | | 8 | ns | 9-3 | ($V_{CC}$ − 0.8V) to 0.8V |
| $t_5$ | CLK2 Rise Time | | 8 | ns | 9-3 | 0.8V to ($V_{CC}$ − 0.8V) |
| $t_6$ | A2–A31 Valid Delay | 4 | 30 | ns | 9-5 | $C_L$ = 120 pF |
| $t_7$ | A2–A31 Float Delay | 4 | 32 | ns | 9-6 | (Note 1) |
| $t_8$ | BE0#–BE3#, LOCK# Valid Delay | 4 | 30 | ns | 9-5 | $C_L$ = 75 pF |
| $t_9$ | BE0#–BE3#, LOCK# Float Delay | 4 | 32 | ns | 9-6 | (Note 1) |
| $t_{10}$ | W/R#, M/IO#, D/C#, ADS# Valid Delay | 6 | 28 | ns | 9-5 | $C_L$ = 75 pF |
| $t_{11}$ | W/R#, M/IO#, D/C#, ADS# Float Delay | 6 | 30 | ns | 9-6 | (Note 1) |
| $t_{12}$ | D0–D31 Write Data Valid Delay | 4 | 38 | ns | 9-5c | $C_L$ = 120 pF |
| $t_{13}$ | D0–D31 Float Delay | 4 | 27 | ns | 9-6 | (Note 1) |
| $t_{14}$ | HLDA Valid Delay | 6 | 28 | ns | 9-6 | $C_L$ = 75 pF |
| $t_{15}$ | NA# Setup Time | 9 | | ns | 9-4 | |
| $t_{16}$ | NA# Hold Time | 14 | | ns | 9-4 | |
| $t_{17}$ | BS16# Setup Time | 13 | | ns | 9-4 | |
| $t_{18}$ | BS16# Hold Time | 21 | | ns | 9-4 | |
| $t_{19}$ | READY# Setup Time | 12 | | ns | 9-4 | |
| $t_{20}$ | READY# Hold Time | 4 | | ns | 9-4 | |
| $t_{21}$ | D0–D31 Read Setup Time | 11 | | ns | 9-4 | |
| $t_{22}$ | D0–D31 Read Hold Time | 6 | | ns | 9-4 | |
| $t_{23}$ | HOLD Setup Time | 17 | | ns | 9-4 | |
| $t_{24}$ | HOLD Hold Time | 5 | | ns | 9-4 | |
| $t_{25}$ | RESET Setup Time | 12 | | ns | 9-7 | |

## 9.5.2 A.C. Specification Tables (Continued)

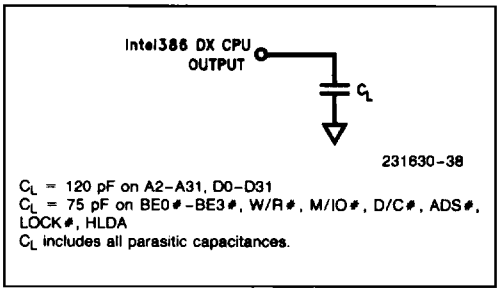
Functional Operating Range: $V_{CC}$ = 5V ±5%; $T_{CASE}$ = 0°C to +85°C

**Table 9-6. 20 MHz Intel386™ DX A.C. Characteristics (Continued)**

| Symbol | Parameter | 20 MHz Intel386™ DX | | Unit | Ref. Fig. | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| $t_{26}$ | RESET Hold Time | 4 | | ns | 9-7 | |
| $t_{27}$ | NMI, INTR Setup Time | 16 | | ns | 9-4 | (Note 2) |
| $t_{28}$ | NMI, INTR Hold Time | 16 | | ns | 9-4 | (Note 2) |
| $t_{29}$ | PEREQ, ERROR#, BUSY# Setup Time | 14 | | ns | 9-4 | (Note 2) |
| $t_{30}$ | PEREQ, ERROR#, BUSY# Hold Time | 5 | | ns | 9-4 | (Note 2) |

**NOTES:**
1. Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.

### 9.5.3 A.C. Test Loads




$C_L$ = 120 pF on A2–A31, D0–D31
$C_L$ = 75 pF on BE0#–BE3#, W/R#, M/IO#, D/C#, ADS#, LOCK#, HLDA
$C_L$ includes all parasitic capacitances.

**Figure 9-2. A.C. Test Load**

### 9.5.4 A.C. Timing Waveforms

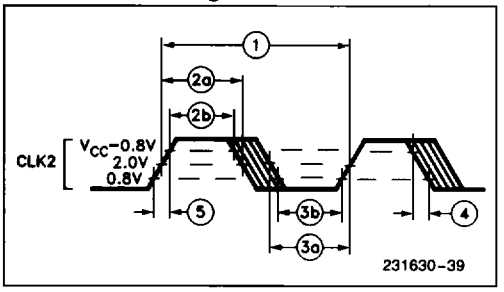



**Figure 9-3. CLK2 Timing**

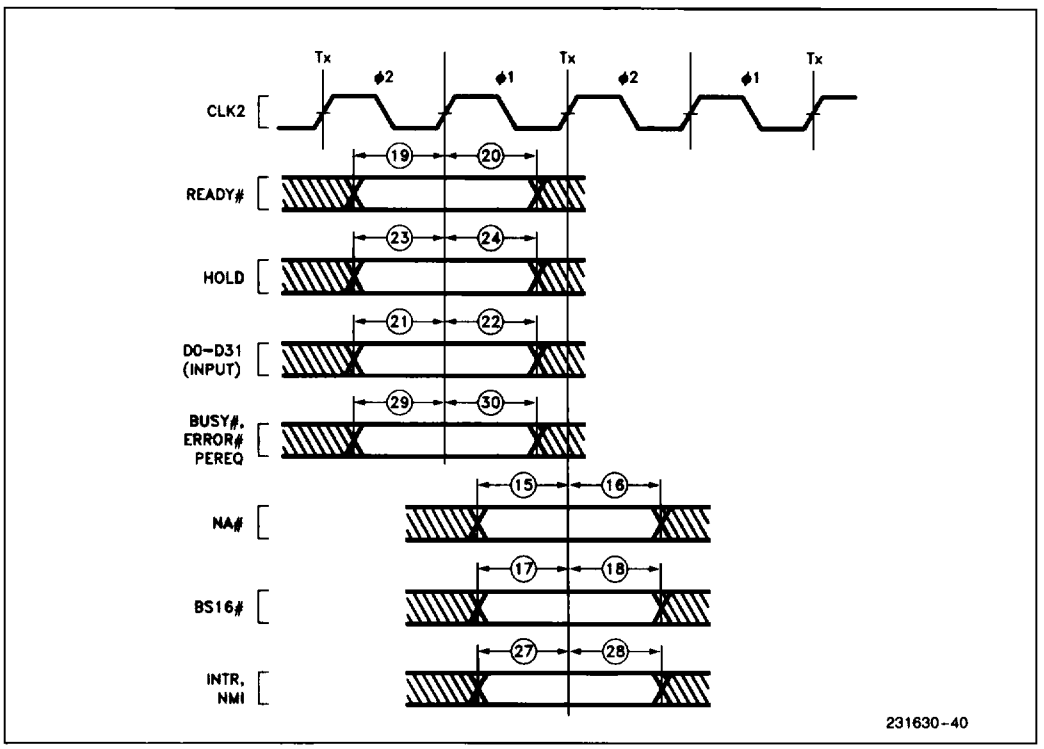



**Figure 9-4. Input Setup and Hold Timing**

3

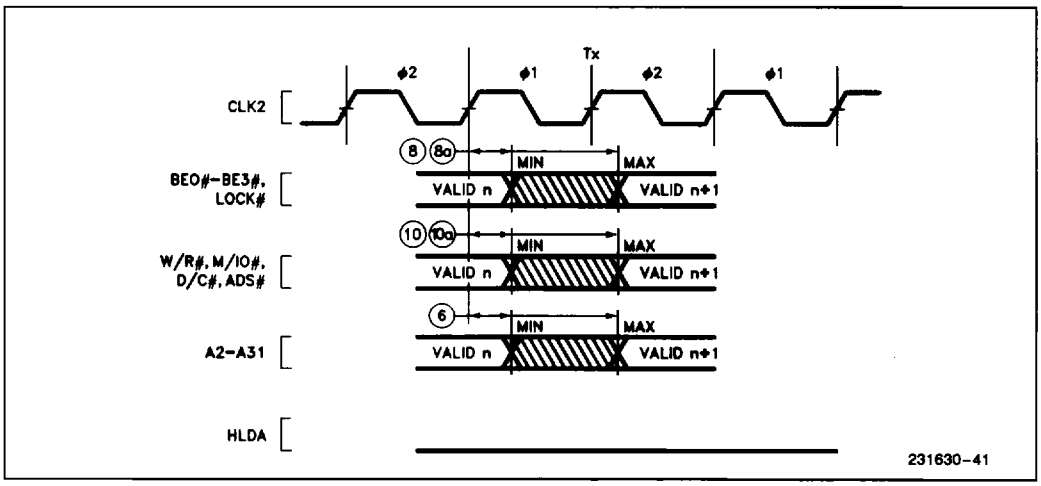



**Figure 9-5. Output Valid Delay Timing**

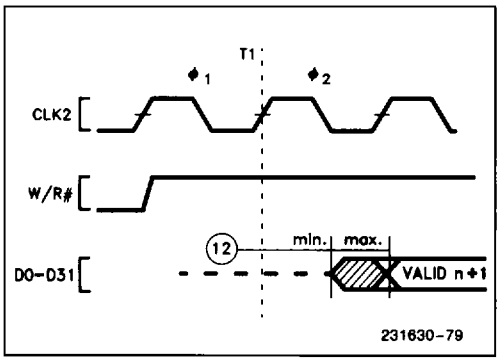



**Figure 9-5a. Write Data Valid Delay Timing (25 MHz, 33 MHz)**

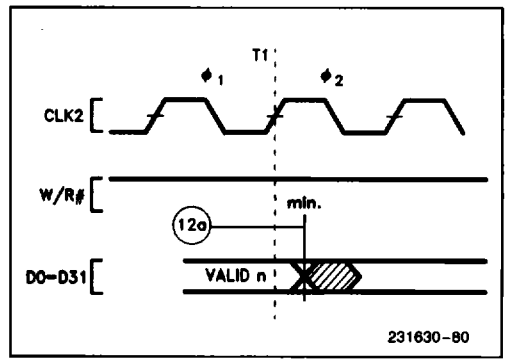



**Figure 9-5b. Write Data Hold Timing (25 MHz, 33 MHz)**

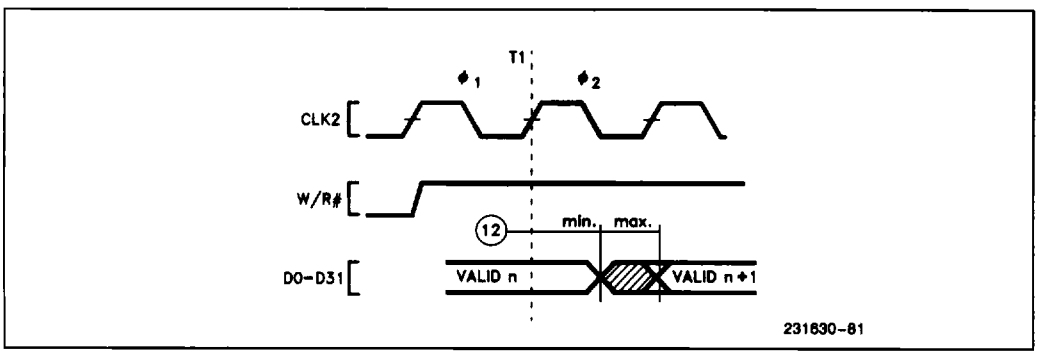
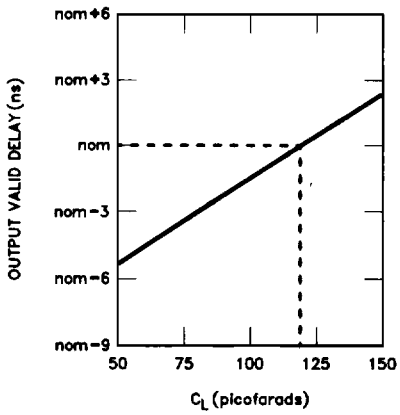



**Figure 9-5c. Write Data Valid Delay Timing (20 MHz)**

### 9.5.5 Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L$ = 120 pF)

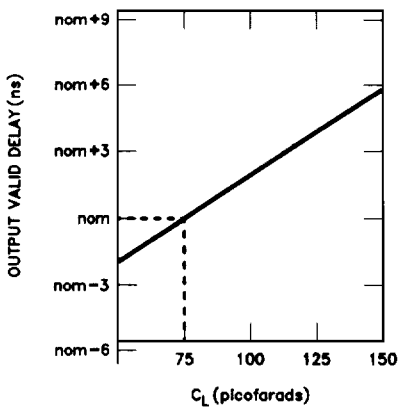



231630-77

**NOTE:**
This graph will not be linear outside of the $C_L$ range shown.

3

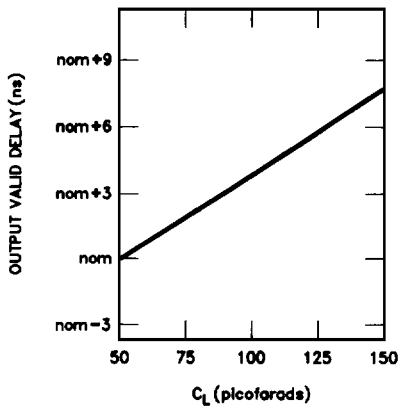
### 9.5.6 Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L$ = 75 pF)




231630-82

**NOTE:**
This graph will not be linear outside of the $C_L$ range shown.

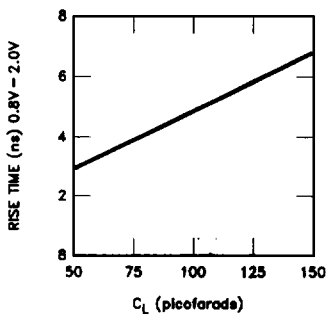
### 9.5.7 Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L$ = 50 pF)




231630-83

**NOTE:**
This graph will not be linear outside of the $C_L$ range shown.

### 9.5.8 Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature




231630-78

**NOTE:**
This graph will not be linear outside of the $C_L$ range shown.

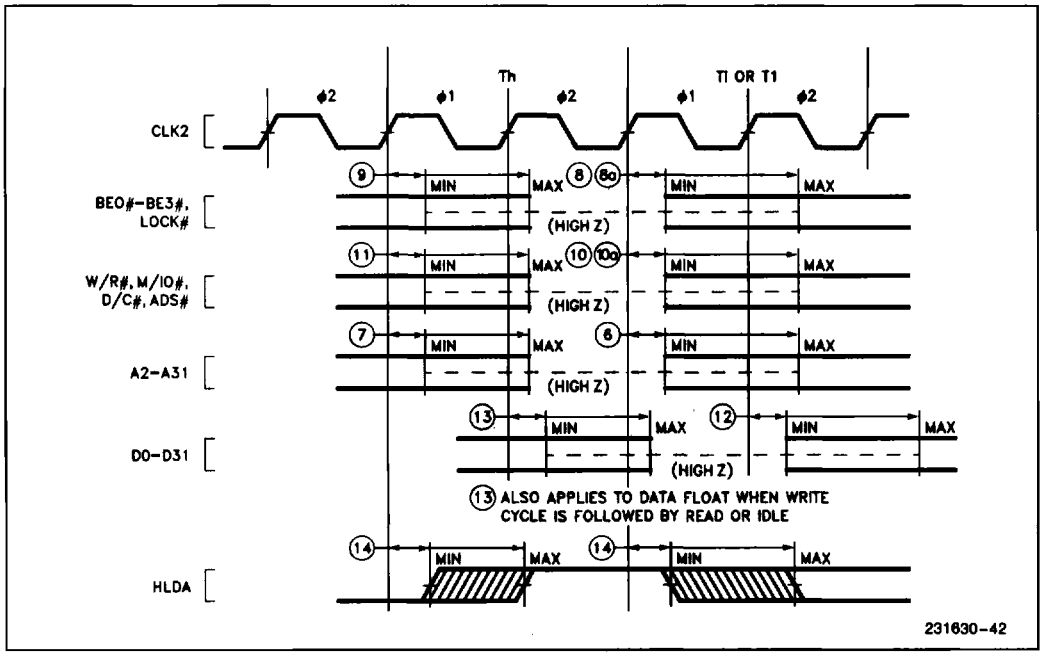
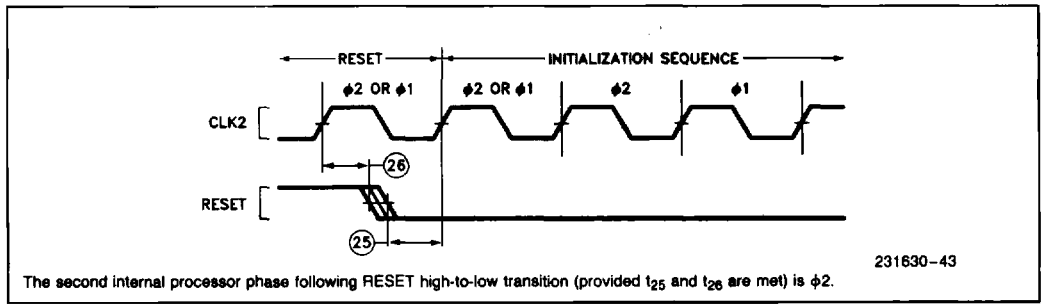



**Figure 9-6. Output Float Delay and HLDA Valid Delay Timing**




The second internal processor phase following RESET high-to-low transition (provided $t_{25}$ and $t_{26}$ are met) is φ2.

**Figure 9-7. RESET Setup and Hold Timing, and Internal Phase**