ADVANCE INFORMATION SPECIFICATION

T-52-33-27

Z53C80

SMALL COMPUTER SYSTEM INTERFACE (SCSI)

FEATURES

- Supports 53C80 pinout
- Low power CMOS
- Asynchronous Interface, supports data transfers up to 3 Mbytes/sec
- Direct SCSI Bus Interface with On-Board 48 mA drivers
- Supports Target and Initiator roles
- Arbitration Support
- DMA or Programmed I/O Data Transfers
- Supports Normal or Block Mode DMA
- Memory or I/O Mapped CPU Interface

GENERAL DESCRIPTION

The Z53C80 SCSI (Small Computer System Interface) controller is a 44-pin PLCC or 48-pin DIP CMOS device. It is designed to implement the SCSI protocol as defined by the ANSI X3.131-1986 standard, and is fully compatible with the industry standard 53C80. It is capable of operating both as a Target and as an Initiator. Special high-current open-drain outputs enable it to directly interface to the SCSI bus. The Z53C80 has the necessary interface hook-ups so the system CPU can communicate with it like with any other peripheral device. The CPU can read from, or write to, the SCSI registers which are addressed as standard or memory-mapped I/Os.

The Z53C80 increases the system performance by minimizing the CPU intervention in DMA operations which the SCSI controls. The CPU is interrupted when it detects a bus condition that requires attention. It also supports arbitration and reselection. The Z53C80 has the proper handshake signals to support normal and block mode DMA operations with most DMA controllers available.

Figure 1 is the functional block diagram of the Z53C80. The pin functions of the Z53C80 are shown in Figure 2. The device is housed in a 48-pin DIP (Figure 3) and a 44-pin PLCC package (Figure 4).*

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

*Note: Power connections follow Conventional descriptions below

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

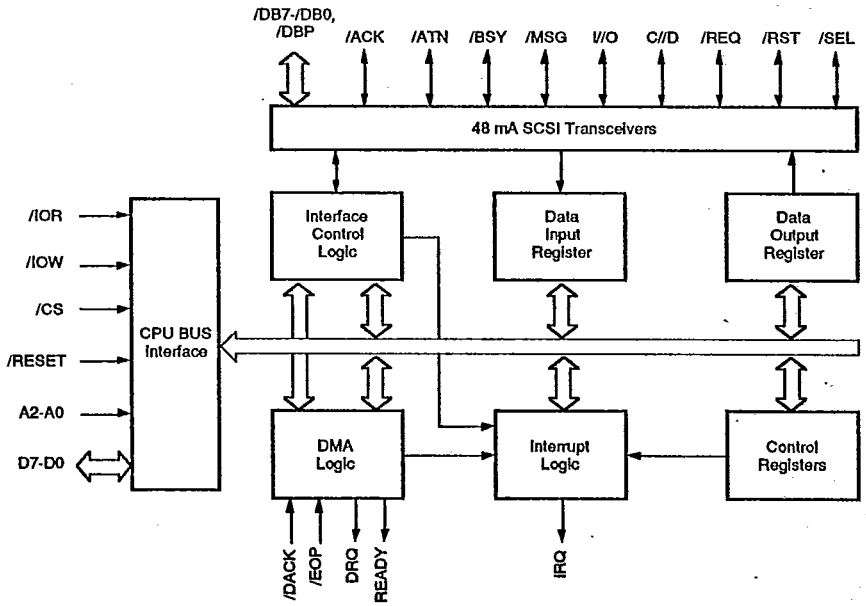

Figure 1. Block Diagram

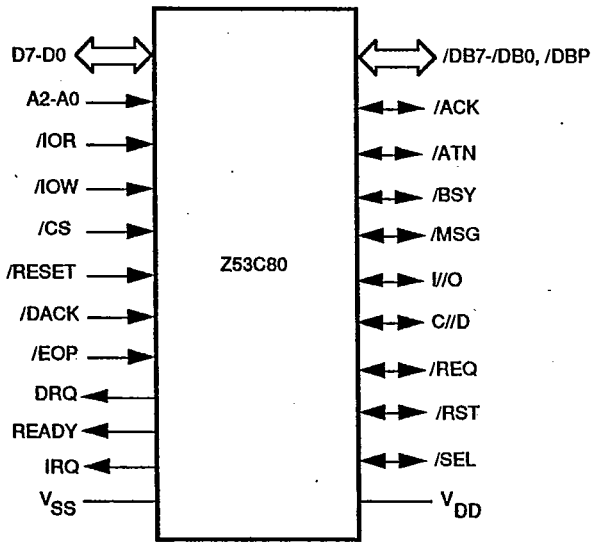

Figure 2. Pin Functions

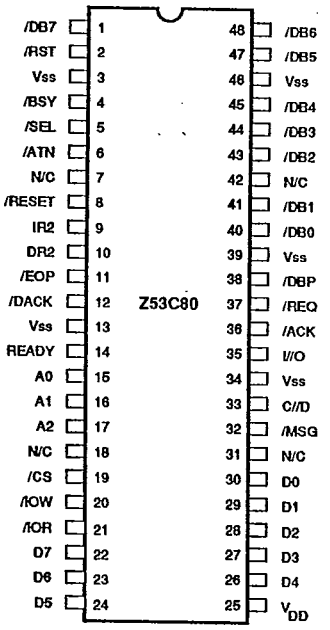

Figure 3. 40-Pin DIP Assignments

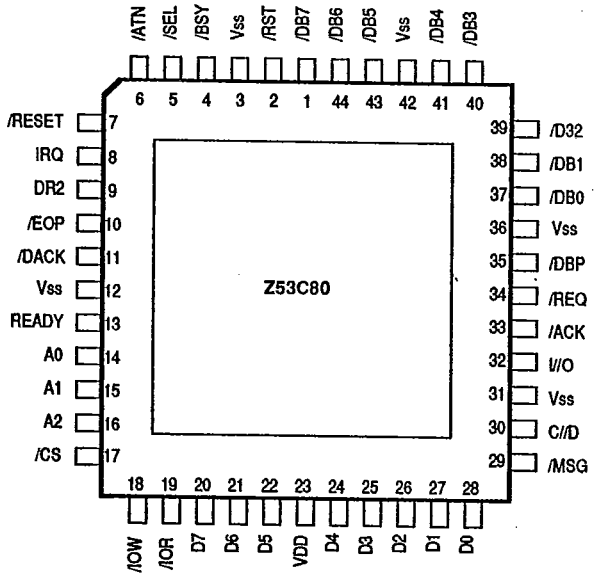

Figure 4. 44-Pin PLCC Pin Assignments

PIN DESCRIPTIONS

Microprocessor Bus

A2-A0. *Address Lines* (Input). Address lines are used with /CS, /IOR, and /IOW to address all internal registers.

/CS. *Chip Select* (Input, Active Low). This signal, in conjuction with /IOR or /IOW, enables the internal registers selected by A2-A0, to be read from or written to.

/DACK. *DMA Acknowledge* (Input, Active Low). /DACK resets DRQ and selects the data register for input or output data transfers. /DACK is used by DMA controller instead of /CS.

DRQ. *DMA Request* (Output, Active High). DRQ indicates that the data request is ready to be read or written. DRQ is asserted only if DMA mode is set in the Command Register. DRQ is cleared by /DACK.

D7-D0. *Data Lines* (Bidirectional, three-state, Active High). Bidirectional microprocessor data bus lines.

/EOP. *End of Process* (Input, Active Low). /EOP is used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred, but no additional bytes will be requested.

/IOR. *I/O Read* (Input, Active Low). /IOR is used in conjunction with /CS and A2-A0 to read an internal register. It also selects the Input Data Register when used with /DACK.

/IOW. *I/O Write* (Input, Active Low). /IOW is used in conjunction with /CS and A2-A0 to write to an internal register. It also selects the Output Data Register when used with /DACK.

IRQ. *Interrupt Request* (Output, Active High). IRQ alerts a microprocessor of an error condition or an event completion.

READY. *Ready* (Output, Active High). READY is used to control the speed of Block Mode DMA transfers. This signal goes active to indicate that the chip is ready to send/receive data and remains Low after a transfer until the last byte is sent or until the DMA Mode bit is reset.

/RESET. *Reset* (Input, Active Low). /RESET clears all registers. It has no effect upon the SCSI /RST signal.

SCSI Interface Signals

The following signals are all bi-directional, active low, open-drain signals with 48mA sink capability. All pins interface directly with the SCSI Bus.

/ACK. *Acknowledge* (Bidirectional, Open-drain, Active Low). Driven by an Initiator, /ACK indicates an acknowledgment for a /REQ//ACK data-transfer handshake. In the Target role, /ACK is received as a response to the /REQ Signal.

/ATN. *Attention* (Bidirectional, Open-drain, Active Low). Driven by an Initiator, received by the Target, /ATN indicates an Attention condition.

/BSY. *Busy* (Bidirectional, Open-drain, Active Low). This signal indicates that the SCSI Bus is being used and can be driven by both the Initiator and the Target device.

C//D. *Control//Data.* (Bidirectional, Open-drain). Driven by the Target and received by the Initiator, C//D indicates whether Control or Data information is on the Data Bus. True indicates Control.

/DB7-/DB0, /DBP. *Data Bus Bits, Data Bus Parity Bit* (Bidirectional, Open-drain). These eight data bits (/DB7-/DB0), plus a parity bit (/DBP) form the data bus. /DB7 is the most significant bit (MSB) and has the highest priority during the Arbitration phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during Arbitration.

I//O. *Input//Output* (Bidirectional, Open-drain). I//O is a signal driven by a Target which controls the direction of data movement on the SCSI bus. True indicates input to the Initiator. This signal is also used to distinguish between Selection and Reselection phases.

/MSG. *Message* (Bidirectional, Open-drain, Active Low). This signal is driven by the Target during the Message phase. The signal is received by the Initiator.

/REQ. *Request* (Bidirectional, Open-drain, Active Low). Driven by a Target and received by the Initiator, this signal indicates a request for a /REQ//ACK data-transfer handshake.

/RST. *SCSI Bus Reset* (Bidirectional, Open-drain, Active Low). This signal indicates a SCSI Bus Reset condition.

/SEL. *Select* (Bidirectional, Open-drain, Active Low). This signal is used by an Initiator to select a Target, or by a Target to reselect an Initiator.