



# STD5NK52ZD, STB5NK52ZD-1 STF5NK52ZD, STP5NK52ZD

N-channel 520 V, 1.22  $\Omega$ , 4.4 A, TO-220, I<sup>2</sup>PAK, I<sup>2</sup>PAK, DPAK, TO-220FP  
Zener-protected SuperMESH™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STB5NK52ZD-1	520 V	< 1.5 $\Omega$	4.4 A	70 W
STD5NK52ZD-1	520 V	< 1.5 $\Omega$	4.4 A	70 W
STD5NK52ZD	520 V	< 1.5 $\Omega$	4.4 A	70 W
STF5NK52ZD	520 V	< 1.5 $\Omega$	4.4 A	25 W
STP5NK52ZD	520 V	< 1.5 $\Omega$	4.4 A	70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Improved ESD capability

## Application

- Switching applications

## Description

The SuperFREDMesh™ series associates all advantages of reduced on-resistance, zener gate protection and very high dv/dt capability with a fast body-drain recovery diode. Such series complements the “FDmesh™” advanced technology.

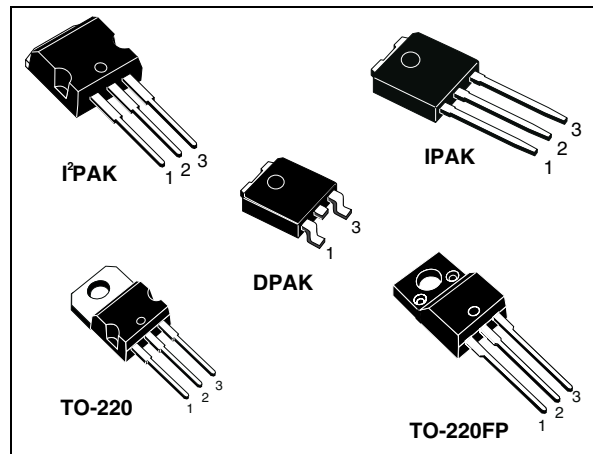


Figure 1. Internal schematic diagram

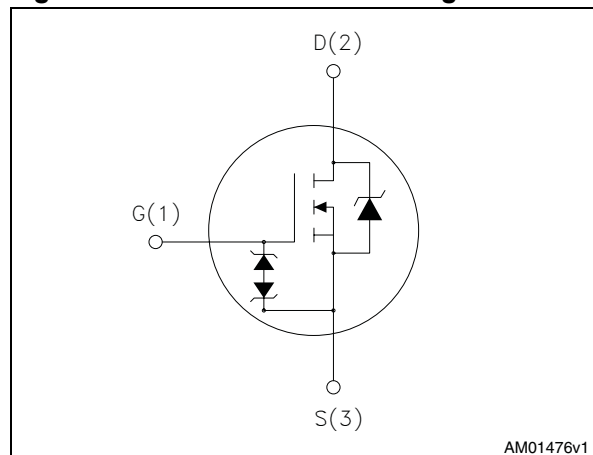


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB5NK52ZD-1	B5NK52ZD	I <sup>2</sup> PAK	Tube
STD5NK52ZD-1	D5NK52ZD	IPAK	Tube
STD5NK52ZD	D5NK52ZD	DPAK	Tape and reel
STF5NK52ZD	F5NK52ZD	TO-220FP	Tube
STP5NK52ZD	P5NK52ZD	TO-220	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		TO-220 I <sup>2</sup> PAK	I <sup>2</sup> PAK DPAK	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	520			V
V <sub>GS</sub>	Gate- source voltage	± 30			V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	4.4		4.4 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	2.7		2.7 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	17.6		17.6 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	70		25	W
	Derating factor	0.56		0.2	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5 kΩ)	2800			V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15			V/ns
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150			°C

1. Limited only by max temperature allowed
2. Pulse width limited by safe operating area
3. I<sub>SD</sub> ≤ 4.4 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> = 80% V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220 I <sup>2</sup> PAK	I <sup>2</sup> PAK DPAK	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.78		5	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5	100	62.5	°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300			°C

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> max)	4.4	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	170	mJ

## 2 Electrical characteristics

(T<sub>case</sub> = 25°C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	520			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	2.5	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.2 A		1.22	1.5	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.2 A		3.1		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		529 71 13.4		pF pF pF
C <sub>OSS eq</sub> <sup>(1)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 416 V		11		pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 416 V, I <sub>D</sub> = 4.4 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 19</a> )		16.9 4.2 8.4		nC nC nC

1. C<sub>OSS eq</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>OSS</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260\text{ V}$ , $I_D = 2.2\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> )		11.4		ns
$t_r$	Rise time			13.6		ns
$t_{d(off)}$	Turn-off-delay time			23.1		ns
$t_f$	Fall time			15		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				4.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				17.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.4\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 23</a> )		97.7		ns
$Q_{rr}$	Reverse recovery charge			300		nC
$I_{RRM}$	Reverse recovery current			5.9		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 23</a> )		139		ns
$Q_{rr}$	Reverse recovery charge			500		nC
$I_{RRM}$	Reverse recovery current			7.2		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 9. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / I<sup>2</sup>PAK

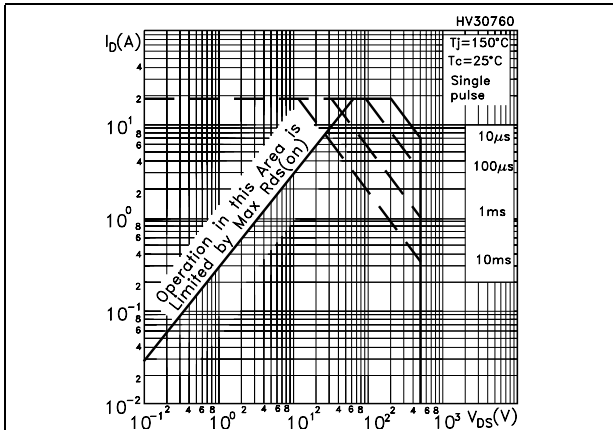


Figure 3. Thermal impedance for TO-220 / I<sup>2</sup>PAK

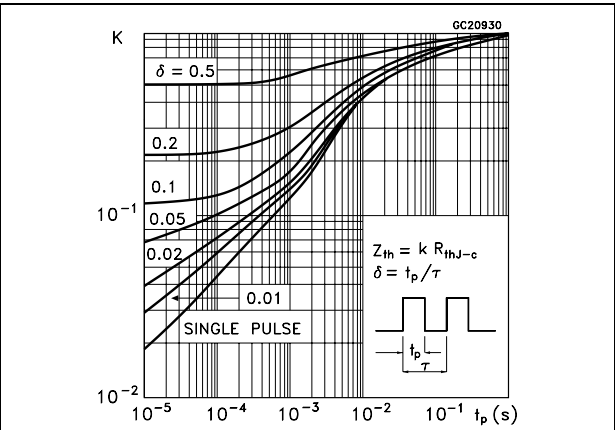


Figure 4. Safe operating area for TO-220FP

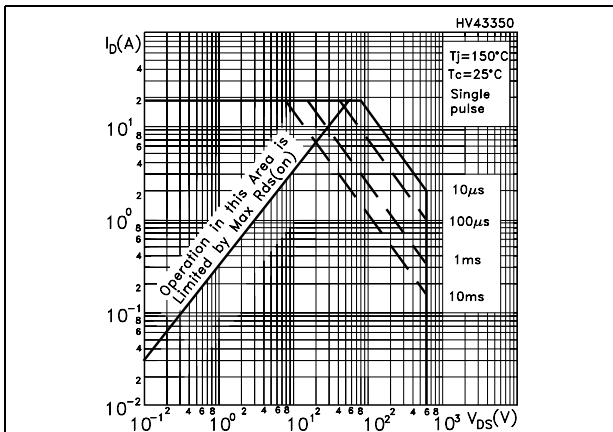


Figure 5. Thermal impedance for TO-220FP

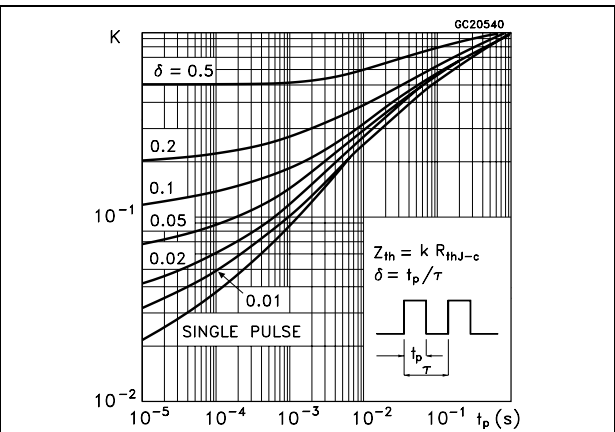


Figure 6. Safe operating area for IPAK/DPAK

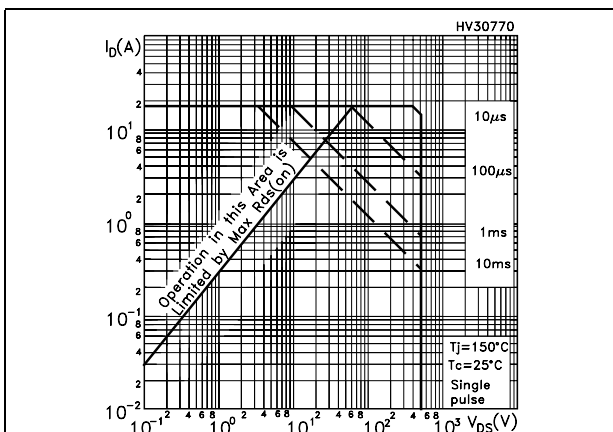


Figure 7. Thermal impedance for IPAK/DPAK

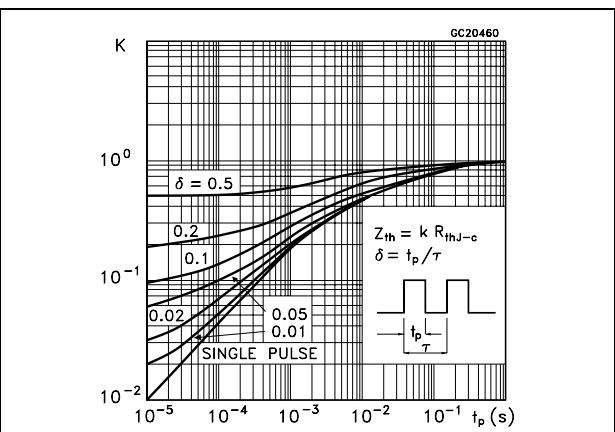


Figure 8. Output characteristics

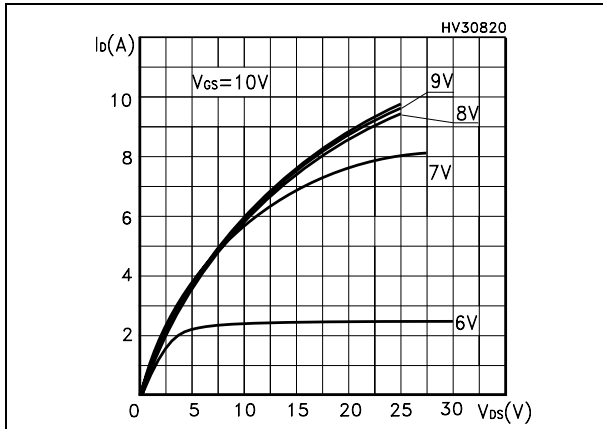


Figure 9. Transfer characteristics

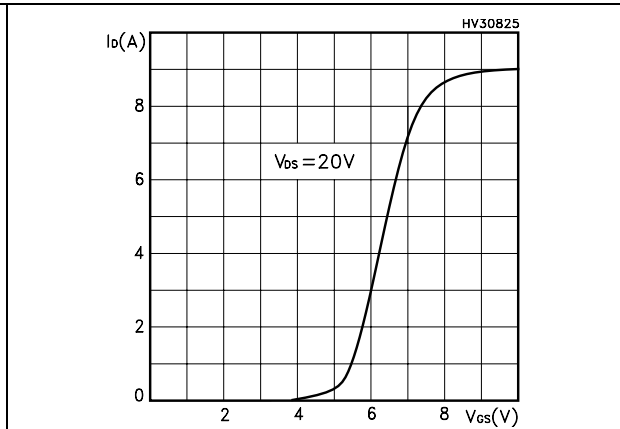


Figure 10. Normalized  $B_{V_{DS}}$  vs temperature

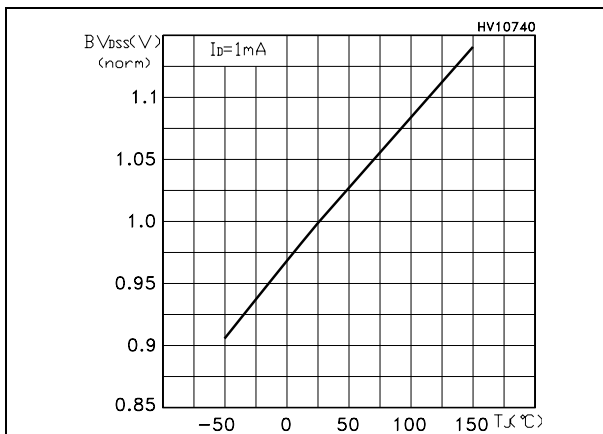


Figure 11. Static drain-source on resistance

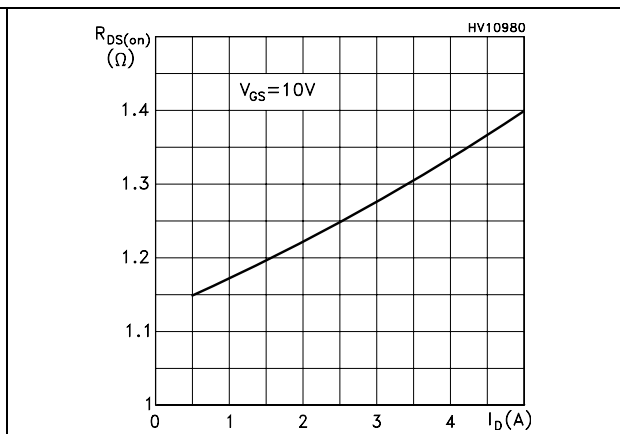


Figure 12. Gate charge vs gate-source voltage

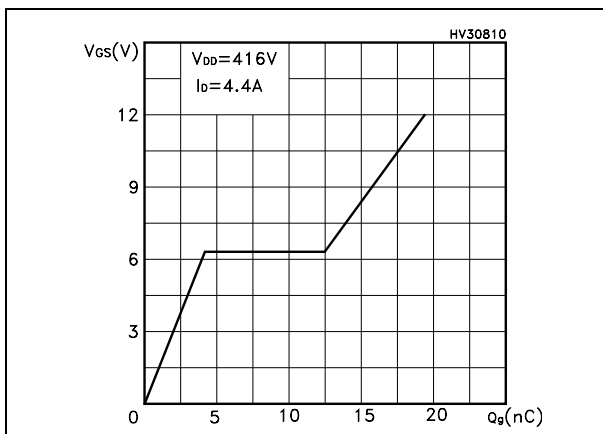


Figure 13. Capacitance variations

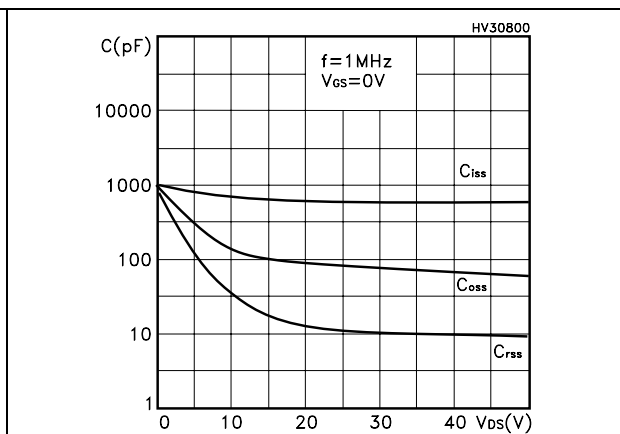


Figure 14. Normalized gate threshold voltage vs temperature

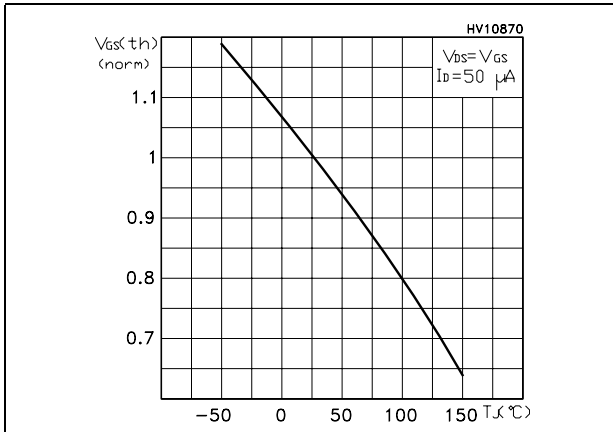


Figure 15. Normalized on resistance vs temperature

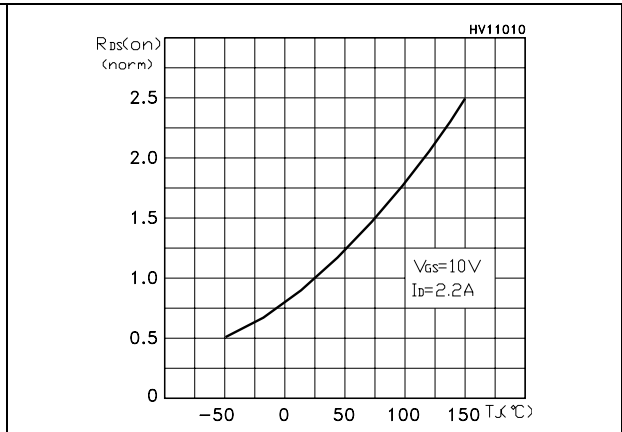


Figure 16. Source-drain diode forward characteristics

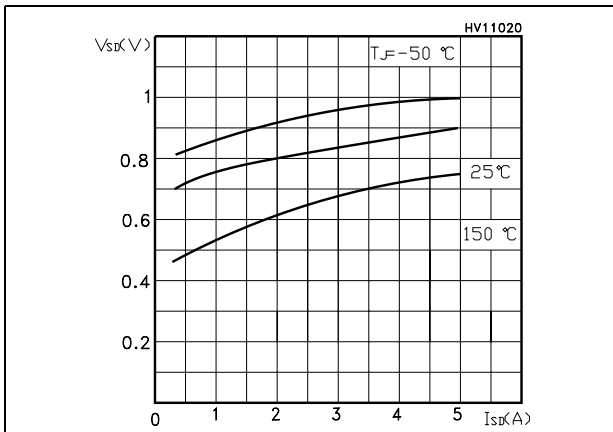
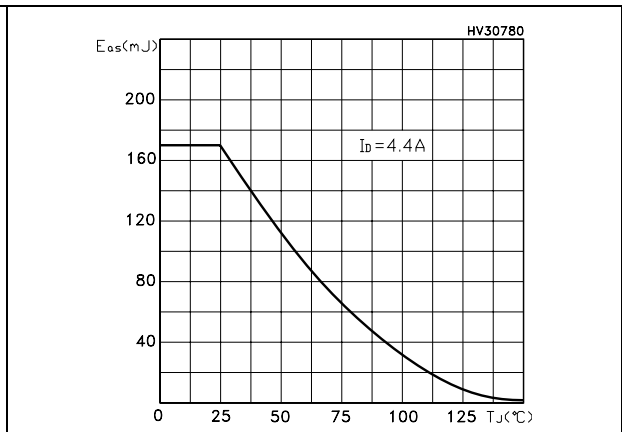


Figure 17. Maximum avalanche energy vs temperature



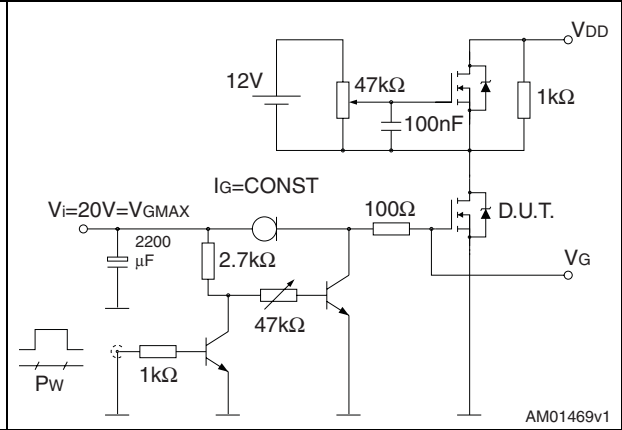


### 3 Test circuits

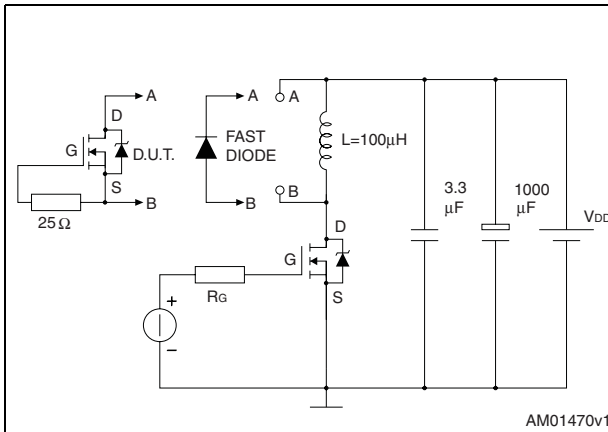
**Figure 18. Switching times test circuit for resistive load**



**Figure 19. Gate charge test circuit**



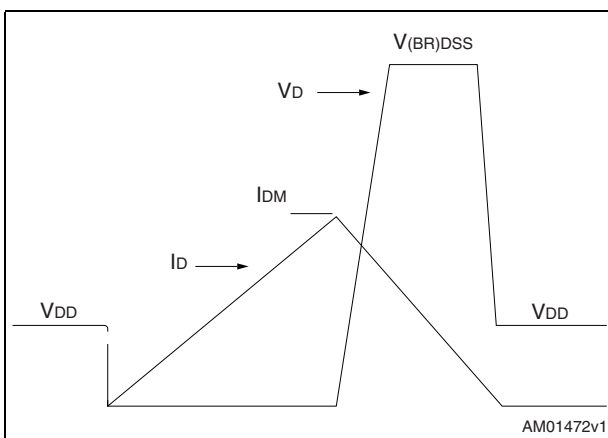
**Figure 20. Test circuit for inductive load switching and diode recovery times**



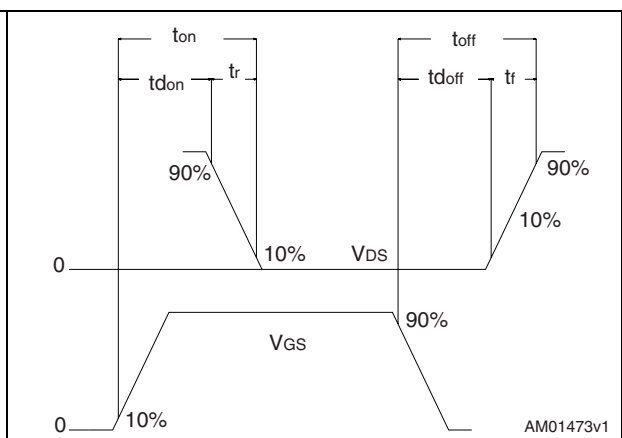
**Figure 21. Unclamped Inductive load test circuit**



**Figure 22. Unclamped inductive waveform**



**Figure 23. Switching time waveform**

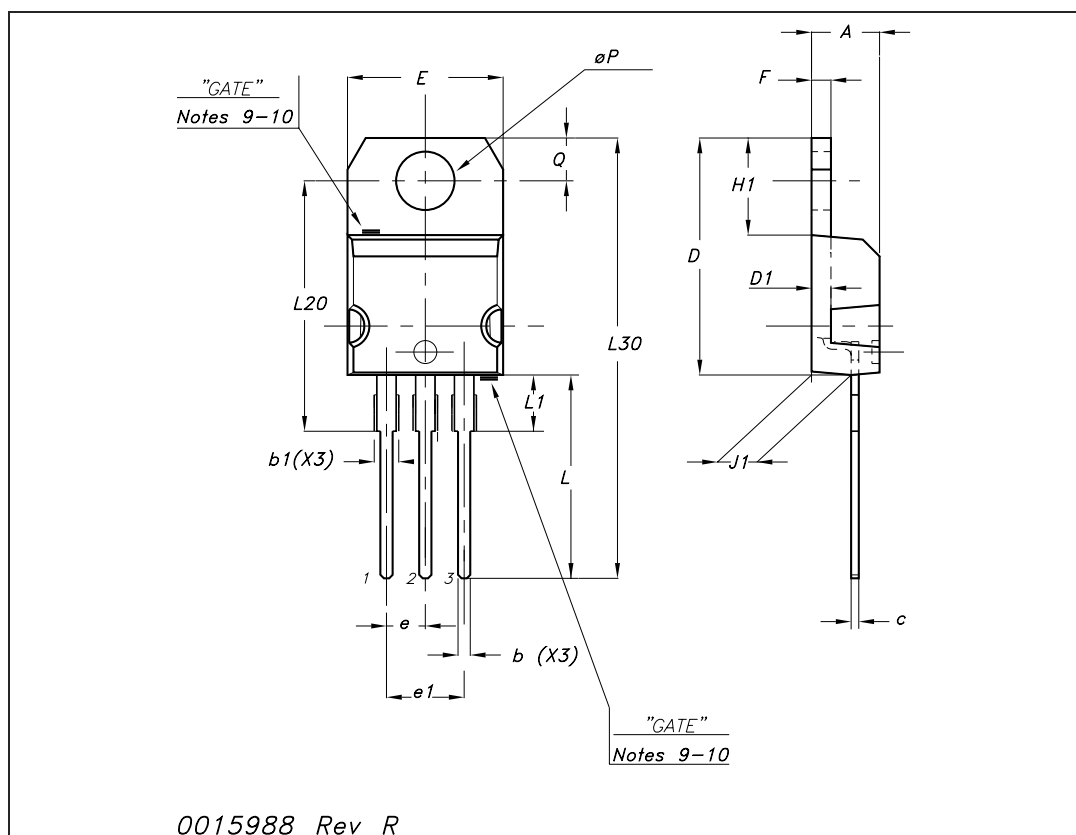


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

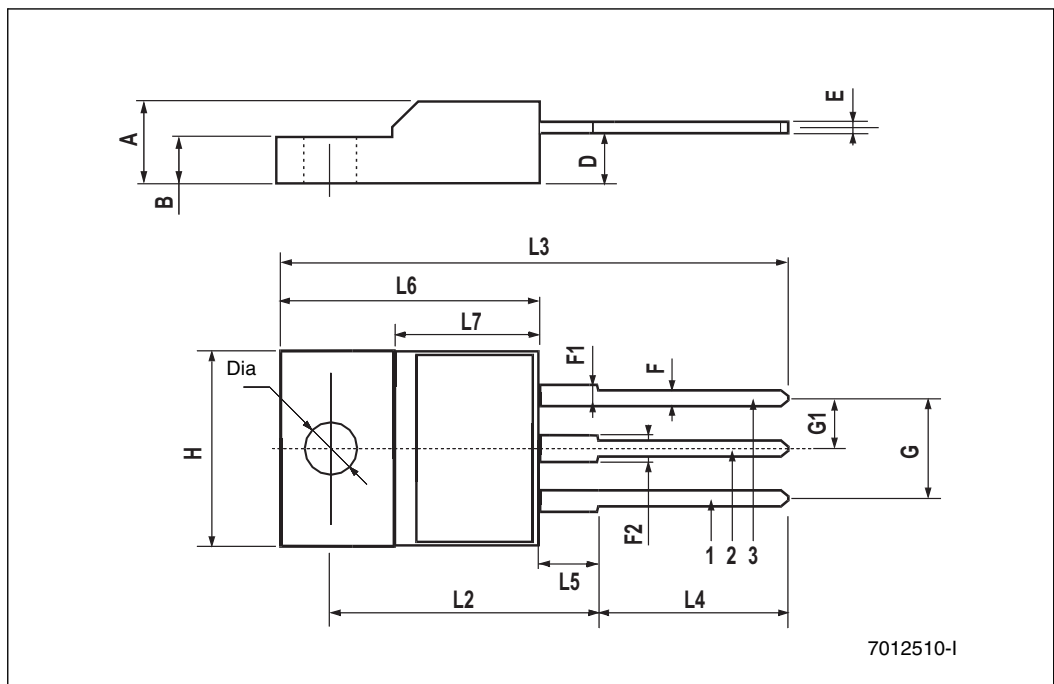
## TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



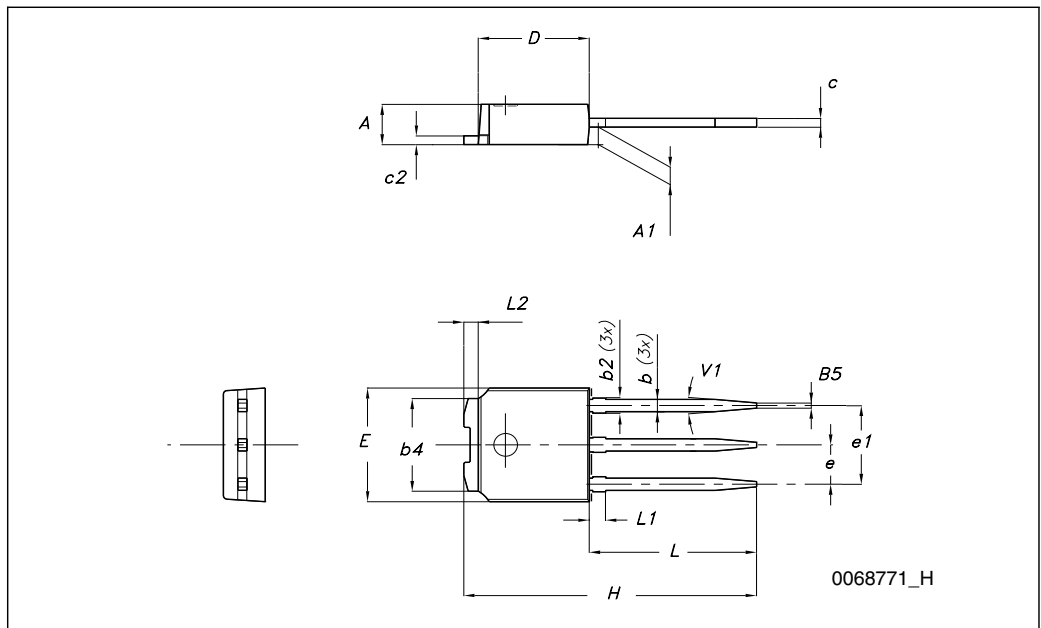
**TO-220FP mechanical data**

Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



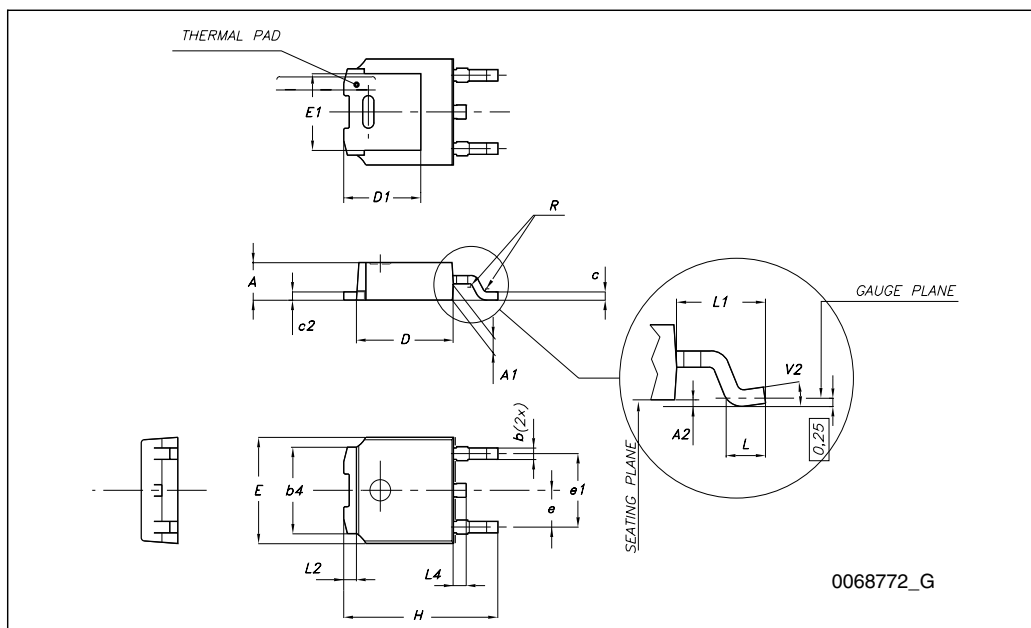
**TO-251 (IPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



**TO-252 (DPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

## 6 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
16-Jun-2005	1	First release
06-Sep-2005	2	Inserted ecopack indication
03-Oct-2005	3	Corrected value on <a href="#">Table 2</a>
23-Mar-2006	4	Complete version. New template
15-Sep-2008	5	Inserted new package: TO-220FP



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