

DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR NP110N055PUJ

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP110N055PUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

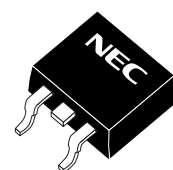
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP110N055PUJ-E1B-AY ^{Note}	Pure Sn (Tin)	Tape 1000 p/reel	TO-263 (MP-25ZP) typ. 1.5 g
NP110N055PUJ-E2B-AY ^{Note}			

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

- Super low on-state resistance
 $R_{DS(on)} = 2.4 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 55 \text{ A)}$
- Low input capacitance
 $C_{iss} = 9500 \text{ pF TYP.}$
- Designed for automotive application and AEC-Q101 qualified

(TO-263)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	55	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 110	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 440	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	288	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +175$	$^\circ\text{C}$
Single Avalanche Energy ^{Note2}	E_{AS}	435	mJ
Repetitive Avalanche Current ^{Note3}	I_{AR}	66	A
Repetitive Avalanche Energy ^{Note3}	E_{AR}	435	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 28 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

3. $T_{ch} \leq 150^\circ\text{C}$, $R_G = 25 \Omega$

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.52	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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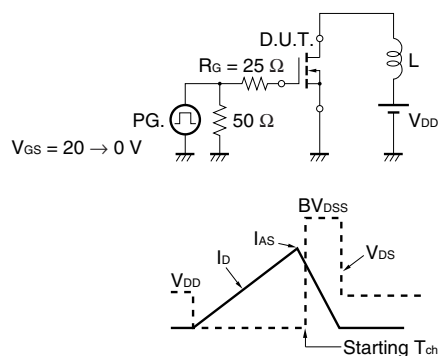
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

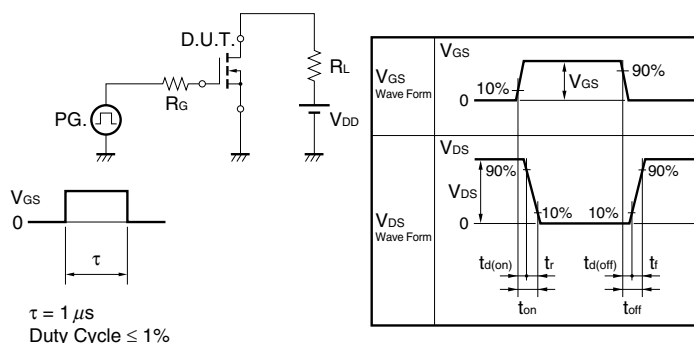
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 5 V, I _D = 55 A	55	117		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 55 A		1.9	2.4	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V,		9500	14250	pF
Output Capacitance	C _{oss}	f = 1 MHz		1060	1590	pF
Reverse Transfer Capacitance	C _{rss}			320	580	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 55 A, V _{GS} = 10 V,		45	100	ns
Rise Time	t _r	R _G = 0 Ω		20	50	ns
Turn-off Delay Time	t _{d(off)}			100	200	ns
Fall Time	t _f			10	30	ns
Total Gate Charge	Q _G	V _{DD} = 44 V, V _{GS} = 10 V,		150	230	nC
Gate to Source Charge	Q _{GS}	I _D = 110 A		35		nC
Gate to Drain Charge	Q _{GD}			45		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 110 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 110 A, V _{GS} = 0 V,		64		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		138		nC

Note Pulsed test

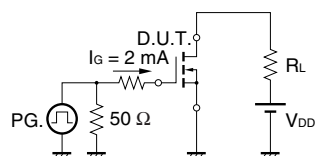
TEST CIRCUIT 1 AVALANCHE CAPABILITY



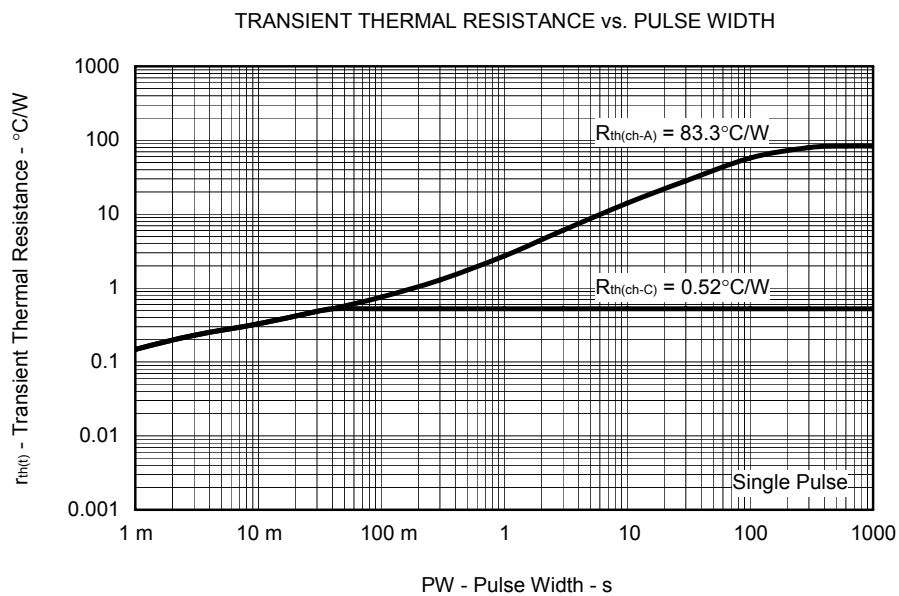
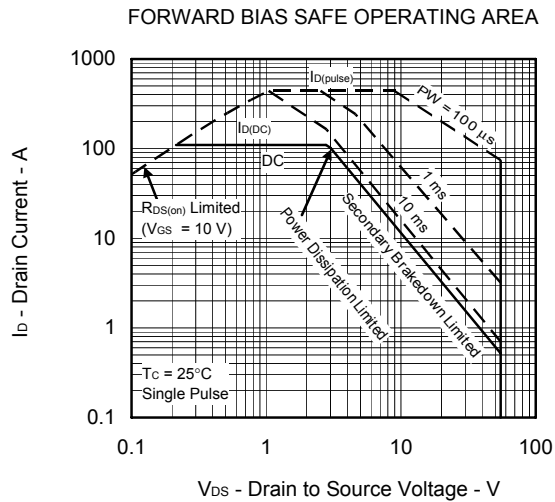
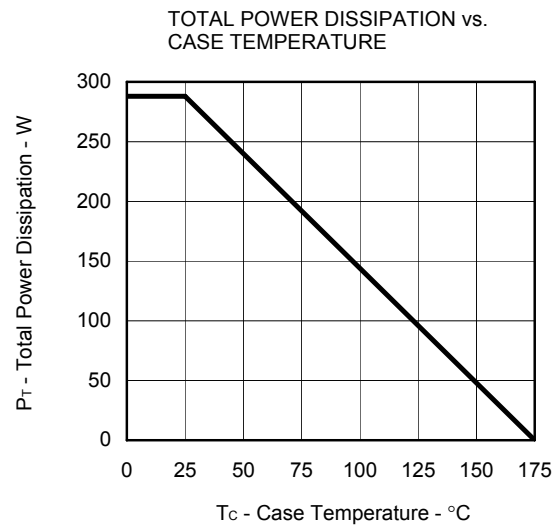
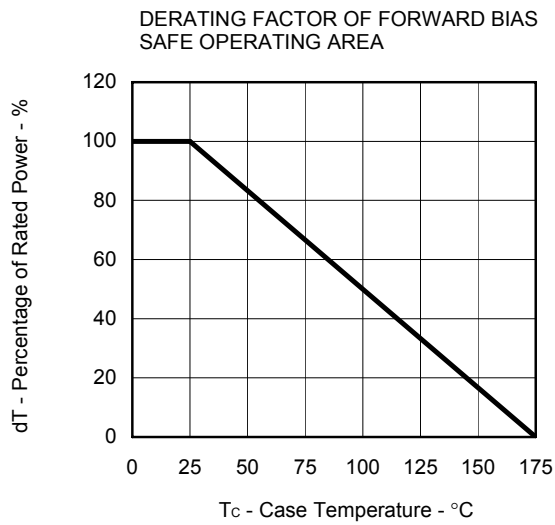
TEST CIRCUIT 2 SWITCHING TIME



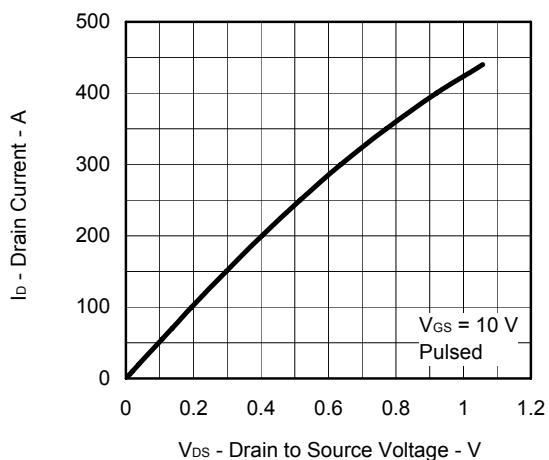
TEST CIRCUIT 3 GATE CHARGE



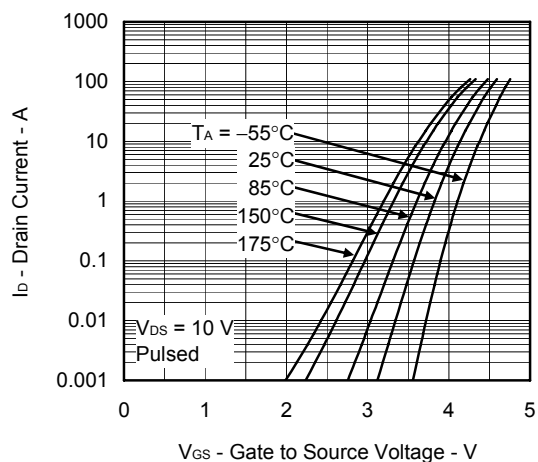
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



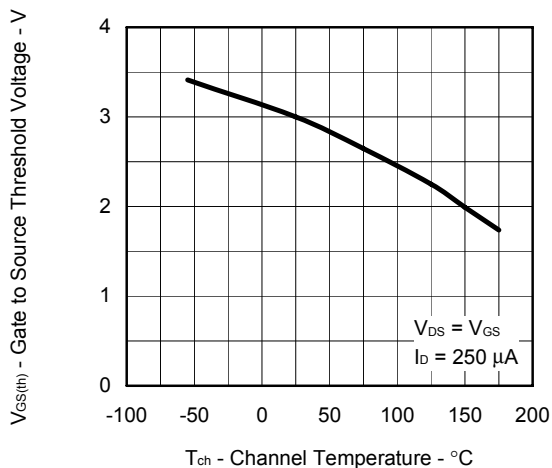
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



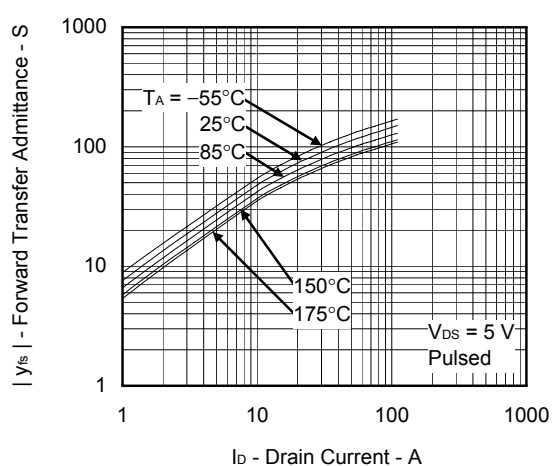
FORWARD TRANSFER CHARACTERISTICS



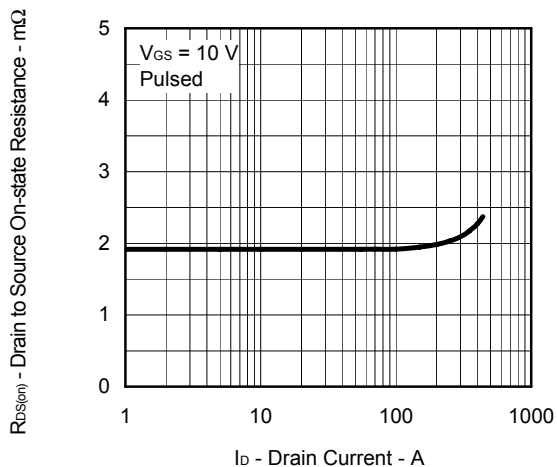
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



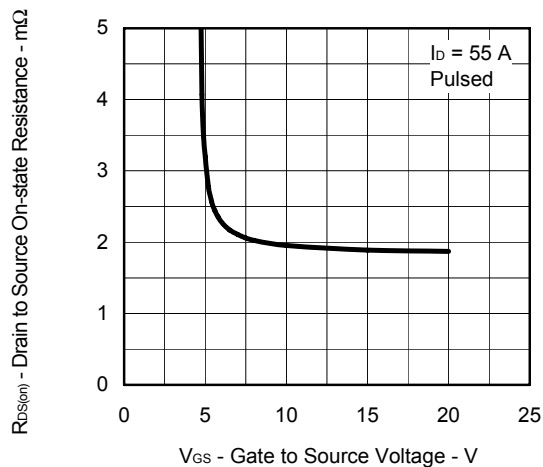
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



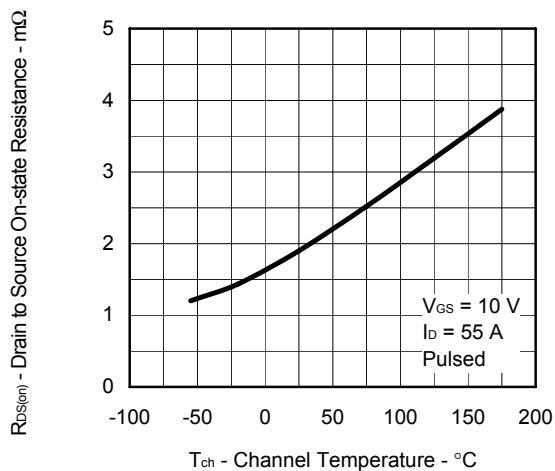
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



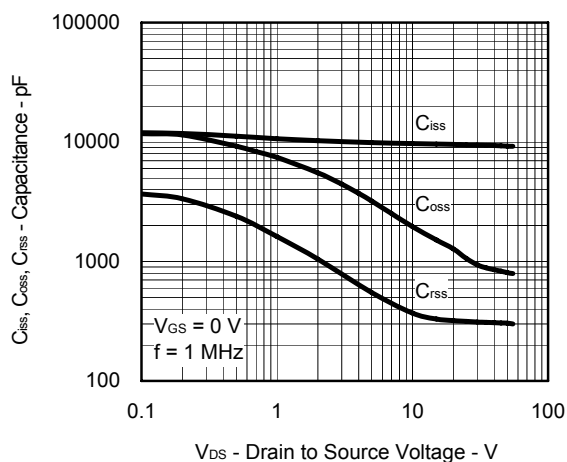
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



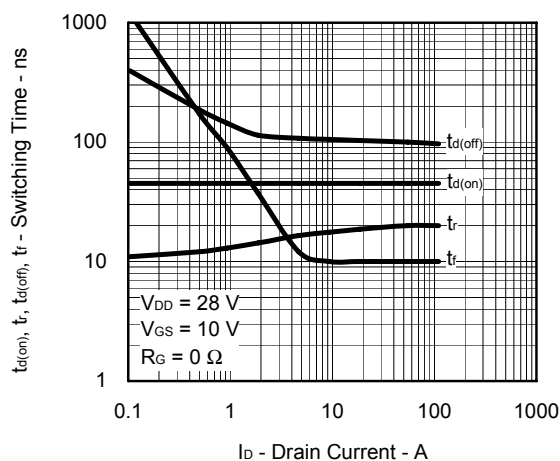
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



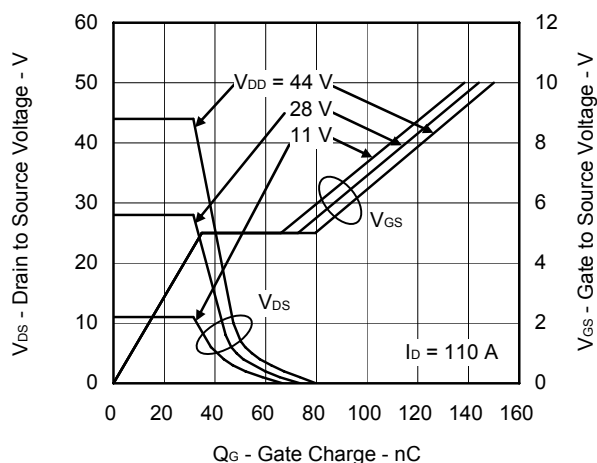
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



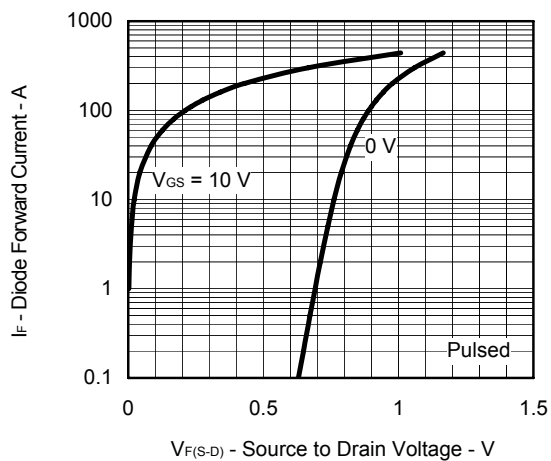
SWITCHING CHARACTERISTICS



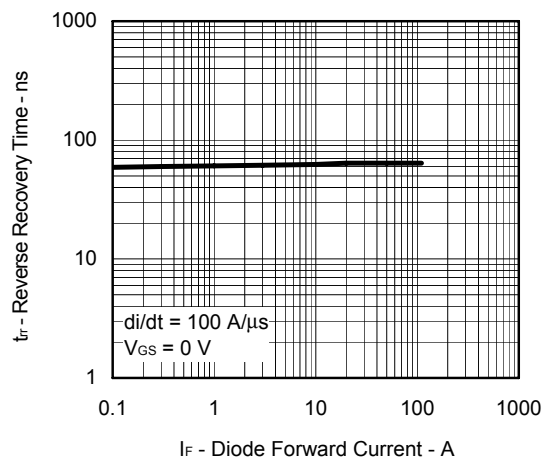
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

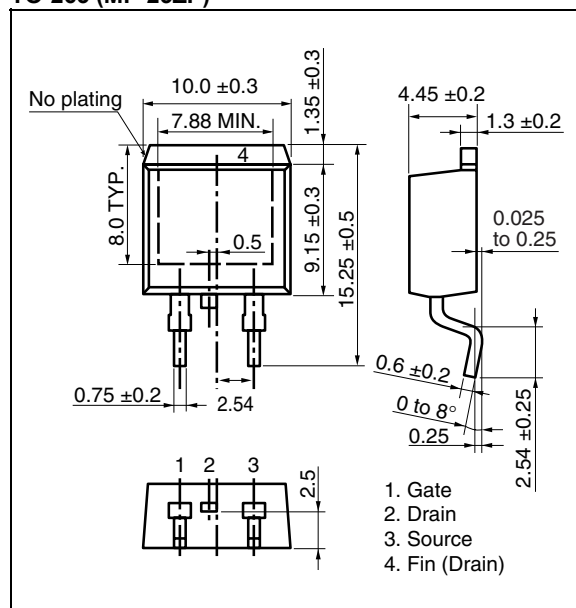


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

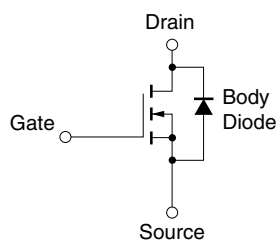


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



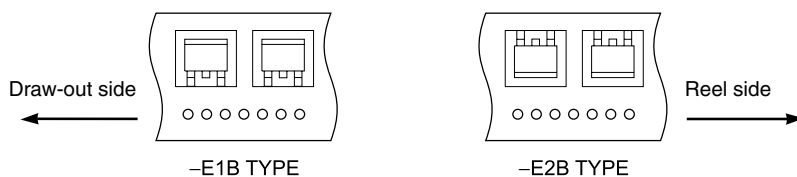
EQUIVALENT CIRCUIT



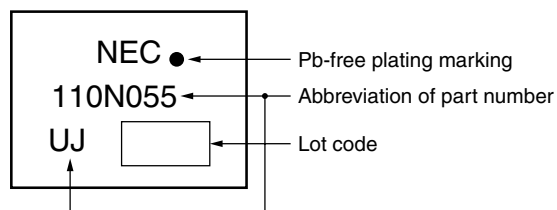
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

TAPE INFORMATION

There are two types (-E1B, -E2B) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP110N055PUJ should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

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