DDR2 VLP Registered SDRAM MODULE

240pin VLP Registered Module based on 512Mb E-die

72-bit ECC

60FBGA with Lead-Free

(RoHS compliant)

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Revision History

Revision	Month	Year	History
1.0	August	2008	- Initial Release

1.0 DDR2 Registered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Parity Register	Height
M392T6553EZA-CF7/E6/D5/CC	512MB	64Mx72	64Mx8(K4T51083QE)*9EA	1	O	18.30mm
M392T2953EZA-CF7/E6/D5/CC	1GB	128Mx72	64Mx8(K4T51083QE)*18EA	2	O	18.30mm
M392T2950EZA-CF7/E6/D5/CC	1GB	128Mx72	128Mx4(K4T51043QE)*18EA	1	O	18.30mm

Note :
1. “Z” of Part number(11th digit) stands for Lead-Free, and RoHS compliant products.
2. “3” of Part number(12th digit) stands for Dummy Pad PCB products.
3. “A” of Part number(12th digit) stands for Parity Register products.
4. “92” of Part number(3~4th digit) stands for VLP(Very Low Profile) Registered DIMM

2.0 Features

- Performance range

	F7(DDR2-800)	E6(DDR2-667)	D5(DDR2-533)	CC(DDR2-400)	Units
Speed@CL3	-	400	400	400	Mbps
Speed@CL4	533	533	533	400	Mbps
Speed@CL5	667	667	533	-	Mbps
Speed@CL6	800	-	-	-	Mbps
CL-tRCD-tRP	6-6-6	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard V_{DD} = 1.8V ± 0.1V Power Supply
- V_{DDQ} = 1.8V ± 0.1V
- 200 MHz f_{CK} for 400Mb/sec/pin, 267MHz f_{CK} for 533Mb/sec/pin, 333MHz f_{CK} for 667Mb/sec/pin, 400MHz f_{CK} for 800Mb/sec/pin
- 4 Banks
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1 , 2 , 3, 4 and 5
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/Nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
  - Support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA - 128Mx4/64Mx8
- All of products are Lead-Free and RoHS compliant

Note: For detailed DDR2 SDRAM operation, please refer to Samsung’s Device operation & Timing diagram.

3.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx4(512Mb) based Module	A0-A13	A0-A9,A11	BA0-BA1	A10
64Mx8(512Mb) based Module	A0-A13	A0-A9	BA0-BA1	A10

4.0 Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5/DQS14
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS5}$	212	NC/$\overline{DQS14}$
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0/DQS9	35	V_{SS}	155	DM3/DQS12	KEY				95	DQ42	215	DQ47
6	$\overline{DQS0}$	126	NC/$\overline{DQS9}$	36	$\overline{DQS3}$	156	NC/$\overline{DQS12}$	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK0}$	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC/Par_In	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	RFU
11	V_{SS}	131	DQ12	41	V_{SS}	161	CB4	70	A10/AP	190	BA1	101	SA2	221	RFU
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V_{DDQ}	102	NC(TEST)	222	V_{SS}
13	DQ9	133	V_{SS}	43	CB1	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6/DQS15
14	V_{SS}	134	DM1/DQS10	44	V_{SS}	164	DM8/DQS17	73	$\overline{WE}$	193	$\overline{S0}$	104	$\overline{DQS6}$	224	NC/$\overline{DQS15}$
15	$\overline{DQS1}$	135	NC/$\overline{DQS10}$	45	$\overline{DQS8}$	165	NC/$\overline{DQS17}$	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	DQS8	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	RFU	47	V_{SS}	167	CB6	76	$\overline{S1}$[4]	196	A13	107	DQ50	227	DQ55
18	$\overline{RESET}$	138	RFU	48	CB2	168	CB7	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	CB3	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1[4]	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7/DQS16
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DM4/DQS13	113	$\overline{DQS7}$	233	NC/$\overline{DQS16}$
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{DQS4}$	203	NC/$\overline{DQS13}$	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC/Err_Out	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2/DQS11	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS2}$	147	NC/$\overline{DQS11}$	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	V_{DDSPD}
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect, RFU = Reserved for Future Use
1. RESET (Pin 18) is connected to both OE of PLL and Reset of register.
2. The Test pin (Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)
3. NC/Err_Out (Pin 55) and NC/Par_In (Pin 68) are for optional function to check address and command parity.
4. CKE1,$\overline{S1}$ Pin is used for double side Registered DIMM.

5.0 Pin Description

Pin Name	Description	Pin Name	Description
CK0	Clock Inputs, positive line	ODT0~ODT1	On die termination
$\overline{CK0}$	Clock inputs, negative line	DQ0~DQ63	Data Input/Output
CKE0, CKE1	Clock Enables	CB0~CB7	Data check bits Input/Output
RAS	Row Address Strobe	DQS0~DQS8	Data strobes
CAS	Column Address Strobe	$\overline{DQS0}$~$\overline{DQS8}$	Data strobes, negative line
WE	Write Enable	DM(0~8),DQS(9~17)	Data Masks / Data strobes (Read)
$\overline{S0}$, $\overline{S1}$	Chip Selects	$\overline{DQS9}$~$\overline{DQS17}$	Data strobes (Read), negative line
A0~A9, A11~A13	Address Inputs	RFU	Reserved for Future Use
A10/AP	Address Input/Autoprecharge	NC	No Connect
BA0, BA1	DDR2 SDRAM Bank Address	TEST	Memory bus test tool (Not Connect and Not Useable on DIMMs)
SCL	Serial Presence Detect (SPD) Clock Input	V_{DD}	Core Power
SDA	SPD Data Input/Output	V_{DDQ}	I/O Power
SA0~SA2	SPD address	V_{SS}	Ground
Par_In	Parity bit for the Address and Control bus	V_{REF}	Input/Output Reference
Err_Out	Parity error found in the Address and Control bus	V_{DDSPD}	SPD Power
RESET	Register and PLL control pin		

*The V_{DD} and V_{DDQ} pins are tied to the single power-plane on PCB.

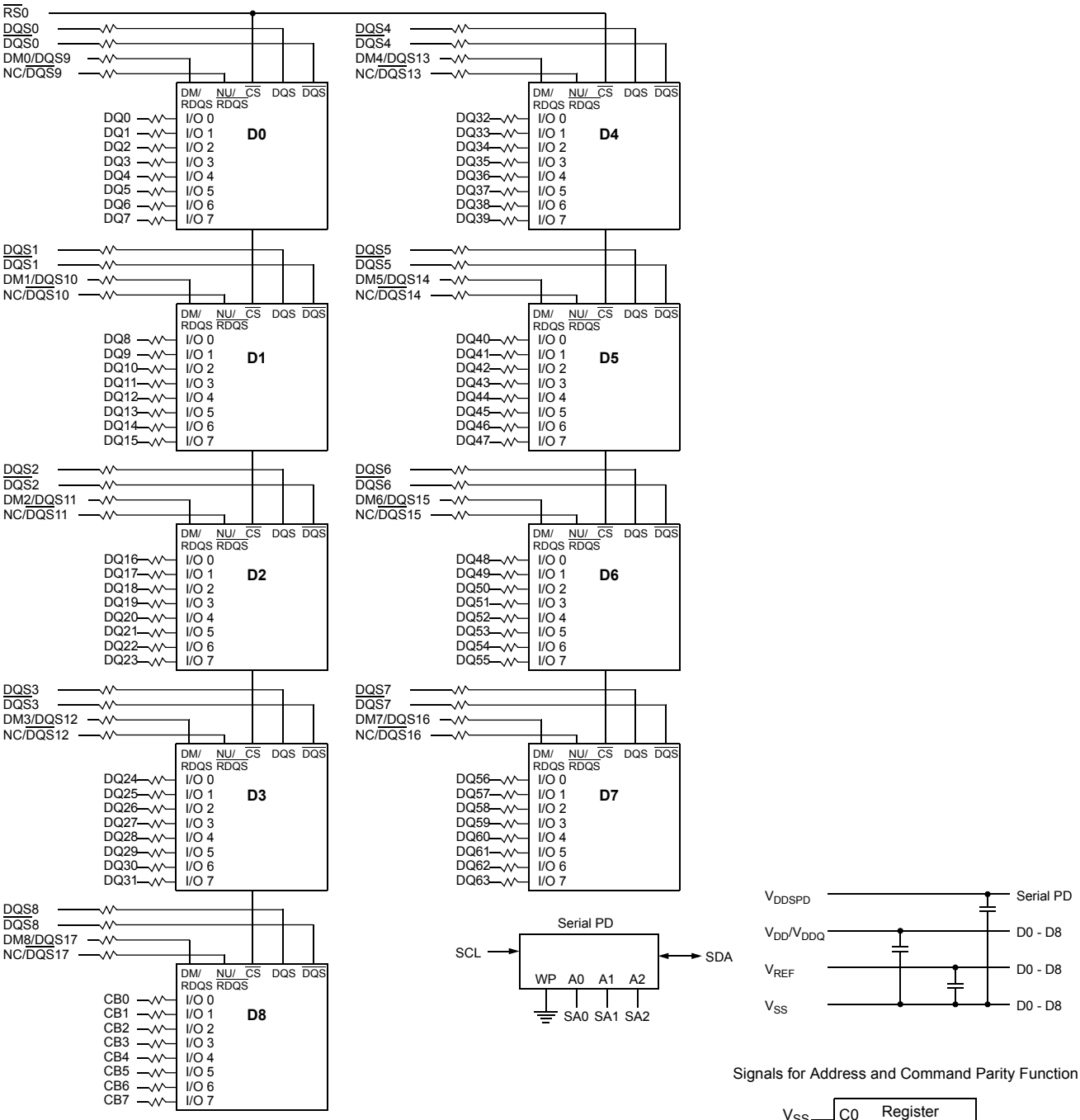
6.0 Input/Output Functional Description

Symbol	Type	Function
CK0	Input	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	Input	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0~CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}0$~$\overline{S}1$	Input	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high.
ODT0~ODT1	Input	I/O bus impedance control signals.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply	Reference voltage for SSTL_18 inputs
V_{DDQ}	Supply	Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0~BA1	Input	Selects which SDRAM bank of four is activated.
A0~A9,A10/AP A11~A13	Input	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be pre-charged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0~63, CB0~CB7	In/Out	Data and Check Bit Input/Output pins
DM0~DM8	Input	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V_{DD}, V_{SS}	Supply	Power and ground for the DDR SDRAM input buffers and core logic
DQS0~DQS17	In/Out	Positive line of the differential data strobe for input and output data.
$\overline{DQS0}$~$\overline{DQS17}$	In/Out	Negative line of the differential data strobe for input and output data.
SA0~SA2	Input	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} to act as a pullup.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pullup.
V_{DDSPD}	Supply	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt operation).
$\overline{RESET}$	Input	The $\overline{RESET}$ pin is connected to the $\overline{RST}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (The PLL will remain synchro-nized with the input clock)
Par_In	Input	Parity bit for the Address and Control bus. (“1 “ : Odd, “0 “ : Even)
$\overline{Err\_Out}$	Input	Parity error found in the Address and Control bus
TEST	In/Out	Used by memory bus analysis tools (unused on memory DIMMs)

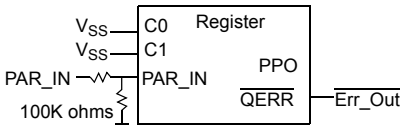
7.0 Functional Block Diagram

7.1 512MB, 64Mx72 Module - M392T6553EZA

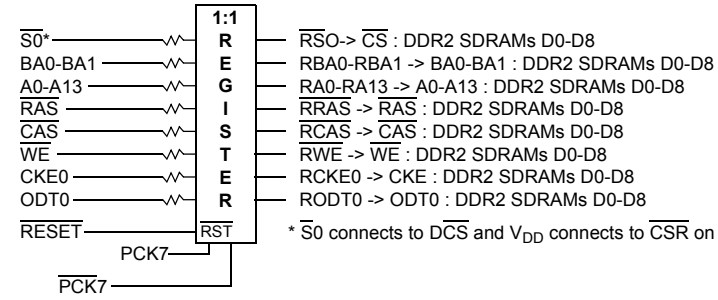
(populated as 1 rank of x8 DDR2 SDRAMs)



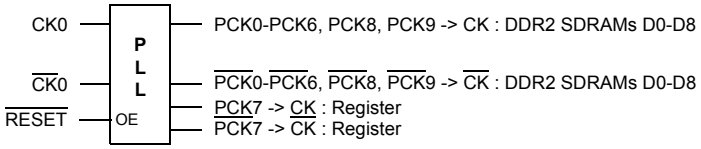
Signals for Address and Command Parity Function



The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"



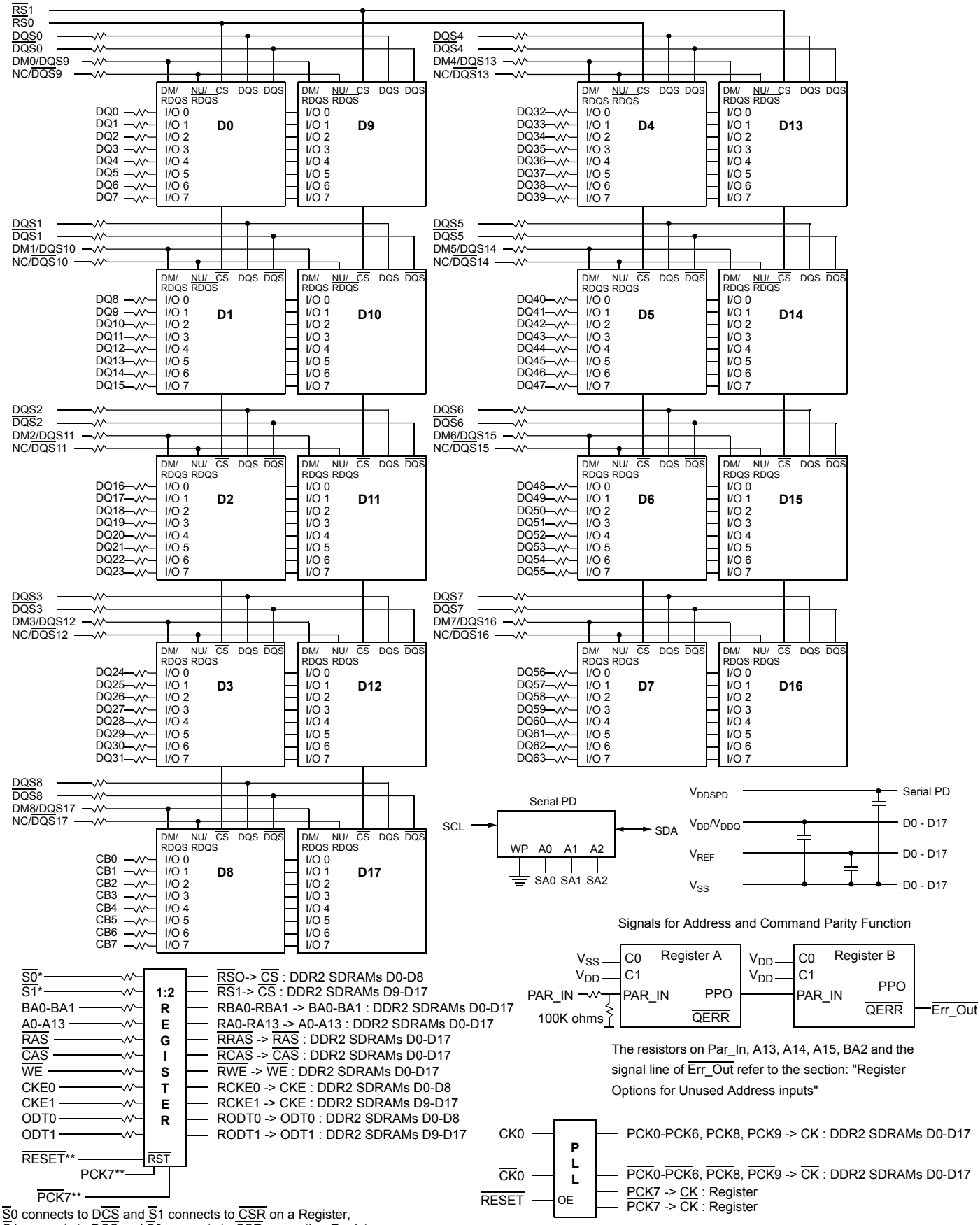
* S0 connects to DCS and V_{DD} connects to CSR on the register. S1, CKE1 and ODT1 are NC.



Note :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. Unless otherwise noted, resister values are 22 Ohms ± 5%

7.2 1GB, 128Mx72 Module - M392T2953EZA

(populated as 2 rank of x8 DDR2 SDRAMs)



The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"

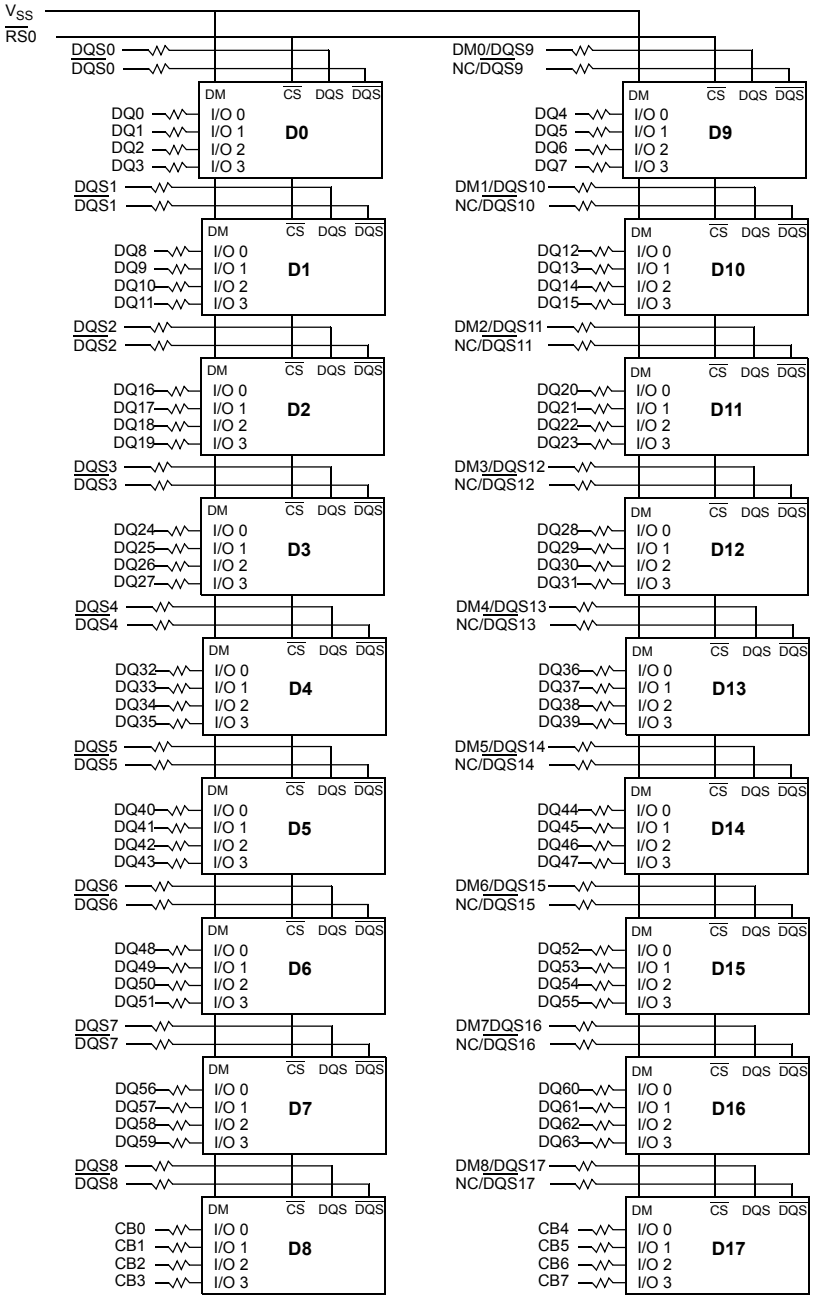
* S0 connects to DCS and S1 connects to CSR on a Register,
S1 connects to DCS and S0 connects to CSR on another Register.

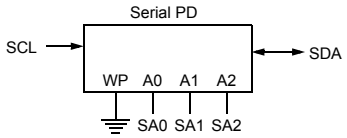
** RESET, PCK7 and PCK7 connects to both Registers.
Other signals connect to one of two Registers.

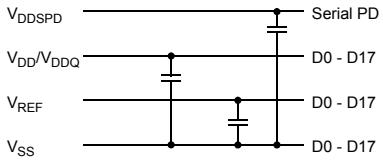
Note :
1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resister values are 22 Ohms ± 5%
3. RS0 and RS1 alternate between the back and front sides of the DIMM

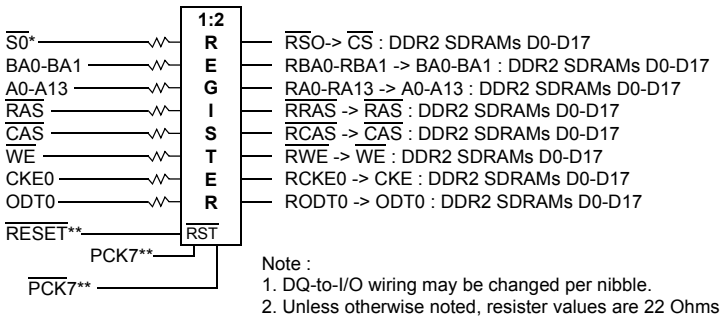
7.3 1GB, 128Mx72 Module - M392T2950EZA

(populated as 1 rank of x4 DDR2 SDRAMs)







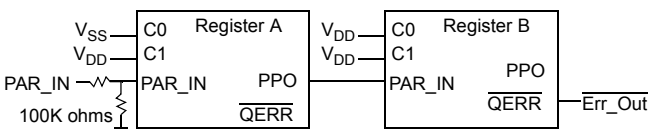


Note :
1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resister values are 22 Ohms ± 5%

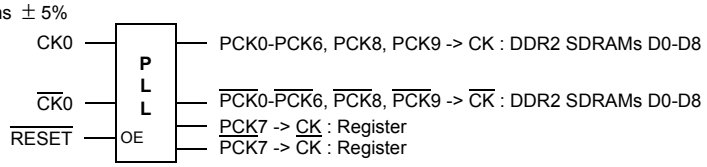
* S0 connects to DCS of Register1 and CSR of Register2. CSR of register 1 and DCS of register 2 connects to V_{DD}.

** RESET, PCK7 and PCK7 connects to both Registers. Other signals connect to one of two Registers. S1, CKE1 and ODT1 are NC.

Signals for Address and Command Parity Function



The resistors on Par_In, A13, A14, A15, BA2 and the signal line of Err_Out refer to the section: "Register Options for Unused Address inputs"



8.0 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	- 1.0 V ~ 2.3 V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

9.0 AC & DC Operating Conditions

9.1 Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Note : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.
1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

9.2 Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 95	°C	1, 2

Note :
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

9.3 Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(DC)	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL}(DC)	DC input logic low	- 0.3	V_{REF} - 0.125	V	

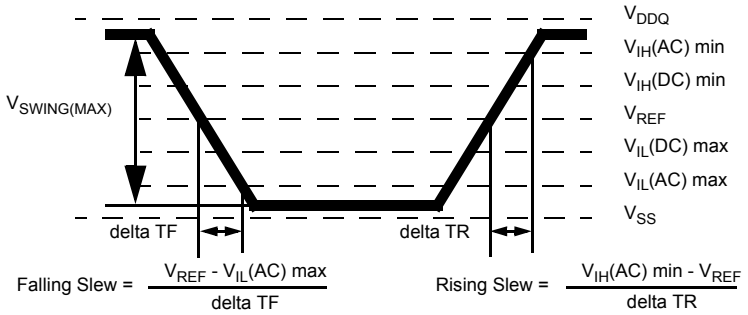
9.4 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units
		Min.	Max.	Min.	Max.	
V_{IH}(AC)	AC input logic high	V_{REF} + 0.250	-	V_{REF} + 0.200		V
V_{IL}(AC)	AC input logic low	-	V_{REF} - 0.250		V_{REF} - 0.200	V

9.5 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Note :
1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.



< AC Input Test Signal Waveform >

10.0 IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions		Units	Note
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current;** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2N	**Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD3P	**Active power-down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA	
		Slow PDN Exit MRS(12) = 1mA	mA	
IDD3N	**Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst auto refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current;** CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA	
		Low Power	mA	
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		mA	

11.0 Operating Current Table :

11.1 M392T6553EZA : 512MB(64Mx8 *9) Module

(T_A=0°C, V_{DD}= 1.9V)

Symbol	F7(800@CL=6)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Units	Notes
IDD0	765	675	675	630	mA	
IDD1	855	810	765	765	mA	
IDD2P	72	72	72	72	mA	
IDD2Q	315	315	270	270	mA	
IDD2N	360	360	315	315	mA	
IDD3P-F	270	270	270	270	mA	
IDD3P-S	108	108	108	108	mA	
IDD3N	540	495	450	450	mA	
IDD4W	1,035	945	810	765	mA	
IDD4R	1,305	1,215	990	900	mA	
IDD5B	1,035	990	990	945	mA	
IDD6*	72	72	72	72	mA	
IDD7	1,935	1,620	1,620	1,620	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.2 M392T6553EZA : 512MB(64Mx8 *9) Module

- considering Register and PLL current value

(T_A=0°C, V_{DD}= 1.9V)

Symbol	F7(800@CL=6)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Units	Notes
IDD0	1,355	1,175	1,085	950	mA	
IDD1	1,495	1,360	1,225	1,135	mA	
IDD2P	552	512	472	432	mA	
IDD2Q	845	775	660	590	mA	
IDD2N	840	780	675	615	mA	
IDD3P-F	820	740	660	580	mA	
IDD3P-S	658	578	498	418	mA	
IDD3N	1,080	965	850	780	mA	
IDD4W	1,555	1,395	1,190	1,075	mA	
IDD4R	1,895	1,725	1,420	1,250	mA	
IDD5B	1,705	1,540	1,420	1,255	mA	
IDD6*	72	72	72	72	mA	
IDD7	2,625	2,200	2,090	1,980	mA	

* IDD6 = DRAM current + standby current of PLL and Register
** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.3 M392T2953EZA : 1GB(64Mx8 *18) Module

(T_A=0ºC, V_{DD}= 1.9V)

Symbol	F7(800@CL=6)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Units	Notes
IDD0	1,125	1,035	990	945	mA	
IDD1	1,215	1,170	1,080	1,080	mA	
IDD2P	144	144	144	144	mA	
IDD2Q	630	630	540	540	mA	
IDD2N	720	720	630	630	mA	
IDD3P-F	540	540	540	540	mA	
IDD3P-S	216	216	216	216	mA	
IDD3N	900	855	765	765	mA	
IDD4W	1,395	1,305	1,125	1,080	mA	
IDD4R	1,665	1,575	1,305	1,215	mA	
IDD5B	1,395	1,350	1,305	1,260	mA	
IDD6*	144	144	144	144	mA	
IDD7	2,295	1,980	1,935	1,935	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.4 M392T2953EZA : 1GB(64Mx8 *18) Module

- considering Register and PLL current value

(T_A=0ºC, V_{DD}= 1.9V)

Symbol	F7(800@CL=6)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Units	Notes
IDD0	1,815	1,625	1,480	1,335	mA	
IDD1	1,985	1,830	1,630	1,520	mA	
IDD2P	784	724	664	604	mA	
IDD2Q	1,340	1,250	1,070	980	mA	
IDD2N	1,290	1,220	1,060	990	mA	
IDD3P-F	1,270	1,170	1,070	970	mA	
IDD3P-S	946	846	746	646	mA	
IDD3N	1,460	1,345	1,185	1,115	mA	
IDD4W	2,045	1,865	1,595	1,460	mA	
IDD4R	2,455	2,255	1,875	1,675	mA	
IDD5B	2,225	2,030	1,835	1,640	mA	
IDD6*	144	144	144	144	mA	
IDD7	3,325	2,850	2,645	2,485	mA	

* IDD6 = DRAM current + standby current of PLL and Register
** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.5 M392T2950EZA : 1GB(128Mx4 *18) Module

(T_A=0°C, V_{DD}= 1.9V)

Symbol	F7(800@CL=6)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Units	Notes
IDD0	1,530	1,350	1,350	1,260	mA	
IDD1	1,710	1,530	1,530	1,530	mA	
IDD2P	144	144	144	144	mA	
IDD2Q	630	630	540	540	mA	
IDD2N	720	720	630	630	mA	
IDD3P-F	540	540	540	540	mA	
IDD3P-S	216	216	216	216	mA	
IDD3N	990	990	900	900	mA	
IDD4W	2,160	1,890	1,620	1,440	mA	
IDD4R	2,340	2,070	1,800	1,620	mA	
IDD5B	2,070	1,980	1,890	1,890	mA	
IDD6*	144	144	144	144	mA	
IDD7	3,870	3,240	3,240	3,240	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.6 M392T2950EZA : 1GB(128Mx4 *18) Module

- considering Register and PLL current value

(T_A=0°C, V_{DD}= 1.9V)

Symbol	F7(800@CL=6)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Units	Notes
IDD0	2,220	1,940	1,840	1,650	mA	
IDD1	2,480	2,190	2,080	1,970	mA	
IDD2P	784	724	664	604	mA	
IDD2Q	1,340	1,250	1,070	980	mA	
IDD2N	1,290	1,220	1,060	990	mA	
IDD3P-F	1,270	1,170	1,070	970	mA	
IDD3P-S	946	846	746	646	mA	
IDD3N	1,550	1,480	1,320	1,250	mA	
IDD4W	2,810	2,450	2,090	1,820	mA	
IDD4R	3,130	2,750	2,370	2,080	mA	
IDD5B	2,900	2,660	2,420	2,270	mA	
IDD6*	144	144	144	144	mA	
IDD7	4,900	4,110	3,950	3,790	mA	

* IDD6 = DRAM current + standby current of PLL and Register
** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

12.0 Input/Output Capacitance

(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A=25°C)

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Part-Number		M392T6553EZA		M392T2953EZA		M392T2950EZA		
Input capacitance, CK and $\overline{CK}$	CCK	-	11	-	11	-	11	pF
Input capacitance, CKE and $\overline{CS}$	CI1	-	12	-	12	-	12	
Input capacitance, Address, $\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$	CI2	-	12	-	12	-	12	
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	-	10	-	10	-	10	

* DM is internally loaded to match DQ and DQS identically.

13.0 Electrical Characteristics & AC Timing for DDR2-800/667/533/400

(0 °C ≤ T_{OPER} ≤ 95 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

13.1 Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

13.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR2-800(F7)		DDR2-667(E6)		DDR2-533(D5)		DDR2-400(CC)		Units
Bin(CL - tRCD - tRP)	6 - 6 - 6		5 - 5 - 5		4 - 4 - 4		3 - 3 - 3		
Parameter	min	max	min	max	min	max	min	max	
tCK, CL=3	-	-	5	8	5	8	5	8	ns
tCK, CL=4	3.75	8	3.75	8	3.75	8	5	8	ns
tCK, CL=5	3	8	3	8	3.75	8	-	-	ns
tCK, CL=6	2.5	8	-	-	-	-	-	-	ns
tRCD	15	-	15	-	15	-	15	-	ns
tRP	15	-	15	-	15	-	15	-	ns
tRC	60	-	60	-	60	-	55	-	ns
tRAS	45	70000	45	70000	45	70000	40	70000	ns

13.3 Timing parameters by speed grade (DDR2-800 and DDR2-667)

(Refer to notes for informations related to this table at the component datasheet)

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-400	400	-450	450	ps	40
DQS output access time from CK/$\overline{CK}$	tDQSCK	-350	350	-400	400	ps	40
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
CK half pulse period	tHP	Min(tCL(abs), tCH(abs))	x	Min(tCL(abs), tCH(abs))	x	ps	37
Average clock period	tCK(avg)	2500	8000	3000	8000	ps	35,36
DQ and DM input hold time	tDH(base)	125	x	175	x	ps	6,7,8,21,28,31
DQ and DM input setup time	tDS(base)	50	x	100	x	ps	6,7,8,20,28,31
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK(avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK(avg)	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC(max)	x	tAC(max)	ps	18,40
DQS/$\overline{DQS}$ low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC(min)	tAC(max)	tAC(min)	tAC(max)	ps	18,40
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC(min)	tAC(max)	2* tAC(min)	tAC(max)	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	ps	13
DQ hold skew factor	tQHS	x	300	x	340	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	39
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	-0.25	0.25	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30
Mode register set command cycle time	tMRD	2	x	2	x	nCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Write preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	
Address and control input hold time	tIH(base)	250	x	275	x	ps	5,7,9,23,29
Address and control input setup time	tIS(base)	175	x	200	x	ps	5,7,9,22,29
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4,32
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4,32

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	35	x	37.5	x	ns	32
Four Activate Window for 2KB page size products	tFAW	45	x	50	x	ns	32
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	x	2	x	nCK	
Write recovery time	tWR	15	x	15	x	ns	32
Auto precharge write recovery + precharge time	tDAL	WR + tnRP	x	WR + tnRP	x	nCK	33
Internal write to read command delay	tWTR	7.5	x	7.5	x	ns	24,32
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3,32
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	32
Exit self refresh to a read command	tXSRD	200	x	200	x	nCK	
Exit precharge power down to any command	tXP	2	x	2	x	nCK	
Exit active power down to read command	tXARD	2	x	2	x	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL	x	7 - AL	x	nCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	nCK	27
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2*tCK(avg) +tAC(max)+1	tAC(min)+2	2*tCK(avg) +tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5*tCK(avg)+ tAC(max)+1	tAC(min)+2	2.5*tCK(avg)+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	nCK	
ODT power down exit latency	tAXPD	8	x	8	x	nCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(avg) +tIH	x	tIS+tCK(avg) +tIH	x	ns	15

13.4 Timing parameters by speed grade (DDR2-533 and DDR2-400)

(Refer to notes for informations related to this table at the component datasheet)

Parameter	Symbol	DDR2-533		DDR2-400		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-500	500	-600	600	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-450	450	-500	500	ps	
CK HIGH pulse width	tCH	0.45	0.55	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half pulse period	tHP	Min(tCL, tCH)	x	Min(tCL, tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	3750	8000	5000	8000	ps	15
DQ and DM input hold time (differential strobe)	tDH(base)	225	x	275	x	ps	6,7,8,21,28
DQ and DM input setup time (differential strobe)	tDS(base)	100	x	150	x	ps	6,7,8,20,28
DQ and DM input hold time (single-ended strobe)	tDH1(base)	-25	x	25	x	ps	6,7,8,26
DQ and DM input setup time (single-ended strobe)	tDS1(base)	-25	x	25	x	ps	6,7,8,25
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC(max)	x14	tAC(max)	ps	18
DQS(/$\overline{DQS}$) low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC(min)	tAC(max)	tAC(min)	tAC(max)	ps	18
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC(min)	tAC(max)	2* tAC(min)	tAC(max)	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	300	x	350	ps	13
DQ hold skew factor	tQHS	x	400	x	450	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK	
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.35	x	0.35	x	tCK	
Address and control input hold time	tIH(base)	375	x	475	x	ps	5,7,9,23
Address and control input setup time	tIS(base)	250	x	350	x	ps	5,7,9,22
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	10	x	ns	4

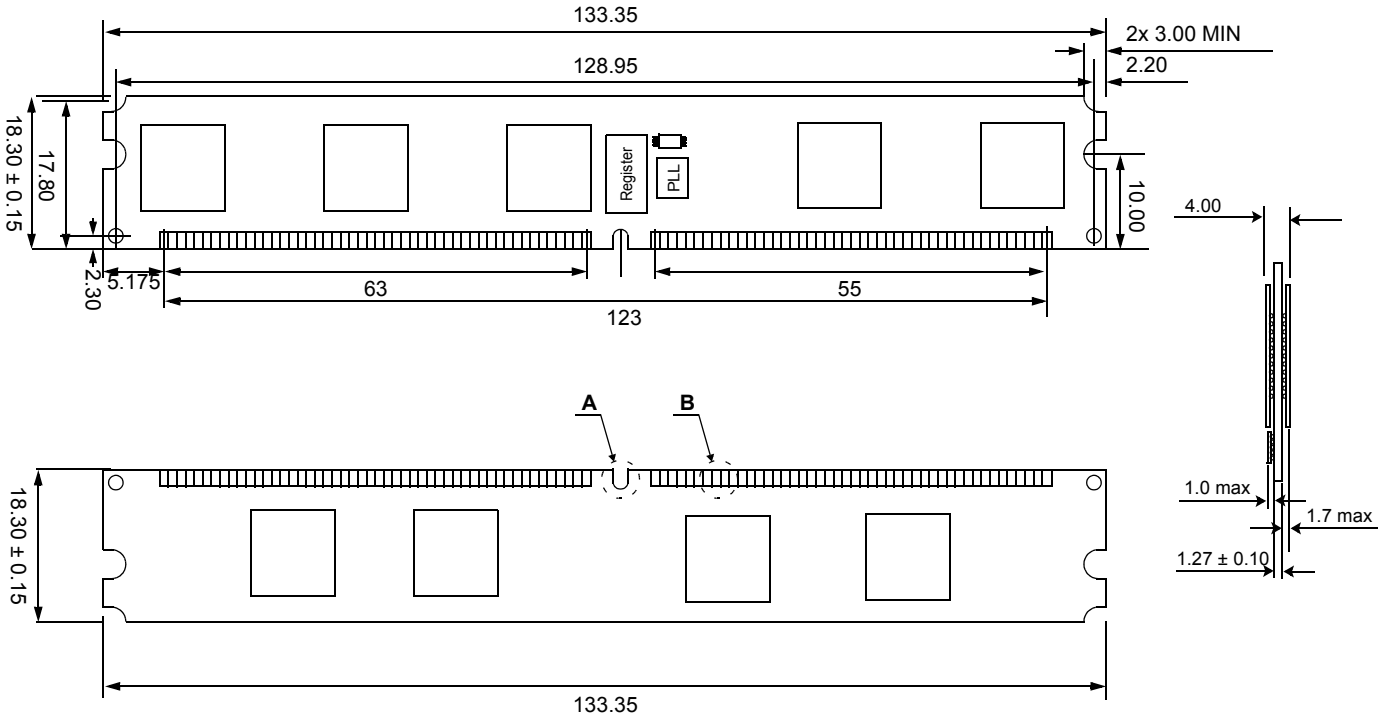
Parameter	Symbol	DDR2-533		DDR2-400		Units	Notes
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	37.5	x	37.5	x	ns	
Four Activate Window for 2KB page size products	tFAW	50	x	50	x	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	x	2	x	tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+tRP	x	tCK	14
Internal write to read command delay	tWTR	7.5	x	10	x	ns	24
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	
Exit self refresh to a read command	tXSRD	200	x	200	x	tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	6 - AL	x	6 - AL	x	tCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	tCK	27
ODT turn-on delay	tAOND	2	2	2	2	tCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	17,44
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	17,44
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	tCK	
ODT power down exit latency	tAXPD	8	x	8	x	tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	x	tIS+tCK+tIH	x	ns	15

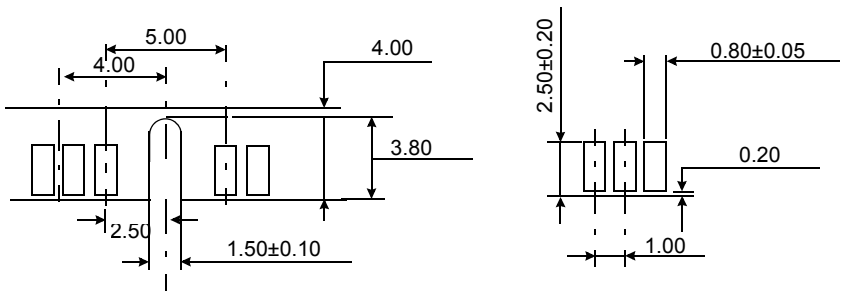
14.0 Physical Dimensions

14.1 64Mbx8 based 64Mx72 Module (1 Rank)

- M392T6553EZA

Units : Millimeters





Detail A

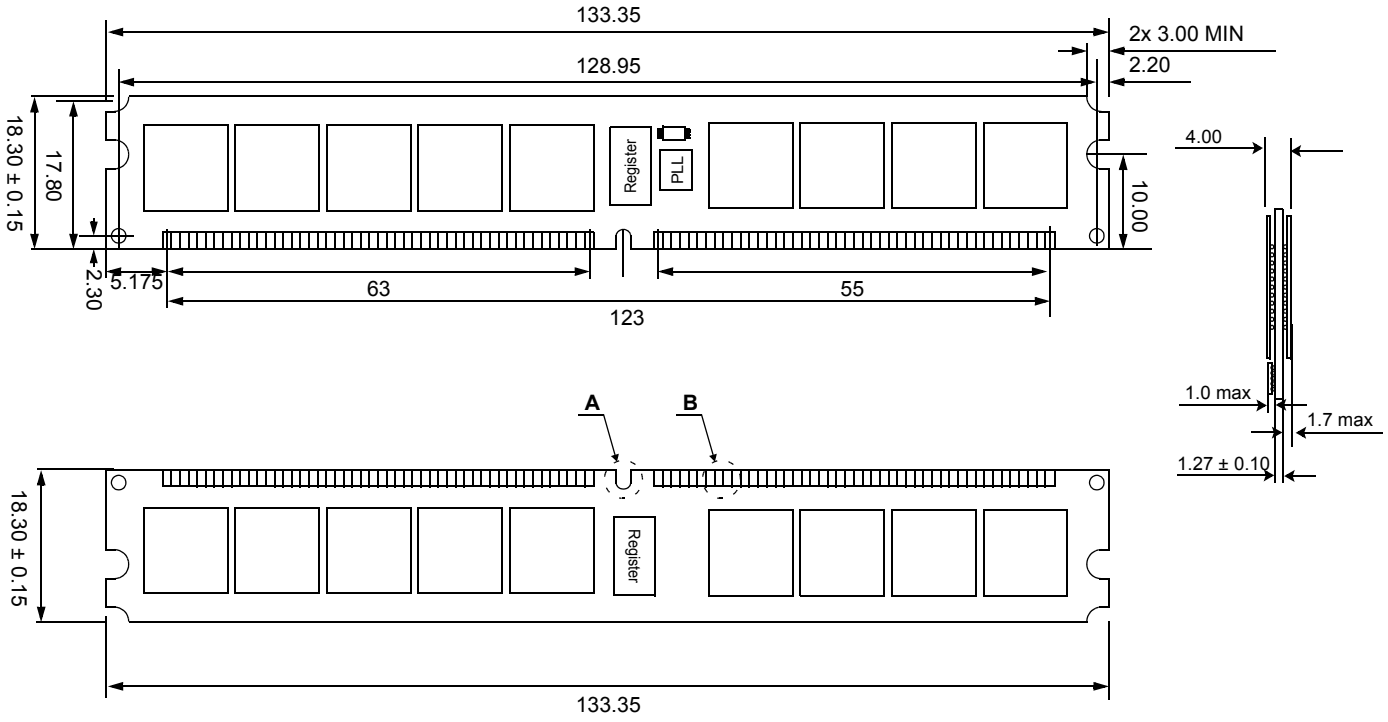
Detail B

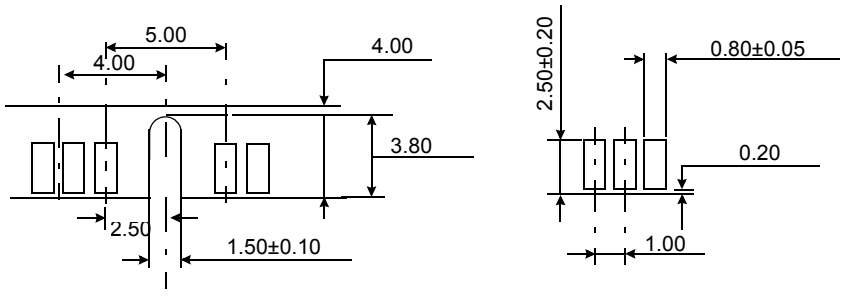
The used device is 64M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QE

14.2 64Mbx8/128Mbx4 based 128Mx72 Module (2/1 Ranks)

- M392T2953EZA / M392T2950EZA

Units : Millimeters



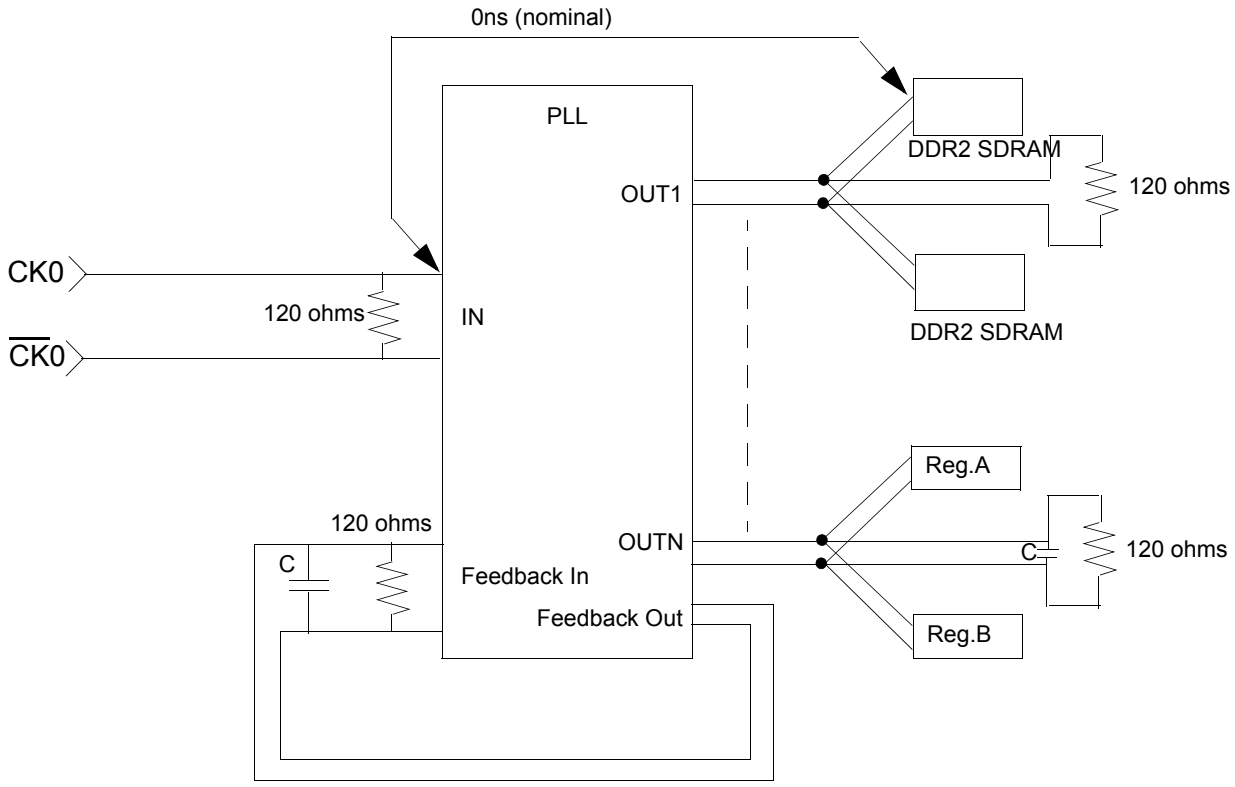


Detail A

Detail B

The used device is 64M x8 / 128M x4 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QE / K4T51043QE

15.0 240 Pin DDR2 Registered DIMM Clock Topology



Note:

1. The clock delay from the input of the PLL clock to the input of any DDR2 SDRAM or register will be set to 0ns (nominal).
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.